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# Power and Speed Evaluation of Hyper-FET Circuits

**JUAN NÚÑEZ AND MARÍA J. AVEDILLO**
Institute of Microelectronics at Seville (IMSE-CNM), CSIC, University of Seville, 41092 Seville, Spain

Corresponding author: Juan Núñez (jnunez@imse-cnm.csic.es)

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**ABSTRACT** Many emerging devices are currently being explored as potential alternatives to complementary metal–oxide–semiconductor technologies for overcoming power density and energy efficiency limitations. It is now generally accepted that these emerging devices need to be evaluated at the circuit level. In this paper, we investigate the speed and power performance of hyper-field-effect transistor (Hyper-FET) circuits, comparing them with both high-performance and low standby power fin-shaped FET designs on the same technology node. The evaluation, which was carried out at the gate level and circuit level, includes a characterization of 8-bit ripple carry adders. Our experiments showed around 80% speed degradation and 30% power savings for a given range of operating frequencies. These power savings were much smaller than those predicted from the transistor- and gate-level estimations. Deviations from the ideal expected behavior of the Hyper-FET circuitry are illustrated, which support the obtained results.

**INDEX TERMS** Hyper-FET, low voltage, low power, phase transition materials, steep subthreshold slope.

## I. INTRODUCTION

In recent years, the scaling of complementary metal-oxide-semiconductor (CMOS) transistor technologies and the appearance of advanced processing techniques have significantly reduced power consumption, allowing IoT applications with decent battery capacity or powered by energy harvesting systems. However, continuing to reduce power consumption when using these conventional CMOS technologies and the computing and communications methods built from them poses a big challenge. This is because the further scaling of supply voltages to reduce dynamic power while maintaining adequate speed, is counterbalanced by the exponential growth of leakage currents, this being the principal factor limiting the boom in IoT applications with strict power consumption requirements or even intermittent power supply sources. To address the demanding consumption and performance constraints of the new applications now dominating the market, many emerging devices are being explored as potential complements or replacements for CMOS technologies, and their benchmarking is an important task that needs to be carried out as research progresses [1]–[4]. It is now generally accepted that these emerging devices need to be evaluated at circuit level [5]–[9]. A reduced set of technological parameters such as *ON* current, *OFF* current, input capacitance and supply voltage may not be enough to estimate gains obtained with respect to CMOS. It is also critical to provide guidance for device design, as evidenced by the extensive use of the term ''device-circuit co-design''. In this paper, we evaluate circuits built from Hyper-Field Effect Transistors (Hyper-FETs), a steep slope device currently receiving much attention, and show how the results obtained differ from device level estimations.

Hyper-FET transistors were proposed by connecting a phase transition material (PTM) to the source terminal of a FET. The abrupt insulator-metal transitions of the PTM are used as a mechanism to obtain steep switching and to boost the ratio of the *ON* current to the *OFF* current [10]. Several Hyper-FETs have been obtained experimentally, producing subthreshold slopes (*SS*) of around 8mV/dec [10], 5mV/dec [11], 59mV/dec [12] and 9.9mV/dec [13]. Recently, in [14], a phase-change Tunnel FET with $SS = 30$mV/dec was proposed.

Hyper-FETs are being explored for different applications: 1) for reducing power consumption in conventional logic computation (associated to *SS* reduction); 2) for implementing new computational paradigms such as neuromorphic architectures or coupled-oscillator based processing [15]; and 3) for enhancing specific circuit topologies [16], [17].

Two recent publications analyzed how Hyper-FET operates [18], [19]. Specifically, [19] showed that Hyper-FET logic gates exhibit degraded DC output voltages (different from $V_{DD}$ and zero). In [20], we analyzed the impact of these non-ideal voltage levels when interconnecting gates. Gates in a logic network were shown to deviate from their desired behavior, leading to smaller power savings than those predicted by gate level analysis or even to power penalties. In this paper, we further investigate Hyper-FET based circuits. Our work's main contributions are:

- The evaluation not only of power but also of speed.
- The consideration of low stand-by power (LSTP) Fin-Shaped Field Effect Transistors (FinFETs) in addition to high performance (HP) FinFETs and Hyper-FETs.
- The analysis is extended to a more complex circuit.

The paper is organized as follows: Section II looks at the background of both the Hyper-FET transistor and the operation of Hyper-FET-based circuits. Section III illustrates and analyzes deviations from ideal gate behavior and how they impact delay and power. Section IV describes the evaluation at circuit level, and finally, some conclusions are given in Section V.

## II. BACKGROUND

### A. HYBRID PHASE-CHANGE FET

A Hybrid Phase-Change FET (Hyper-FET) integrates a phase-transition material (PTM) into the source terminal of a conventional transistor [11], [18], as shown in Fig 1a.

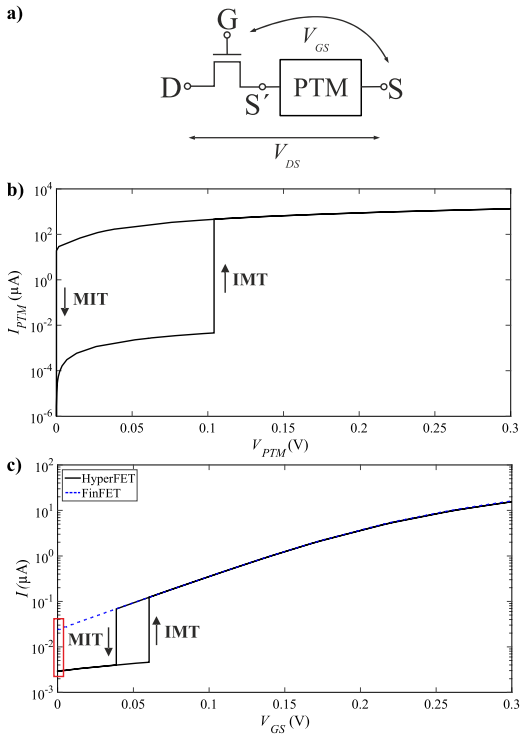


**FIGURE 1.** a) Schematic for the Hyper-FET. b) I-V curve of the PTM device. c) Comparison between the I-V characteristics of the selected FinFET and Hyper-FET.

PTMs undergo insulator-metal transitions under given electrical (or other) stimuli. That is to say, they abruptly switch from/to a high-resistivity state (insulating phase) to/from a low-resistivity state (metallic phase). Hyper-FETs use current-driven PTMs to achieve steep switching. PTMs tend to stabilize in the insulating phase with no electrical stimuli. When a higher voltage is applied, the current circulating through the PTM also increases linearly (according to Ohm's Law). When a sufficiently high current density flows through it, Insulator-to-Metal Transition (IMT) occurs, as depicted in Fig 1b. Because of the large reduction in PTM resistivity, the current abruptly increases. Increasing the applied voltage further again produces linear increment in the current. Likewise, reducing the applied voltage produces a linear decrease in the current. When a sufficiently low current density flows, Metal-to-Insulator Transition (MIT) takes place.

The Hyper-FET transistor exploits the difference in orders of magnitude between insulating and metallic state resistances to boost the ratio of its *ON* current ($I_{ON}$) and its *OFF* current ($I_{OFF}$), thereby achieving a steep subthreshold slope. When the transistor inside the Hyper-FET (intrinsic transistor) is in the OFF state, the small current flowing through the Hyper-FET forces the PTM into the insulating state. Thus, the effective gate-to-source ($V_{GS}{}'$ in Fig 1a) and drain-to-source ($V_{DS'}$ in Fig 1a) voltages seen by the intrinsic transistor are reduced and $I_{OFF}$ is also decreased. When the gate-to-drain voltage is increased, the current through the Hyper-FET also rises, switching the PTM to the metallic state. Thanks to the PTM's small metallic resistance in relation to that of the intrinsic transistor, the $I_{ON}$ current of the Hyper-FET is barely reduced with respect to that of intrinsic transistors. $I_{ON}/I_{OFF}$ is thus increased. To achieve the operating principle described above for the Hyper-FET and boost the current ratio, proper tuning of the PTM and the intrinsic transistor is critical [18].

Two different scenarios are possible. PTMs can be combined with conventional FETs to reduce their leakage current without significantly reducing their *ON* currents, as described in the previous paragraph, or the Hyper-FET can be designed to match the leakage current of conventional FETs by lowering the threshold voltage of the intrinsic transistors with respect to conventional FETs. In this second case, the Hyper-FET exhibits higher on-state current than the conventional FET.

This paper explores the first scenario. We combined a predictive 14nm High Performance (HP) FinFET transistor [21] (model available from [22]) with the PTM-Sim in [18], the characteristic parameters of which are shown in Table 1, as described in [19] and [20]. For the PTM-Sim, a Verilog-A model inspired by the macromodel proposed in [18] was derived. The electrical parameters used in that model were calculated from the material and geometrical properties. MIT and IMT are abrupt but not instantaneous, so a transition time (*TT*) was also considered in the same macro-model to take this into account. For this, the value reported in [18] (50ps) was used. In addition, a parallel

**TABLE 1. PTM_Sim characteristic parameters.**

| Parameter | Parameter description | PTM-Sim |
|---|---|---|
| $\rho_{INS}$ | Resistivity of the insulating state | 100 Ω·cm |
| $\rho_{MET}$ | Resistivity of the metallic state | $10^{-3}$ Ω·cm |
| $J_{C\text{-}IMT}$ | Current density which triggers the insulator to metal transition (IMT) | $5.2{\cdot}10^{2}$A/cm$^2$ |
| $J_{C\text{-}MIT}$ | Current density which triggers the metal to insulator transition (MIT) | $8{\cdot}10^{3}$ A/cm$^2$ |
| $L$ | Length | 20 nm |
| $A$ | Area | 42·21 nm$^2$ |

parasitic capacitance of 1fF was included, in accordance with [18].

Fig 1b was obtained with this model and shows good agreement with [18].

Fig 1c compares the I-V characteristics of the Hyper-FET we used with that of its intrinsic transistor (14nm predictive HP FinFET transistor) at $V_{DS} = V_{DD} = 0.3$V. Note the reduction by almost one order of magnitude of $I_{OFF}$ (the red rectangle in Fig 1c). In the rest of the paper, $V_{DD} = 0.3$V is used if no value is explicitly specified.

### B. HYPER-FET CIRCUITS

Fig 2 shows the schematic for a Hyper-FET inverter and its voltage transfer characteristic (a), and its behavior (b). A correct logic operation can be seen in Fig 2b (waveforms *IN* and *OUT*). The two waveforms at the bottom represent the state of each of the PTMs in the inverter. The one associated to the *p*-type Hyper-FET is denoted by ''STATE P'' and the one corresponding to the *n*-type Hpyer-FET is denoted by ''STATE N''. The low level means the PTM is in the metallic state (MET) and the high level indicates it is in the insulating state (INS). During transitions, a single PTM switches to the metallic state, the *p* PTM for rising output transitions and the *n* PTM for falling output transitions. In the metallic state, the current through the Hyper-FET transistor is almost the same as the current through the transistor alone (see Fig 1c) and so no increase in delays is assumed [19], [20]. Once the output transition has taken place, the current decreases and the PTM which switched to the metallic state switches back to the insulating state. With both PTMs in the insulating state, static/leakage currents decrease and power savings can therefore be expected.

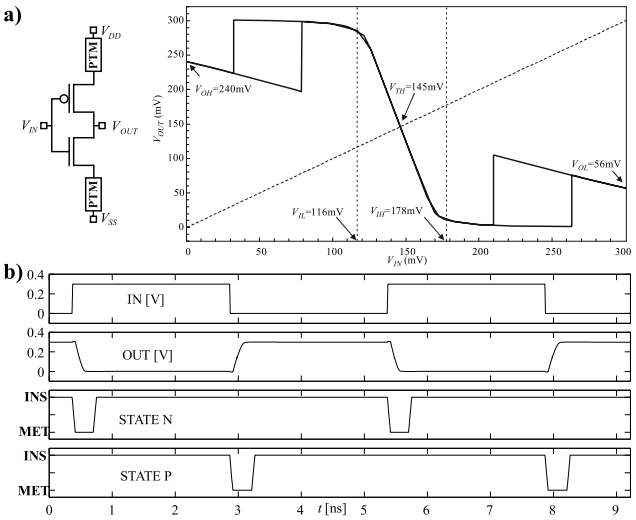


**FIGURE 2. a) Voltage transfer characteristic of a Hyper-FET inverter (schematic also shown). (b) Waveforms corresponding to a Hyper-FET inverter with the internal states of the *n*-type and *p*-type Hyper-FETs.**

Hyper-FET logic gates show degraded DC output voltages (different from $V_{DD}$ and zero), as can be seen in the voltage transfer characteristic in Fig 2a and in agreement with [19]. Although the $V_{OH}$ and $V_{OL}$ values suggest robustness concerns with regard to noise, it is stated in [19] that classic DC-based approaches to evaluating noise margins may yield misleading results, and that, even though the output of the gates is connected to supply rails through the PTM in the insulating (high resistance) state for low and high input voltages, a ''self-recovering'' mechanism exists that mitigates noise intolerance.

Degraded output voltage values are not appreciated in the waveforms in Fig 2b because of the input switching frequency used. A slower input signal is required to observe how output voltages evolve towards degraded DC values, as will be shown later. In [20], we analyzed the impact of the degraded DC output voltage levels of Hyper-FET logic gates on circuit operation. It was shown that the logic operation of the circuits is not compromised due to the intrinsic self-recovering capability of Hyper-FET gates. However, the expected power advantages, associated to the reduction of the leakage currents with respect to the intrinsic transistor of the Hyper-FETs, can reduce, cancel, or even switch to power penalties at the circuit level.

In this paper, our analysis in [20] is extended in different directions. Firstly, we address speed evaluation. We assumed that Hyper-FET gates have delays equal (or very similar) to those of gates built from transistors alone, since during transitions the PTM device in the charging (discharging) path is in the metallic state (very low resistance), and so its combined resistance in series with the transistor is therefore almost equal to the resistance of the transistor alone. However, delays can be affected by different factors, as we will explain in the next section.

Secondly, the Hyper-FET studied was proposed to reduce the OFF current of a given transistor. More specifically, in that paper, we combined a FinFET HP transistor with a PTM and compared the power results of the Hyper-FET and the FinFET HP counterparts. However, comparison with FinFET LSTP is also of great interest.

Finally, in our previous paper, most of the analysis was conducted on a single chain of inverters driven with a periodic

input signal. Only a few results were obtained for a functional circuit. We now deepen that analysis into a more complex case study and compare the results obtained for both circuits.

## III. DEVIATIONS FROM IDEAL BEHAVIOR

In order to better explain deviations from ideal behavior in Hyper-FET circuits, two scenarios are illustrated separately. Both delay and power aspects are addressed.

### A. GATES WITH IDEAL INPUTS

Fig. 3 depicts the delay of a single Hyper-FET inverter as a function of the PTM transition time (*TT*) for three frequencies of the input signal. The delay of a FinFET HP inverter (remember this is the intrinsic transistor of our Hyper-FET), also polarized at 0.3V, is shown for purposes of comparison. The average of the rising and falling delays was used. As expected, the gate delay depends on the PTM transition time from one state to the other. The longer this time, the greater the delay. As already mentioned, in our model of the PTM we used the value reported in [18] (50ps). This is also the value used in the rest of the paper. It can be seen that the delay also depends on the input frequency, increasing when it is measured at a higher frequency. This is due to the degradation of the DC output levels for the Hyper-FET gates. Although the output charges to $V_{DD}$ or discharges to ground after an input transition, it later evolves towards degraded DC output voltages. When a slow input signal is used for delay measurement, therefore, the delay is smaller since the output is already at some value higher than 0V (for the rising transition) or lower than $V_{DD}$ (for the falling transition). This translates to smaller logic swing and delays.

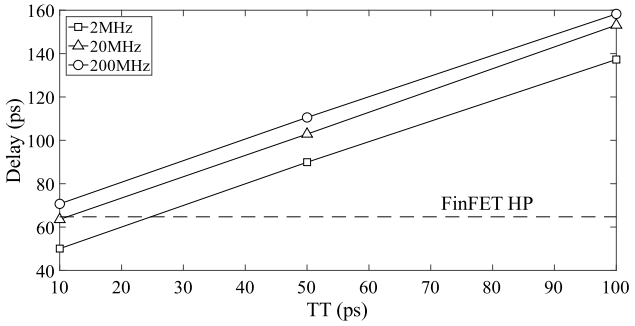


**FIGURE 3.** Delay versus PTM transition time for Hyper-FET inverter.

Power for the Hyper-FET inverter with logic 0 (logic 1) constant input was 0.81nW (0.75nW), while for the FinFET HP inverter it was 7.24nW (6.18nW). As expected, the reduction in leakage current translates into static power advantages. Relative reductions decrease with frequency since dynamic power dominates.

### B. GATES EMBEDDED INTO A CIRCUIT

We then analyzed a gate embedded in a circuit - and therefore with non-ideal inputs. Fig. 4b shows waveforms for the input (*IN*) and the output of the second and the third stages

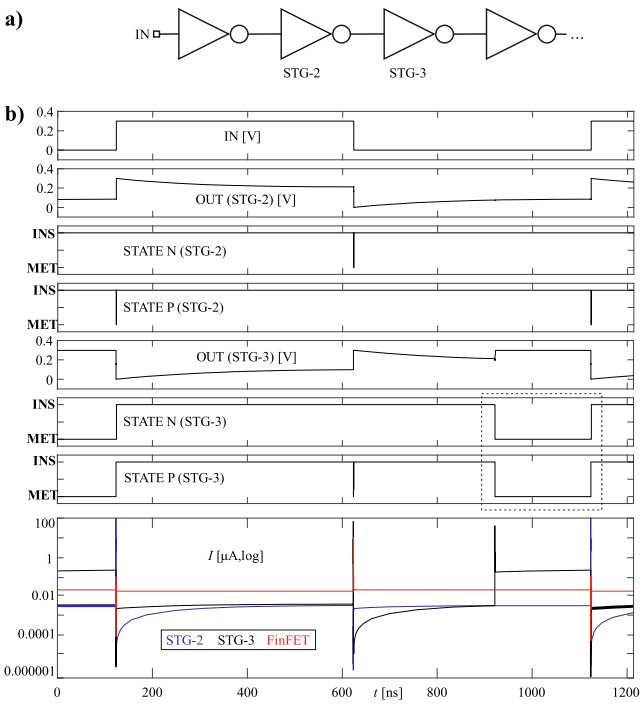


**FIGURE 4.** Embedded stages. Output, state of PTMs and currents for second and third stages.

of the circuit of chained inverters shown in Fig. 4a. At the simulated frequency, the second inverter behaves according to the ideal operating principle, with PTMs in the insulating state most of the time and one of them switching to the metallic state when a transition occurs (STATE N (STG-2) and STATE P (STG-2) in Fig. 4), as explained previously. The aforementioned degradation of the logic levels can also be seen in the figure (OUT (STG-2)). The third stage behaves differently. Note that there is a fraction of time with both PTMs in metallic (STATE N (STG-3) and STATE P (STG-3)). During this time, output (OUT (STG-3)) is at $V_{DD}$. It is therefore recharged to $V_{DD}$ after having degraded but, after that, both PTMs are in the metallic state. The difference is due to the degraded input level (0 logic) driving by the third inverter.

Fig. 5 shows the delay of the third inverter at different input frequencies. The delay of the third inverter in an equivalent FinFET HP inverter chain is also depicted.

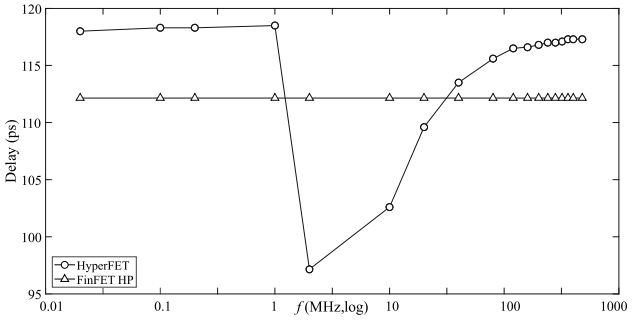


**FIGURE 5.** Delay versus frequency for an embedded inverter.

This latter delay (112ps) is larger than that in the gate driven by ideal inputs in the previous experiment (65ps). Again, Hyper-FET's dependence on frequency is evident. There are two regions where the delay is almost constant: frequencies up to 1MHz and frequencies over 20MHz. Delay values in between are lower than in FinFET technologies. Delay differences between Hyper-FET and FinFET HP are also smaller for the embedded inverter than for the ideal inverter. Delays may be modified by a number of different factors. Firstly, as described in the previous sub-section, degraded logic levels at the output of the gates tend to reduce delay. Secondly, degraded logic levels at the input of the gate (output of the second inverter) translate into lower current and so tend to increase delay. Finally, non-ideal input transition times also degrade speed. The balancing of these factors varies with frequency, hence the results obtained.

It is also interesting to compare the delay measured for the third inverter (this Sub-section) with that measured with ideal inputs (Sub-section A). Table 2 summarizes the ratio between those two delays for both Hyper-FET and FinFET HP. It can be seen that the ratio obtained for FinFET HP is larger than that for Hyper-FET. It can also be seen that similar delay ratios (around 1) are obtained for the Hyper-FET embedded gate and the one with ideal inputs from 2MHz.

**TABLE 2. Ten stage inverter chain delays.**

| Hyper-FET | | FinFET HP | FinFET LSTP |
|---|---|---|---|
| $f$(MHz) | Delay (ns) | Delay (ns) | Delay (ns) |
| 0.2 | 1.18 | 1.07 | 121.41 |
| 2 | 0.97 | | |
| 20 | 1.10 | | |
| 200 | 1.17 | | |

The bottom waveform in Fig. 4 depicts currents through the second and third inverters and an equivalent FinFET HP inverter. The static current of the second inverter is lower than that of the FinFET inverter because of the PTMs in the insulating state. The static current of the third inverter is larger than that of the FinFET when both PTMs are in metallic. Significant power savings can thus be expected for the second inverter with respect to its FinFET counterpart, but are not expected for the third inverter. Power for the third Hyper-FET inverter with constant logic 0 (logic 1) applied to the input of the first inverter is 75nW (70.7nW). This increment of almost two orders of magnitude with respect to the gate with ideal inputs is due to two factors.

Firstly, both PTMs are in metallic, so the reduction observed for the Hyper-FET gate with ideal inputs with respect to the FinFET inverter does not occur. Secondly, its input is degraded, so currents are higher than in the FinFET third inverter, where input is not degraded. Depending on frequency, the third inverter will show less power savings than the second one or even lead to power penalties.

## IV. CIRCUIT-LEVEL CASE STUDIES

This section explores how the deviations from the ideal behavior described in the previous section impact the performance of Hyper-FET circuits by evaluating power-speed curves.

### A. TEN-STAGE CHAIN OF INVERTERS

The first case study is a ten-stage chain of inverters. Table 3 shows the measured delays. In accordance with the embedded inverter characterization carried out in the previous section, both a slight degradation in speed or faster operation with respect to FinFET HP were obtained. The FinFET LSTP design was also evaluated. At 0.3V, its delay was much larger than that of the other two designs.

**TABLE 3. Ratio of the delay of an embedded gate to the delay of a gate with ideal inputs.**

| Hyper-FET | | FinFET |
|---|---|---|
| $f$(MHz) | Delay ratio | Delay ratio |
| 0.1 | 1.31 | 1.62 |
| 2 | 1.05 | |
| 20 | 1.02 | |
| 200 | 1.01 | |

Fig. 6 shows power ratios versus operating frequency for different input patterns. 100MHz, for example, means that input changes every 10ns. Both an alternating 0 and 1 sequence (Fig. 6a) and a random sequence (Fig. 6b) were evaluated. Note that the figure shows Hyper-FET/FinFET HP power (blue) and Hyper-FET/Power FinFET LSTP power (red). The inset graphs depict results for frequencies up to 100MHz using a logarithmic scale for the Y-axis. Results were obtained up to a conservative frequency, assuming a

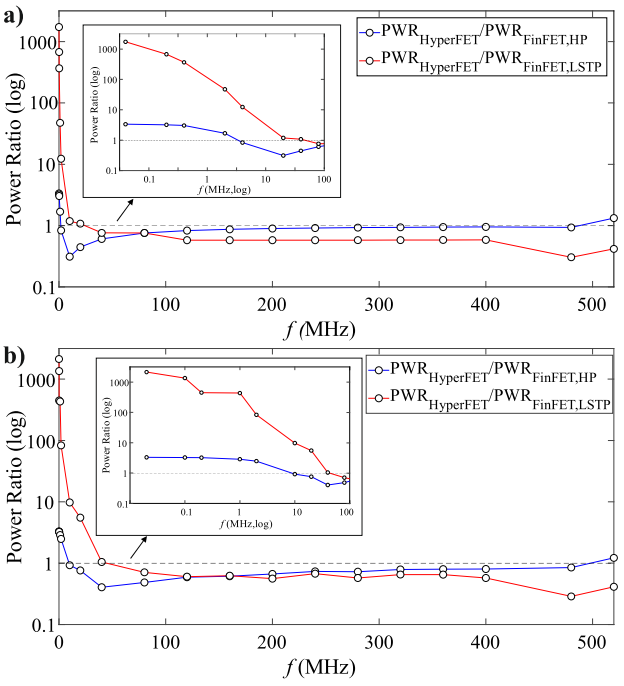


**FIGURE 6. Power ratios versus frequency for inverter chain a) periodic input b) random input.**

given fixed clock cycle time for accommodating delays and set-up time for memory elements, clock skew and other non-idealities. The experiment's maximum operating frequency corresponded to that of the FinFET HP circuit (the fastest one), with 0.3V of supply voltage. The supply voltage of the other circuits was raised, when necessary, to achieve the target frequencies. Hyper-FET required a higher supply voltage (0.35V) only for the last target frequency. For the FinFET LSTP circuit, $V_{DD} = 0.55$V was required to guarantee correct operation at the maximum operating frequency.

Points in the curves higher than 1 mean that the Hyper-FET power is larger than the corresponding FinFET power. Values lower than 1 indicate power advantages for Hyper-FET. In the first input sequence, it can be seen that up to 2MHz both curves are higher than 1 (no power savings for the Hyper-FET). Up to 20MHz, Hyper-FET is better than FinFET HP, but the best power results correspond to LSTP FinFET (the red curve is the only one higher than 1). From 20 MHz to 480MHz, both curves are lower than 1, and the best power results are therefore obtained with Hyper-FET. Power savings ranged from 17% at 120MHz to 6% at 480MHz. Over 490MHz, the best power results were obtained with FinFET HP.

The results were slightly different for the random input sequence. Here, power savings ranged from 40% at 120MHz to 15% at 480MHz. Note that the power savings in the region in which both curves are lower than 1 are now larger. This is due to the fact that when using random input, static and short powers make up a larger fraction of total power in comparison with periodic input. Increasing resistance in the supply to ground path by adding PTMs reduces those power components, but does not decrease switching power.

We will now analyze the operation of a circuit involving different logic gates and more realistic interconnection patterns.

### B. RIPPLE CARRY ADDER

An 8-bit RCA was designed and evaluated in each of the three technologies (Hyper-FET, FinFET HP and FinFET LSTP). The corresponding logic diagram is shown in Fig. 7. Each full adder was implemented with NAND2 and NAND3 gates. The gates were equally sized in the three adders, and the same parasitic capacitances were considered. We first carried out simulations with random inputs, monitoring the internal nodes of the Hyper-FET design. In most cases, voltage levels differed from ground and supply voltage. This is illustrated in the waveforms in Fig. 8. We also analyzed the operation of the PTMs. Fig. 8 also shows the state of two internal Hyper-FETs to illustrate the different cases. The fraction of time the PTMs were in the metallic state (low) was larger than expected.

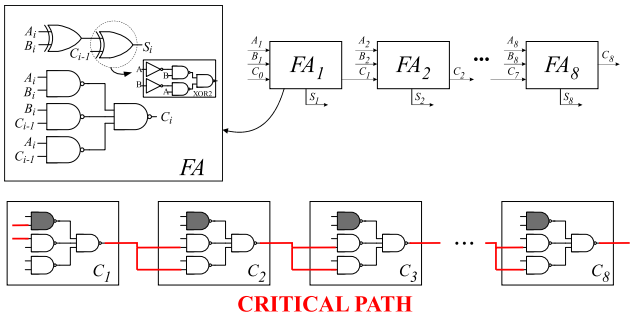


**FIGURE 7.** Logic diagram of an 8-bit RCA.

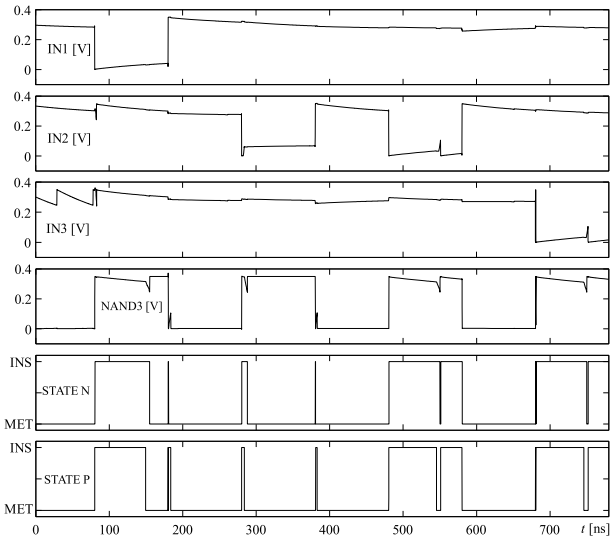


**FIGURE 8.** Waveforms for internal nodes and state of PTMs of the RCA.

Secondly, we evaluated the delay of the carry chain (critical path shown in Fig. 7) of each circuit by having an input transition propagate through it. A fixed DATA-A = (1111 1111) was used while DATA-B switched between (0000 0000) and (0000 0001). Table 4 shows the results obtained at different operating frequencies. Note that the delay of the Hyper-FET design not only depends on the input frequency, as in embedded gates and the ten-stage inverter chain, but also changes

**TABLE 4.** Critical path delay for several frequencies and clock cycles.

| $f$(MHz) | HYPER-FET #CYCLE | HYPER-FET DELAY (ns) | FINFET HP DELAY (ns) | FINFET LSTP DELAY (ns) |
|---|---|---|---|---|
| 2 | 2 | 3.7 | 2 | 246.8 |
| | 3 | 3.6 | | |
| | 4 | 3.6 | | |
| | 5 | 3.7 | | |
| 20 | 2 | 2.8 | 2 | 18.8 ($V_{DD}$=0.40V) |
| | 3 | 3.1 | | |
| | 10 | 3.4 | | |
| | 30 | 3.4 | | |
| 200 | 2 | 2.3 | 2 | 3.4 ($V_{DD}$=0.50V) |
| | 10 | 2.7 | | |
| | 100 | 3.6 | | |
| | 200 | 3.6 | | |
| 250 | 2 | 2.3 | 2 | 2.1 ($V_{DD}$=0.55V) |
| | 10 | 2.6 | | |
| | 100 | 3.6 | | |
| | 200 | 3.6 | | |

for a given frequency. Different measurements were obtained in distinct cycles. Delay stabilized after a given number of cycles, depending on frequency. This behavior is due to the fact that only one input bit switches. The fixed values applied to the remaining inputs translate into degraded voltage levels at the output of the marked gates, which are the inputs of the gates in the critical path shown in Fig. 7. These voltage levels slowly evolved towards the DC voltages associated with logic values. More cycles were required for delays to stabilize at higher input frequencies. A delay degradation of 80% was obtained for the Hyper-FET in comparison with the FinFET HP alone. In other words, the frequency penalty was larger for the RCA than for the embedded inverter or the inverter chain. Note that supply voltage had to be increased for the FinFET LSTP design to achieve operation at the reported frequencies. The required supply voltage value is also shown in the table. Increased supply voltage impacts power, as shown in the next experiment.

Thirdly, we simulated long random input sequences at different frequencies for power measurements. Fig 9 shows the results obtained. Again, the power of the Hyper-FET version is shown, normalized with respect to the FinFET HP and FinFET LSTP designs. The frequency range shown starts at the frequency at which FinFET LSTP ceases to be competitive in terms of power (around 75MHz). The upper frequency (360MHz) was calculated as in the inverter chain experiment in Sub-Section A. The supply voltage was also raised when required. Up to 160MHz, the Hyper-FET circuit consumed the least power of the three versions. The power inefficiency of the FinFET LSTP design at the shown frequency range is due to the higher supply voltages it requires.

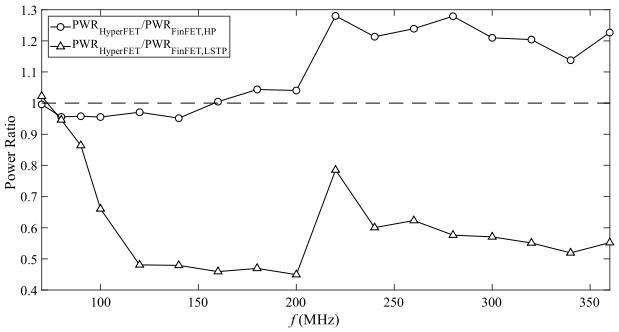


**FIGURE 9.** Power ratio versus frequency for an 8-bit RCA.

Fig 10 shows power savings with respect to FinFET HP. Positive values mean power savings in percentage. Negative values correspond to power overheads. Results for the complete RCA in Fig. 7 (RCA_1) shows, in a different way, information already in Fig 9: average power savings for the RCA, when they exist, are under 10%. Power savings for the "Sum" subcircuits (part of the FA generating the Sum output $S_i$) are also shown (RCA_1_Sum). Note that in this case there are power overheads.

Finally, we evaluated the power performance of a different logic implementation of the Sum subcircuits. Each XOR gate

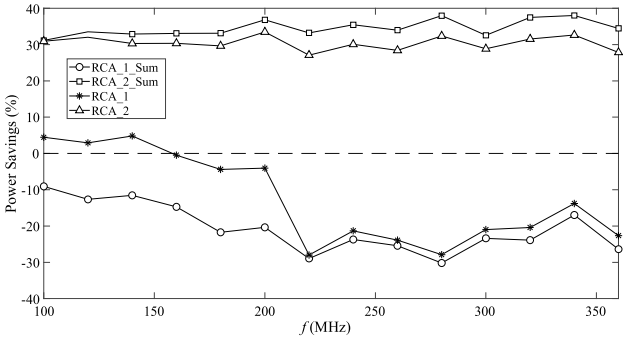


**FIGURE 10.** Power savings versus frequency for two implementations of the 8-bit RCA.

in Fig. 7 was implemented with three gates (two of them inverters), instead of using the logic diagram with five gates depicted in that figure. Absolute values of the measured powers were larger for the original implementation than for the second in both technologies. This was, as expected, due to the reduced number of gates and circuit nodes in the second implementation. However, our interest lay in the power savings/overheads of Hyper-FET with respect to FinFET in each case. Results for both the complete, modified RCA (RCA_2) and its "Sum" part (RCA_2_Sum) are also shown in Fig 10. Hyper-FET RCA_1_Sum consumes more power than its FinFET counterpart (from 10% to 30% overhead in the explored frequency range). RCA_2_Sum consumes less power than its FinFET counterpart (around 30% savings in the frequency range shown). Hyper-FET RCA_2 exhibits similar 30% power advantages.

To compare power and speed tradeoffs in the three technologies, widely accepted metrics were evaluated. Energy ($E$, average energy per operation) and energy delay product ($EDP$), measured at the maximum operating frequency achieved by each RCA_2 design at 0.3V, are shown in Table 5. Slightly lower energy was obtained with Hyper-FET with respect to FinFET HP, although the lowest energy was achieved by FinFET LSTP. With regard to EDP, Hyper-FET was slightly worse than FinFET HP, but both of them had a much better power delay tradeoff than FinFET LSTP.

**TABLE 5.** Power delay Metrics for RCA_2 @ 0.3V.

| | HYPER-FET | FINFET HP | FINFET LSTP |
|---|---|---|---|
| $E$ (fJ) | 14.45 | 18.66 | 11.85 |
| $EDP$ (fJ·μs) | 0.07 | 0.05 | 5.92 |

It may be useful to put these results in perspective and to this end, the power savings achieved by tunnel transistors - widely studied steep slope devices - may be of interest. In [7], an experiment using the same RCA as the one described in this Section (RCA_1) is carried out, in which FinFET and projected tunnel technologies were compared. Much larger power savings, up to 95% in the same frequency range, were reported.

The results obtained from the different experiments are analyzed altogether below.

### C. RECAPITULATION

Concerning speed, delay depends – as expected - on the transition time of the PTM device. But it also depends on the frequency of the input used for its measurement. Using the 50ps value reported in reference works, we found that: 1) the delay of single gates with ideal inputs is larger (smaller) than the delay exhibited by FinFET HP (LSTP) gates and it decreases when the input frequency is reduced due to the reduced output logic swing associated with the degraded DC logic outputs of such gates; 2) embedded gates and circuits present more complex variation patterns with frequency since there are now advantages and disadvantages associated with degraded DC output levels, and delays even smaller than those of FinFET HP have been obtained at some frequencies; 3) estimated speed degradation for an 8 bit RCA with respect to FinFET HP is around 80%.

Concerning power, expected power reduction with respect to FinFET HP (associated to the around one order of magnitude leakage current reduction) has been obtained for isolated gates with ideal inputs, but not for circuits. For these, we found that: 1) FinFET LSTP is much better than FinFET HP and Hyper-FET for low-frequency operation; 2) Hyper-FET circuits exhibit power advantages at moderate frequencies; 3) Power savings achieved by Hyper-FET circuits are heavily impacted by the logic implementation; 4) Measured power savings for the 8-bit RCA with respect to FinFET HP are around 30%.

## V. CONCLUSIONS

The performance of Hyper-FET circuits in terms of both speed and power was analyzed and compared with FinFET counterparts. Delays in Hyper-FET circuits show complex behavior, with a dependency on input frequency and even on past inputs applied. Significant speed degradation was measured for the most complex of the circuits studied. The analyzed Hyper-FET technology is useful from the frequency above which the LSTP technology is not able to operate at much reduced supply voltage up to a frequency which varies depending on the logic structure of the circuit itself. The power savings achieved were smaller than those predicted exclusively from leakage current reduction, since they occurred at operating frequencies at which static power was not dominant. Although we analyzed one specific Hyper-FET technology, these qualitative conclusions are independent of specific device parameters since they are drawn from the degraded DC output voltages exhibited by the circuits. It is important to point out that this paper addresses only one of the two scenarios outlined in the introduction. It would be of great interest also to explore the other one: that is to say, the addition of the PTM to boost the *ON* current of the intrinsic transistor instead of for reducing its *OFF* current.

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**JUAN NÚÑEZ** received the telecommunication engineering degree, in 2005, and the Ph.D. degree from the University of Seville, in 2011. Since 2005, he has been with the Institute of Microelectronics of Seville (IMSE-CNM) and the Department of Electronics and Electromagnetism, University of Seville, where he is currently a Researcher.

His current research interests include the design and evaluation of logic circuits and fine pipeline logic networks using deep-submicron and emerging technologies.

**MARÍA J. AVEDILLO** received the Ph.D. degree *(summa cum laude)* from the Department of Electronics and Electromagnetism, University of Seville, in 1992. She joined the Department of Electronics and Electromagnetism, University of Seville, in 1988, as an Assistant Professor, where she has been a Full Professor, since 2010. In 1989, she became a Researcher with the Department of Analog Design, National Microelectronics Center (currently, Institute of Microelectronics at Seville). She has participated in several research projects financed by the Spanish CICYT and in ESPRIT Projects. She has authored over 60 technical papers in main international journals and conferences. She has organized special sessions on threshold logic and also has co-authored a chapter titled *Threshold Logic* in the *Wiley Encyclopaedia of Electrical and Electronics Engineering*. Her current research interests include the design of threshold logic circuits, the design and applications of logic circuits using emerging technologies, and the development of CAD tools logic synthesis. She received the KELVIN Premium of The Council of the Institution of Electrical Engineers for two articles published, in 1994.