observed in an ordinary asymmetric reflectivity DFB laser without $\lambda/4$ phaseshift was due to a mode partition between the DFB mode and Fabry–Perot modes caused by insufficient AR coating at one end of the laser. So far TE–TM mode partition as shown in Fig. 3 has not been observed.

In the $\lambda/4$ shifted DFB laser the threshold gain difference $\Delta\alpha L$ among TE modes or among TM modes is around 0·7 when optimally designed,[3] i.e., $\kappa L$ is 1·25, while the mode selection between TE and TM mode provided by the difference in the coupling coefficient and the mode confinement factor is very small. Theoretical calculation assuming a rectangular shaped corrugation using a model by Streifer *et al.*[4] showed that there was no difference in the coupling coefficient between TE and TM modes for the active layer thickness $d_a$ of 0·15 $\mu$m. For a thinner $d_a$ of 0·1 $\mu$m there was a slight difference. However, even in this case, the $\Delta\kappa L$ for optimum $\kappa L$ of 1·25 was only 0·06, which corresponded to the threshold gain difference $\Delta\alpha L$ between TE and TM mode of only 0·07. The difference in mode loss owing to the mode confinement factor could not be as large because of the small absorption coefficient of the cladding layers. The mode selection between TE and TM mode in a $\lambda/4$ shifted DFB laser is much smaller than that in an ordinary asymmetric reflectivity DFB laser in which TE–TM mode selection is provided by the facet reflectivity. Fig. 4 shows the time averaged spectra of a $\lambda/4$ shifted DFB laser under modulation measured using a polariser. We can identify a small amplitude TM emission. This small amplitude TM emission is evidence of TM mode lasing with a very small probability, of the order of $10^{-10}$, under modulation due to the gain overshoot.

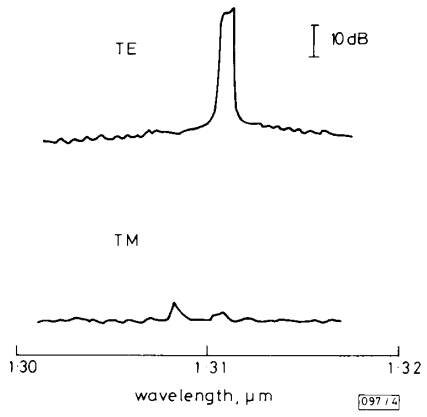


**Fig. 4** *Time averaged spectra under modulation*
TM spectrum was measured using a Glan-Thompson polariser

We have developed a very-low-threshold-current high-efficiency $\lambda/4$ shifted DFB laser having bandwidth of 11 GHz. However, transmission experiment revealed that there existed a mode partition between TE and TM mode. This mode partition is due to a small threshold gain difference between TE and TM mode. To make full use of the attractive feature of the $\lambda/4$ shifted DFB laser, i.e., the large threshold gain difference between modes, we must incorporate a strong mode selection mechanism between TE and TM mode. This is especially important for a laser to be used in several Gbit/s systems under a direct modulation scheme.

The authors wish to thank M. Matsuda for his fabrication of the $\lambda/4$ shifted corrugations, and S. Isozumi, T. Kusunoki, T. Tanahashi, H. Sudo and M. Sugano for their co-operation in this work. They also wish to thank T. Misugi, M. Kobayashi, and T. Sakurai for their encouragement.

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## SWITCHED-CAPACITOR NEURAL NETWORKS FOR LINEAR PROGRAMMING

*Indexing terms: Neural networks, Switched-capacitor networks, Linear programming solvers, Circuit theory and design*

A circuit for online solving of linear programming problems is presented. The circuit uses switched-capacitor techniques and is thus suitable for monolithic implementation. The connection of the proposed circuit to analogue neural networks is also outlined.

*Introduction:* It has been shown that both linear and nonlinear programming problems can be solved by using analogue circuits with a neural-like structure.[1,2] These circuits exhibit strong potential for those applications where online optimisation is required as is the case in robotics, satellite guidance, etc. Breadboard prototypes have been built using off-the-shelf circuit components.[1–3] Since the required component-count is very high even for simple examples, it makes sense to explore the possible realisation of these circuits using fully integrated techniques.

Nonlinear programming solvers are particular examples of the broader family of analogue neural networks, which is of increasing interest because it seems to pave the way for analogue artificial intelligence circuits.[1,4] However, the field of analogue neural networks is just emerging and very little has been done on the practical implementation of the different classes of such networks. In a very recent letter, Tsividis and Anastassiou[5] proposed a technique for the VLSI implementation of a type of analogue neural network using a switched-capacitor neural cell. The proposed technique is adequate for solving optimisation problems that can be formulated in an explicit form,[1] but not readily applicable to linear and nonlinear programming problems. A different strategy is required for this type of analogue neural network, since the equations describing mathematical programming problems are implicit in nature and do not admit to being cast in an explicit form.[1]

In this letter we propose a method for the realisation of linear programming solvers using switched-capacitor techniques. The proposed circuits are members of the general family of analogue neural networks, being more adequate for monolithic implementation than previous linear programming solver proposals.

*Problem formulation and proposed circuit structure:* The general linear programming problem can be stated as follows.[6] Minimise a scalar cost function

$$\Phi(\boldsymbol{x}) = \sum_{i=1}^{n} a_i x_i \qquad (1)$$

subject to a set of $p$ constraints,

$$f_j(\boldsymbol{x}) = \sum_{i=1}^{n} b_{ji} x_i \geq 0 \qquad 1 \leq j \leq p \quad (2)$$

where $\boldsymbol{x}$ is the vector of variables for the problem, $p$ and $n$ are integer numbers and $\boldsymbol{a}$ and $\boldsymbol{b}_j$, for each $_j$, are vectors of coefficients.



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By using the concept of the penalty function[6] and applying a gradient strategy we obtain the following numerical algorithm to solve the above general linear programming problem,

$$x(q+1) = x(q) - \frac{1}{\alpha}\left[ w(f)\nabla\Phi(x) + \sum_{j=1}^{p} \nabla\rho_j(x) \right] \quad (3)$$

where $\alpha$ is an arbitrary positive constant, $q$ is an integer number for the iteration count and functions $w(f)$ and $\rho_j$ are defined as follows,

$$w(f) = \begin{cases} 1 & \text{if } f_j \geq 0 \text{ for every } j \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

$$\rho_j(f_j(x)) = \left.\begin{cases} 0 & \text{if } f_j \geq 0 \\ \beta\,|f_j| & \text{otherwise} \end{cases}\right\} \quad \text{for } 1 \leq j \leq p \quad (5)$$

where $\beta$ is an arbitrary positive constant.

Note that the introduction of the function $w(f)$ means a modification of the traditional way of combining $f$ and $\Phi$ to define penalty functions.[6] This modification is important to improve the convergence of the algorithm.

Using eqns. 4 and 5 and eqns. 1 and 2 in eqn. 3 we obtain the following relationship for each component of $x$:

$$x_i(q+1) = x_i(q) - \frac{1}{\alpha}\left[ w(f)a_i - \frac{\beta}{2}\sum_{j=1}^{p}[1 - \text{sgn}\,(f_j)]b_{ji} \right] \quad (6)$$

where sgn (.) is the well-known sign function.

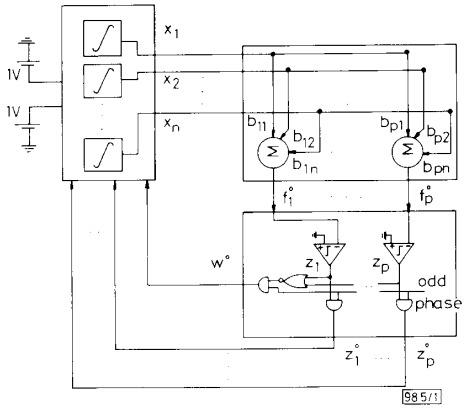


**Fig. 1** *Block diagram of proposed linear programming solver*

Fig. 1 shows the conceptual block diagram for the implementation of the general linear programming problem using switched-capacitor techniques. Note that one integrator is required per program variable. The $p$ constraint functions are obtained via a set of summers whose inputs are the integrator outputs. The nonlinear functions $w(f)$ given in eqn. 4, and $z_j(f_j) = \frac{1}{2}(1 - \text{sgn}\,(f_j))$ are respectively obtained from the outputs of the summers via the block at the bottom of the Figure on the right, henceforth called the constraint block.

Fig. 2 shows a detail of the $i$th integrator block. A two-phase clock signal is used to control the analogue switches. The input switches are directly controlled by one of the phases (the even clock phase) and the switches connected to the op-amp negative input lead are controlled by the outputs of the constraint block. These outputs are defined during the odd clock phase. By elementary analysis involving charge conservation principles it is clear that the circuit in Fig. 2 implements eqn. 6. The summer block appearing in Fig. 1 can be implemented by using techniques reported elsewhere.[7]

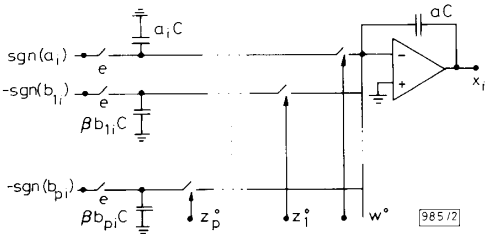


**Fig. 2** *Detail of integrator block*

*Practical results:* The proposed circuit has been computer simulated using DIANA[8] and a detailed macromodel for the op-amps.[9] The simulated programming problems are listed in Table 1, where both the theoretical solution and the one computed by DIANA are shown for every example. Also included in Table 1 is the number of clock periods required for the circuit to reach its final state. In all the cases, the initial state was the origin of the program variable space. As can be seen it is possible to obtain a very approximate solution in relatively few clock periods.

*Conclusions:* A circuit structure is proposed for implementing linear programming problems using switched-capacitor techniques. This structure is based on a reduced set of basic cells that are interconnected following a dense regular pattern. The resulting circuits exhibit a very high modularity and in this sense can be considered as members of the general family of analogue neural networks. The method is valid for any linear programming problem and is also suitable for monolithic implementation, a significant advantage as compared to previous analogue neural linear programming solvers.[1,2]

*Acknowledgments:* This research has been supported by Spanish CICYT under contract no. ME87-0004.

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*9th February 1988*

**Table 1** THEORETICAL AND SIMULATION RESULTS FOR TWO PROBLEMS

| Scalar function and constraints | Theoretical solution | Simulated solution using DIANA | Number of clock periods |
|---|---|---|---|
| $\Phi = v_1 + v_2$<br>$f_1 = 35/12 - (5/12)v_1 + v_2$<br>$f_2 = 35/2 - (5/2)v_1 - v_2$<br>$f_2 = 5 + v_1$<br>$f_2 = 5 - v_2$ | $v_1 = -5$<br>$v_2 = -5$ | $v_1 = -4{\cdot}99 \pm 0{\cdot}03$<br>$v_2 = -5{\cdot}03 \pm 0{\cdot}08$ | 40 |
| $\Phi = 3v_1 + (1/2)v_2 - (1/2)v_3$<br>$f_1 = 6 + v_1 + v_2 + v_3$<br>$f_2 = 6 - v_1 - v_2 - v_3$<br>$f_3 = 6 + v_1 + v_2 - 2v_3$<br>$f_4 = 6 - v_1 - v_2 + 2v_3$<br>$f_5 = 6 + v_1 - 2v_2 + v_3$<br>$f_6 = 6 - v_1 + 2v_2 - v_3$ | $v_1 = -6$<br>$v_2 = 0$<br>$v_3 = 0$ | $v_1 = -5{\cdot}88 \pm 0{\cdot}3$<br>$v_2 = -0{\cdot}04 \pm 0{\cdot}11$<br>$v_3 = -0{\cdot}01 \pm 0{\cdot}15$ | 40 |



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## HIGH-CURRENT PULSE-DOPED GaInAs MESFET


*Indexing terms: Semiconductor devices and materials, Field-effect transistors, Gallium compounds*



We report the DC and microwave performance of pulse-doped GaInAs power MESFETs. For a 0·7 $\mu$m gate-length device, a maximum drain-current density of 870 mA/mm and a peak transconductance of 325 mS/mm were measured. A maximum stable gain of 11·7 dB at 26 GHz, and an extrapolated $f_t$ of 33 GHz were obtained. These values are the highest reported for MESFETs having gates as long as 0·7 $\mu$m.


Power amplifiers based on GaAs/AlGaAs HEMTs suffer from low drain-saturation current. Recently, multichannel and pseudomorphic HEMTs have been developed to increase current densities,[1–4] but the low thermal conductivity of the GaAs substrate limits the maximum achievable power of these devices. Improved performance can be obtained by using AlInAs/GaInAs heterostructure FETs, which combine high mobility with high sheet-carrier concentration. In addition, the InP substrate offers higher thermal conductivity than GaAs. The microwave performance of AlInAs/GaInAs HEMTs is beginning to surpass that of GaAs/AlGaAs HEMTs.*[5] We recently reported $n^+$-pulse-doped GaInAs MESFETs of 0·7 $\mu$m gate length with excellent maximum stable gains of 14 dB at 26·5 GHz, and a maximum frequency of oscillation of greater than 100 GHz.[6] In this letter, we report the fabrication and performance of $n^+$-GaInAs-channel MESFETs with both high current densities and high gains.

The pulse-doped GaInAs MESFET structure was grown by MBE on a semi-insulating InP substrate. The device structure consisted of a 2500 Å AlInAs buffer layer, 100 Å of undoped GaInAs, a 200 Å $n^+$-GaInAs layer, 500 Å of undoped AlInAs, and a 100 Å $n^+$-GaInAs cap. All the layers were lattice matched to InP. The undoped AlInAs layer reduces the gate leakage current and increases the barrier height. We have grown three structures with varying electron concentration. For the first structure (48N), a Hall mobility of 4100 $cm^2/Vs$ with an electron concentration of $4·8 \times 10^{12}$ $cm^{-2}$ was measured at 300 K. A Hall mobility of 4100 $cm^2/Vs$ with an electron concentration of $5·8 \times 10^{12}$ $cm^{-2}$ was measured for the second structure (58N). We have measured for the third structure (80N) sheet concentrations as high as $8 \times 10^{12}$ $cm^{-2}$ with mobilities of 3500 $cm^2/Vs$.

The processing of these MESFETs was similar to that reported previously.[6] The MESFETs had a gate length of 0·7 $\mu$m with a 4·0 $\mu$m source/drain spacing. The $I/V$ characteristics of 58N-structure MESFET having a 100 $\mu$m gate width are shown in Fig. 1. A drain saturation current of 870 mA/mm and complete pinch off at a gate voltage of −3·5 V is achieved. For the 48N structure MESFET, a drain current of 680 mA/mm with a pinch off voltage of −3·0 V was measured. For devices on the 80N-structure with a sheet concentration of $8·0 \times 10^{12}$ $cm^{-2}$, we measured currents as high as 1·0 A/mm but they could not be pinched-off. Fig. 2 shows the variation of the transconductance with gate voltage for the 58N-structure MESFET. The large bandgap AlInAs confines the carriers in the channel, resulting in the broad peak in the transconductance against gate voltage and improved linearity for high-power FETs. Extrinsic transconductances as high as 325 mS/mm were achieved. For the 48N-structure MESFETs, we achieved transconductances between 250 and 310 mS/mm. A gate/drain breakdown voltage of 3·2 V was measured at a leakage current of 0·5 $\mu$A/$\mu$m of gate width for the 58N structure. Higher breakdown voltages can be obtained with thicker undoped AlInAs layers, but at a sacrifice of transconductance.

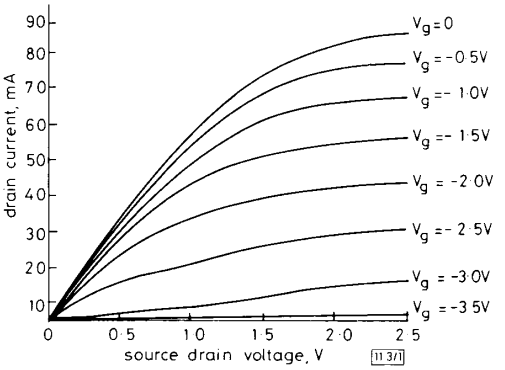


**Fig. 1** *I/V characteristics of a pulse-doped GaInAs MESFET*

The microwave performance of these MESFETs for different source/drain voltages and gate voltages was measured over the frequency range 0·5–26·5 GHz using an automated Cascade wafer probe and an HP 8510 network analyser. Fig. 3 is a plot of the maximum stable gain (MSG) against frequency computed from the measured $S$-parameters. An MSG of 11·7 dB at 26·0 GHz and an extrapolated $f_{max}$ of over 100 GHz was obtained. The current gain was also computed from the measured $S$-parameters. Extrapolating a 6 dB/octave roll-off, a current-gain cutoff frequency ($f_t$) of 33 GHz was obtained. The microwave-gain measurements were performed both before and after isolating the gates from the edge of the mesa.* After gate isolation, we measured an increase in the MSG, which we attributed to a decrease in the gate-leakage current.

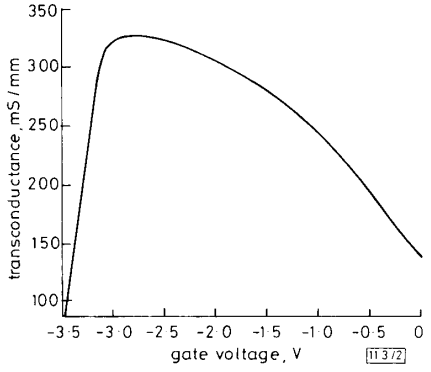


**Fig. 2** *Transconductance against gate voltage for pulse-doped GaInAs MESFET*

* FATHIMULLA, A., ABRAHAM, J., and LOUGHRAN, T.: 'High performance InGaAs/InAlAs HEMTs and MESFETs'. Submitted for publication (*IEEE Electron. Device Letts.*)




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