A Mixed-Signal Integrated Circuit for FM-DCSK Modulation

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***Abstract*—This paper presents a mixed-signal application-specific integrated circuit (ASIC) for a frequency-modulated differential chaos shift keying (FM-DCSK) communication system. The chip is conceived to serve as an experimental platform for the evaluation of the FM-DCSK modulation scheme, and includes several programming features toward this goal. The operation of the ASIC is herein illustrated for a data rate of 500 kb/s and a transmission bandwidth in the range of 17 MHz. Using signals acquired from the test platform, bit error rate (BER) estimations of the overall FM-DCSK communication link have been obtained assuming wireless transmission at the 2.4-GHz ISM band. Under all tested propagation conditions, including multipath effects, the system obtains a BER $= 10^{-3}$ for E_b/N_o lower than 28 dB.**

***Index Terms*—Application-specific integrated circuits (ASICs), mixed analog–digital integrated circuits, spread-spectrum communication.**

I. Introduction

CHAOTIC signals exhibit broadband continuous spectra and are hence adequate to be used as communication carriers in spread-spectrum applications. On the one hand, using these signals enables spreading to be accomplished concurrently with modulation, with no extra processing step needed [1], [2]. On the other hand, since the signals, generated either by different chaos generator instances or by a single generator instance with different initial conditions, are almost uncorrelated (orthogonal), chaos-based communications enable multiple access capability [2]–[5]. Finally, the nonperiodicity and long-term unpredictability of chaotic signals confer these communication systems a certain level of security in a cryptographic sense [5], [6].

During recent years, different approaches have addressed the use of chaos for communications. Among them, the frequency-modulated differential chaos shift keying (FM-DCSK) technique has deserved considerable attention. Advantages of this technique include precise control of the spectral profile and processing gain of the transmitted signal, and increased robustness against multipath effects and channel imperfections [2]. It has also been demonstrated that FM-DCSK communication systems are tolerant to jamming attacks [7]. Furthermore, they can coexist with narrow-band conventional systems whose frequency bands fall within those of the chaos-based system [8]. These appealing features are complemented with the low complexity of the demodulation scheme, which makes these systems appropriate for low-cost, low-to-medium performance applications. Currently, enhancements of the basic FM-DCSK modulation scheme are being explored to increase transmission data rates and to exploit the underlying determinism of chaotic dynamics for improved noise performance [9]–[11].

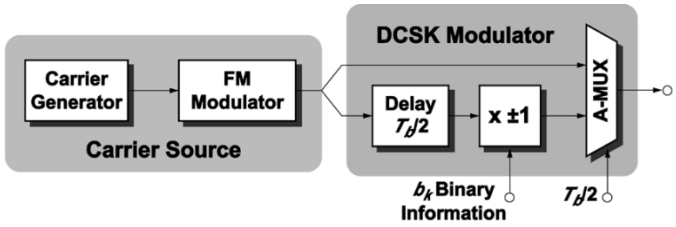

Fig. 1. Conceptual diagram of an FM-DCSK modulator.

The application-specific integrated circuit (ASIC) presented in this paper demonstrates that FM-DCSK can be efficiently and robustly implemented in silicon—a remarkable precedent of a quasi-chaotic FM-DCSK radio system using an FPGA baseband section can be found in [12]. It has been fabricated in a two-poly three-metal 0.35-μm CMOS technology, operates from a 3.3-V supply, and consumes less than 100 mW. This ASIC is a programmable device which embeds all the nonstandard functions required for FM-DCSK modulation, i.e., all the functions related to the generation and handling of the chaotic signals. Programming capabilities refer to the most critical parameters of the modulation; namely chip rate, transmission bandwidth, and spreading characteristics. Taking advantage of these programming features, the ASIC has been used as the core of a test platform to evaluate FM-DCSK performance for different settings and propagation conditions.

This paper is organized as follows. Section II briefly describes the FM-DCSK modulation concept, presents the target specifications of the test platform (derived from a typical wireless local area network application), and outlines the architecture of the modulator with emphasis on the designed ASIC prototype and its interface to other off-chip elements of the demonstrator. Section III focuses on the analog part of the ASIC. In particular, the basic topology, the switched-capacitor (SC) schematics and the building block implementations on the carrier generator are described. Considerations on the required accuracy of the building blocks and the robustness of the chaotic oscillations are presented in [13]. Section III also gives experimental measurements on the performance of the carrier generator, which can be made externally accessible for test purposes through dedicated circuitry. Section IV shows experimental results from the test platform illustrating the operation of the FM-DCSK modulator, and highlights the different programming features of the

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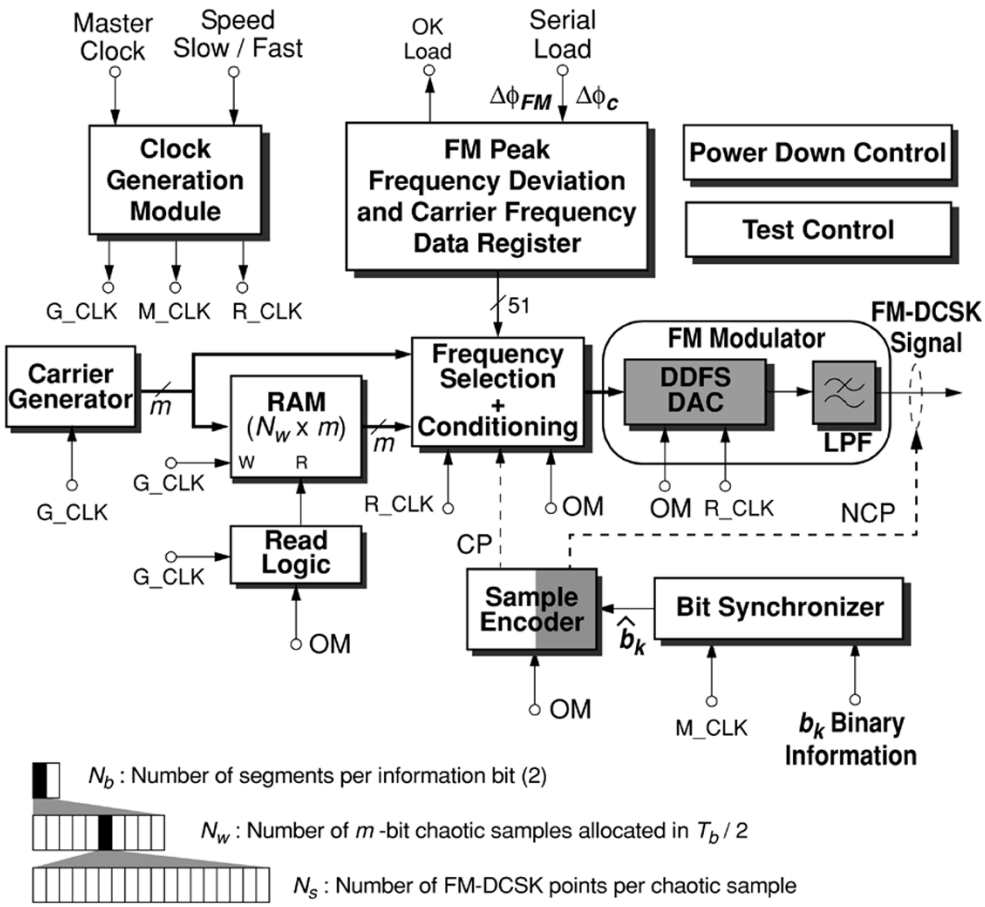

Fig. 2. Simplified block diagram of the proposed FM-DCSK modulator. The output of the carrier generator takes the form of an m-bit long digital word. The shaded blocks are implemented off-chip. The sample encoder block operates external to the chip or not, depending on the selected operation mode, NCP or CP, respectively.

ASIC. Section V provides estimations of the bit error rate (BER) of the FM-DCSK communication under multipath propagation environments, based on signals acquired from the test platform. Such estimations have been obtained by computer simulation with tapped delay line channel models for indoor applications, recommended by the Personal Communication System Joint Technical Committee (PCS JTC) [2], [14]. Finally, Section VI concludes the paper.

II. FM-DCSK Modulation Concept and Architecture

Fig. 1 shows the conceptual diagram of a binary FM-DCSK modulation scheme [2]. Every incoming binary data b_k is mapped onto two sample functions of duration $T_b/2$ (T_b denotes the time slot of a bit), which are transmitted one after the other. The first sample function is a reference signal while the second one conveys the information. Depending on whether the information symbol is either '1' or '0', the second sample function is either an exact replica or an inverted version of the reference signal, respectively. If sample functions are obtained from a chaos generator, the above operation defines a generic DCSK modulation process. In the case of FM-DCSK, chaotic sample functions are FM modulated (with center frequency f_c and peak frequency deviation Δf) prior to undergoing the DCSK operation [15].

The designed ASIC includes only the modulation tasks; i.e., those tasks which involve the generation and handling of the chaotic signals. A core component of the ASIC is the carrier generator which employs sampled-data models and circuits to deliver m-bit quantized chaotic digital outputs. Demodulation tasks are not included in the ASIC because they can be accomplished by using a conventional noncoherent correlation receiver [2].

Fig. 2 shows the block diagram of the FM-DCSK modulator platform which makes use of the herein designed ASIC. This block diagram is a modified version of Fig. 1 in which DCSK modulation is accomplished in two stages, namely, sample function generation, on the one hand, and concatenation and controlled sign inversion, on the other. The two operations in this latter stage, which will be jointly referred to as sample encoding, can be realized either after FM modulation or before FM modulation. This choice defines two different operation modes denoted as non-continuous phase (NCP) and continuous phase (CP), respectively. The purpose of separating the DCSK modulation into two stages is to translate the delay operation involved in the process of sample generation (the most critical function in terms of timing accuracy) to lower frequencies, namely, at the chip rate of the chaos generator.

Most of the operations of the FM-DCSK platform are embedded into the ASIC. Only the shaded blocks in Fig. 2

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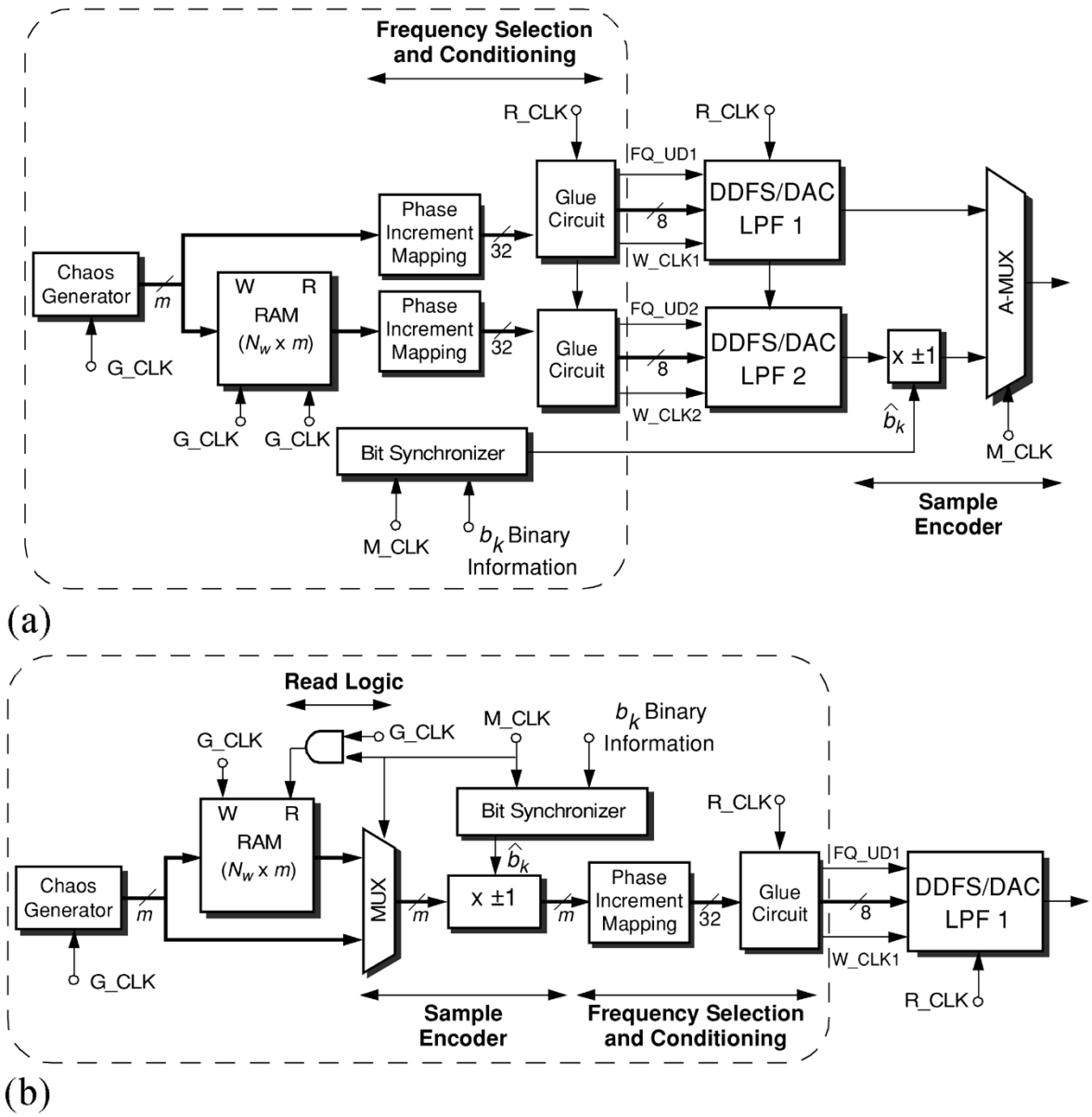

Fig. 3. Supported operation modes for FM-DCSK modulation. (a) NCP mode and (b) CP mode. The blocks inside the dashed boxes are implemented on-chip.

are off-chip. They include the sample encoder in the NCP operation mode and the FM-modulation block. This latter block is implemented by commercial direct digital frequency synthesizers (DDFS) with embedded digital-to-analog (D/A) converters [16], followed by passive low-pass reconstruction filters. The DDFS/DAC operates with a system reference clock of $f_{R\_\mathrm{CLK}} = 180$ MHz. This reference clock determines the frequency $f_{\mathrm{out},i}$ of the output signal of the DDFS/DAC according to the following expression [16]:

$$V_{\mathrm{out},i} = (\Delta P_i \cdot f_{R\_\mathrm{CLK}})/2^{32} \tag{1}$$

where ΔP_i represents the decimal value of a 32-bit phase increment tuning word. Taking into account (1), the m-bit length digital output of the chaos generator can be regarded as a phase increment which, after processing, must be uniquely mapped into the tuning word ΔP_i.

With the exception of the carrier generator, which is a mixed-signal circuit, the building blocks of the ASIC are digital. For instance, the delay operation is implemented by using a programmable RAM as shown in Fig. 2. In the write phase, the m-bit digital word generated by the carrier generator is stored, row by row, in the RAM memory at a rate determined by the clock frequency of the chaos generator, f_{G_CLK}. In the read phase, the digital words stored in the RAM are sequentially read out in the same order as they were written into the memory. Row selection during the read and write phases are easily accomplished with an N_w-bit binary counter and a decoder, where N_w represents the number of chaotic samples allocated in $T_b/2$.

Those blocks in Fig. 2 controlled by signal OM (Operation Mode) are reconfigurable, and vary depending on whether the NCP or CP mode is enabled. Both configurations are detailed in Fig. 3. The NCP mode, illustrated in Fig. 3(a), is an implementation of the FM-DCSK modulator functionally equivalent to the scheme of Fig. 1, as originally proposed in [2]. It uses two different paths for the reference and (delayed) information-bearing segments, and sample encoding is accomplished

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after FM modulation. Note that FM modulation requires two different DDFS/DAC blocks, one for each path. In this configuration there are noncontinuous transitions among frequency modulated sample functions because encoding is accomplished off-chip in the amplitude domain. This explains the NCP term used for this operation mode. Samples concatenation is realized by a 2-input multiplexer controlled by M_CLK, the underlying clock of the output data, and programmable sign inversion is implemented by an analog amplifier with gain $+1$ or -1 depending on bit $\hat{b}_k$ (this is a version of the information bit b_k aligned to the edges of M_CLK by means of a bit synchronizer). In the NCP mode, the RAM works as a first-in first-out (FIFO) memory, and the logic circuitry used to read the data stored in the RAM is reduced to a wired connection to the G_CLK clock. The frequency selection and conditioning circuit to drive the off-chip DDFS/DACs consists of two sets, composed by a phase increment mapping circuit and a glue logic block, for each of signal paths. The phase increment mapping block performs the arithmetic operations (multiplication and addition) required for the calculation of ΔP_i in (1), in terms of its m-bit input digital word $\Delta\phi_i$. Depending on the path, this word comes directly from the chaos generator or from the RAM memory. The operation of this block is simply given by

$$\Delta P_i = \Delta\phi_c + \Delta\phi_{\mathrm{FM}} \times \Delta\phi_i \tag{2}$$

where $\Delta\phi_c$ is a 31-bit phase increment digital word corresponding to the center frequency f_c of the FM modulation, and $\Delta\phi_{\mathrm{FM}}$ is a 20-bit phase value which determines the peak frequency deviation Δf, according to

$$\Delta f = (\Delta\phi_{\mathrm{FM}} \cdot f_{R\_\mathrm{CLK}})/2^{32-(m+1)}. \tag{3}$$

As shown in Fig. 2, digital words $\Delta\phi_c$ and $\Delta\phi_{\mathrm{FM}}$ must be serially loaded into a register before FM-DCSK modulation starts (a flag signal reveals if incorrect data are loaded). The glue logic block converts the output of the phase increment mapping circuit, which is in parallel 32-bit format, into five serial 8-bit words (one of them added for control), in order to make data compatible with the input format of the DDFS/DAC [16]. Signals FQ_UDx and W_CLKx, also provided by the glue logic block, are used for the validation and loading control of sequences, as shown in Fig. 3.

In the CP mode, illustrated in Fig. 3(b), the ASIC implements a modification of the original FM-DCSK modulator which uses a single path for both the reference and information-bearing segments, thus saving considerable hardware as compared to the NCP operation (a single DDFS/DAC and its corresponding frequency selection and conditioning blocks are required). Blocks that are not used in the CP mode, both inside and outside the ASIC, are disabled by a power-down control circuitry integrated in the chip. In this configuration, samples encoding is accomplished on-chip in the phase domain, which guarantees continuous transitions among frequency modulated sample functions. The logic circuitry used to read the RAM differs from that of the NCP mode. In this case, data stored are only read when M_CLK is in the high state, i.e., during the time slot of the second sample function associated to bit $\hat{b}_k$. In Fig. 3(b), this is simply accomplished by an AND gate. Sample concatenation is realized by a digital multiplexer, controlled by M_CLK, which takes alternatively segments from the chaos generator and the RAM. Programmable sign inversion is realized by selectively altering, depending on bit $\hat{b}_k$, the sign of input $\Delta\phi_i$ in the phase increment mapping block. Regarding (2), this is equivalent to altering the sign of the second term in the right-hand side of the equation, according to the logic level of $\hat{b}_k$. On the receiver side of the FM-DCSK system, this makes it possible to carry out an unbiased estimation of the transmitted bit, similar to what happens in the NCP operation mode [2]. The price of this notable hardware simplification at the modulator is a modest increase in complexity on the receiver side of the FM-DCSK system, which in CP mode requires a frequency detector before the auto-correlation process (as occurs in some Bluetooth receiver implementations [17]–[19]).

TABLE I
NOMINAL OPERATION CONDITIONS OF THE FM-DCSK MODULATOR

Speed operation mode	slow	fast
Bit duration T_b	2μs	
Master clock frequency, $f_{\mathrm{R\_CLK}}$ (MHz)	180	
Clock of the chaos generator, $f_{\mathrm{G\_CLK}}$ (MHz)	10	15
FM center frequency, f_c (MHz)	36	
FM peak frequency deviation, Δf (MHz)	8.5	7.8

Specifications for the FM-DCSK modulator ASIC are based on those of a commercial direct sequence baseband processor designed to IEEE Standard 802.11(1999 E) [20]. Two nominal operation conditions have been defined. They are summarized in Table I and denoted as slow and fast speed modes, respectively. They differ on the transmission bandwidth $2\Delta f$, and the clock frequency of the chaos generator, f_{G_CLK}, (obtained by the programmable frequency division of a $f_{R\_\mathrm{CLK}} = 180$ MHz system clock). Assuming that the output data rate is fixed at 500 kb/s ($T_b = 2\ \mu$s and clock M_CLK is obtained by the frequency division of R_CLK by 360), altering the chip rate of the chaos source modifies the number of frequency hops N_s per sampled chaotic segment according to

$$N_s = \frac{f_{R\_\mathrm{CLK}}}{f_{G\_\mathrm{CLK}}} \tag{4}$$

and, hence, N_s amounts to 18 in the slow speed mode and 12 in the fast case. On the other hand, the number N_w of chaotic samples allocated in $T_b/2$ is given by

$$N_w = \frac{f_{G\_\mathrm{CLK}}}{N_b \cdot f_{M\_\mathrm{CLK}}} \tag{5}$$

where $N_b = 2$ represents the number segments per information bit. From (5), $N_w = 10$ in the slow speed mode and 15 in the fast case. For illustration purposes, at the bottom of Fig. 2, a conceptual timing diagram of the modulator operated in the slow speed mode is shown.

As it is demonstrated in [2], the product $2\Delta f T_b$ is critical on the noise performance of the FM-DCSK communication scheme. For a given bit duration T_b, decreasing the RF transmission bandwidth improves the noise performance of the

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system, i.e., the BER over an additive white Gaussian noise (AWGN) channel lowers; however, it simultaneously degrades the multipath performance. Data in Table I offer a good tradeoff between processing gain and multipath tolerance [21], and because of the availability of theoretical and simulation results [2], [21], the experimental results taken from the test platform can be easily contrasted.

III. Carrier Generator

The carrier generator in the proposed FM-DCSK modulator platform provides an m-bit quantized digital output from an analog chaotic waveform which is internally generated in fully autonomous manner. This section discusses the architecture and circuit implementation of this block. Also, Section III-D presents experimental measurements on the performance of the carrier generator when isolated through proper setting of the embedded test control block.

A. Architecture

Fig. 4 shows the conceptual block diagram of the mixed-signal carrier generator implemented in the ASIC. It can operate either in externally-driven mode (signal O/C in the 'high' state) or in autonomous mode (signal O/C in the 'low' state). The former is selected during analog calibration at start-up. It is also selected when the block is used as a conventional analog-to-digital (A/D) interface to an external carrier $V_{\rm ext}$; in such a case, the signal ϕ_s defines the loading interval.

In autonomous mode, the circuit can be seen as a cyclic redundant signed digit (RSD) A/D converter (ADC) [21], modified in such a way that the input of the sample-and-hold (S/H) block is permanently connected to the output of the residue amplifier. Owing to such a modification, the feedback loop enters in chaotic regime and the output of the S/H amplifier wanders randomly along the signal range $[V_{R-}/2, V_{R+}/2]$ with uniform probability in the nominal case [13] ($V_{R-}/4$ and $V_{R+}/4$ are the lower and upper threshold levels of the coarse ADC, and voltages V_{R-} and V_{R+} are referred to ac ground). This feature guarantees a uniform spreading of the information and, hence, a balanced coverage of the transmission band.

The digital correction logic (DCL) block in Fig. 4 combines the most recent r-bit codes provided by the coarse ADC and those obtained in previous iterations to synthesize the m-bit digital quantized versions of the analog iterations. Its operational principle closely follows that of DCL blocks for pipeline ADCs [22]. After DCL operation, the reconfiguration logic (RL) block, a piecewise-linear digital FIR filter, can be used to modify the statistical properties of the digitally corrected words [13]. This is illustrated in Fig. 5, which shows the return maps and the power spectra experimentally obtained at the input [Fig. 5(a)] and output [Fig. 5(b)] of the RL block (for a 25-MHz clock). The parameters used in the prototype are $r = 2, m = 10$, and a nominal gain of the residue amplifier $A = 2$. In both cases shown in Fig. 5, the signals remain uniformly distributed. However, their spectra are quite different. Namely, that obtained after RL processing shows a flat white noise-like profile [Fig. 5(b)] instead of a high frequency excess-noise characteristic [Fig. 5(a)]. In the ASIC, the RL block can be either bypassed or enabled

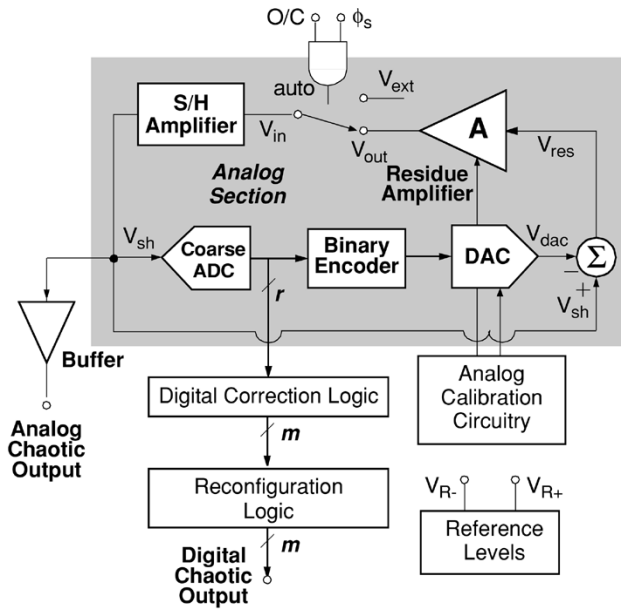

Fig. 4. Block diagram of the carrier source implemented in the ASIC.

and, hence, two different carrier signals are available. They will be called in the following the H-type carrier (for highpass-like spectrum, RL block disabled) and F-type carrier (for flat-like spectrum, RL block enabled).

B. Switched-Capacitor Implementation

The analog part of the carrier generator, shown in the shaded area in Fig. 4, has been implemented using fully differential SC circuits operating at 25 MHz (a dedicated clock input is enabled for testing the carrier generator alone). In the autonomous mode (signal auto permanently in the 'low' state), reference voltages are $V_{R+} = 1$ V and $V_{R-} = -1$ V, and the trapping region of the chaotic oscillations becomes 2 Vp-p differential. Fig. 6 shows the schematic of the SC circuit in which the square boxes are symbolic representations of analog switches and the label inside each box indicates the clock phase during the ON state. Two major blocks can be identified in Fig. 6, namely, a flip-around sample-and-hold amplifier and a 1.5-bit MDAC—similar to those used in pipelined ADCs [23]. The schematics depicted in Fig. 6 have been chosen because they are advantageous versus alternative circuits in terms of kT/C noise, distortion introduced by amplifier gain variation, and power dissipation for a given speed [23]. The amplifiers in both structures incorporate offset cancellation techniques which require the amplifiers to be connected in unity gain configurations during their respective sampling phases [24]. Regarding the two pairs of capacitors, C_1 and C_2, they have been implemented using trim arrays which can be calibrated to obtain a residue gain as close as possible to the nominal value of 2 [25].

The operation of the circuit in Fig. 6 is controlled by the two nonoverlapped clock-phases ϕ_1 and ϕ_2 shown at the bottom of the figure. Two delayed versions of the above phases, $\phi_{1\rm D}$ and $\phi_{2\rm D}$, are also used to suppress charge injection effects from bottom plate switches [25]. In the nonautonomous case, signal auto is determined by ϕ_s (see Fig. 4) which turns ON during a

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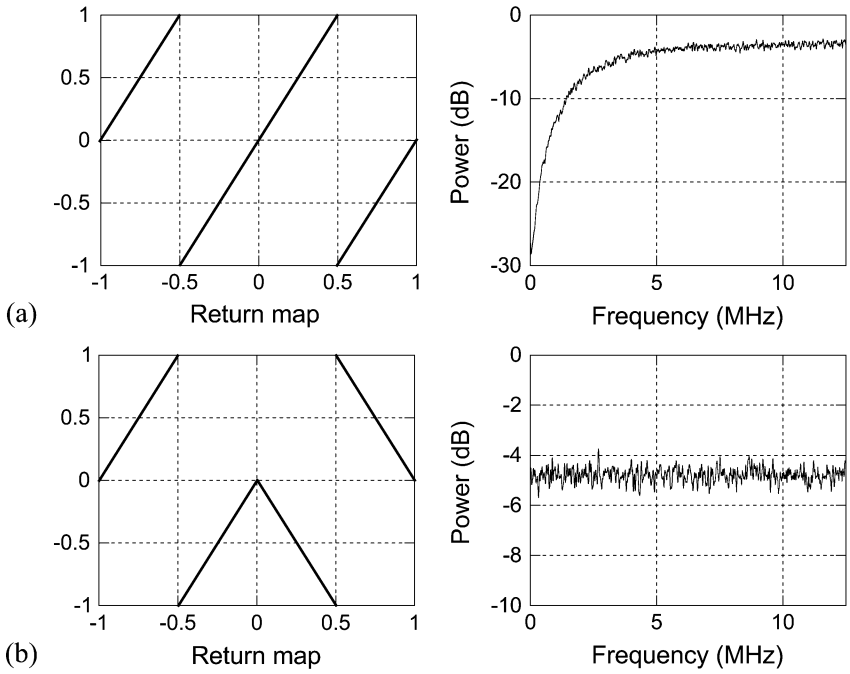

Fig. 5. Effect of RL processing. Experimental return map and power spectrum characteristic at (a) the DCL output signal and (b) the RL output signal.

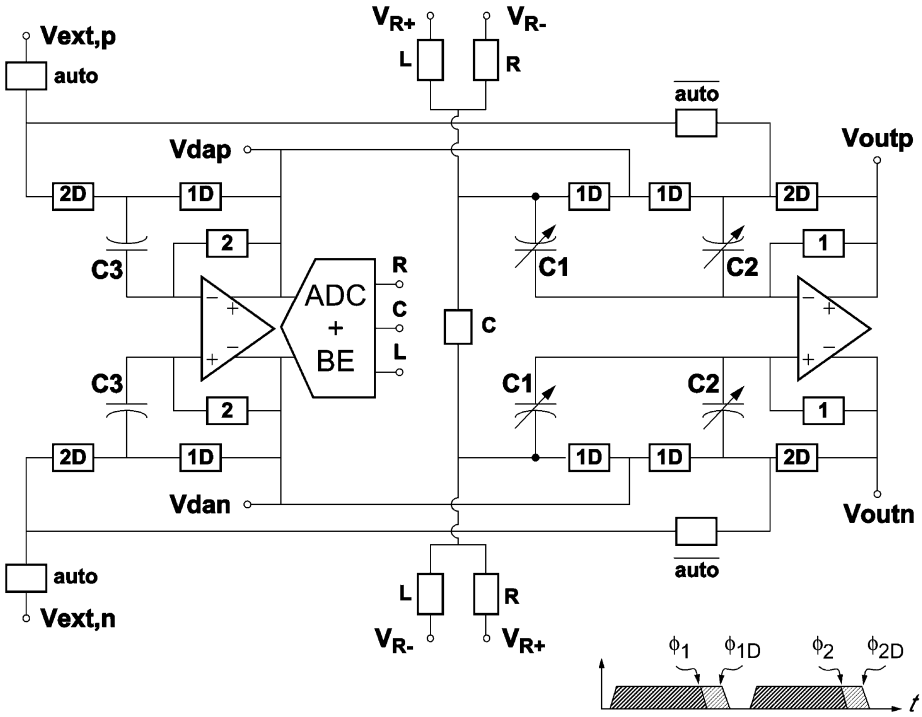

Fig. 6. SC implementation of the analog section of the chaos generator (shaded area).

first ϕ_{2D} phase, to load the external voltage $V_{\rm ext}$, and then remains OFF during the following ten clock periods in order for the cyclic converter to resolve the digital output. Signals L, C, and R are generated by the circuit of Fig. 7, formed by a coarse ADC, whose comparators are latched at the end of phase ϕ_{1D}, and a binary encoder (BE) (both blocks have been symbolically combined in Fig. 6). These signals are enabled during phase ϕ_{2D}, and exhibit a 1-out-of-3 format. The data bits MSB and LSB form the 2-bit digital word that feeds the DCL block in Fig. 4. Differential comparators at the front of the coarse ADC in Fig. 7 use an input SC differencing network followed by a preamplifier, as in [26]. The schematic of the differential comparator is shown in Fig. 8.

C. Building Blocks

The operational amplifiers for the S/H and MDAC use a two-stage cascode compensated architecture [22], [27]. Such a choice is dictated by the high output swing requirements and the demanding dc-gain and dynamic-performance specifications. Particularly, a very high slew rate is needed to deal

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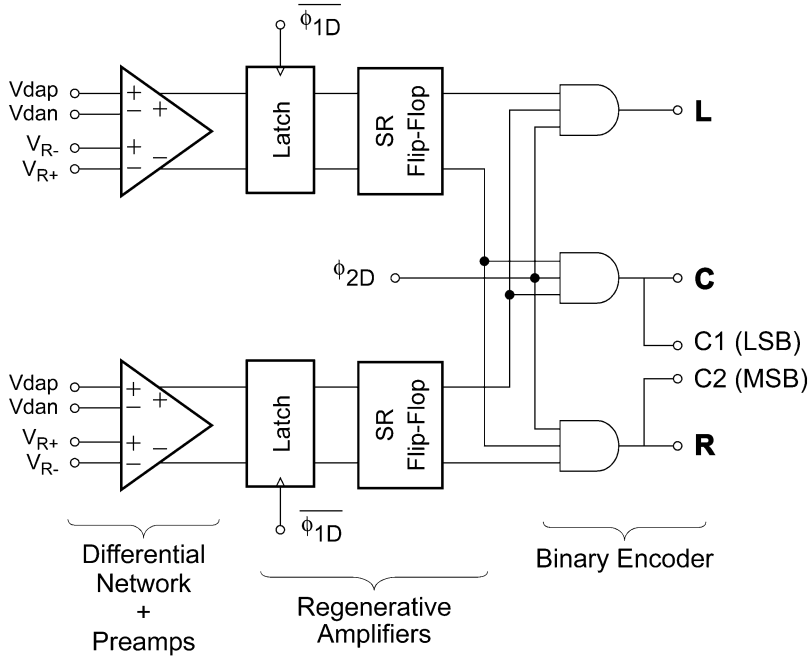

Fig. 7. Schematics of the coarse ADC and the binary encoder.

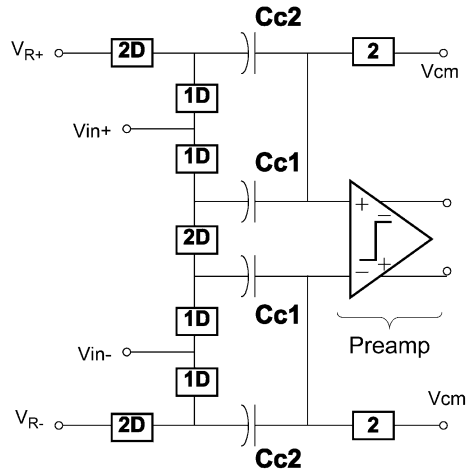

Fig. 8. Differential comparator (nominally, $\mathrm{Cc1} = 3 * \mathrm{Cc2}$).

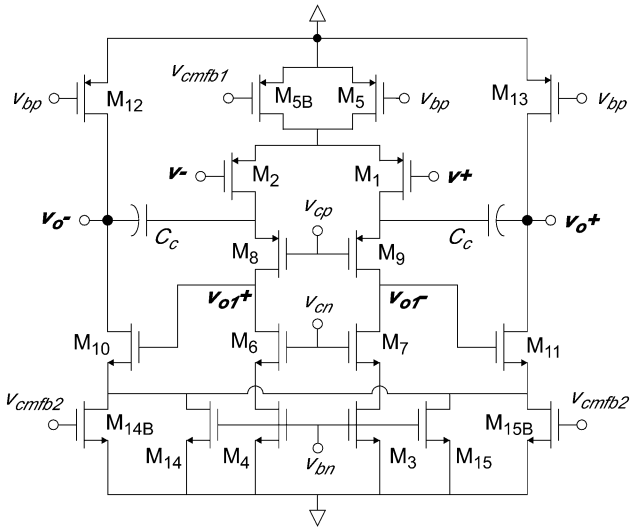

Fig. 9. Schematic of the operational amplifier used at the S/H and MDAC stages.

with the occasional large jumps of the chaotic waveform [13]. Fig. 9 shows the amplifier schematic. It consists of a telescopic first stage and a fully differential second stage. A dynamic SC common-mode feedback (not shown in Fig. 9) is used to define the voltages of the high impedance output nodes V_{o1+} and V_{o1-}.

The telescopic topology has a number of advantages over its folded-cascode counterpart, namely, fewer noise-contributing devices, fewer current legs, and wider bandwidth for a given current level. Note that the input transistors are pMOS. On the one hand, using these transistors allow us to cancel the body effect of the input transistors and, hence, to reduce the substrate noise coupling [29]. On the other hand, $1/f$ noise of nMOS devices available in the used technology is considerably larger than that of pMOS ones.

The second stage of the amplifier employs a fully differential structure, instead of a quasi-differential common-source structure. This is dictated by different considerations. On the one hand, having a tail-current device eliminates the need for a power-hungry inversion stage for the common-mode feedback amplifier [28]. This enables the use of a dynamic switched-capacitor common-mode feedback circuit, as in the first stage, which does not dissipate any static power. On the other hand, the fully differential second stage amplifier also eliminates the need for a dynamic level shift between the output of the first stage and the input of the second stage. Finally, this fully differential topology improves the power-supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR).

The tail currents of both stages are provided to some extent by a fixed current source (through transistors Mx) and the rest by the common-mode feedback (through transistors MxB) for improved settling and stability.

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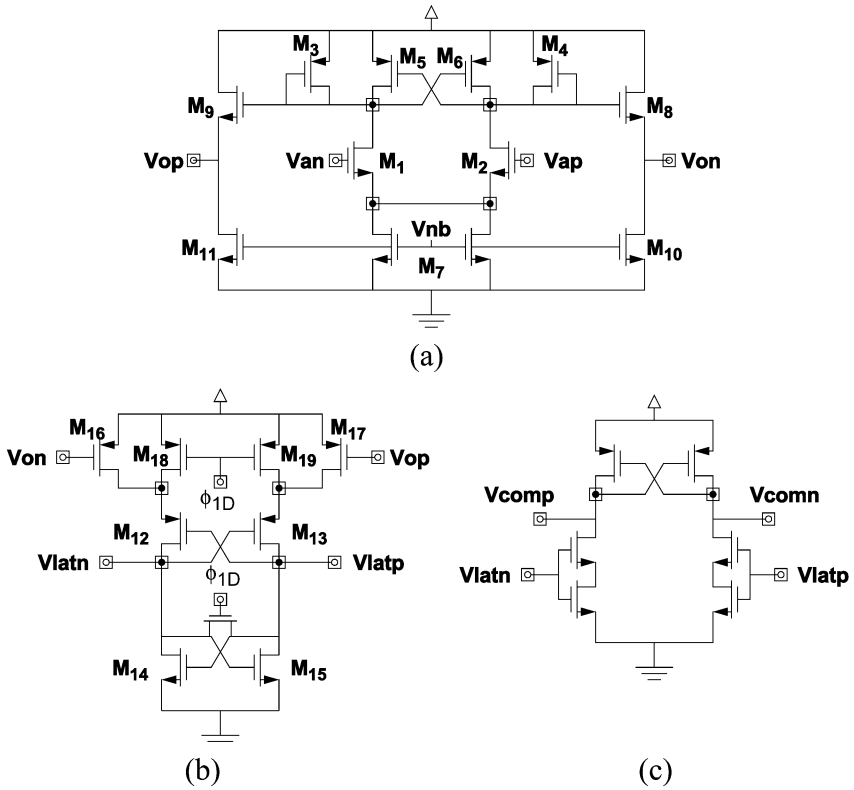

Fig. 10. Building blocks of the comparators in the coarse ADC. (a) Preamplifier. (b) Regenerative amplifier. (c) SR latch.

The design of the CMOS switches has been carried out with two main considerations in mind. First, the nonzero on-resistance has a large impact on the dynamics of the SC amplifiers, slowing down their transient response. Second, the switch on-resistance is highly dependent on voltage in low-voltage implementations. According to settling considerations, resistances in the range of 250 Ω can be tolerated in combination with the amplifier dynamics. In our process, such a value can be obtained using standard-threshold CMOS transmission gates, with no need for clock boosters. The sizes of the pMOS and nMOS devices are selected to equalize their transconductances, keeping the resistance of the transmission gate as linear as possible.

Fig. 10 shows the different building blocks of the comparators in the coarse ADC (see Figs. 7 and 8). They include a preamplifier with partial positive feedback [Fig. 10(a)] which attenuates the impact of common-mode interferences, a regenerative stage [Fig. 10(b)] and an SR latch [Fig. 10(c)]. In the regenerative amplifier, the small voltage imbalance created across the nMOS switch controlled by $\phi_{1\mathrm{D}}$ during the reset phase is rail-to-rail regenerated during the positive-feedback comparison phase. The latter starts when $\overline{\phi}_{1\mathrm{D}}$ goes high, thus making the latch react before the integrator output changes at the beginning of $\phi_{2\mathrm{D}}$. Different supply paths are used for the pre-amplifier and the regenerative latch in order to reduce the sensitivity to digital switching noise and supply bouncing.

Analog buffers in Fig. 4, employed to observe the chaotic waveforms generated by the carrier source, use slew-rate enhanced folded-cascode operational amplifiers with low input capacitance [31]. Other building blocks such as the reference voltage generator and the clock phase synthesizer and its drivers have been designed as in [32].

D. Measured Results

Fig. 11(a)–(b) shows the measured peak-to-peak differential nonlinearity (DNL) and integral nonlinearity (INL) of the converter as functions of the clock frequency. As may be observed, the DNL remains within ± 0.3 LSB (at 11-bit resolution) from 5 MHz to 30 MHz and notably degrades at 35 MHz. In the case of INL, the plots are confined to the range ± 1.25 LSB from 5 to 25 MHz. Fig. 12(a) and (b) presents the DNL and INL plots for a sampling frequency of 25 MHz. They correspond to the encircled bars of Fig. 11(a) and (b), respectively.

It is worth mentioning that both the DNL and the INL have been evaluated through a (full speed) *free-running code density test* [13], taking advantage of the autonomous operation of the generator. No external low-frequency sinusoidal input has been used during the tests, as occurs with conventional ADC testing. In the externally driven mode with a sinusoidal input of 5 MHz and a clock frequency of 20 MHz, the measured SNDR is 58 dB. The power consumption of the complete carrier generator, including the buffers for testing analog signals, is lower than 40 mW.

IV. Measured Results

Fig. 13(a) shows a microphotograph of the ASIC fabricated in a two-poly three-metal 0.35-μm CMOS technology. It occupies an active die area of 4.2 mm^2 and consumes less than 100 mW in the CP mode. The digital section of the ASIC, at the bottom of

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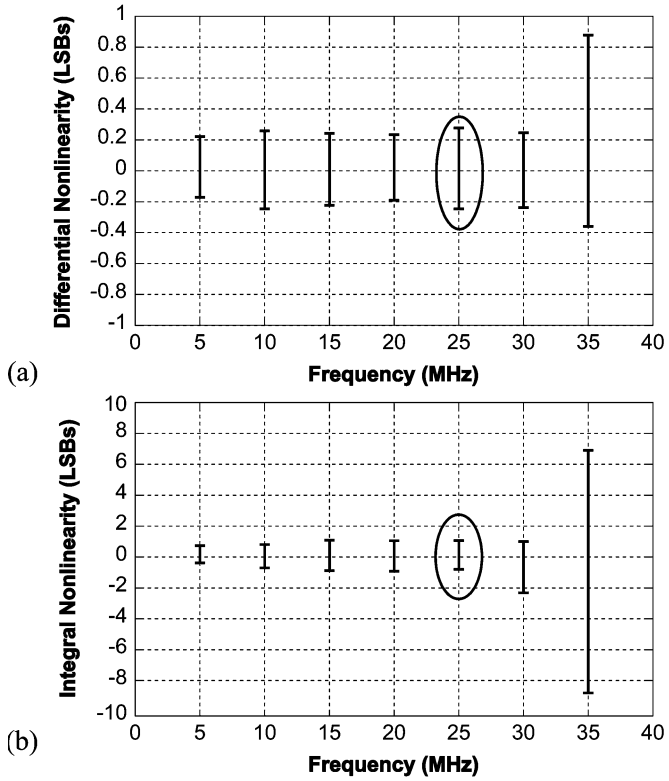

Fig. 11. (a) Peak-to-peak DNL and (b) INL characteristics (measured at 11-bit resolution) of the cyclic converter after calibration in terms of the clock signal.

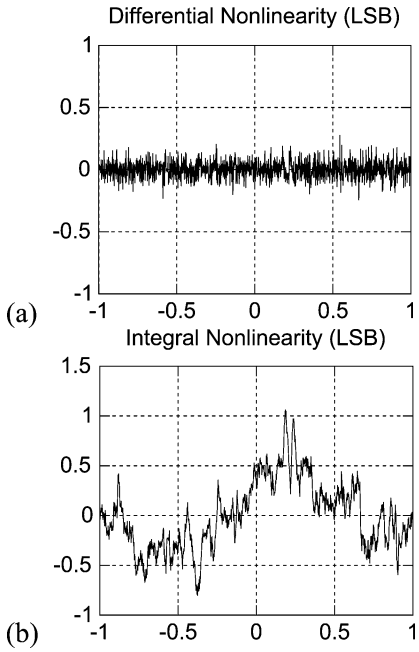

Fig. 12. (a) DNL and (b) INL plots of the carrier generator measured at 11-bit resolution for a sampling frequency of 25 MHz. They correspond to the encircled bars of Fig. 11(a) and (b), respectively.

the microphotograph, has been designed following a synthesis procedure from VHDL register transfer descriptions. The clock tree was optimized to meet the timing requirements, mainly the tight signaling interface between the ASIC and the DDFS/DAC blocks. Fig. 13(b) shows a picture of the test board.

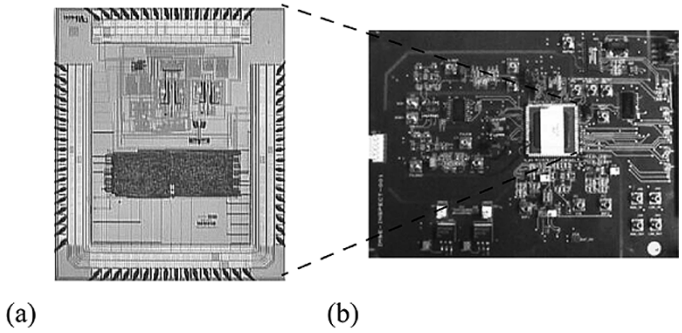

Fig. 13. (a) ASIC microphotograph. (b) FM-DCSK board.

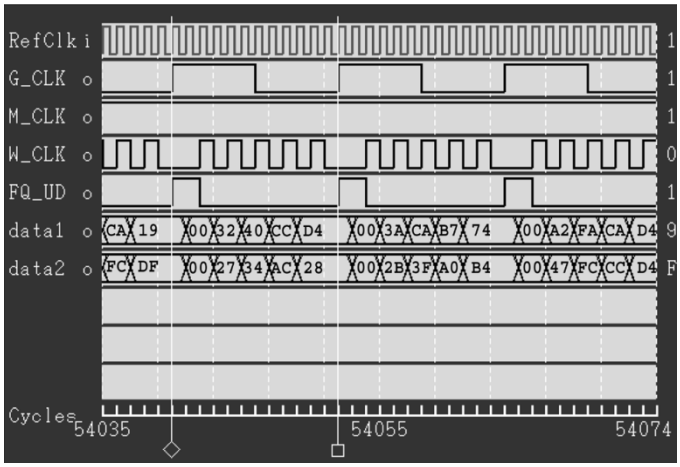

Fig. 14. Waveform display for DDFS/DAC write operation in the NCP mode at 15 MS/s rate, taken from HP82000. Data are in hexadecimal notation.

Some illustrative waveforms taken from the HP82000 automatic test equipment are displayed in Fig. 14, showing the DDFS/DAC write cycle for the NCP mode at a 15 MS/s rate. Every G_CLK cycle, the 32-bit output of the DCSK is translated into one 8-bit control word (00 in the data of the figure) plus four 8-bit data words. The five words are serially loaded onto the DDFS/DAC through five pulses in W_CLK signal and are uploaded with a final pulse in FQ_UD. This write operation must be done in one G_CLK cycle, 66 ns in the 15 MS/s fast rate mode.

An extensive experimental characterization of FM-DCSK signals, under all major operation settings, has been realized. As a major noticeable fact, it was found that the out-of-band spectrum profile is sharper (side lobes are smaller) in the CP operation mode than in the NCP mode under the same FM-modulation conditions, speed mode, and carrier selection. This can be explained because of the reduced envelope variation of the FM-DCSK signal in the former case—an additional advantage of the CP mode versus the NCP counterpart.

For illustration purposes, Fig. 15 shows the measured power spectra of synthesized FM-DCSK signals for a chip rate of 10 MS/s, CP operation mode and autonomous carrier generator with the RL block disabled (H-type waveforms). Those in Fig. 15(a) are obtained for an FM frequency deviation of 6.4 MHz, and an FM center frequency varying from 8 to 36 MHz at 7-MHz steps (available f_c tuning: 0–36 MHz at 0.04-Hz steps). Those in Fig. 15(b) are obtained for an FM

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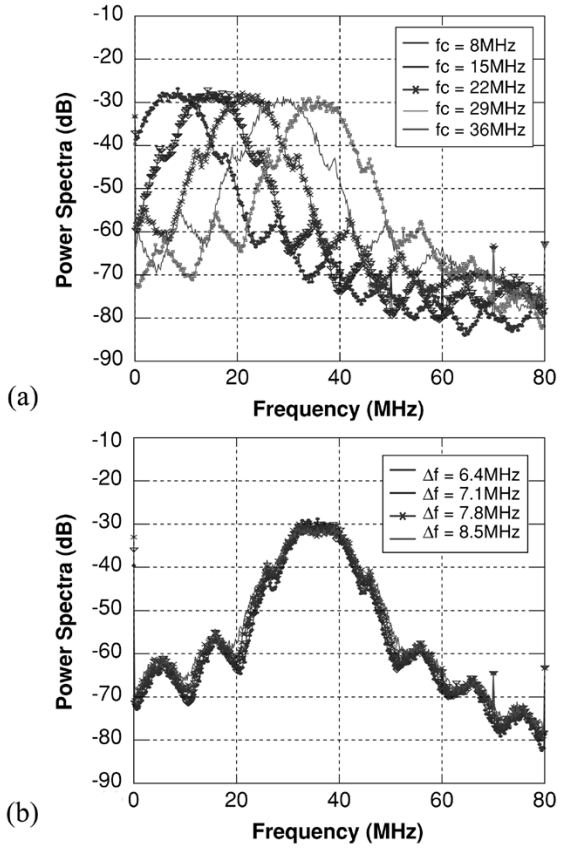

Fig. 15. Measured power spectra of synthesized FM-DCSK signals for a chip rate of 10 MS/s with H-type carriers. (a) Variation with FM center frequency. (b) Variation with FM frequency deviation.

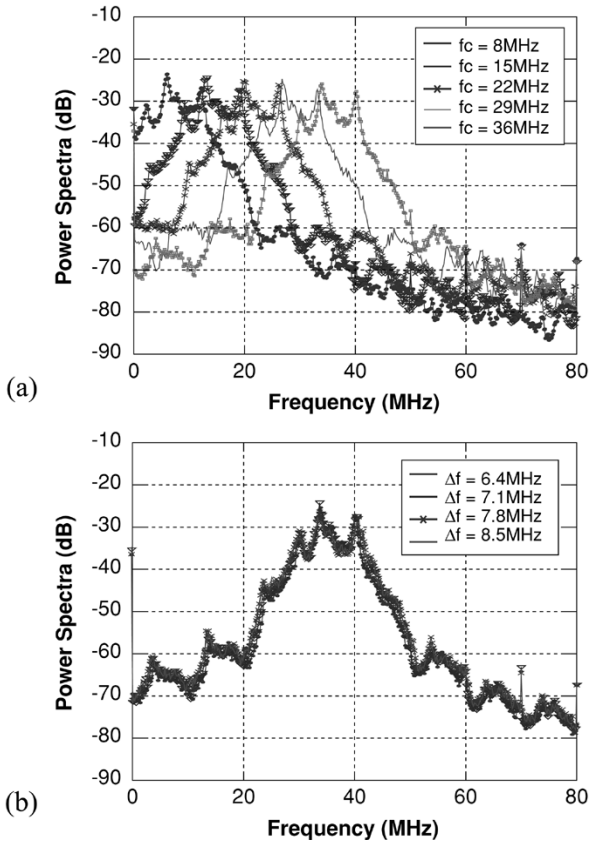

Fig. 16. Measured power spectra of synthesized FM-DCSK signals for a chip rate of 10 MS/s with F-type carriers. (a) Variation with FM center frequency. (b) Variation with FM frequency deviation.

center deviation of 36 MHz, and an FM frequency deviation varying from 6.4 to 8.5 MHz at 0.7 MHz steps (available Δf tuning: 0–15 MHz to 15 Hz steps). In all cases, close agreement with behavioral simulations is observed [2]. An equivalent set of measured spectra was also obtained, this time with F-type carriers. Results are given in Fig. 16. The apparently distorted spectra have been theoretically explained in [15].

V. Estimated BER Performance

BER estimations of FM-DCSK using signals acquired from the test platform have been also realized. FM-DCSK signals have been quantized (10-bit resolution) at a rate defined by the system reference clock of $f_{R\_\mathrm{CLK}} = 180$ MHz using a commercial ADC, captured by the HP82000 digital tester, and then transferred to a host computer for processing. Stored signals have been time-aligned with the transmitted bit stream (a binary random sequence) and then processed by a fast BER evaluator developed in the MATLAB environment [33], based on a low-pass equivalent model for FM-DCSK which supports multipath effects. Similar to [2], different channel models (proposed by the Personal Communication System Joint Technical Committee) have been considered. They include models for typical indoor office, residential, and commercial environments [14]. All of them, as well as two-ray models with balanced and unbalanced attenuation in both paths, have been used for evaluation. All these cases have assumed RF transmission in the 2.4-GHz ISM band and a variable RF center frequency, from 2.4 to 2.412 GHz at steps of 2 MHz. Demodulation at the receiver is assumed to be accomplished in the digital domain after an ADC of 6-bit resolution at 200-MHz sampling. As pointed out in Section II, the demodulator consists of a conventional delay correlator and a threshold circuit in the NCP case [2] and it additionally includes a frequency detector between the ADC and the correlator in the CP case. All these blocks have been properly modeled in the MATLAB environment for BER evaluation.

Following the above procedure, it has been found that both the CP and the NCP perform similarly and that under all tested propagation conditions the system obtains a BER $= 10^{-3}$ for signal-to-noise ratio (E_b/N_o) lower than 28 dB. As a reference, Bluetooth receivers based on GFSK modulation require 21 dB in AWGN channels and a fading margin of 8 dB [34]. Also, experiments reveal that noise performance improves at higher chip rates, and that RL processed carrier signals slightly improve BER performance (signal power can be reduced by about 0.4 dB) at the expense of a nonsmooth transmission power profile. All these measurements agree with the theoretical predictions and simulations in [2].

VI. Conclusion

A mixed-signal ASIC for FM-DCSK modulation has been fabricated in a two-poly three-metal 0.35-μm CMOS technology. Taking advantage of its many programming features, the ASIC can be used as the core of a test platform to characterize FM-DCSK under different propagation conditions.

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The ASIC integrates a novel continuous-phase FM-DCSK modulation which considerably reduces the hardware budget as compared to the original scheme. A fundamental part of the ASIC is a low complexity carrier generator able to produce chaotic waveforms both in the analog and digital domain. This feature could be exploited, in addition to the proposed application, to implement dithering mechanisms in conventional ADCs.

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