NONLINEAR TIME-DOMAIN MACROMODELING OF OTA CIRCUITS

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ABSTRACT

In this paper we present an accurate nonlinear macromodel of the OTA which is suitable for the transient simulation of OTA-based CMOS analog integrated circuits. As compared to device-level OTA models, the proposed macromodel is advantageous in terms of CPU time. Besides, in circuits with many OTAs, it does not have the problems of convergence that the device-level has. All the macromodel parameters can be calculated from measurements made at the OTA terminals. Experimental results from a $3\mu m$ CMOS OTA prototype as well as simulation results from device-level models are included and compared to simulation results from the macromodel.

INTRODUCTION

For many years the conventional voltage Operational Amplifier (opamp) has been the workhorse for analog circuit design. Recently, the Operational Transconductance Amplifier (OTA) has been demonstrated to be potentially advantageous for the synthesis of high-frequency analog building blocks [1-4]. One reason for this is that transconductance amplifiers do not have any high internal impedance node, hence not requiring internal compensation capacitors and thereby yielding larger bandwidths that the opamp. Another appealing feature of the OTA is that its transconductance gain can be externally controlled, thereby allowing programmable applications. These previous features have motivated an interest in the application of the OTA for the synthesis of continuous-time analog circuits, either for linear [5,6] or for nonlinear [7,8] applications. These efforts run parallel to the proposal of new CMOS OTA implementations that are capable of linear operation in larger input voltage ranges [1,3,4,9]. The ultimate goal is the implementation of high-frequency continuous-time analog circuits in fully monolithic form.

The design of integrated circuits rely on the efficient use of an appropriate set of CAD tools. In particular, electrical simulation tools (like SPICE2) are essential for the design of analog integrated circuits. Although electrical simulation can be done using device-level models, resorting to macromodels is a common strategy to reduce the CPU-time required in simulating complex analog systems. Several opamp macromodels have been reported in the past (see references in [10]). However, little have been still done about OTA macromodeling, the few contributions existing [11,12] not being specifically focused on the inclusion of the macromodel in a electrical simulation tool. It restricts our ability to properly analyze complex OTA-based analog integrated circuits. In this paper we overcome this drawback by presenting an OTA macromodel which is suitable for the time-domain simulation of OTA-based CMOS analog circuits.

OTA MACROMODEL

OTA specifications and parameters

Figure 1 shows a generic CMOS OTA architecture consisting of an input transconductance stage followed by current mirrors [2]. The input stage performs the core operation of differential-voltage to current conversion while the current mirrors are used to steer the output currents of the differential amplifier to a high impedance output node. Several types of current mirrors [13] and transconductance stages [1,3,4,9] can be used in Fig.1, thereby resulting in a broad catalog of practical OTA implementations.

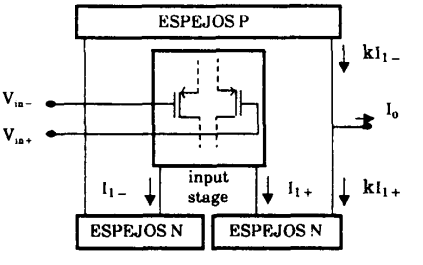

Figure 1: Generic CMOS OTA block diagram

The ideal model of Fig.1 is a linear differential-voltage-controlled current-source, the only parameter required to describe this ideal model being the DC transconductance gain of the OTA, g_m. The behavior of practical OTAs deviate from what is expected using the ideal model in different ways. In the following there is a list of the parameters and specifications to be considered in the proposed macromodel.

g_{m1}	DC small-signal OTA transconductance gain
C_{in}	Input capacitance
V_{os}	Input referred offset voltage

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$(\delta_{1-},\delta_{1+})$	Linear region (less than 1% deviation) for the voltage to current conversion
$(\delta_{2-},\delta_{2+})$	Nonsaturated region for the voltage to current conversion
I_{B+}	Maximum output current
I_{B-}	Minimum output current
ω_1	High-frequency pole
E_{S+}	Maximum output voltage
E_{S-}	Minimum output voltage
T_{D+}	Delay for the top voltage-saturation state
T_{D-}	Delay for the bottom voltage-saturation state
I_{S-}	Minimum output current in the top voltage-saturation state
I_{S+}	Maximum output current in the bottom voltage-saturation state
R_o	Output Resistance
C_o	Output Capacitance

Each parameter above is directly related to the corresponding OTA specification and can be calculated from external measurements at the OTA terminals.

Macromodel architecture

Figure 2 shows the block diagram of the proposed macromodel consisting of four stages. The different stages are connected by voltage-controlled sources.

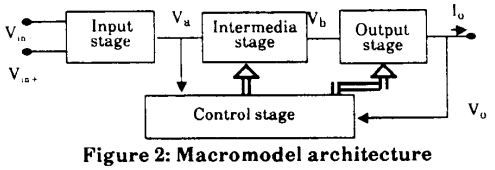


Figure 2: Macromodel architecture

All the nonlinearities in the macromodel are implemented using analog switches, as it is done in [10] for the opamp. The control stage in Fig.2 generates the threshold signals required for controlling the analog switches. The input stage includes the input impedance, offset voltage and CMRR. Its implementation is similar to the corresponding stage in [10].

Figure 3a shows the implementation of the intermediate stage. The conditions for each analog switch to be at the position ① are given in the first row of Table 1; the corresponding conditions for the position ② are included in the second row.

The intermediate stage is driven by the output voltage of the input stage, V_a, and develops an output voltage V_b. Analysis gives the following dynamic equation to describe the input-output operation of Fig.3a:

$$C_1 \frac{dV_b}{dt} + \frac{V_b}{R_1} = I(V_a)$$

where $I(V_a)$ is the nonlinear function depicted in Fig.3b. When particularized for small-signal, this equation accounts for the DC transconductance gain (parameter g_{m1} in the list above) also providing a single-pole approach [2] to the high-frequency behavior of the OTA (parameter $\omega_1 = 1/R_1C_1$). The nonlinearities in the OTA voltage to current conversion are modeled by the transfer characteristics of Fig.3b (via the parameters $I_{B+}, I_{B-}, \delta_{1-}, \delta_{1+}, \delta_{2-}, \delta_{2+}$).

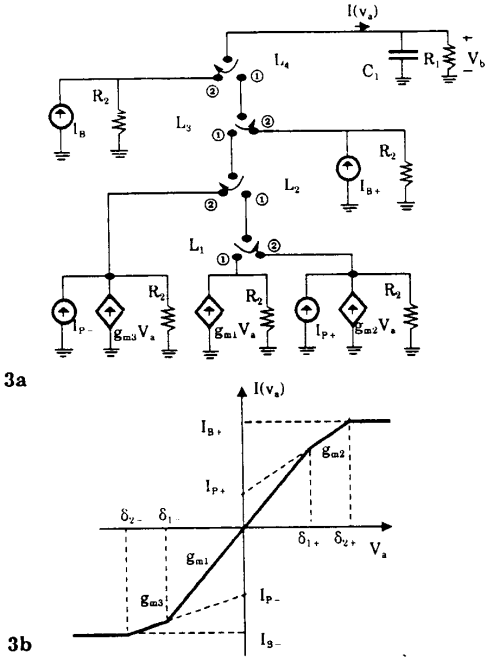


Figure 3: a)Intermediate stage, b)DC OTA transfer characteristic

	L_1	L_2	L_3	L_4
①	$v_a<\delta_{1+}$	$v_a>\delta_{1-}$	$v_a<\delta_{2+}$	$v_a>\delta_{2-}$
②	$v_a>\delta_{1+}$	$v_a<\delta_{1-}$	$v_a>\delta_{2+}$	$v_a<\delta_{2-}$

Table 1: Switching conditions for Fig.3a ($I_b \doteq V_b/R_1$)

The output stage is shown in Fig.4. The switching conditions for the analog switches used in this stage are given in Table 2. As for Table 1, the first row corresponds to the position ①. Besides, the switches L_9 and L_{11} exhibit a controlable delay in the ① to ② transition.

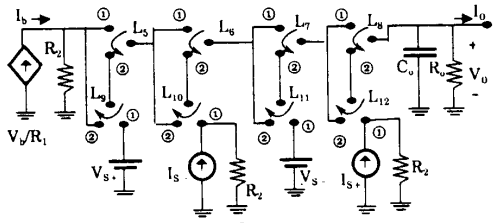


Figure 4: Output stage

The output stage is driven by the output voltage of the intermediate stage, V_b, and models the output impedance and the output voltage saturation

characteristics, including the limitations on the available current when the output voltage is at saturation, and the time delays appearing when the OTA is driven out of the voltage saturation states (parameters I_{S-}, I_{S+}, T_{D-} and T_{D+}).

L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}
$V_o<ES+$	$V_o<ES+$	$V_o>ES-$	$V_o>ES-$	$I_b>I_o$	$I_{S-}>I_o$	$I_b<I_o$	$I_{S+}<I_o$
$V_o>ES+$	$V_o>ES+$	$V_o<ES-$	$V_o<ES-$	$I_b<I_o$	$I_{S-}<I_o$	$I_b>I_o$	$I_{S+}>I_o$

Table 2: Switching conditions for Fig.4 ($I_b \doteq V_b/R_1$)

Most of the element values of the macromodel can be directly calculated from measurements. R_2 is included to avoid the current sources from being in open circuit at any time and must be selected large enough.

MACROMODEL PERFORMANCE

Figure 5 is a microphotograph of a CMOS 3μm double metal prototype of the OTA architecture of Fig.1, where we have used enhanced Wilson current mirrors [13] and the extended-range differential amplifier of Fig.6 [1].

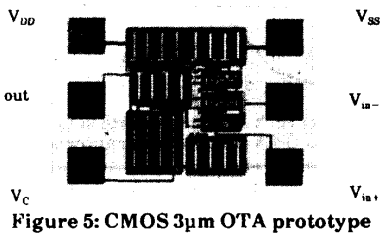


Figure 5: CMOS 3μm OTA prototype

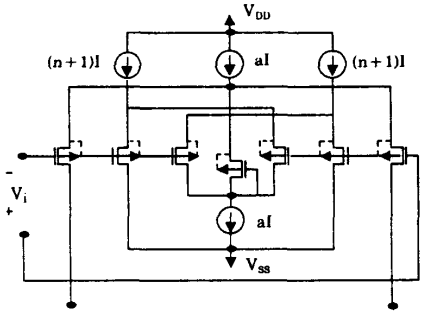
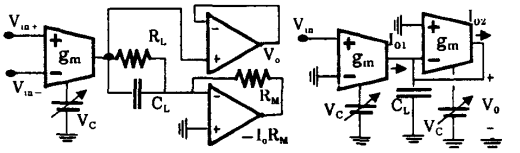


Figure 6: Linearized differential pair [1]

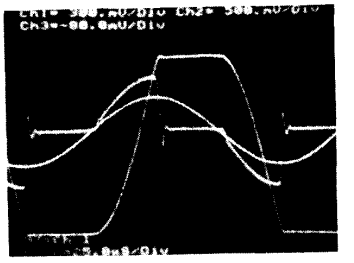
Different measurements have been made on the test circuit of Fig.7a, where the prototype of Fig.5 is connected to several ancillary off-chip components.

Figures 8a,c show two osciloscope displays from the test circuits of Fig.7a. Figures 8b,d show the corresponding waveforms obtained by simulation using DIANA [14] and the OTA macromodel. Figures 8a,b are for $C_L = 33pF$, $G_L = 1/R_L = 0$, the signal driving the test circuit being a 5Khz sinusoidal waveform.On the other hand, Figs.8c,d are for $C_L = 200pF$, $R_L = 212K\Omega$ and a square input signal.



7a 7b

Figure 7: Tests circuits ($R_M = 50K\Omega$)



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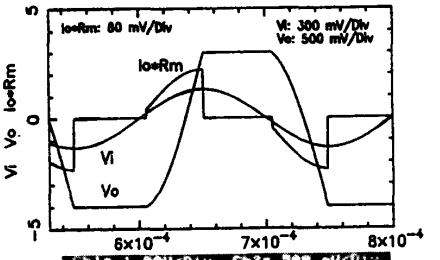
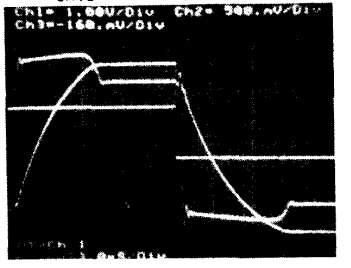
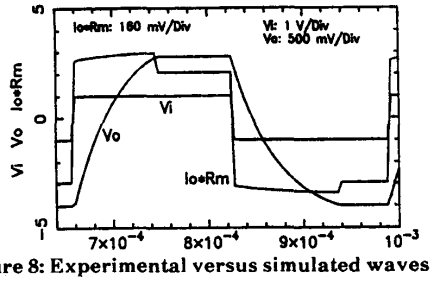


8b



8c

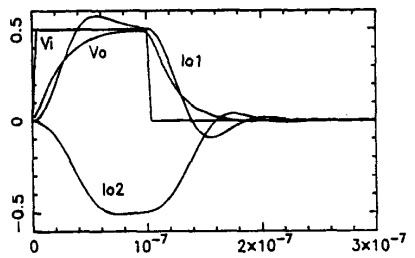


8d

Figure 8: Experimental versus simulated waves

Previous figures shows a very close agreement between experimental and simulation results. The overshoots in the experimental waveforms are due to the reactive behavior of the experimental setup.

The performance of the new macromodel has been also compared to that of device-level models. By the way of example, Fig.9a shows several waveforms obtained when simulating the test circuit of Fig.7b by using SPICE2 and device-level models. The corresponding results when using our macromodel in DIANA are shown in Fig.9b. The OTAs for this example used a conventional noncompensated differential amplifier and enhanced Wilson current mirrors. As it can be seen, the agreement between the macromodel and the device-level model is very good. However, the former is much more efficient in terms of CPU-time than the latter. Concerning this point, our experience for this and many other examples and simulation runs gives a ratio $n=T_D/T_M$ which ranges between *4* and *30*, where T_D is the CPU-time for the device-level model and T_M is the corresponding time for the macromodel.



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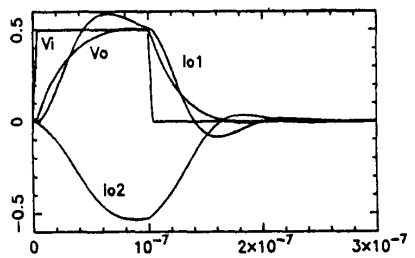

9b

Figure 9: Simulation results for Fig.7b
a) Device-level model, b) Macromodel
voltages: 0.1volts /dv; currents: 10 μA/dv

DISCUSSION OF RESULTS

A macromodel for the OTA has been presented whose features can be summarized in the following points:

1) It is a large signal nonlinear macromodel.
2) It models the input-output behavior of the OTA, thus being adequate for different OTA implementations (for instance, two different OTAs are considered in the section on macromodel performance).
3) All the nonlinearities in the new macromodel are simulated using threshold functions [10].
4) The macromodel parameters can be calculated from measurements made at the OTA terminals.
5) It yields reasonably accurate simulations, providing important advantages in terms of CPU-time saving.
6) Besides the reduced CPU-time, the macromodel in circuits with many OTAs does not have the serious problem of convergence (in SPICE2) that the device-level model has.

Future research will focus on the input stage and common mode effects. Also, a classification of a large catalog of OTA architectures will be done. Finally, frequency-domain macromodels will be developped.

REFERENCES

[1] A. Nedungadi and R. L. Geiger: "High-Frequency Voltage Controlled Continuous Time Low-Pass Filter using Linearized CMOS Integrators". *Electronic Letters*, vol 22, pp 729-731, June 1986.

[2] K. D. Peterson et al.: "Amplifier Design Considerations for High Frequency Monolithic Filters". *Proceedings of the 1987 European Conference on Circuit Theory and Design*, pp 321-326, September 1987.

[3] C. S. Park and R. Schaumann:"Design of a 4-Mhz Analog integrated CMOS Transconductance-C Bandpass Filter". *IEEE Journal of Solid-State Circuits*, vol SC-23, pp 987-996, August 1988.

[4] F. Krummenacher and N. Joel:"A 4-Mhz CMOS Continuous-Time Filter with On-Chip Automatic Tuning". *IIEEE Journal of Solid-State Circuits*, vol SC-23, pp742-749, June 1988.

[5] R. L. Geiger and E. Sánchez-Sinencio:"Active Filter Design Using OTAs: A Tutorial". *IEEE Circuits and Devices Magazine*, vol 1, pp 20-32, March 1985.

[6] E. Sánchez-Sinencio et al.:"Generation of Continuous-Time Two Integrator Loop OTA Filter Structure". *IEEE Trans. Circuits and Systems*, vol CAS-35, pp 936-946, August 1988.

[7] A. Rodríguez Vázquez et al.: "On the Design of Cuasi-Sinusoidal Oscillators using OTAs". *IEEE Trans. Circuits and Systems*, to be published.

[8] J. Silva-Martínez and E. Sánchez-Sinencio: "Analogue OTA Multiplier without Input Voltage Swing Restrictions, and Temperature Compensated". *Electronic Letters*, vol 22, pp 599-600, May 1986.

[9] R. R. Torrance et al.: "CMOS Voltage to Current Transducers". *IEEE Trans. Circuits and Systems*, vol CAS-32, pp 1097-1104, Nov 1985.

[10] B. Pérez-Verdú et al.:"A New Nonlinear Time-Domain Op-Amp Macromodel Using Threshold Functions and Digitally Controled Network Elements". *IEEE Journal of Solid-State Circuits*, vol SC-23, pp 959-971, August 1988.

[11] M. J. Ogorzalek and A. R. Scibich: "Improved Macromodel of Operational Transconductance Amplifier (OTA)". *Proceedings of the 1984 IEEE/ISCAS*, pp 1474-1476, May 1984.

[12] W. M. C. Sansen et al.: "Transient Analysis of Charge Transfer in SC Filters-Gain Error and Distortion". *IEEE Journal of Solid-State Circuits*, vol SC-22, pp 268-276, April 1986.

[13] P.E. Allen and D. Holdberg: "*CMOS Analog Circuit Design*". Holt, Rinehart & Winston 1987.

[14] G. Arnout et al. "*DIANA V7E user's guide*". ESAT Laboratory, Katholieke Universiteit Leuven, 1983.