# A PROTOTYPE TOOL FOR OPTIMUM ANALOG SIZING USING SIMULATED ANNEALING

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***Abstract*** - It is shown that using simulated annealing in combination with electrical simulation provides a powerful tool allowing unexperienced designer to size complex analogue building blocks starting from scratch. A cost function structure is proposed to map a set of specification targets into a combinatorial optimization problem which is in his turn solved by statistical methods. Applicability of the tool is demonstrated via several examples. In particular via the design of the building blocks for a $2\mu m$ CMOS 16bits 20 KHz second-order sigma-delta modulator.

## I. INTRODUCTION

Sizing an analog circuit for a set of *specifications* (like for instance slew-rate, DC gain, etc.) and *design objectives* (like for instance minimum area) is a very complicated and time consuming problem. This is due to the fact that analogue circuits display very complex nonlinear relationships among performance specification and *design parameters* (transistor sizes and passive component values). Also, the number of specifications to deal with is usually very large, the specification themselves varying over wide ranges from one to another application.

Due to these difficulties, manual analog sizing is usually made by following a *semi-empirical* approach where the design parameters are iteratively updated and the corresponding circuit operation evaluated via an electrical simulator (SPICE - like) until specification are achieved. For efficiency of this heuristic procedure proper updating of the design parameters, and hence a deep knowledge about the circuit operation, is required.

The lack of expert analog designers together with the necessity to reduce the total design time in modern mixed-mode ASICs (mainly in MOS VLSI technologies) have motivated a growing interest in the field of analog design automation.

Several tools have evolved for the automated dimensioning of analogue building blocks [1-7]. Most of these tools are closed systems working on a reduced number of fixed schematics for which either design equations or human expert knowledge have been stored in a database. In [7] an open analog design system is proposed which exploits *symbolic analysis* for the automatic analytical modeling of new topologies. However a problem remains in that symbolic analysis does not provide equations neither for the transient nor for the DC characteristics, which must hence still be manually included in the database. As a consequence, this approach may not be appropriate for cases where large signal specifications play a dominant role in the design, as it happens in the building blocks for A/D and D/A converters.

A more general approach to analogue sizing is to automate the semi-empirical manual approach via the formulation of the sizing problem as a *combinatorial optimization* one; for each iteration some cost functions are evaluated by an electrical simulator while an optimizer tool decides how to update the design parameters. This approach is followed in [8] by combining DELIGHT (a general *algorithmic optimizer*) and SPICE. Also, advanced simulators, like HSPICE [9], incorporates an optimization facility to automatically select design component values for optimum achievement of some specifications and design objectives. Since no design equations are required in these approaches (they use electrical simulations to evaluate the circuit performance), they are intrinsically *non-fixed* topology systems. However, as it is stated in [9], for improved optimization using algorithmic techniques, and to increase the likelihood of a convergent solution, an initial estimate of the sizes should be made which produces a circuit with specifications near the original target. Thus we can conclude that the use of algorithmic optimization is very well suited for fine tuning but may not be appropriate for cases where sizing has to be completed starting from scratch.

In this communication a prototype tool is described which combines electrical simulation and *statistical optimization* for the automatic sizing of analogue building blocks. A function cost structure is proposed which when minimized by using simulated annealing [10-12] yields optimum solutions starting from arbitrarily selected initial points. The concept has been proven for different analog circuits being demonstrated in the communication for the building blocks required in a sigma-delta modulator. Since no expertise on analog design is required to size complex analogue building blocks we think the proposed approach may be of interest to help reducing design times in mixed-mode ASICs.

## II. PROPOSED TOOL ARCHITECTURE

Fig. 1 is a conceptual block diagram of the implemented tool. Design parameters (transistor sizes as well as passive component values) are viewed as components of a vector $\underline{x}$ defining a multidimensional *parametric space*. The process of sizing involves describing a trajectory in this parametric space



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starting at some initial point $\underline{x}_0$ (arbitrarily selected by the user) and ending at a point $\underline{x}^*$ where a cost function $\Phi(\underline{x})$ is minimized. This trajectory consists of successive discrete displacements in the parameter space. Such displacements are made by following the principles of simulated annealing [10-12]. A *random* movement is generated at each iteration. Whether it yields minimization of the cost function, such movement is automatically accepted. Otherwise it may also be accepted according to a *probabilist function* depending of a *temperature parameter* $T$. The probability of accepting displacements yielding $\Delta\Phi > 0$ changes during the process, being high at the beginning (for $T$ large) and decreasing as the system becomes cooled ($T$ decreasing). The fact that movement increasing the cost function can be accepted allows the system to scape from local minima, thus increasing the likelihood of convergence towards a global minimum of the cost function.

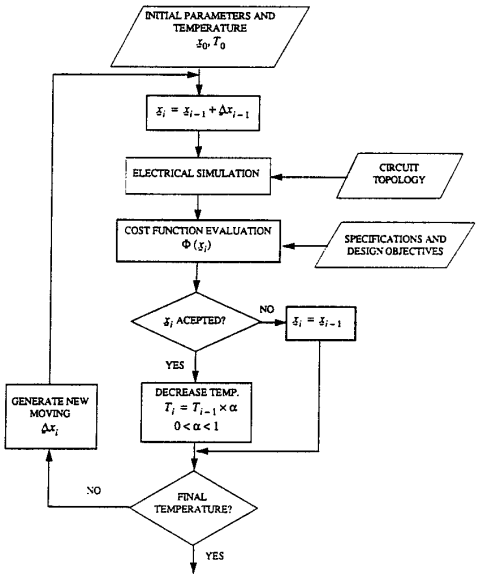



*Figure 1: Conceptual block diagram of the proposed tool.*

As it can be seen from Fig. 1 user of the tool must provide as inputs a SPICE - like netlist of the circuit topology to be sized as well as a list of the block electrical specifications (DC gain, gain-bandwidth product, slew-rate, settling-time, etc.) and any additional design objective (for instance, minimum area occupation). Other inputs are the initial values of the design parameters (remind they can be arbitrarily selected) and the initial and final temperatures.

## III. COST FUNCTION FORMULATION

Crucial for proper operation of the iterative loop of Fig. 1 is the formulation of the cost function $\Phi(\underline{x})$. It does not directly depends upon the design parameter $\underline{x}$, but via a set of *intermediate variables* $\underline{Y} = \{y_1(\underline{x}), y_2(\underline{x}) \ldots y_N(\underline{x})\}^T$. These intermediate variables comprises: a) electrical specs whose values can be measured from HSPICE outputs (DC gain, slew-rate, etc.) and b) constraints on the area and the minimum and maximum values of the design parameters. Many different cost function structures have been tried by us, the one which we have found most appropriate being the following:

$$\Phi = \log\{\prod_{i=1}^{N}\left[G_i\left(\frac{Y_{ie}}{Y_i}\right)\right]^{K_i}\}$$

where $N$ is the number of specs and design objectives (it is, the dimension of vector $\underline{Y}$), $Y_i$ denotes the *i-th* component of $\underline{Y}$ and $Y_{ie}$ is the corresponding target value.The exponential parameter $K_i$ is used to take priority on fulfillment of the corresponding spec $Y_i$. Finally $G_i(.)$ denotes a nonlinear function which takes one between two alternative expressions depending on that the target for $Y_i$ be $Y_i \geq Y_{ie}$ or $Y_i \leq Y_{ie}$. For those specs whose target is $Y_i \geq Y_{ie}$ the following applies:

$$G_i\left(\frac{Y_{ie}}{Y_i}\right) = \begin{cases} \frac{Y_{ie}}{Y_i}, & \frac{Y_{ie}}{Y_i} > 1 \\ 1 & otherwise \end{cases} \qquad (2a)$$

while for the other possible case it is,

$$G_i\left(\frac{Y_{ie}}{Y_i}\right) = \begin{cases} \frac{Y_i}{Y_{ie}}, & \frac{Y_{ie}}{Y_i} < 1 \\ 1 & otherwise \end{cases} \qquad (2b)$$

## IV. EMPIRICAL RESULTS

The proposed tool has been validated for several analog CMOS building blocks. Satisfactory designs were obtained by unexperienced designers and with minimum cost in human resources. In what follows experimental results are given for the two opamps shown in Fig. 3. Consider first the Miller OTA of Fig. 3a [13]. It was sized to accomplish:

DCgain ($A_0$) $\geq$ 80 dB
Gain-bandwidth product (GB) $\geq$ 4 Mhz
Phase margin (PM) > 30°
Slew-Rate (SR) > 9 V/μs
Output Swing (OS) > 4 V peak-to-peak.

in a 1.5μm single poly CMOS n-well technology (a digital technology), for ±2.5V biasing and a capacitive charge of 6pF. Design parameters for this problem were the following:

$x_1=W_1=W_2$ ; $x_2=L_1=L_2$ ; $x_3=W_3=W_4$ ; $x_4=L_3=L_4$
$x_5=W_5$ ; $x_6=L_5$ ; $x_7=W_6$ ; $x_8=L_6$ ; $x_9=L_7$ ; $x_{10}=W_8$
$x_{11}=C_C$ ; $x_{12}=V_{BIAS}$

An equation was provided for the calculation of the random offset due to deviation in the MOS technological parameters [14]. Minimum random offset was required as a design objective. The calculated parameters values are shown in table 1. Measurements on three samples of the prototype showed an input offset voltage of less than 0.5 mV. A fourth sample exhibited an offset of 1.7 mV. The average values of the specifications measured on these four samples were the following:

A0 = 90.4 dB
GB (CL=6pF) = 4.7 Mhz
PM (CL=6pF) = 30.5°
SR = 10 V/µs
OS = 4 V peak-to-peak

which are in accordance to the specifications.

*Table 1: Sizes for the Miller OTA*

| | | | | | |
|---|---|---|---|---|---|
| $M_{1,2}$ | 111.1/15.8 | µm | $M_{3,4}$ | 48.4/7.3 | µm |
| $M_5$ | 24.2/10 | " | $M_6$ | 360.9/5.4 | " |
| $M_7$ | 638.3/10 | " | $M_8$ | 11.9/20 | " |
| $M_9$ | 35.7/20 | " | $C_C$ | 2.55 | pF |
| $V_{BIAS}$ | -1.29 | V | | | |

Let us consider now the fully differential OTA of Fig. 3(b) [15].It had to be sized to be included in a 16bits-20Khz second-order sigma-delta modulator [16] (Fig. 2), requiring the following target:

$A_0 \geq 60$ dB.
GB (CL=2pF) ≥ 35 Mhz.
PM ≥ 60°
OS ≥ 6 v.
Power Dissipation ≤ 10 mW.

for a 2µm n-well double poly CMOS technology in a ±2.5V biasing environment.

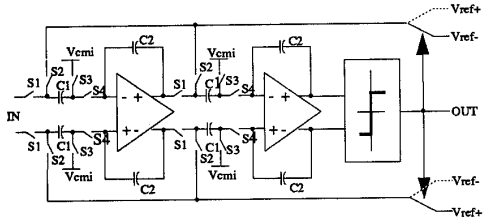
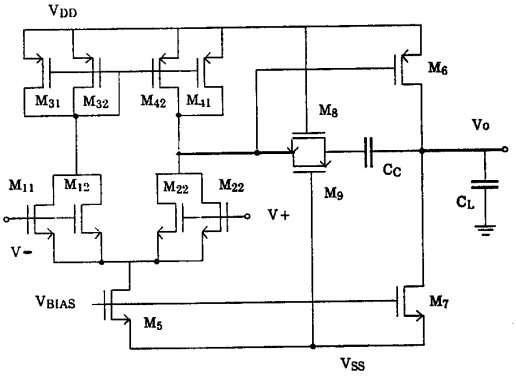
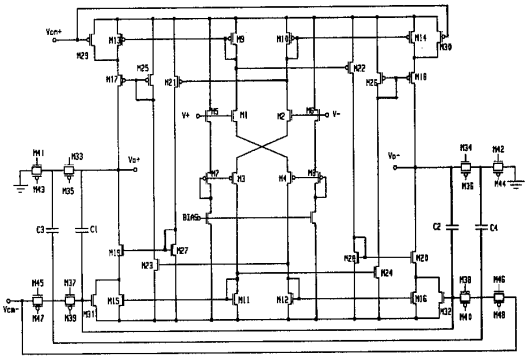



*Figure 2. 2th-Order ΣΔ modulator.*

Initial temperature was $T_0$=3.0, the final one being $T_f$=0.03. Design parameters were the transistor sizes (transistors were grouped into 18 different matched pairs), the capacitor values (the four capacitor were matched) and the bias current. It took about $4\frac{1}{2}$ hours CPU time on a SUN4 Sparcstation 1 to get the values of the design parameters sowed in Table 2.




(a)



(b)

*Figure3. CMOS opamps: a) Miller OTA, b) fully differential OTA.*

*Table 2: Sizes for the fully differential OTA*

| | | | | | |
|---|---|---|---|---|---|
| $M_{1,2}$ | 96.9 / 3 | µm | $M_{21,22}$ | 50.6 / 3 | µm |
| $M_{3,4}$ | 53.3 / 3 | " | $M_{23,24}$ | 40.7 / 3 | " |
| $M_{5,6}$ | 125.7 / 3 | " | $M_{25,26}$ | 9.4 / 3 | " |
| $M_{7,8}$ | 69.2 / 3 | " | $M_{27,28}$ | 7.1 / 3 | " |
| $M_{9,10}$ | 107.2 / 3 | " | $M_{29,30}$ | 50.0 / 5 | " |
| $M_{11,12}$ | 111.1 / 3 | " | $M_{31,32}$ | 50.0 / 5 | " |
| $M_{13,14}$ | 75.3 / 3 | " | $M_{33\text{-}48}$ | 24.0 / 3 | " |
| $M_{15,16}$ | 78.0 / 3 | " | $M_{bias}$ | 123.4/5 | " |
| $M_{17,18}$ | 87.0 / 3 | " | $C_{1\text{-}4}$ | 0.2 | pF |
| $M_{19,20}$ | 104.9 / 3 | " | $I_{bias}$ | 136.85 | µA |

Fig. 4 shows the evolution of the cost function during the design cycle, as a function of the temperature parameter. At the end of the process simulated values for the specifications were the following:

$A_0$: 68.9 dB
GB: 34.4 Mhz

PM: 58.5 °
OS: 6.85 V
Power Dissipation: 3.89mW

which are in accordance to the targets.

Robustness of the yielded design has been assessed by statistical analysis assuming measured deviations in transistor model parameters and capacitor values (data provided by the foundry) and considering a very pessimistic case in which all the transistor are uncorrelated. Results of a Monte Carlo analysis under this assumption showed a standard deviation in DC gain of 69.05 for a mean value of 2748.5. Also, mean value for GB was 34.79 MHz, the corresponding standard deviation being 0.90 MHz. Similar figures were obtained for the remaining opamp specifications. These figures were good enough for the targets in the sigma-delta modulator (Fig. 2) which is currently being processed.

Measurements have been made on the different prototypes of the fabricated circuits. Static measurement resulted in the followings:

$A_0 = 68.6$ dB
OS = 8 V
$P_w = 3.9$ mW

Concerning the gain-bandwidth product it was measured for two different charge conditions yielding:

GB ($C_L \cong 16$pF) = 4.14 Mhz (simulated value: 4.5Mhz)
GB ($C_L \cong 8$pF) = 7.50 Mhz (simulated value: 7.8Mhz)

which are also in accordance to the targets.

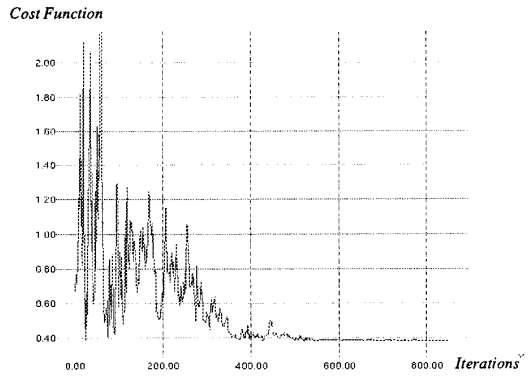



*Figure 4. Cost function vs number of iterations.*

The slight deviation between measured and calculated value of GB can be explained taking into account that compensation in this opamp structure is achieved at the output node and no buffering for this node was provided in the measured prototype. It makes difficult to accurately evaluate the actual value of the load capacitor.

In summary, results in this communication demonstrate de suitability of the proposed technique and cost function structure. Research is still to be done to increase the computational efficiency of the technique via the incorporation of alternative priority schemes and cooling schedules.

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