Live Demonstration: Multiplexing AER Asynchronous Channels over LVDS Links with Flow-Control and Clock-Correction for Scalable Neuromorphic Systems

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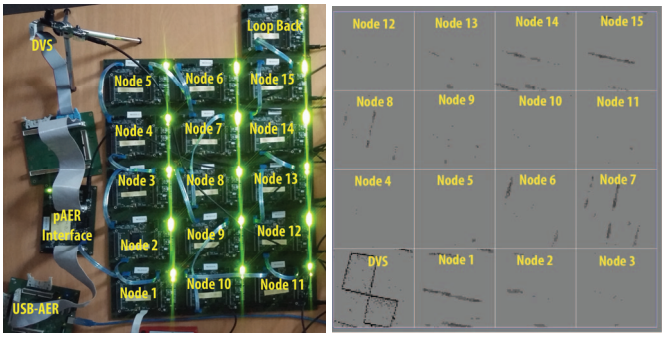
***Abstract*— In this live demonstration we exploit the use of a serial link for fast asynchronous communication in massively parallel processing platforms connected to a DVS for real-time implementation of bio-inspired vision processing on spiking neural networks.**

I. DEMONESTRATION SETUP

In this demo we show a solution for real-time implementation of distributed and scalable spiking neural networks in multi-FPGA platforms by introducing a robust asynchronous serial link with 3.0Gbps data-rate [1]. In addition, we also show how to use this link to communicate with the SpiNNaker [2] platform, used for emulation of spiking neural networks in real-time.

In both cases, we use a frame-less camera sensor or Dynamic Vision Sensor (DVS) [3] as the real-time input spike source, plus one layer of Spiking Convolutional Neural Network (SCNN) implementing Gabor filters with 15 different orientations.

For the Multi-FPGA platform, we use 17 AER-Node board with Spartan-6 FPGA connected through LVDS links as shown in Fig. 1 (a). Each Gabor filter is implemented in one FPGA board from Node 1 to Node 15.



(a) (b)

Fig. 1. (a) Multi-FPGA platform for Spiking Neural Networks (b) Visualization of output spikes in jAER

For the SpiNNaker platform, we use the same LVDS link to send and receive spikes in real-time from a DVS to a SpiNN-5 board that contains 48 SpiNNaker chips. We implement the same Gabor filters on the SpiNN-5 board by using 30 SpiNNaker chips (480 ARM cores). The setup for this demo is shown in Fig. 2.

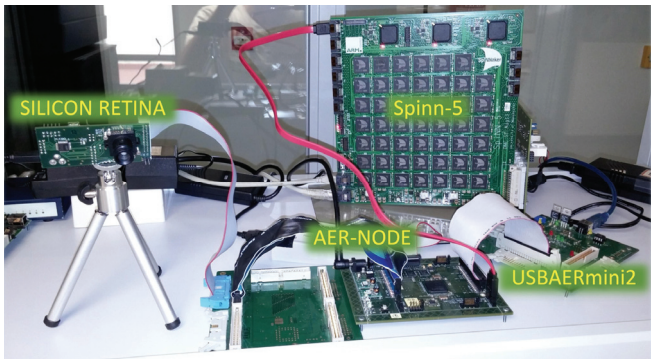


Fig. 2. SpiNN-5 board connected to DVS by using LVDS link

II. VISITOR'S EXPERIENCE

Visitors can see the real-time running of the Spiking Neural networks in the multi-FPGA and the SpiNNaker platforms as shown in [4]. They can present different objects to the DVS and see the output spikes in the jAER visualization software as shown in Fig. 1 (b). They can also bypass some FPGA nodes to remove part of the neural network when it is running and see the results in jAER.

III. BIBLIOGRAPHY

[1] A. Yousefzadeh, et al, "Multiplexing AER Asynchronous Channels over LVDS Links with Flow-Control and Clock-Correction for Scalable Neuromorphic Systems," *Proc. IEEE Int. Symp. Circ. and Systems* (ISCAS 2017), June 2017.

[2] M.Kahn et al, "SpiNNaker: Mapping Neural Networks onto a Massively-Parallel Chip Multi-Processor," *IEEE Int. Joint. Conf. on Neural Networks (IJCNN- WCCI),* June 2008.

[3] T. Serrano-Gotarredona and B. Linares-Barranco, "A 128x128 1.5% Contrast Sensitivity 0.9% FPN 3us Latency 4mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Amplifiers," *IEEE J. Solid-State Circuits,* 2013.

[4] A. Yousefzadeh, "Live Demonstration: Massively Parallel platform for Spiking neural networks," 2016. [Online] Available: https://youtu.be/TJUllyGIoEc .