

A High TCMRR, Inherently Charge Balanced Bidirectional Front-End for Multichannel Closed-Loop Neuromodulation

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Abstract—This paper describes a multichannel bidirectional front-end for implantable closed-loop neuromodulation. Stimulation artefacts are reduced by way of a 4-channel H-bridge current source sharing stimulator front-end that minimizes residual charge drops in the electrodes via topology-inherent charge balancing. A 4-channel chopper front-end is capable of multichannel recording in the presence of artefacts as a result of its high total common-mode rejection ratio (TCMRR) that accounts for CMRR degradation due to electrode mismatch. Experimental verification of a prototype fabricated in a standard 180 nm process shows a stimulator front-end with 0.059% charge balance and 0.275 nA DC current error. The recording front-end consumes 3.24 μ W, tolerates common-mode interference up to 1 Vpp and shows a TCMRR > 66 dB for 500 mVpp inputs.

Index Terms—closed-loop neuromodulation, TCMRR, charge balance, stimulation artefacts.

I. INTRODUCTION

Implantable closed-loop neuromodulation has been proposed as a form of treatment for Parkinson’s and epilepsy, among other neural disorders [1]. The idea is that the dynamics of the brain inform the state of the stimulators, thus establishing closed-loop control of region-specific brain activity. In a practical implementation, this scheme presents an intrinsic self-interference caused by stimulation artefacts that saturate the recording front-end of the neuromodulator. Stimulation artefacts are a product of residual charge accumulation in the electrodes which is in turn caused by mismatch in the stimulation cathodic and anodic phases. Artefact magnitude is proportional to the stimulation current amplitude and proximity between stimulation and recording electrodes. A common-mode artefact can reach up to hundreds of millivolts [2] and also exhibits a differential component as well as a ratcheting effect [3]. Fig. 1 shows a typical power spectrum for artefacts that reveals the presence of harmonics and an increase in magnitude due to time-dependent residual charge accumulation. An accurate charge-balancing scheme is therefore fundamental for the chronic operation of closed-loop neuromodulators. Traditional multichannel recording front-ends are specially susceptible to artefacts. A significant degradation in common-mode rejection presents itself under the conventional electrode

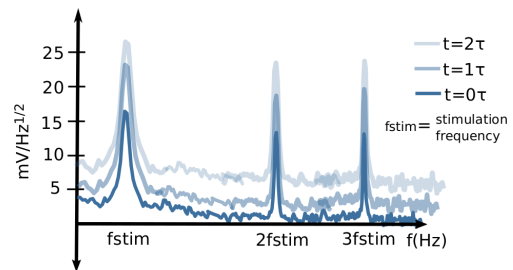


Fig. 1. Frequency domain (Log scale) view of artefacts and their input-referred magnitude increase due to residual charge accumulation over time.

reference sharing configuration due to impedance mismatch between reference and signal inputs. This situation gives rise to the concept of total common-mode rejection ratio (TCMRR) that accounts for impedance mismatch in a multichannel front-end as follows [4]:

$$TCMRR = \left(\frac{1}{ICMRR} + \left(\frac{1 + 2(|Z_{IN}/Z_e| + N\epsilon)}{2(N\epsilon - 1)} \right)^{-1} \right)^{-1}, \quad (1)$$

where N is the number of channels sharing a single reference electrode, ϵ is the mismatch factor between reference and signal electrodes ($\epsilon=1$ when both electrodes are matched), $|Z_{IN}/Z_e|$ is the impedance ratio between input and electrode impedances and ICMRR is the intrinsic common-mode rejection ratio (i.e. the CMRR of a single channel). In order to maintain a sufficiently high TCMRR, $|Z_{IN}/Z_e|$ should be high, ICMRR high and N should be modest. This phenomenon was originally described by [4] with common-mode interference from capacitive coupling of electrical supply voltages in mind (as high as 100 mVpp). Evidently, it acquires greater importance in the presence of large common-mode stimulation artefacts (as high as 1 Vpp). A model for a single recording channel is shown in Fig. 2. Previously reported closed-loop neuromodulators deal with artefacts by input blanking [5], pole-shifting [6] or by placing stimulation and recording electrodes far from each other [7] [8]. These strategies somewhat

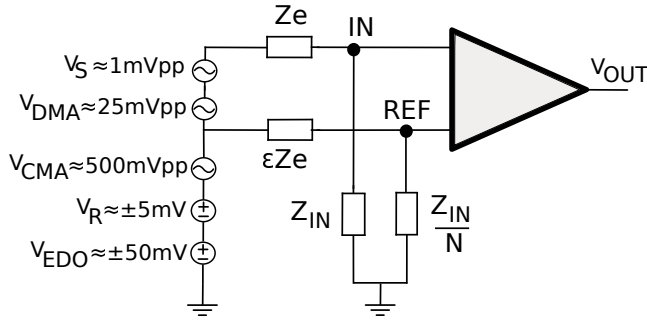


Fig. 2. Model for a single channel in a multichannel recording interface in the presence of self-interference (extended from [4]). V_S is the neural signal of interest, V_{DMA} is the differential-mode artefact, V_{CMA} is the common-mode artefact, V_R is the ratcheting effect and V_{EDO} is the electrode DC offset. Amplitudes for V_{DMA} , V_{CMA} , V_R will increase over time if the stimulation pulses are not balanced.

defeat the purpose of closed-loop neuromodulation since they imply either loss of information (during and right after stimulation) or a non-local control loop. The works reported by [9]–[11] do manage same electrode array closed-loop operation, however, they make no account for TCMRR meaning that simultaneous multichannel recording during stimulation might be degraded. Moreover, only [9] considers stimulator charge balance even though the link between residual charge in the electrodes (i.e. stimulator charge imbalance) and artefact generation has been well established. In this work we present a bidirectional front-end for multichannel closed-loop neuromodulation. The role in artefact generation by the charge balance scheme of the stimulators is acknowledged from the very beginning: a 4-channel stimulator front-end based on an H-bridge topology that shares the same current source for both phases of biphasic stimulation is proposed. This topology inherently balances the stimulation current in both phases. Since artefacts are unavoidable, the aim is to produce a stimulation system that generates non-saturating artefacts. A 4-channel low-noise low-power front-end based on chopper amplifiers comprises the recording side of the front-end. In order to tolerate artefacts, the chopper amplifiers are designed for large ac common-mode interferer range, high differential input range and large DC offset rejection. To maintain high TCMRR, the front-end includes input impedance boosting and high ICMRR for large common-mode inputs.

II. BIDIRECTIONAL FRONT-END FOR MULTICHANNEL CLOSED-LOOP NEUROMODULATION

Figure 3 shows the block diagram of the proposed 8-channel bidirectional front-end. The circuit is comprised by a 4-channel stimulator front-end and a 4-channel recording front-end. The system is powered by $V_{DDH}=3.3$ V (stimulator) and $V_{DDL}=1.8$ V (recording) supply.

A. H-Bridge Inherently Charge-Balanced Stimulator

In a biphasic stimulation scheme, charge imbalance comes from unavoidable mismatch between the stimulator current sources. Additional circuitry to compensate for residual charge

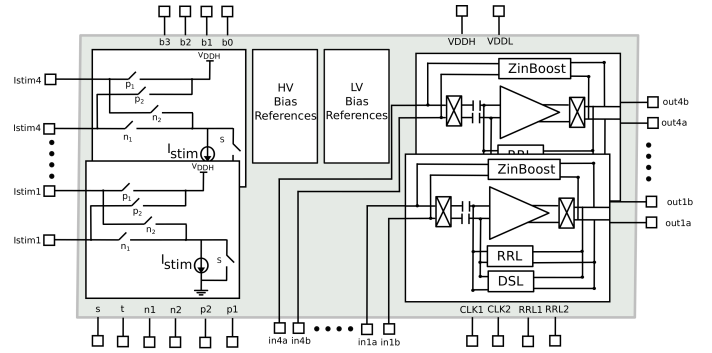


Fig. 3. Proposed bidirectional front-end.

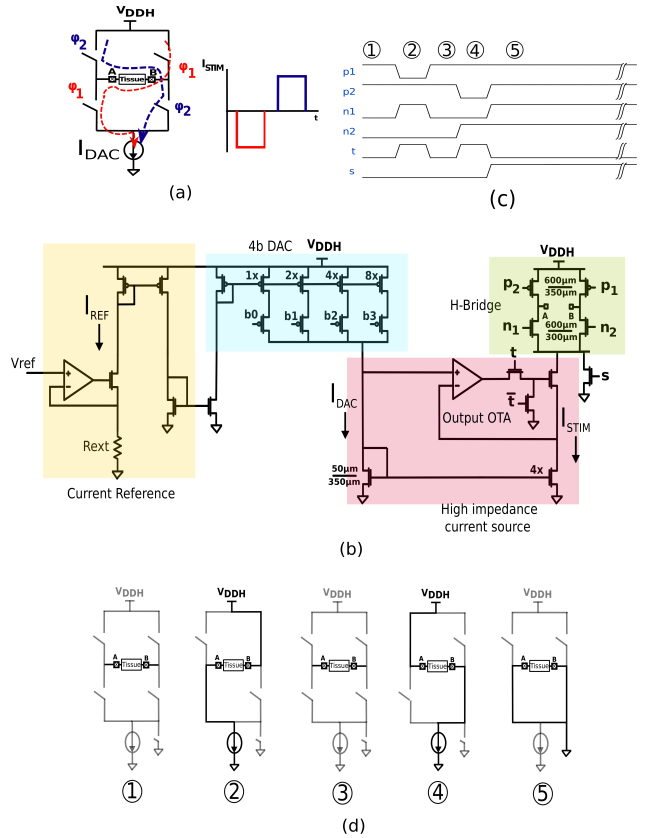


Fig. 4. (a) H-bridge (b) Proposed Stimulator (c) Time diagram (d) Stimulator Operation.

in the electrodes is necessary since good layout matching can only do so much. In order to avoid mismatch between current sources, we implement an H-bridge (Fig. 4(a)) operation to produce a biphasic pulse from a single current source, thus obviating the need for a charge compensation scheme. The proposed neural stimulator is shown in Fig. 4(b). An additional transistor is added to the H-bridge to short the output electrodes to ground after each biphasic pulse (passive discharge). The output H-bridge sinks the stimulation current to a high-output impedance current driver that also accurately copies I_{DAC} , which is set by a 4-b DAC. The timing diagram of the stimulator is shown in Fig. 4(c). The stimulator is turned

off in State 1. State 2 sees the current flow from A to B, thus creating the cathodic pulse. State 3 defines an interphase delay, usually much shorter than the width of each pulse. The anodic pulse is created in State 4 where the current flows from B to A. State 5 shorts the outputs to discharge the electrodes after each biphasic pulse, thus providing a DC current error that is safe for both the neural tissue and microelectrodes. Fig. 4(d) depicts the operation of the stimulator.

B. Chopper Amplifier for High TCMRR Recording

The proposed chopper amplifier is shown in Fig. 4. Chopper amplifiers typically exhibit high ICMRR [12]. However, the input impedance defined as $Z_{IN} = \frac{1}{2f_C C_{IN}}$, jeopardizes its direct implementation in a high TCMRR scheme. This can be compensated by setting the chopping clock (f_C) at 2.5 kHz to minimize its impact on input impedance. An input capacitor $C_{IN} = 1$ pF is chosen, which translates as a theoretical $Z_{IN} = 200$ M Ω , nevertheless, a positive feedback impedance boosting loop has been included to obtain higher input impedance. The gain is set to 20 V/V by way of C_{IN}/C_{FB} in order to amplify both V_S and V_{DMA} without saturating the front-end. A current mirror amplifier with partial positive feedback has been chosen for OTA_1 [13]. This OTA features a rail-to-rail output and high enough open-loop gain so that a second OTA in the forward path can be avoided. The bandwidth is set by a passive low-pass filter. A DC servoloop introduces a high-pass frequency corner in the front-end by feedbacking an integrator with a very large time constant. Its specific role is then, to reject V_R and V_{EDO} . Chopper modulation introduces an output ripple whose magnitude is dependent on the offset of the first stage. This was attenuated by sensing it in the output with a switched-capacitor integrator that produces a proportional voltage which in turn generates a compensating current by means of an auxiliary differential pair in OTA_1 [12].

III. MEASUREMENT RESULTS

Fig. 6 shows a microphotograph of the fabricated prototype. Fig. 7(a) shows the stimulation waveform for a $R=5$ k Ω $C=100$ nF load. The maximum current of a single stimulator (Fig. 7(b)) is 300 μ A, for a 5 k Ω load. More than one stimulator can be combined in a single load for higher current capability. Charge balance was characterized by stimulating 10 biphasic pulses of 600 μ s. The residual voltage was measured right after the last pulse. The final shorting phase was removed for this test. Fig. 7(c) shows the residual voltage for each stimulator. In all cases, a residual voltage under the water window is achieved. Fig. 7(d) shows the residual charge for each stimulator. The worst case residual charge is about 106 pC. The worst case charge mismatch is (residual/injected) x 100, which is 0.059%. The recording front-end shows a 600 Hz bandwidth and draws 3.24 μ W/channel from a 1.8 V supply. Fig. 8(a) shows the measured input-referred noise, which is about 250 nV/rtHz. Differential input range, measured in terms of total harmonic distortion (Fig. 8(b)) is 2.85% for a 120 mVpp input. Fig. 8(c) shows a 5% gain drop for 1 Vpp

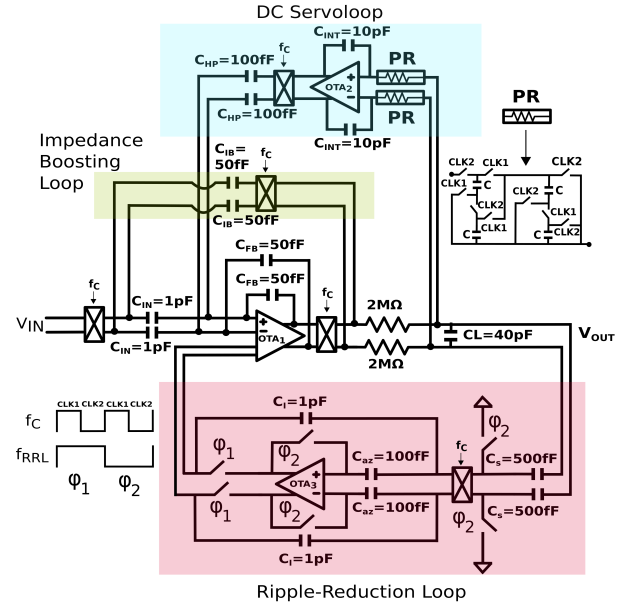


Fig. 5. Proposed chopper amplifier.

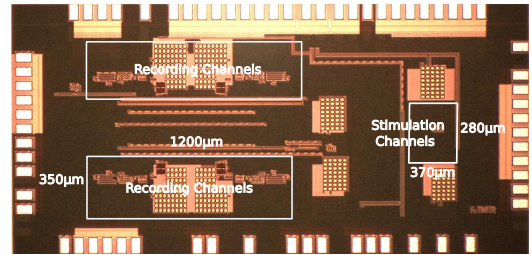


Fig. 6. Die microphotograph.

common-mode inputs while ICMRR measured for 500 mVpp inputs is kept above 80 dB in the amplifier bandwidth. Input impedance and ICMRR measured for each channel for 500 mVpp inputs at 200 Hz is shown in Table I. The calculated TCMRR at 200 Hz for each channel and electrode impedance = 100 k Ω is > 66 dB. The specifications are summarized and compared with previous art in Table II.

IV. CONCLUSIONS

This work presented an 8-channel bidirectional front-end for closed-loop neuromodulators. Previously reported front-ends generally ignore large ac common-mode interference, CMRR degradation due to electrode mismatch and charge balance in

TABLE I
TOTAL COMMON-MODE REJECTION RATIO AT 200 HZ.

| Recording channel | Z_{IN} (M Ω) | ICMRR (dB) | TCMRR (dB) |
|-------------------|------------------------|------------|------------|
| A | 826 | 81 | 66.9 |
| B | 816 | 83 | 67.1 |
| C | 795 | 80 | 66.4 |
| D | 884 | 88 | 68.4 |

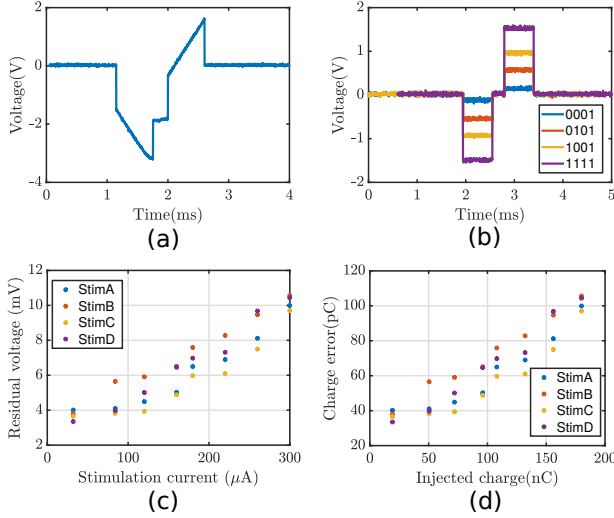


Fig. 7. Stimulator front-end. (a) Waveform for an R+C load (b) Waveform for an R load (c) Residual voltage after 10 biphasic pulses (d) Charge error.

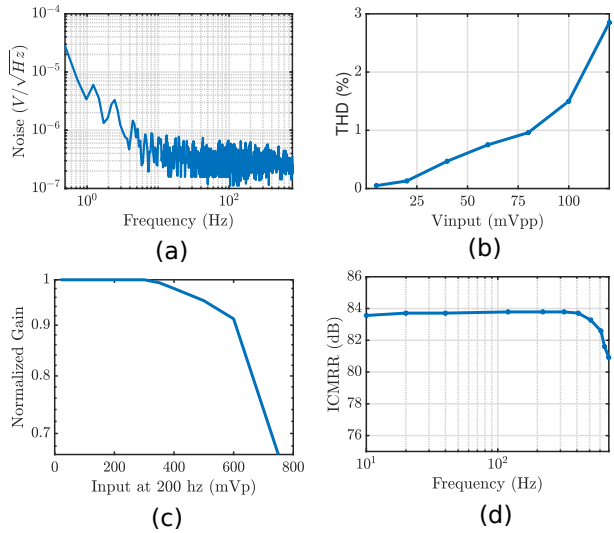


Fig. 8. Recording front-end. (a) Noise (b) Total harmonic distortion (c) Input ac common-mode interferer range (d) Intrinsic common-mode rejection ratio.

TABLE II
COMPARISON WITH CLOSED-LOOP NEUROMODULATORS

| | [10] | [11] | [9] | This work |
|----------------------------------|----------------------|--------------------|------------------|-------------------|
| Process / Year | 40 nm, 180 HV / 2018 | 65 nm / 2018 | 180 nm HV / 2017 | 180 nm / 2019 |
| Channels Recording / Stimulation | 64 / 8 | 8 / 2 | 64 / 4 | 4 / 4 |
| Power (Recording) (μ W) | 8.2 | 2.7 | 8 | 3.24 |
| Bandwidth (Hz) | 250 | 8.3 k | 500 | 600 |
| Noise | 2.2 μ Vrms | 8.2 μ Vrms | 71 nV/rtHz | 250 nV/rtHz |
| THD | -81 dB at 100 mVpp | -77 dB at 200 mVpp | 0.7% at 100mVpp | 2.85% at 120 mVpp |
| AC CMI range | - | - | - | 1 Vpp |
| ICMRR (dB) | - | - | - | > 80 |
| TCMRR (dB) | - | - | - | > 66 |
| Charge Balance | - | - | <1% | 0.059% |
| DC current error | - | - | - | 0.275 nA |

relation to artefact generation. This work is therefore, the first one to account for these specifications concurrently. Future work will deploy a complete characterization of the front-end.

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