A 5.3mW, 2.4GHz ESD Protected Low-Noise Amplifier in a 0.13μm RFCMOS Technology

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***Abstract*—An Electrostatic Discharge (ESD) protected Low-Noise Amplifier (LNA) for the 2.4GHz ISM band designed in a 0.13μm standard RFCMOS technology is presented. The amplifier, including packaging effects, achieves 16.8dB power gain, reflexion coeffcients S_{11}, S_{22} < -30dB over the 2.4GHz ISM band, a peak noise figure of 1.8 dB, and an IIP_3 of 1dBm, while drawing less than 4.5mA dc biasing current from the 1.2V power supply. Further, the LNA withstands a Human Body Model (HBM) ESD stress up to ±2.0kV, by means of the additional custom protection circuitry.**

***Index Terms*—LNA, Electrostatic discharge (ESD) protection, Noise figure, RF CMOS.**

I. Introduction

This paper presents the design of a 1.2V CMOS LNA, implemented in a 0.13μm RF process, for short range communications in the 2.4GHz unlicensed ISM (Industrial, Scientific and Medical) band, as defined by the standards Bluetooth, IEEE 802.11b/g or IEEE 802.15.4. The amplifier uses an inductively degenerated common-source topology and includes pads with ESD protection for reliability reasons. The influence on the amplifier performance of the parasitics from the ESD protection circuit, input and output pads, bondwires and package leads has been considered during design. The LNA achieves 16.8dB power gain with an input match of S_{11}<-30dB over the ISM band, a peak noise figure lower than 1.8 dB, and an IIP_3 of 1dBm, while drawing less than 4.5mA dc biasing current. Additionally, the protection circuits at the RF pads provide HBM ESD withstand voltages of ±2.0kV.

The paper is organized as follows. In Section II, details on the design of the LNA are given. Section III describes the ESD protection circuitry and its influence on the LNA performance. Section IV summarizes the main characteristics of the amplifier, obtained from electrical simulations of the extracted layout. Finally, Section V gives some conclusions.

II. LNA Design

Fig.1 shows a simplified schematic of the designed CMOS LNA. It uses an inductively degenerated common-source cascoded topology, in which the source inductance is

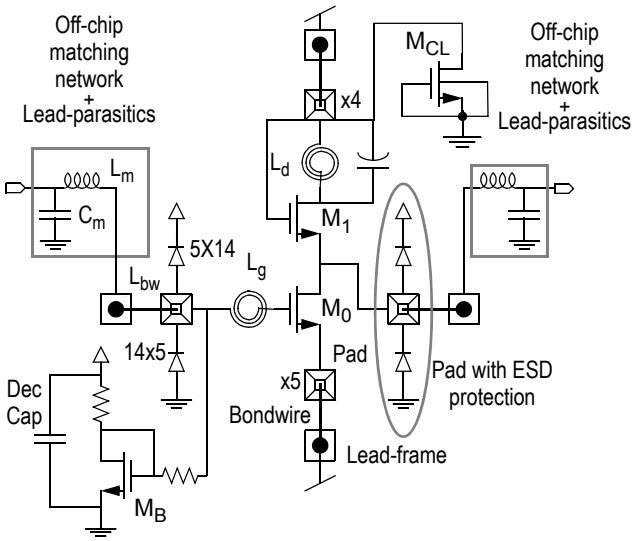

Figure 1. Schematic of the packaged LNA circuit with ESD Protection.

implemented by five paralleled low-loss bond wires. Fig.2(a) shows the equivalent small-signal circuit for the input stage of the LNA. The off-chip L-type network composed by C_m and L_m is designed to match a known source impedance R_s to a smaller resistance value, R_p, at the resonance frequency, ω_0 [1]. Sizing of C_m and L_m must also consider the parasitics of the selected QFN package. The inductance contributed by the series gate bondwire is represented by L_{bw} and C_p denotes the sum of the parasitic capacitances due to the pad, C_{PAD}, and the ESD protection circuit, C_{ESD}. The integrated spiral coil has been modelled by an inductance L_g in series with a resistance R_g which accounts with its ohmic losses. The common source transistor M_0 of Fig.1 has a transconductance g_m, a gate-to-source capacitance C_{gs} and a gate resistance r_g. The impedance at the drain of M_0 is assumed to be negligible small by the effect of the cascode transistor M_1. Also it is assumed that the Miller effect arising from the gate-

1. If C_p is sufficiently large compared to the C_{gs} of the LNA input device, the impedance level at the LNA input becomes too low to be matched 50Ω only by employing a series inductance [1], [2]. For this reason, similar to other designs [2], the input impedance level of the proposed LNA exhibits a value lower than 50Ω (about 20Ω).

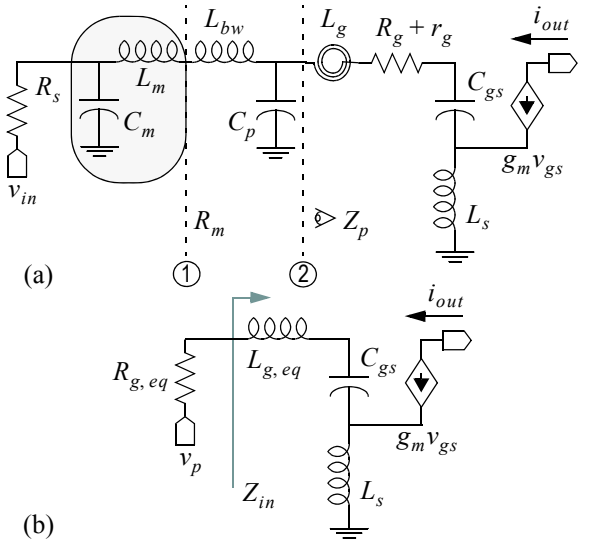

Figure 2. (a) Small-signal circuit for the input stage of the LNA. (b) Equivalent simplified schematic.

to-drain capacitance C_{gd} of M_0 can be ignored. Finally, L_s represents the degenerative source inductance, implemented by five paralleled bondwires – therefore, $L_s \approx L_{bw}/5$. Due to the low loss of the bondwires, no parasitic resistance is considered.

The impedance Z_p seen at the left of the reference plane ② of Fig.2(a) can be written as $R_{eq} + j\omega_0 L_{eq}$, where R_{eq} and L_{eq} are given by,

$$\begin{aligned} R_{eq} &= \frac{R_m}{\omega_0^2 C_p^2 R_m^2 + (1-\omega_0^2 C_p L_{bw})^2} \\ L_{eq} &= \frac{L_{bw} - C_p(\omega_0^2 L_{bw}^2 + R_m^2)}{\omega_0^2 C_p^2 R_m^2 + (1-\omega_0^2 C_p L_{bw})^2} \end{aligned} \tag{1}$$

where it is assumed that the impedance at the reference plane ① is purely resistive with resistance,

$$R_m = \frac{R_s}{1 + (\omega_0 C_m R_s)^2} \tag{2}$$

Combining Z_p with the integrated inductor and the parasitic resistances at the gate of M_0, the simplified schematic of Fig.2(b) is obtained where

$$\begin{aligned} R_{g,eq} &= R_{eq} + R_g + r_g \approx R_{eq} \\ L_{g,eq} &= L_{eq} + L_g \end{aligned} \tag{3}$$

From Fig.2(b), the power matching condition at the input of the LNA can be found to be [3],

$$R_{g,eq} \approx \frac{g_m L_s}{C_{gs}} \equiv \omega_T L_s \tag{4}$$

where ω_T denotes the cut-off angular frequency of the transistor. Note that since ω_T for the 0.13μm process is high, a low value of L_s is required for input matching – this justifies the use of five bondwires in parallel. On the other hand, the resonance condition at the input stage of the LNA reads as [3]-[5],

$$\omega_0 = \frac{1}{\sqrt{(L_{g,eq} + L_s) C_{gs}}} \tag{5}$$

which can be recursively solved to obtain L_g in terms of ω_0 (in this design, f_0 is set to 2.44Ghz).

Taking advantage of the equivalent simplified schematic of Fig.2(a) and Fig.2(b), the magnitude of the output current i_{out} of the input stage can be calculated, making use (4) and (5), as

$$|i_{out}| = g_m |v_{gs}| = \frac{g_m |v_p|}{|2j\omega_0 R_{g,eq} C_{gs}|} = \left|\frac{v_p}{2j\omega_0 L_s}\right| \tag{6}$$

which can be written as

$$|i_{out}| = \frac{|v_{in}|}{2\omega_0 L_s} \zeta(R_s, L_{bw}, C_p, C_m) \tag{7}$$

where $\zeta(R_s, L_{bw}, C_p, C_m)$ is given by Eq. (8), at the bottom of this page. Using (7), the transconductance of the LNA input stage is given by,

$$G_m = \left|\frac{i_{out}}{v_{in}}\right| = \frac{\zeta(R_s, L_{bw}, C_p, C_m)}{2\omega_0 L_s} \tag{9}$$

and the LNA voltage gain at the nominal operation frequency by

$$A_v = G_m |Z_d(j\omega_0)| \tag{10}$$

where $Z_d(j\omega_0)$ is the impedance of the LC resonator circuit at the drain of M_1 (see Fig.1). In the proposed design, the inductance of this tank circuit has been optimized to maximize the voltage gain of the LNA. Then, the capacitance has been tuned so that the tank resonates at the nominal operation frequency.

Fig.3 depicts a small-signal circuit for the noise analysis of the proposed LNA. In this circuit, $\overline{v_s^2}$ represents the noise power contribution of the source, $\overline{v_{R_g}^2}$ is the noise contribu-

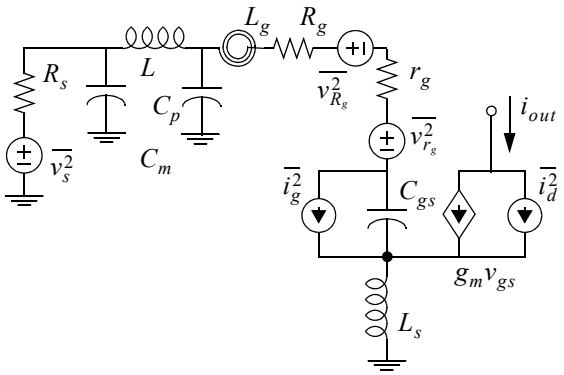

Figure 3. Small Signal Circuit for Noise Figure Analysis of the proposed LNA with ESD Protection

$$\zeta(R_s, L_{bw}, C_p, C_m) = \left\{ \omega_0^2 \left[\left(\frac{1}{\omega_0} - \omega_0 C_m (L_{bw} - C_p R_s R_m) \right)^2 + (\omega_0^2 C_m L_{bw} R_s C_p + C_p R_m + R_s C_m)^2 \right] \right\}^{-1} \equiv \frac{\xi}{\omega_0} \tag{8}$$

tion from the ohmic losses of the integrated coil, $\overline{v_{r_g}^2}$ is the noise power due to the gate parasitic resistance of transistor M_0, $\overline{i_d^2}$ is the noise contribution of its channel and the underneath substrate resistance R_{sub}, and $\overline{i_g^2}$ is the gate-induced current noise power. For the sake of simplicity, the noise contribution from the cascode stage has been neglected – it has low impact on the overall noise performance of the LNA. Assuming perfect power matching, the noise power contributions from the above sources to the LNA output current, can be calculated at the resonance frequency,

$$\begin{aligned}
\overline{i_{n,R_s}^2} &= \frac{G_m^2 \overline{v_s^2}}{4} = G_m^2 k_B T R_s \\
\overline{i_{n,R_g}^2} &= \frac{k_B T R_g g_m^2}{\omega_0^2 C_{gs}^2 (R_{g,eq} + R_g + \omega_T L_s)^2} \\
\overline{i_{n,r_g}^2} &= \frac{k_B T r_g g_m^2}{\omega_0^2 C_{gs}^2 (R_{g,eq} + r_g + \omega_T L_s)^2} \\
\overline{i_{n,d}^2} &= \frac{\gamma}{\alpha} k_B T g_m + k_B T g_{mbs}^2 R_{sub} \\
\overline{i_{n,g}^2} &= \frac{1 + (g_m \omega_0 L_s)^2}{(\omega_0 L_s)^2} \cdot \frac{k_B T \alpha \delta}{5 g_m}
\end{aligned} \tag{11}$$

where $g_{mbs} = \eta g_m$ and η, α, δ and γ are bias dependent parameters [3]. If the parasitic losses of the tank circuit at the drain of M_1 are modelled by a parallel resistor R_d at the frequency operation, its noise contribution to the LNA output noise current is,

$$\overline{i_{n,R_d}^2} = 4 k_B T / R_d \tag{12}$$

From (11)- (12), the noise factor of the LNA is found by adding up the different noise power contributions (taking into account the correlation between the drain and gate-induced noise contributions [4]), and normalizing by the noise current due to R_s. This gives,

$$\begin{aligned}
F \approx 1 + \frac{R_{g,eq}^2}{R_s \xi^2} \left(\frac{\omega_0}{\omega_T}\right)^2 \Bigg[& \frac{4 \omega_T^2 R_g}{(R_{g,eq} + R_g + \omega_T L_s)^2} + \dots \\
& + \frac{4 \omega_T^2 r_g}{(R_{g,eq} + r_g + \omega_T L_s)^2} + \frac{\gamma}{\alpha} \omega_0^2 g_m \Psi + \dots \\
& + \omega_0^2 g_{mbs}^2 R_{sub} \Bigg] + \frac{1}{G_m^2 R_d R_s}
\end{aligned} \tag{13}$$

where $\Psi = 1 + 2c\sqrt{\frac{\delta}{5\gamma}} + \frac{\alpha^2 \delta}{5\gamma}$ and c is the correlation coefficient of the gate and drain noise sources [3].

III. ESD Protection Circuitry Design

In the LNA, the input and output terminals have been ESD-protected by means of dual-diode arrays as shown in Fig.1 [5]. Each array consists of 5 rows and 14 columns of diodes. Major issues on the design of this protection circuit have been the added shunt capacitance, C_{ESD}, and the tolerable ESD current.

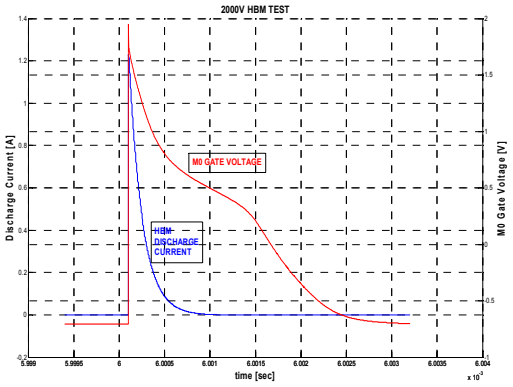

Figure 4. Discharge Current and Breakdown Voltage from 2kV HBM Test

At RF, capacitance C_{ESD} becomes a low impedance path that will short the signal to ground, thus affecting the power gain and the noise figure of the LNA. Additionally, ESD protection structures, being extra devices to the circuit core, will cause noise coupling to the substrate through C_{ESD}. Therefore, C_{ESD} must be reduced as much as possible. In this design, the ratio C_{ESD}/C_{gs} is about 0.4 and the total shunt capacitance of the protection circuit is $C_{ESD} = 95\text{fF}$, giving an overall parasitic capacitance $C_p = 240\text{fF}$, including bond pads effects.

Reducing the shunt capacitance runs against the need to sustain large ESD currents, as this improves with the size of the diodes. In this design, the sizing of diode arrays has been accomplished by exciting the LNA with HBM discharges as defined by the standard MIL-STD-883G [6]. As an example, Fig.4 shows the discharge current and the gate voltage of M_0 when the LNA is stressed by a +2kV HBM signal. The breakdown voltage for this transistor is 2.7V, higher than the peak voltage at the gate of M_0. Similar tests have been also applied for negative peak values and other voltages ranging from 0.5kV to 2kV. Table 1 summarizes the HBM ESD characteristics of the LNA, indicating the different satisfied classes.

TABLE 1. Human Body Model Tests

HBM Voltage level	Peak Current	Rise Time	Decay Time	SatisfiedClass
500 V	**315 mA**	**3.5 ns**	**150 ns**	**Class Ib**
1000 V	**622 mA**	**2.5 ns**	**160 ns**	**Class Ic**
2000 V	**1280 mA**	**2.5 ns**	**160 ns**	**Class II**

Together with the ESD protections, a low on-resistance grounded gate NMOS (ggNMOS) device, M_{CL} in the Fig. 1, is used for power clamping the supply node.

IV. LNA Performance

Fig.5 shows the layout of the LNA which occupies and area of 0.7mm^2, including pads, in a 0.13µm CMOS technology. The size of the input device M_0 was chosen according to

[3] and employs a finger structure to reduce as much as possible its gate resistance. The size of M_1 has been chosen to be the same as M_0 and, in the layout, they have been placed next to each other [2]. This choice adequately reduces the Miller effect and also facilitates merging of the drain of M_0 and source of M_1, reducing the cascode node capacitance. Critical nodes of the circuit (including input and output pads) have been shielded from the substrate by metal plates to ground – this prevents the parasitic substrate resistance from degrading the *NF*. The layout includes metal-sandwich decoupling capacitors between the power supply and ground to stabilize the LNA biasing.

Figs.6-7 have been obtained using electrical simulations from extracted layout, including foundry-provided estimations of the package parasitics and bondwire electrical characteristics. The input and output terminals of the LNA have been 50Ω matched with reflection coefficients S_{11} < -30dB and S_{22} = -30dB over the 2.4GHz ISM band. The measured power gain of the amplifier is shown in Fig.6. The gain has a peak value of 16.8dB at 2.46GHz and remains above 16.5dB over the ISM band. Fig.7 shows the noise figure of the LNA, revealing that it remains around 1.8dB in the band of interest. The proposed LNA achieves a reverse isolation value lower than -29dB and a stability factor of about 1.8. Finally, as Fig.8 shows, the achieved IIP_3 is 1dBm, obtained by a two-tone test with 2MHz beat frequency in the 2.4GHz ISM band.

V. Conclusions

A 1.2V 2.4GHz 0.13µm CMOS LNA has been presented. The LNA is HBM ESD-protected ±2.0kV and achieves less than 1.8dB noise figure. The circuit uses 15 pins of a QFN24 package and occupies 0.7mm^2. The current consumption of the LNA is about 4.4mA and obtains almost 17dB power gain.

Acknowledgments

This work has been supported by the TIC2003-02355 and the TEC2006-03022 Projects.

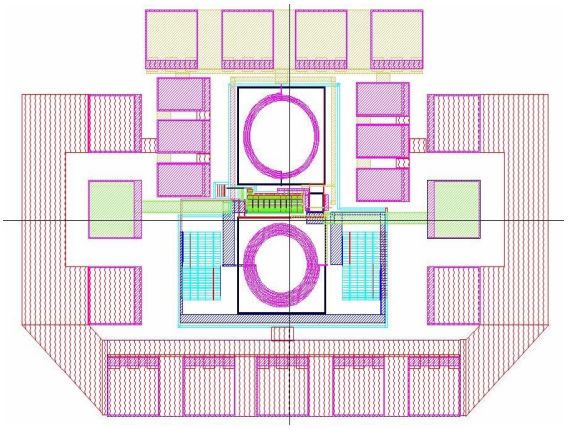

Figure 5. Layout of the LNA.

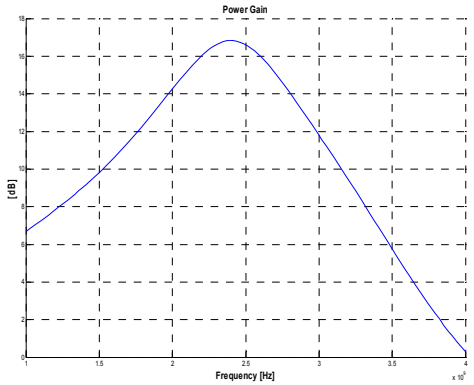

Figure 6. Power Gain.

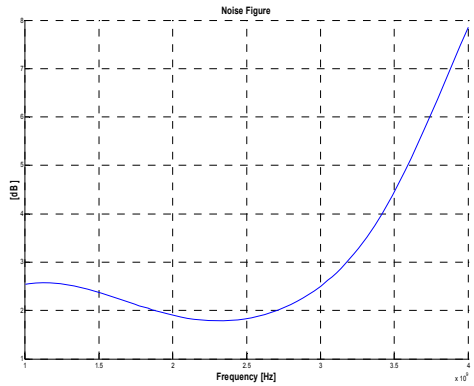

Figure 7. Noise Figure.

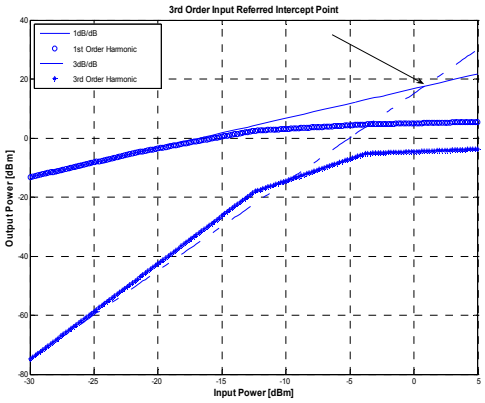

Figure 8. Two-Tone IIP3 measure.

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