A Chaotic Switched-Capacitor Circuit for Characteristic CMOS Noise Distributions Generation

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***Abstract*—A switched-capacitor circuit is proposed for the generation of noise resembling the typical noise spectral density of MOS devices. The circuit is based on the combination of two chaotic maps, one generating $1/f$ noise (*hopping* map) and the other generating white noise (*Bernoulli* map). Through a programmable weighted adder stage, the contribution of each map can be controlled and, thereby, the position of the corner frequency. Behavioral models simulations were carried out to prove the correct functionality of the proposed approach.**

I. Introduction

Noise signals are required for instrumentation, signal processing, cryptography and communications, among other application areas [1][2][3]. For instance, noise signals are used in instrumentation for testing the dynamic behavior of electronic systems [4]. Noise signals are also used for dithering analog-to-digital converters, thus spreading quantization errors and other spurious behaviors over the spectrum [5]. In many of these areas, embedding and compactness requirements call for simpler possible realizations. Actually, embedded noise generators are required for the implementation of Built-In Self-Test (BIST) techniques [6].

In the quest of compact noise source implementations, the use of chaotic discrete maps is a very convenient choice for three reasons: i) discrete maps are dynamical systems, represented by deterministic models in finite differences, which are able to generate random behaviors. Their extremely large sensitivity to the initial conditions makes them highly unpredictable [7]; ii) they are readily realized by using state-of-the-art switched-capacitor circuit techniques and have been profusely demonstrated through monolithic implementations [8]; iii) they intrinsically provide rail-to-rail analog noise signals without further amplification needed.

Two discrete maps of special relevance for noise generation are the Bernoulli map (white noise generator) and the hopping map ($1/f$ noise generator). As will be shown in this paper, their outputs can be linearly combined to obtain a typical CMOS noise distribution which fits to a $1/f$ distribution up to a corner frequency (*fc*) where white noise becomes dominant. The position of this corner frequency can be adjusted by weigthing the contribution of each noise source.

This paper details the design of a switched-cpacitor circuit for the generation of MOS-like noise distributions and is organized as follows. Section II describes the discrete maps mentioned above and introduces their circuital implementation. Simulation results with Matlab® Simulink® and Verilog-A models in Cadence® Virtuoso® are shown in Section III. Section IV introduces the programmability of the map. Finally, the conclusions are drawn in Section IV.

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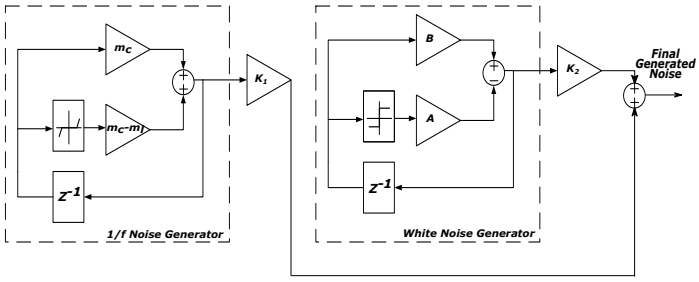

Fig. 1. Block Diagram of proposed system for generating CMOS noise distributions.

II. Discrete Maps For Generating Noise Distributions

Every mathematical model for chaos generation has two components: dynamics and nonlinearity. In the case of chaotic discrete maps, the dynamics is implemented through delays and the nonlinearity is typically carried out with dynamic comparators. The proposed noise generator is based on the combination of two discrete maps, the hopping map and the Bernoulli map, as shown in Fig. 1. The electronic implementations of the dynamics and nonlinearity for both maps are described next.

A. The Bernoulli Map

Fig. 2 (a) displays a representation of the Bernoulli map, which is described by the recursive equation

$$x(k+1) = B \cdot x(k) - A \cdot sgn(x(k)) \tag{1}$$

where parameter *A* sets the definition interval, parameter *B* defines the slopes of the return map at both sides of the transition and function *sgn(x(k))* determines the sign of x at instant k.

For its electronic implementation (see Fig. 3), the slope *B* is set by the capacitor ratio C_2/C_3 and parameter *A* is defined

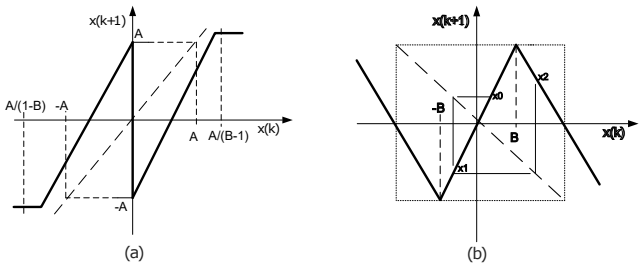

Fig. 2. (a) The Bernoulli map implementation without parasitic stable points. (b) The hopping map with transition point examples and margins to not lock in parasitic stable points.

by the dc voltage V_E scaled by C_1/C_3 [8]. Both ratios are implemented through a weighted adder built around Op-amp A_1. This adder also adds half delay in the circuit dynamics and amplifier Op-amp A_2 adds the other necessary half delay for implementing (1). Regarding the nonlinearity, it is achieved via a phase-reverse switch arrangement controlled by a dynamic comparator. Thus, digital signal α determines if parameter *A* is added or subtracted in the return map.

Care must be taken in guaranteeing the return map does not get locked in parasitic states due to the saturation of Op-amps. To avoid this situation, the dc voltage V_E has to be chosen so that

$$\begin{aligned} A < V_{sat+} < A/(B-1) \\ A/(1-B) < V_{sat-} < -A \end{aligned} \tag{2}$$

where V_{sat+}, V_{sat-} denote the positive and negative saturation levels of the Op-amps.

B. The Hopping Map

The $1/f$ noise is an ubiquitous noise contribution in MOS technologies which is dominant at low frequencies. The hopping map [7], also known as *zigzag* map [9], has been demonstrated to generate controllable *colored* noise. This map is described as

$$x(k+1) = \begin{cases} m_l \cdot x(k) + K & B < x(k) < m_c \cdot B \\ m_c \cdot x(k) & -B < x(k) < B \\ m_l \cdot x(k) - K & -m_c \cdot B < x(k) < -B \end{cases} \tag{3}$$

where $K = (m_c - m_l)B$, m_c being the positive slope, m_l the negative slope and B the point where the slope change, as it can be seen in Fig. 2 (b).

The electronic implementation of this map (see Fig. 4) is similar to the *Bernoulli* although in this case three different states must be defined. The dynamic and the nonlinearity are implemented in the same way: dynamic is achieved by using two Op-amps (A_1, A_2) to introduce a delay cycle (half cycle each one) and the nonlinearity is realized via a phase-reverse switch arrangement controlled by two dynamic comparators which determine the region of the map where $x(k)$ is situated, i.e, $Z^+ = Z^- = 0$, $Z^* = 1$ for the central piece, $Z^+ = Z^* = 0$, $Z^- = 1$ for the left one and $Z^* = Z^- = 0$, $Z^+ = 1$ for the right one. The Op-amp A_3 introduces a half cycle delay for reaching values of $x(k)$ situated in one of the negative slopes

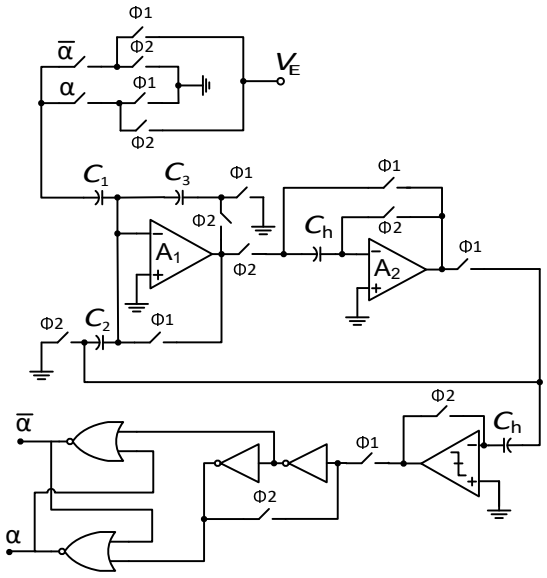

Fig. 3. SC schematics for the Bernoulli map.

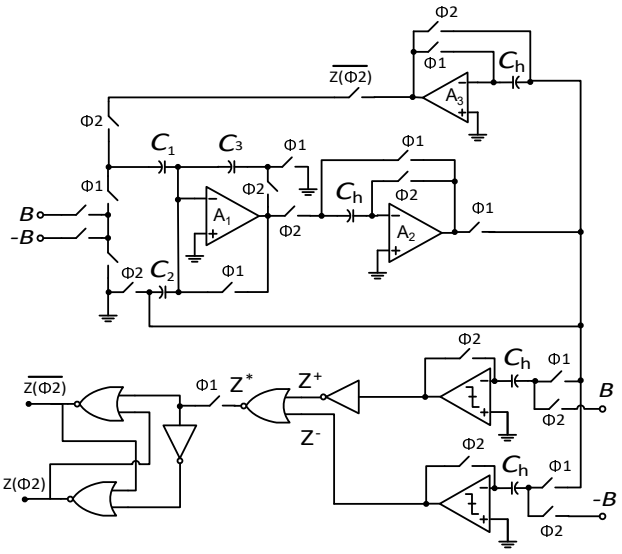

Fig. 4. SC schematics for the hopping map.

of the map, while the Op-amp A_1 and its related capacitor acts as a weighted adder which controls the slopes of the map

$$m_c = \frac{C_2}{C_3} \qquad m_l = \frac{C_2 - C_1}{C_3} \tag{4}$$

To not get locked at parasitic stable points due to Op-amps saturation voltages, the length of the margins of the map in Fig. 2 (b) must be $2 \cdot m_c \cdot B$ for being inside the Op-amps saturation levels.

III. Programmability Of The Circuit

The herein proposed architecture generates typical MOS noise distributions by combining the two discrete maps above. This combination is achieved, by a programmable weighted adder (see Fig. 5) with the variable capacitors being realized by

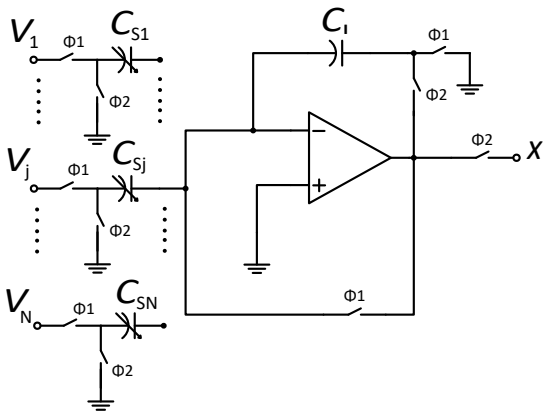

Fig. 5. Weighted adder with programmable gain.

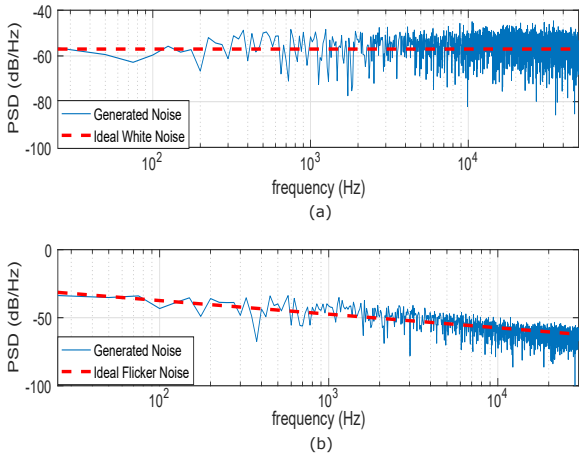

Fig. 6. PSD comparison between generated noise from simulation and ideal noise distribution (a) the Bernoulli map. (b) the hopping map.

programmable capacitor banks. Similar adders were also used in the implementation of the discrete maps (Op-amps A_1 and related capacitors for both maps). By applying the charge conservation principle, the operation of the weighted adder is defined by

$$\begin{aligned} x(k+1) &= \textstyle\sum_{j=1}^{N} \frac{C_{Sj}}{C_I} \cdot v_j(k+1/2) \\ x(k+1/2) &= 0 \end{aligned} \tag{5}$$

Based on this, two different programmability levels can be defined in the proposed circuit. First, the weighted adders in the individual discrete maps make their respective slopes tunable, what translates into significant differences in the generated noise distributions such as, for instance, the power exponent of the flicker distribution. Second, the weighted adder which combines both discrete maps adds to the circuit the possibility of changing the gain of each distribution, varying the total integrated noise and the corner frequency of the final distribution.

The proposed noise generation method also offers a low complexity alternative for the synthesis of flicker noise in mathematical packages, such as Matlab® Simulink®. Default functions in these tools (as `DSP.Colorednoise` in Matlab® [10]) rely on shaping white noise distributions with high-order autoregressive filters, which requires far more computations than by adding the contributions of two simple discrete maps. Hence, this method allows the designer to use the same approach to generate noise from the first mathematical approach to the final IC.

IV. Simulation Results

The power spectral density of each map has been obtained in order to prove the correct generation of an uniform distribution, for white noise, and a $1/f$ distribution, for flicker noise. Furthermore, ideal distributions for both signals (uniform and $1/f$) have been generated using Matlab® Simulink®. Fig. 6 (a) shows a comparison between the ideal uniform distribution and that obtained with the Bernoulli map. It can be observed that the generated noise distribution featured by the map is very similar to the ideal one. In the case of the $1/f$ noise, the comparison is shown in Fig 6 (b). To better appreciate how the noise generated by the circuit fits to the ideal one, they have been integrated in a frequency band from 25 Hz to 100 kHz. For white noise it is obtained 0.090 V_{rms} for the generated distribution and 0.078 V_{rms} for the ideal one, and for $1/f$ noise it is obtained 0.101 V_{rms} for the generated and 0.091 V_{rms} for the ideal one. Thus, both distributions could be considered valid approximations of the ideal distributions.

In order to check the performance of the proposed circuit, various simulations were carried on Cadence® Virtuoso® with behavioral models –using Verilog-A descriptions for the amplifiers– of the circuit components. The robustness of the circuit has been assessed by taking into account capacitor mismatches and reference voltage variations. The most dramatic impact of these non-idealities would be the onset of parasitic stable states, where trajectories may get locked. This potential problem has been tackled by employing structural stability techniques reported in [8] and [11]. Additionally, *MonteCarlo* simulations have been carried out for addressing the impact of capacitor mismatches, assuming 10% variations of the reference voltages as well. These simulations do not reveal significant changes on the statistical properties of the circuit and, indeed, the return maps of the noise generators are only slightly modified, as shown in Fig. 7. In these plots, the capacitors of both circuits have been nominally set to achieve: $B = 1.9; A = 1; f_{clk} = 200kHz$ for the Bernoulli map and $m_c = 2.5; m_l = -1.7; B = 0.4; f_{clk} = 200kHz$ for the hopping map. Furthermore, various noise distributions generated by the complete circuit with different corner frequencies (f_c) have been generated and their corresponding integrated noise (int_{noise}) from 100 Hz to 30 kHz have been calculated (see Fig. 8). As shown in the caption of this figure (ony two configurations are shown for simplicity), there are no significant deviations in the position of the corner frequency or the integrated noise.

Finally, a comparison has been made between the proposed circuit and noise results from simulations of a LNA for neural recording applications (Fig. 9) in CMOS $0.18\mu m$ technology,

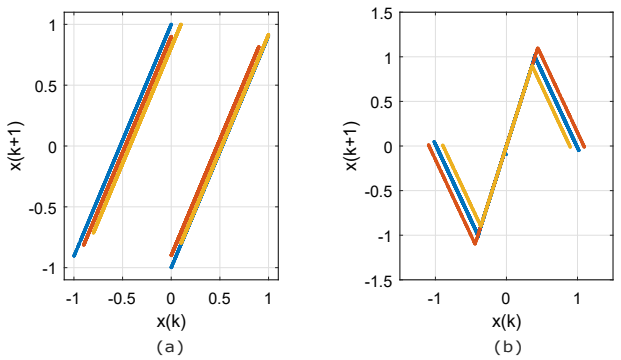

Fig. 7. Simulation results of implementing maps with capacitor mismatch and variations of the voltage references (a) the Bernoulli map. (b) the hopping map.

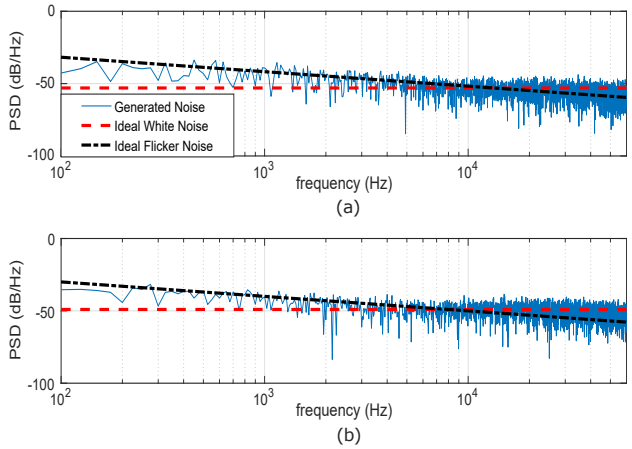

Fig. 8. Different PSDs generated by the SC circuit (a) PSD for $fc \simeq 11 \pm 0.3kHz$ and $int_{noise}(100Hz - 30kHz) \simeq 0.201 \pm 0.02V_{rms}$. (b) PSD for $fc \simeq 7.5 \pm 0.25kHz$ and $int_{noise}(100Hz - 30kHz) \simeq 0.144 \pm 0.015V_{rms}$.

previously presented in [12]. Fig. 9 (a) shows that the corner frequency is practically the same for both distributions (around 500 Hz). However, in order to prove the validity of these results, both distributions have been integrated in band from 10 Hz to 5 kHz. The results of this integration show a difference of 0.09 μV_{rms} between the integrated noise from LNA (2.82 μV_{rms}) and the integration of the generated noise by the circuit (2.91 μV_{rms}), thus verifying the correct performance of the proposed circuit.

V. Conclusion

An architecture is reported for the generation of typical MOS spectral noise distributions using discrete maps and switched-capacitor circuits. The distribution can be shaped by properly changing circuit design parameters through capacitor ratios. Such kind of noise source is of interest for applications whose noise sensibility is one the most crucial parameters for the correct performance of the circuit, such as biomedical and another sensing applications.

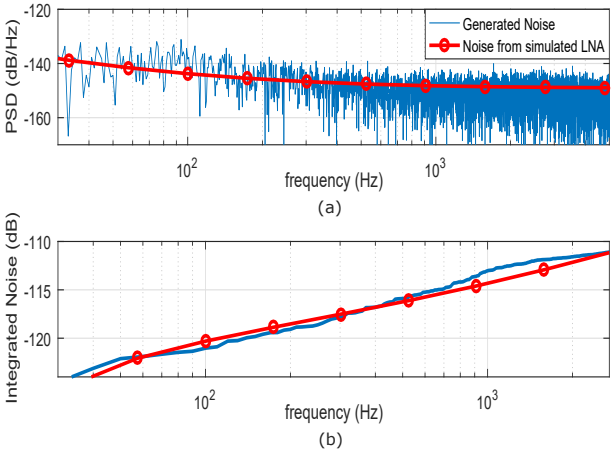

Fig. 9. Comparison between generated noise by discrete maps and simulated results from a LNA in CMOS $0.18\mu m$ (a) PSD comparison. (b) Integrated noise comparison.

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