Accurate Settling-Time Modeling and Design Procedures for Two-Stage Miller-Compensated Amplifiers for Switched-Capacitor Circuits

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***Abstract*—We present modeling techniques for accurate estimation of settling errors in switched-capacitor (SC) circuits built with Miller-compensated operational transconductance amplifiers (OTAs). One distinctive feature of the proposal is the computation of the impact of signal levels (on both the model parameters and the model structure) as they change during transient evolution. This is achieved by using an event-driven behavioral approach that combines small- and large-signal behavioral descriptions and keeps track of the amplifier state after each clock phase. Also, SC circuits are modeled under closed-loop conditions to guarantee that the results remain close to those obtained by electrical simulation of the actual circuits. Based on these models, which can be regarded as intermediate between the more established small-signal approach and full-fledged simulations, design procedures for dimensioning SC building blocks are presented whose targets are system-level specifications (such as ENOB and SNDR) instead of OTA specifications. The proposed techniques allow to complete top-down model-based designs with 0.3-b accuracy.**

***Index Terms*—Analog circuit design, data converters, design methodology, operational amplifiers, switched-capacitor (SC) circuits.**

I. Introduction

THE performance of switched-capacitor (SC) circuits is determined in many practical situations by that of the operational transconductance amplifiers (OTAs) used to build them [1]–[5]. Modern applications require SC-based data converters and filters with cutting-edge performance specifications and reduced power budget. These requirements pose demanding challenges on the OTAs; challenges which can be only addressed by means of thorough electrical design of these amplifiers. To that purpose, designers rely on *models* to capture the impact of OTA nonideal behaviors and make use of structured *top-down* methodologies [6], [7], and *optimization* tools [8]–[12]. However, available models, procedures and tools do not suffice for accurate design at high speed due to different reasons, namely those given as follows.

- The settling performance of SC building blocks is typically evaluated by means of *small-signal* models with fixed parameter values. These parameter values are extracted by characterizing the OTA behavior in *open-loop* configuration. Actual closed-loop conditions are emulated by accounting for the impact of the driving and feedback capacitors onto equivalent loading values [13]–[18]. However, there are significant phenomena not accounted for such as: 1) the impact of the signal level and, hence, the biasing, on the parameter values; 2) the lack of model structures capable to capture hard nonlinear deviations versus the ideal linear behavior; 3) the movement of closed-loop poles and zeros due to changes of the model parameters during transient evolution. As a consequence, significant errors (more than one order of magnitude in some cases) arise in the evaluation of the settling behavior, thereby precluding optimum electrical design of the amplifiers.
- Conventional top-down methodologies employed for structured design map specifications of the subsystems (such as signal-to-noise-plus-distortion ratio (SNDR) or effective number of bits (ENOB) of data converters) onto specifications pertaining to the open-loop behavior of the OTAs (such as dc gain, gain-bandwidth product, or phase margin). However, such mapping is not bi-univocal; i.e., using OTAs with the so calculated open-loop specifications does not guarantee achieving the targeted subsystem performance when the feedback loop around the OTAs is closed. Hence, in practice, the so-calculated open-loop specifications must be refined by *bottom-up* iterative simulation loops to guarantee proper behavior within closed-loop conditions.

Designers do typically circumvent these drawbacks by simply *over-sizing* OTAs. This limits the ability of OTAs to achieve aggressive specifications and, hence, the potential of submicron technologies.

This paper presents modeling techniques and design procedures to overcome above drawbacks by:

- using accurate models for the settling performance of OTA-based building blocks; these models account for: 1) the jumps of the initial conditions caused by charge redistribution between consecutive clock phases; 2) the accurate estimation of parasitics capacitances from technological parameters; 3) the limitations of internal currents due to transistor nonlinearities; and 4) the impact of the variation of the dc gain of OTAs with the signal level.
- using high-level specifications (such as SNDR or ENOB) instead of open-loop OTA specifications, as targets for the design procedure; results for 130-nm and 90-nm technologies are presented showing very efficient solutions to the sizing problem for given ENOB target.

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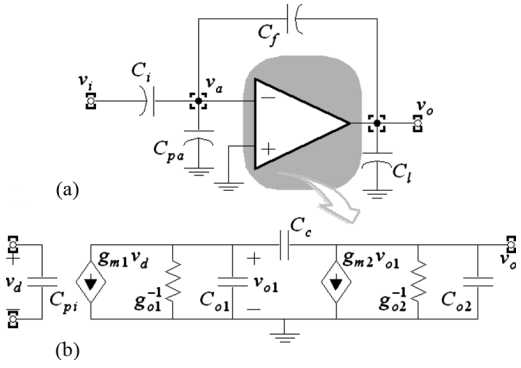


Fig. 1. (a) Typical configuration of an SC circuit during the charge-transfer phase. (b) Two-stage Miller-compensated opamp small-signal model.

To the best of our knowledge, no previously reported models have accounted for the variation of dc gain as signal evolves during the transient process. The herein reported model accounts for these variations and shows capable to evaluate settling errors with down to 3% accuracy versus fully detailed electrical simulations.

We focus herein on two-stage Miller-compensated OTAs (MC-OTA). The reason is that these topologies are better suited than single-stage ones to achieve large values of the dc gain concurrently with large output swing in low-voltage submicron technologies [19]–[21]. In any case, the herein proposed concepts can be applied to single-stage as well as to other multistage OTA topologies [4].

This paper is organized as follows. Section II presents a small-signal model for a closed-loop SC amplifier using a two-stage MC-OTAs and illustrates the errors obtained by using this model. The proposed behavioral model is described in Section III. Section IV uses this model for a design procedure oriented towards satisfying system-level specifications with minimum power consumption. Several examples illustrating the performance of the proposed design procedure are presented in Section V. Finally, Section VI gives some concluding remarks.

II. Closed-Loop Small-Signal Analysis

Fig. 1(a) shows the capacitive feedback configuration typically found in SC circuits during the charge transfer phase [1]–[5].[1] Although this figure is single-ended for simplicity, all results are extendable to differential structures. In Fig. 1(a), C_i and C_f model the sampling and feedback capacitances, respectively, and C_{pa} and C_l stand for the sum of all of the extrinsic capacitances at the input and output terminals of the OTA, respectively. These latter capacitances include parasitics associated with switches and capacitors and any other external capacitance loading the node.

Let us consider an MC-OTA modeled by the small-signal equivalent circuit of Fig. 1(b). Each of the two stages is characterized by a single-pole network defined by a transconductance, output resistance, and output capacitance. Capacitor C_{pi} represents the input capacitance of the amplifier, and the Miller pole-splitting capacitor C_c provides the frequency compensation mechanism to avoid closed-loop instability. By replacing this model into Fig. 1(a), the transfer function for the holding phase is found, given as (1) shown at the bottom of the page, where

$$C_{\rm eq} = \left(C_p + C_i + \frac{C_t}{\beta}\right)\frac{1}{\beta_c} + \frac{C_{o1}}{\beta} \tag{2}$$

is the equivalent capacitive load of the amplifier in closed-loop configuration, feedback factors β and β_c are defined as

$$\beta = \frac{C_f}{C_p + C_i + C_f} \quad \beta_c = \frac{C_c}{C_c + C_{o1}} \tag{3}$$

and ε_g, ε_{g1}, ε_{g2}, and ε_z are error terms due to the finite dc-gain of the amplifier stages which are defined, respectively, as $A_1 = g_{m1}/g_{o1}$ and $A_2 = g_{m2}/g_{o2}$. Such error terms are given by

$$\begin{aligned} \varepsilon_{g1} &= \frac{1}{\beta A_1}\left(\frac{1 + C_p + C_i + C_t/\beta}{C_c}\right) \\ \varepsilon_{g2} &= \frac{1}{A_2\beta_c} \\ \varepsilon_g &= \frac{1}{\beta A_1 A_2} \end{aligned} \tag{4}$$

$$\varepsilon_z = \frac{C_f}{A_1 C_c}. \tag{5}$$

Finally, capacitances C_p and C_t sum up all of the grounded capacitances at the input and output of the amplifier, i.e., $C_p = C_{pa} + C_{pi}$ and $C_t = C_{o2} + C_l$.

The poles and zeros of (1) are calculated as

$$\begin{aligned} p_{1,2} &= -\alpha\left(1 \pm \sqrt{1 - \frac{g_{m1}g_{m2}}{C_c C_{\rm eq}\alpha^2}(1+\varepsilon_g)}\right) \\ &\equiv -\alpha\left(1 \pm \sqrt{1 - \frac{\omega_n^2}{\alpha^2}}\right) \end{aligned} \tag{6}$$

$$z_{1,2} = -\frac{g_{m1}\beta_c}{2C_f}(1+\varepsilon_z)\left(1 \pm \sqrt{1 + \frac{4g_{m2}C_f}{g_{m1}C_c\beta_c(1+\varepsilon_z)^2}}\right) \tag{7}$$

where

$$\alpha = \left[\frac{g_{m2}}{\beta}(1+\varepsilon_{g2}) - g_{m1}(1-\varepsilon_{g1})\right]\frac{1}{2C_{\rm eq}}. \tag{8}$$

$$H(s) = \frac{\left(s^2 + \frac{g_{m1}\beta_c}{C_f}(1+\varepsilon_z)s - \frac{g_{m1}g_{m2}\beta_c}{C_cC_f}\right)\frac{C_i}{\beta_c C_{\rm eq}}}{s^2 + \left(\frac{g_{m2}}{\beta}(1+\varepsilon_{g2}) - g_{m1}(1-\varepsilon_{g1})\right)\frac{s}{C_{\rm eq}} + \frac{g_{m1}g_{m2}}{C_cC_{\rm eq}}(1+\varepsilon_g)} \tag{1}$$

[1]In this work, the effect of the *RC* time constants arising from the switch resistances on the settling performance of the SC circuit is assumed to be nondominant. Their impact has been thoroughly analyzed in [22] and [23].

Let us now assume for illustration purposes that the system is *critically damped*.[2] It means that the poles of $H(s)$ are real and identical and that the damping factor $\zeta = \alpha/\omega_n$ of the system is 1. Thus, the poles and zeros become

$$p = \frac{\frac{-2g_{m1}}{C_c(1+\varepsilon_g)}}{\frac{1+\varepsilon_{g2}}{\beta} - \frac{1-\varepsilon_{g1}}{R}} = -\omega_n = -\alpha \tag{9}$$

$$z_{1,2} = -\frac{g_{m1}\beta_c}{2C_f}(1+\varepsilon_z) \times \left(1 \pm \sqrt{1 + \frac{4RC_f}{C_c\beta_c(1+\varepsilon_z)^2}}\right) \tag{10}$$

where the transconductance ratio $R = g_{m2}/g_{m1}$ is constrained by the expression

$$R = \frac{\beta(1-\varepsilon_{g1})}{1+\varepsilon_{g2}} + \frac{2\beta C_{\rm eq}(1+\varepsilon_g)}{C_c(1+\varepsilon_{g2})^2} \times \left(1 + \sqrt{1 + \frac{(1+\varepsilon_{g2})(1+\varepsilon_{g1})C_c}{(1+\varepsilon_{g2})^2\beta C_{eq}}}\right). \tag{11}$$

Based on previous analysis, the transfer function of Fig. 1(a) is written as

$$H(s) = A_{cl}\frac{(1-\frac{s}{z_1})(1-\frac{s}{z_2})}{s^2+2\alpha s+\alpha^2} \tag{12}$$

where $A_{cl} = C_i/(C_f(1+\varepsilon_g))$ is the dc gain of the system. Using (12) and assuming null initial conditions, the dynamic response to a step signal of amplitude V_i, applied at $t = 0$, is given by (13), shown at the bottom of the page.

Considering a clock signal of period T_s and 50% duty cycle, the error voltage at the end of the holding phase, after $T_s/2$ s, is given by

$$v_e\left(\frac{T_s}{2}\right) = \frac{C_i}{C_f}V_i - v_o\left(\frac{T_s}{2}\right) = \frac{\varepsilon_g + \varepsilon_s\left(\frac{T_s}{2}\right)}{1+\varepsilon_g}\frac{C_i}{C_f}V_i. \tag{14}$$

This expression takes into account the *finite dc gain error*, represented by ε_g and the so-called *settling error*, obtained from (13), as shown by (15) at the bottom of the page.

Previous models and expressions can be employed for *synthesis*, i.e., to guide a sizing process for given settling-time target specifications. This is actually how conventional approaches work [13]–[18]. However, it means assuming that the model topology of Fig. 1(b) and its parameters remain unchanged for the whole signal range. These assumptions produce significant deviations which are illustrated via the sample-and-hold (S/H) SC circuit of Fig. 2.

[2]Models for the under- and over-damped cases have been also developed. Techniques and results presented in this section are applicable to these cases as well.

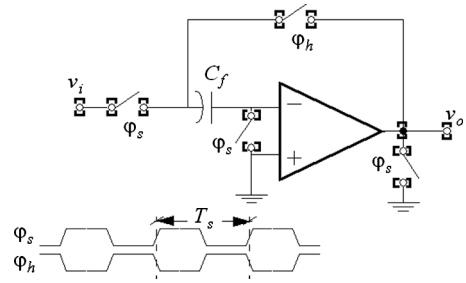


Fig. 2. Flip-around-type S/H SC amplifier.

TABLE I
MODEL PARAMETERS

Sampling capacitor C_i (pF)	0
Feedback capacitor C_f (pF)	3
Compensation capacitor C_c (pF)	1.05
Input parasitic capacitance C_p (pF)	0.06
First-stage transconductance g_{m1} (mA/V)	1.29
First-stage output cap. C_{o1} (pF)	0.54
First-stage gain A_{o1}	96.2
Second-stage transconductance g_{m2} (mA/V)	14.71
Second-stage output cap. C_t (pF)	0.47
Second-stage gain A_{o2}	20.1

Table I recasts parameters for the small signal of Fig. 2. These parameters have been extracted from a fully sized transistor-level design of a fully differential MC-OTA. Fig. 3 compares the transient evolution of the small-signal model to that obtained from electrical simulations of the transistor-level circuit under the same excitation. Discrepancies are noticeable. Actually, whereas the model yields a settling error of only 0.15 mV, transistor-level simulations produce an error of 1.72 mV. This renders the approach hardly feasible for practical usage.

III. BEHAVIORAL MODEL: ACCOUNTING FOR LARGE-SIGNAL EFFECTS

The herein proposed model overcomes these drawbacks by: 1) capturing topological model changes caused by hard nonlinearities (such as saturations of the voltage-controlled-current-

$$v_o(t) = A_{cl}\left[1 - e^{-\alpha t}\left(1 - \frac{\alpha^2}{z_1 z_2} + \alpha\left(1+\frac{\alpha}{z_1}\right)\left(1+\frac{\alpha}{z_2}\right)t\right)\right]V_i \tag{13}$$

$$\varepsilon_s(t)|_{t=T_s/2} = e^{-\alpha T_s/2}\left(1 - \frac{\alpha^2}{z_1 z_2} + \alpha\left(1+\frac{\alpha}{z_1}\right)\left(1+\frac{\alpha}{z_2}\right)\frac{T_s}{2}\right) \tag{15}$$

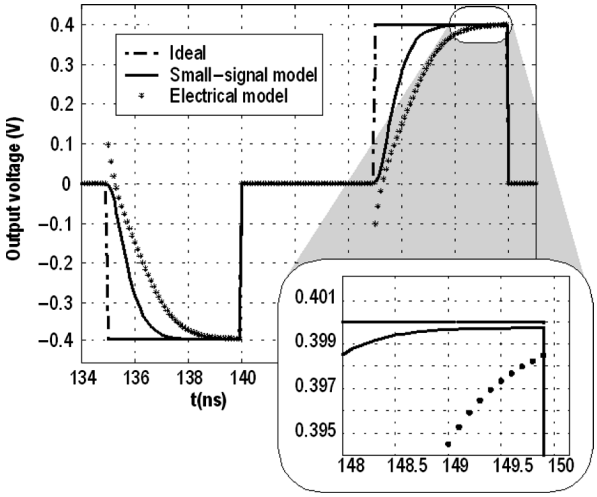


Fig. 3. Output waveforms of the S/H amplifier of Fig. 2 obtained both from small-signal model and transistor-level simulations, together with the ideal response.

sources); 2) capturing variations of the small-signal parameters due to changes of the signal levels and hence of the biasing conditions; and 3) accounting for modifications of the initial conditions caused by charge redistribution at the clock edges.

Because the detailed formulation is rather involved, in what follows, only a brief description of the effects considered and how they have been tackled will be presented.

As can be seen at Fig. 3, initial conditions at the beginning of every holding phase play a significant role in the dynamic response of the SC block. *Charge conservation* makes the output of the SC block, v_o, jumps in the opposite direction to its final value, producing a discontinuity at every switching instant which worsens the settling behavior of the SC circuit. Similar transients also happen at the input, v_a, and internal, v_{o1}, nodes of the amplifier [see Fig. 1(a))]. The values of these jumps just after switching from the previous storage phase can be obtained by applying the charge conservation principle, resulting in

$$v_{ai} = \frac{1}{\beta C_{\text{eq}}} \times \begin{bmatrix} C_l v_{l,n-1} - (\beta_c C_{o1} + C_t)\, v_{f,n-1} + \\ \frac{C_i}{C_f}\,(C_f + \beta_c C_{o1} + C_t)\,(v_{i,n} - v_{i,n-1}) \end{bmatrix} \quad (16)$$

$$v_{oi} = \frac{1}{\beta_c C_{\text{eq}}} \begin{bmatrix} \frac{1}{\beta} C_l v_{l,n-1} + (C_p + C_i)\, v_{f,n-1} + \\ C_i (v_{i,n} - v_{i,n-1}) \end{bmatrix} \quad (17)$$

$$v_{o1i} = \frac{1}{C_{\text{eq}}} \begin{bmatrix} \frac{1}{\beta} C_l v_{l,n-1} + (C_p + C_i)\, v_{f,n-1} + \\ C_i (v_{i,n} - v_{i,n-1}) \end{bmatrix} \quad (18)$$

where $v_{i,n-1}$, $v_{f,n-1}$, and $v_{o,n-1}$ are the voltages stored in the sampling C_i, feedback C_f, and load C_l capacitors during the previous clock phase, respectively.[3] Following the jumps, the SC circuit should ideally evolve according to the small-signal model of Section II. However, depending on initial conditions, it may occur that some of the transconductors in Fig. 1(b), or both, saturate so that the corresponding node evolves at a fixed slew-rate. Let us use i_{o1} and i_{o2} to denote the maximum output currents of the first and second amplifier stages, respectively. Four situations can be distinguished for the initial evolution of the node voltages in the circuit. Table II recasts the equations corresponding to the output voltage for the critically damped case. The model also computes the evolution of the internal nodes $v_a(t)$ and $v_{o1}(t)$, but they are omitted here for simplicity. Obviously, as time evolves, the circuit may change from one of these situations to another possibility which is contemplated in the proposed behavioral model.

Let us now consider the change of dc gain with signal level. It is quite obvious that this effect must be considered for accuracy since the small-signal parameters and, hence, the dc gain depends on biasing; and biasing changes with the signal level. Fig. 4(a) illustrates the variation of the dc gain of the amplifier considered in previous section. The dc gain of the first OTA stage A_1 and that of the second OTA stage A_2 are depicted. Changes of the latter are significant while those of the former are attenuated by A_2.

DC gain nonlinearity not only impacts the static resolution of the SC block but also the locations of the system poles as they depend on the error factors ε_g, ε_{g1} and ε_{g2}, which, in their turn, vary with A_1 and A_2. This is illustrated in Fig. 4(b), which shows how the poles of the S/H amplifier described in Section II evolve with the output voltage. At the nominal operating point, the system is critically damped and the poles coincide. However, as the output voltage moves from this point, the dc gain of the amplifier decreases, poles split along the real axis, and the system becomes over-damped and, hence, slower. This effect translates into a notable increase in harmonic distortion as shown in Fig. 4(c), where the output spectra of an OTA in a practical case (the so-called scenario B in Table III, assuming a 90 nm CMOS technology) has been evaluated with and without nonlinear dc gain influence.

Since the dc gain of the input stage remains practically constant with the output voltage in most practical cases, only the nonlinear behavior of the second stage is considered in the proposed behavioral model. This nonlinear dependence is expressed in polynomial form as

$$A_2 = A_{o2}\left(1 + a_1 v_o + a_2 v_o^2 + a_3 v_o^3 + a_4 v_0^4\right) \quad (19)$$

where A_{o2} is the dc gain of the output stage at the quiescent point, and $a_1, a_2, \ldots$ are nonlinear coefficients, usually given in $\%/\text{V}$, $\%/\text{V}^2, \ldots$

Fig. 5 shows the basic flowchart implemented in the proposed behavioral model for the estimation of the transient response of a two-stage Miller-compensated amplifier during the charge transfer phase of a conventional SC circuit. It is worth noticing that the impact of the amplifier nonlinear gain depends at every moment on the output voltage, which, in its turn, is continuously evolving with time. Therefore, in order to emulate this time dependence, the charge-transfer phase is divided into M subintervals, in which the gains and pole positions of the system are recalculated. Note that the system may eventually exhibit a different damping factor from one subinterval to another and, therefore, the set of equations describing the transient evolution may also vary depending on the subinterval.

Fig. 6 illustrates the results of transient analysis using the proposed model under the same conditions in Fig. 3. Actually, two behavioral simulations have been included in the plot. In

[3]In this paper, the notation $v_{x,n}$ will be used to represent $v_x(nT_s)$.

TABLE II
EVOLUTION IN AMPLIFICATION PHASE OF THE TWO-STAGE MILLER-COMPENSATED OTA

Evolution	Expression for $v_o(t)$	Condition
1stg linear 2stg linear	$v_{oi}-\frac{v_{ai}}{\beta}+\left[\frac{v_{ai}}{\beta}\left(1+\left(\alpha+\frac{g_{m1}}{C_{eq}}\right)t\right)-\frac{g_{m2}v_{o1i}}{\beta\beta_c C_{eq}}t\right]e^{-\alpha t}$	$\lvert v_{ai}\rvert \le i_{o1}/g_{m1}$ $\lvert v_{o1i}\rvert \le i_{o2}/g_{m2}$
1stg slew 2stg linear	$v_{oi}-\frac{1}{\beta_c}\left(1-e^{-\frac{g_{m2}t}{\beta C_{eq}}}\right)v_{o1i}+\left[\left(1+\frac{\beta C_{eq}}{C_c}\right)\left(1-e^{-\frac{g_{m2}t}{\beta C_{eq}}}\right)-\frac{g_{m2}t}{C_c}\right]\frac{i_{o1}}{g_{m2}}$	$\lvert v_{ai}\rvert \ge i_{o1}/g_{m1}$ $\lvert v_{o1i}\rvert \le i_{o2}/g_{m2}$
1stg linear 2stg slew	$v_{oi}+\frac{1}{\beta}\left(1-e^{\frac{g_{m1}t}{C_{eq}}}\right)\left(\frac{i_{o2}}{\beta_c g_{m1}}-v_{ai}\right)$	$\lvert v_{ai}\rvert \le i_{o1}/g_{m1}$ $\lvert v_{o1i}\rvert \ge i_{o2}/g_{m2}$
1stg slew 2stg slew	$v_{oi}+\left(i_{o1}-\frac{i_{o2}}{\beta_c}\right)\frac{t}{\beta C_{eq}}$	$\lvert v_{ai}\rvert \ge i_{o1}/g_{m1}$ $\lvert v_{o1i}\rvert \ge i_{o2}/g_{m2}$

one case, the dc gain variation effect is accounted for whereas, in the other case, all model parameters remain the same but the dc gain variation effect is ignored.

Fig. 6 confirms a close agreement between the electrical simulation and the full-blown behavioral model, i.e., that including the dc gain variation effect; the discrepancy at the end of the holding period amounts to only 5 μV, instead of the 1.57-mV deviation obtained with the model in previous section. In case the dc-gain variation effect is neglected, the discrepancy of the behavioral model rises up to 0.97 mV

IV. DESIGN PROCEDURE

The model described in Section III can be used to support a systematic, structured sizing procedure. Design variables are the value of the compensation capacitor and the parasitic capacitances, transconductances, maximum output currents, and finite dc-gains of the amplifier stages. All of these variables depend ultimately on electrical-level parameters such as widths, lengths, and overdrive voltages of MOS transistors, which are the final outcomes of the design procedure. Circuit elements and parasitics in the SC block other than the OTA itself are regarded as inputs of the algorithm. The design objective is to meet high-level specifications such as the equivalent input noise $\overline{v}_n^2$, output voltage swing OS, and dc gain A_o of the OTA or the ENOB of the whole SC block with minimum power consumption.

The *design space* of this optimization problem can be reduced by imposing constraints on the design variables and the electrical-level parameters. First, *overdrive* voltages of MOS transistors must not exceed an upper value determined by the supply voltage and input/output swing requirements. In the proposed approach overdrive voltages are user-defined parameters. Design criteria for choosing their values are, on the one hand, to guarantee that transistors operate in the saturation region within strong inversion (this poses a lower limit of about 0.1 V on overdrive voltages) and, on the other hand, to enhance tolerance against transistor mismatch and, hence, to reduce random offsets [1]. A second constraint can be extracted from noise requirements. Neglecting flicker contributions, the equivalent input noise of a two-stage OTA can be modeled as

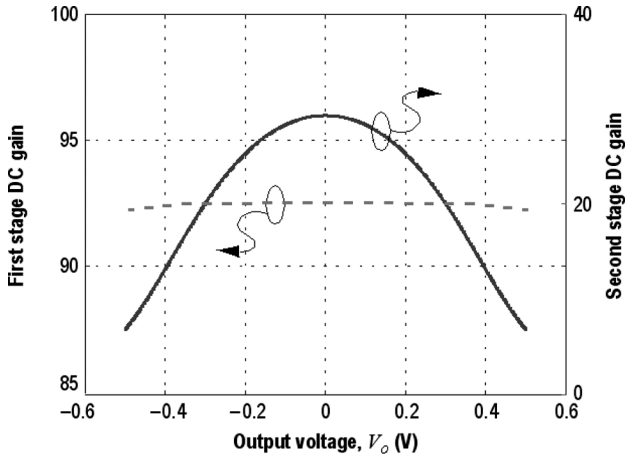
$$\overline{v}_n^2 \approx \frac{8KT}{3g_{m1}}(1+\eta_T) \tag{20}$$

where η_T is a topology-dependent noise factor. Hence, by compelling an upper limit on $\overline{v}_n^2$, a minimum value for the transconductance of the first stage g_{m1} can be derived. Finally, the required system ENOB demands a minimum value for the settling error, or equivalently, a given distribution of poles. Assuming a critically damped response, this implies a minimum value $\alpha_{\min}$ for the natural frequency in α (8).

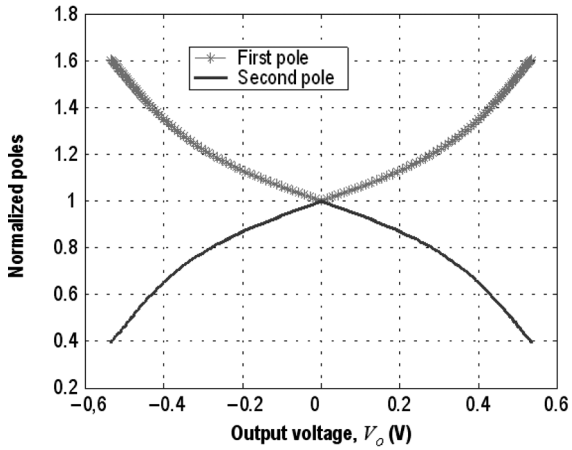
Fig. 7 shows the main flow diagram of the synthesis procedure for a critically damped system. It consists of an iterative search procedure using parameter α as running variable. Extension to other dynamic responses can be simply made by specifying a damping factor $\zeta \neq 1$ correspondingly. The computational loop starts by guessing an initial value for parameter α, in accordance to the provided high-level specifications. In most practical situations, a convenient value for $\alpha_{\min}$ is obtained from $V_{\rm FS}\exp(-\alpha_{\min}T_s/2) < 1$ LSB , where $V_{\rm FS}$ is the full-scale input signal range of the SC circuit and LSB stands for the amplitude of the least significative bit, determined by the required resolution. Then, the OTA is sized by means of the procedure depicted in Fig. 8 to be discussed afterwards. After sizing, the performance of the SC block, including the designed OTA, is evaluated by using the behavioral simulator, described in Fig. 5. If the estimated ENOB is lower than specified, the pole frequency is increased and the process is repeated again.

The OTA sizing routine depicted in Fig. 8 is found at the core of the synthesis procedure of Fig. 7. It consists of a computational loop with the compensation capacitor as running variable. Bound values (C_{ci} and C_{cf}) and discrete increments ΔC_c are user-defined. At each iteration, a new configuration (new transistor sizes and biasing currents) is obtained and the corresponding power consumption is stored. When the loop stops, the routine selects that configuration with the lowest power consumption as the final outcome of the algorithm.

Each iteration in the aforementioned loop starts by guessing initial values for the parasitic capacitances (C_{pi}, C_{o1}, C_{o2}), the finite dc gains of both amplifier stages (A_1, A_2), the topology-dependent noise factor (η_T) and the lengths for the MOS transistors. From these values, intermediate variables such as feedback (β, β_c) and error $(\varepsilon_g, \varepsilon_{g1}, \varepsilon_{g2})$ factors, equivalent load (C_{eq}) and transconductance ratio (R) are evaluated according to (2)–(5) and (11). Then, the minimum value for the transconductance of the first stage (g_{m1}) is computed by



(a)



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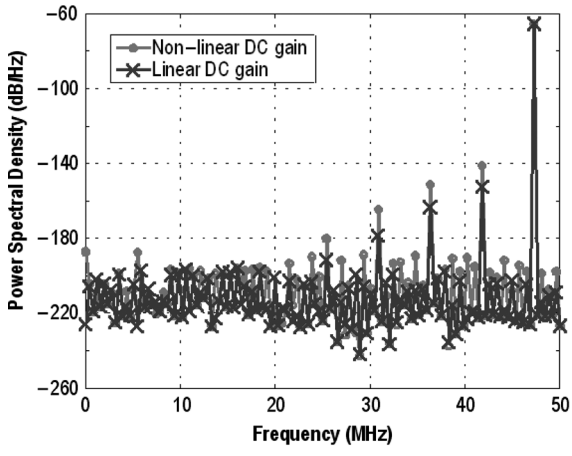

(c)

Fig. 4. Variation with the output voltage of (a) the dc gain of amplifier stages and (b) pole positions. Poles are normalized to their values at the nominal operating point. (c) Output spectra of an OTA in a practical case taking into account or not the nonlinear dc gain effect The estimated third-order harmonic distortion worsens by more than 12 dB if this effect is considered.

TABLE III
DESIGN SCENARIOS

Specifications	Scenario A	Scenario B	Scenario C
SC configuration	S/H	S/H	MDAC
OTA topology	Cascode	Simple	Simple
Number of bits	-	-	3
Sampling capacitor (pF)	-	-	0.15
Feedback capacitor (pF)	3	3	0.15
Load capacitor (pF)	1.1	1.1	0.3
Output swing (V)	≥±0.5	≥±0.5	≥±0.5
Eq. input noise (nV/√Hz)	≤15	≤9.5	≤13
DC-gain	≥2500	≥2500	≥2000
ENOB (bits)	≥8	≥12	≥10
Sampling freq. (MHz)	100	100	100

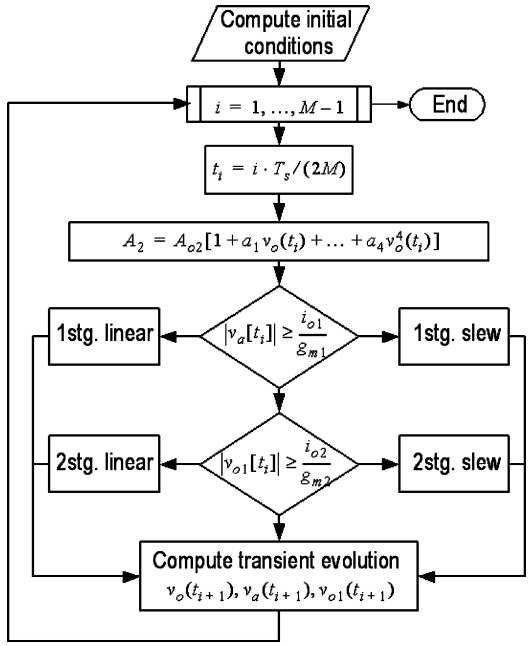

Fig. 5. Basic flowchart of the proposed behavioral model for the two-stage Miller-compensated OTA.

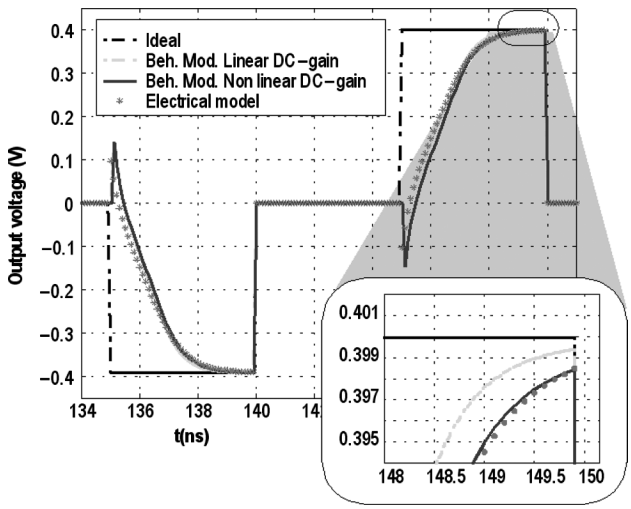

Fig. 6. Same as Fig. 3, but using the proposed behavioral model instead of small-signal simulations.

taking into account noise $(\overline{v}_n^2)$ and speed (α) requirements, whatever more restrictive. Next, the transconductance of the second stage (g_{m2}) is calculated from the calculated transconductance ratio R. With these data, together with the previously planned overdrive voltages, the sizes, the currents and the bias voltages of the OTA MOS transistors can be calculated using technology parameters. In our routine such parameters are extracted from look-up tables obtained from batches of electrical-level simulations. At this point, the overall power

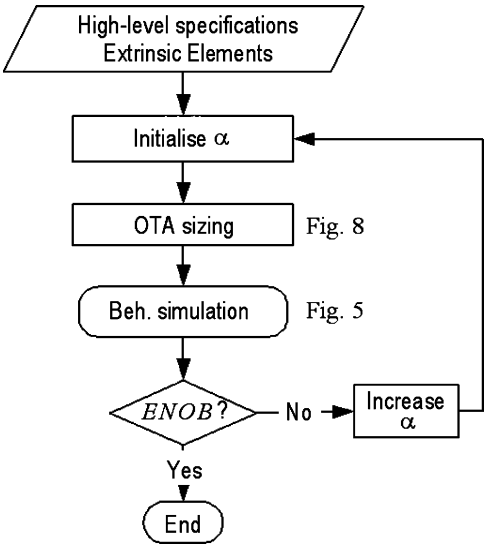

Fig. 7. Main flow diagram of the synthesis procedure.

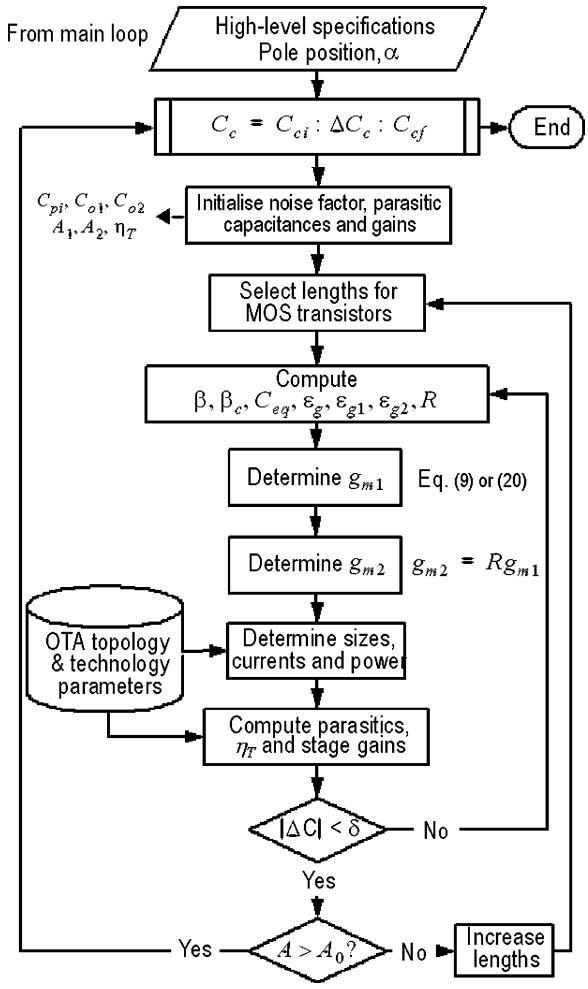

Fig. 8. OTA sizing procedure.

consumption of the OTA can be estimated. In the following step, parasitic capacitances are newly calculated and compared with those previously stored. If discrepancies are higher than a user-defined tolerance value, δ, the iterative process is repeated again until convergence is reached. Finally, if the estimated dc gain $(A = A_1A_2)$ is lower than the required one (A_o), the lengths of MOS transistors are increased and the algorithm is repeated again. It is worth mentioning that despite the iterative nature of the design procedure, it only takes three or four iterations to converge. Also, it is interesting to observe that no *ad hoc* fitting parameter needs to be adjusted in the design procedure.

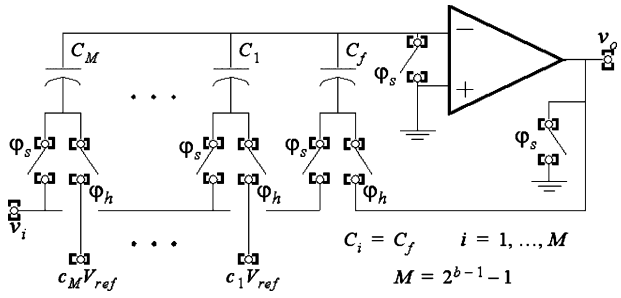

Fig. 9. b-b MDAC SC circuit.

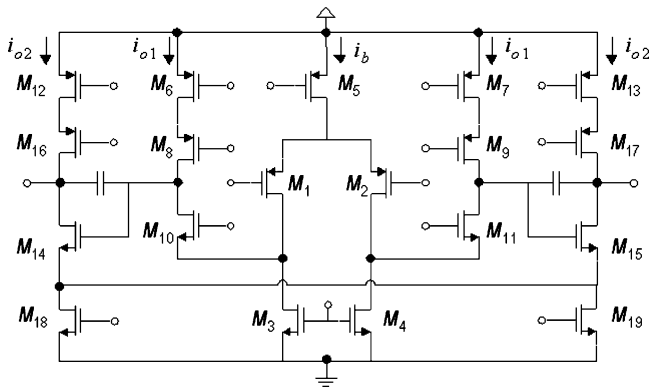

Fig. 10. Selected OTA topology.

V. Examples and Applications

This section illustrates the design of MC-OTAs embedded in SC circuits using the proposed synthesis procedure. In order to demonstrate the efficiency and flexibility of the approach, different technologies and design scenarios are considered. Such scenarios, summarized in Table III, differ on the OTA topology, the SC block which makes use of the amplifier, and the design objectives. The SC block in the scenarios A and B is the flip-around S/H amplifier of Fig. 2, whereas that in the scenario C is the 3-b multiplying digital-to-analog converter (MDAC) circuit shown in Fig. 9. Both SC configurations are commonly used in pipeline analog-to-digital converters (ADCs) [4].

Regarding the OTA topologies, we have considered a fully differential two-stage structure composed by a p-input folded-cascode first stage and a differential n-type class-A amplifier second stage. The schematic is shown in Fig. 10. The only difference between the OTA considered in scenario A, on the one hand, and those used in scenarios B and C, on the other hand, is that the former uses p-type cascoded current sources in the second stage, whereas simple current sources are used in the latter, i.e., cascode transistors M_{16} and M_{17} in Fig. 10 are simply replaced by short circuits.

TABLE IV
SIZING RESULTS FOR 130-nm TECHNOLOGY

	SCENARIO A		SCENARIO B		SCENARIO C	
Parameters	Estimated	Electrical	Estimated	Electrical	Estimated	Electrical
$W_{1,2}/L_{1,2}$ (μm/μm)	25/0.3	25/0.3	59/0.3	56/0.3	25/0.3	26/0.3
$W_{3,4}/L_{3,4}$ (μm/μm)	23/0.4	21/0.4	55/0.4	53/0.4	24/0.4	20/0.4
W_5/L_5 (μm/μm)	72/0.4	78/0.4	167/0.4	178/0.4	72/0.4	72/0.4
$W_{6,7}/L_{6,7}$ (μm/μm)	83/0.4	85/0.4	201/0.4	240/0.4	86/0.4	86/0.4
$W_{8,9}/L_{8,9}$ (μm/μm)	83/0.4	85/0.4	201/0.4	240/0.4	86/0.4	86/0.4
$W_{10,11}/L_{10,11}$ (μm/μm)	16/0.4	16/0.4	39/0.4	45/0.4	17/0.4	17/0.4
$W_{12,13}/L_{12,13}$ (μm/μm)	506/0.4	530/0.4	1176/0.4	1250/0.4	282/0.4	285/0.4
$W_{14,15}/L_{14,15}$ (μm/μm)	96/0.4	96/0.4	226/0.4	200/0.4	54/0.4	50/0.4
$W_{16,17}/L_{16,17}$ (μm/μm)	506/0.4	530/0.4	-	-	-	-
W_{18}/L_{18} (μm/μm)	191/0.4	190/0.4	451/0.4	430/0.4	108/0.4	108/0.4
$C_{pi} \mid C_{o1} \mid C_{o2}$ (pF)	0.06 | 0.55 | 0.43	0.06 | 0.54 | 0.47	0.15 | 1.1 | 0.8	0.13 | 0.97 | 0.78	0.06 | 0.4 | 0.31	0.06 | 0.37 | 0.30
$\beta \mid \beta_c$	0.980 | 0.655	0.981 | 0.662	0.953 | 0.568	0.958 | 0.600	0.226 | 0.385	0.228 | 0.405
$C_t \mid C_{eq}$(pF)	1.53 | 3.04	1.57 | 3.05	1.90 | 4.92	1.88 | 4.49	0.61 | 10.04	0.60 | 9.35
$A_o \mid A_{o1} \mid A_{o2}$	2890 | 98.9 | 29.2	2711 | 92.6 | 29.3	2588 | 126.1 | 20.5	2750 | 130 | 21.2	2588 | 126.2 | 20.5	2918 | 137.1 | 21.3
Output swing | Overdrive voltage(V)	≥±0.25 | 0.15	0.27/-0.26 | 0.15	≥±0.25 | 0.125	0.38/-0.35 | 0.125	≥±0.25 | 0.125	0.37/-0.35 | 0.125
$g_{m1} \mid g_{m2}$ (mA/V)	1.22 | 14.25	1.29 | 14.71	2.23 | 26.70	2.31 | 26.91	0.96 | 6.41	0.99 | 6.60
$i_b \mid i_{o1} \mid i_{o2}$ (mA)	0.21 | 0.24 | 1.5	0.22 | 0.24 | 1.53	0.32 | 0.39 | 2.27	0.33 | 0.42 | 2.48	0.14 | 0.17 | 0.55	0.14 | 0.18 | 0.54
Compensation capacitor (C_c) (pF)	1.05	1.05	1.45	1.45	0.25	0.25
Equivalent input noise (nV/√Hz)	10.50	10.27	7.92	7.8	12.11	11.15
Product Gain-Bandwidth (MHz)	175	160	225	209	518	477
Phase Margin (degrees)	66	66.5	62.6	62	14.9	14.4
ENOB (bits)	**8.1**	**7.86**	**12.1**	**11.97**	**10.1**	**9.78**
Power consumption (mW)	**4.44**	**4.51**	**6.77**	**7.37**	**1.87**	**2.00**

The three design scenarios listed in Table III have been implemented in a 130-nm technology and in a 90-nm technology, assuming critically damped performance. Results are shown in Tables IV and V, respectively. For each scenario, sizing results and performance metrics calculated with the proposed design procedure and obtained from electrical-level simulations are respectively shown.[4] In this latter case, the transistor dimensions have been fine tuned to guarantee that pMOS and nMOS transistors carry the same currents through the amplifier branches. This is so done to nullify systematic offset errors. As can be seen, sizing deviations rarely exceed 10%. Tables IV and V demonstrate that there is an excellent agreement between the performance metrics obtained using our approach and those obtained by electrical simulations. Indeed, deviations from the target resolution requirements remain below 0.3 b equivalent in all cases. This agreement is further illustrated in Fig. 11 which compares the output spectrum of the circuit in Fig. 9 (scenario C in 90-nm technology) obtained through behavioral simulations, on the one hand, and through electrical-level simulations, on the other. It is seen that low-order harmonics are accurately predicted by the proposed tool.

Besides accuracy, another important feature of the design procedure is the reduced computational cost. The synthesis of each design in Tables IV and V takes about 2 s of CPU time, using a 1.8-GHz Intel Centrino processor. This kind of short computation time renders the proposed design procedure suitable to explore the design space, as the paragraphs below will illustrate.

As an example of design space exploration, Fig. 12 shows the evolution of the power consumption of the OTA in Fig. 9 (scenario C in 130-nm technology) in terms of the pole frequency α, and the compensation capacitor C_c. As noted in Section IV, they are the running variables of the main (Fig. 7) and inner (Fig. 8) loops of the synthesis routine, respectively. The plot assumes that the equivalent input noise of the OTA is lower than $13\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. As can be seen, for a given dynamic resolution, determined by parameter α, there is a compensation capacitance which obtains the minimum power consumption. As parameter α sweeps from 1.5 to 3.0 GHz, these optimum power dissipation values form a continuously increasing 3-D curve which can be interpreted as the *Pareto-optimal front* of the OTA in this particular scenario [7]. Note that as the speed requirement increases the valley which surrounds the Pareto front becomes steeper. This is due to the increasing impact of parasitic capacitances on the system dynamics as poles move to higher frequencies.

To further illustrate the capabilities of the procedures for design space exploration, Fig. 13 shows how the optimized power consumption of the OTA evolves when the sampling C_i and feedback C_f capacitances of the SC circuit are jointly varied. Fig. 13 assumes scenario C in 130-nm technology and a clock frequency of 200 MHz. As can be seen, the power consumption does not continuously decrease by reducing these capacitances, as might be intuitively expected, but achieves a minimum value at $C_i = C_f \approx 0.2$ pF. Below this value, parasitic capacitances are dominant, the feedback factor, β, is smaller, and the equivalent load, C_{eq}, increases according to (2). Above the optimum value, parasitic capacitances have a lower impact on the equivalent load, which is now dominated by C_i and C_f.

Prior to concluding this section, we would like to emphasize that, although the SC blocks in Tables IV and V have been sized for a damping factor $\zeta = 1$, other ζ values can be considered as well. An *a priori* plausible choice could be, for instance, to slightly reduce the damping factor to some value between 0.7 and 1.0 in order to speed up the dynamic response of the second-order system [15]. However, the critically damped case

[4]In theses tables, the impact of thermal noise on ENOB has been suppressed to better appreciate the accuracy of the proposed settling-time modeling.

TABLE V
SIZING RESULTS FOR 90-nm TECHNOLOGY

Parameters	SCENARIO A		SCENARIO B		SCENARIO C	
	Estimated	Electrical	Estimated	Electrical	Estimated	Electrical
$W_{1,2}/L_{1,2}$ (μm/μm)	18/0.3	18/0.3	49/0.3	45/0.3	24/0.3	24/0.3
$W_{3,4}/L_{3,4}$ (μm/μm)	12/0.4	12/0.4	35/0.4	33/0.4	17/0.4	17/0.4
W_5/L_5 (μm/μm)	49/0.4	49/0.4	136/0.4	130/0.4	66/0.4	66/0.4
$W_{6,7}/L_{6,7}$ (μm/μm)	56/0.4	56/0.4	163/0.4	170/0.4	79/0.4	79/0.4
$W_{8,9}/L_{8,9}$ (μm/μm)	56/0.4	56/0.4	163/0.4	170/0.4	79/0.4	79/0.4
$W_{10,11}/L_{10,11}$ (μm/μm)	8/0.4	10/0.4	25/0.4	25/0.4	12/0.4	12/0.4
$W_{12,13}/L_{12,13}$ (μm/μm)	392/0.4	392/0.4	868/0.4	820/0.4	228/0.4	215/0.4
$W_{14,15}/L_{14,15}$ (μm/μm)	57/0.4	57/0.4	130/0.4	118/0.4	35/0.4	35/0.4
$W_{16,17}/L_{16,17}$ (μm/μm)	392/0.4	392/0.4	-	-	-	-
W_{18}/L_{18} (μm/μm)	113/0.4	120/0.4	260/0.4	245/0.4	69/0.4	65/0.4
$C_{pi} \mid C_{o1} \mid C_{o2}$ (pF)	0.05 | 0.39 | 0.29	0.04 | 0.39 | 0.30	0.12 | 0.73 | 0.46	0.10 | 0.64 | 0.42	0.06 | 0.31 | 0.23	0.05 | 0.30 | 0.22
$\beta \mid \beta_c$	0.985 |0.683	0.986 | 0.685	0.961 | 0.642	0.968 | 0.672	0.227 | 0.442	0.230 | 0.452
$C_t \mid C_{eq}$(pF)	1.39 | 2.53	1.40 | 2.53	1.56 | 3.48	1.52 | 3.14	0.53 | 7.82	0.523 | 7.46
$A_o \mid A_{o1} \mid A_{o2}$	3967 | 135.2 | 29.3	3652 | 125.8 | 29	2603 | 135.4 | 19.2	2788 | 134.5 | 20.7	2606 | 135.4 | 19.3	3200 | 151 | 21.2
Output swing | Overdrive voltage(V)	≥±0.25 | 0.15	0.25/-0.25 | 0.15	≥±0.25 | 0.125	0.32/-0.38 | 0.125	≥±0.25 | 0.125	0.32/-0.37 | 0.125
$g_{m1} \mid g_{m2}$ (mA/V)	0.91 | 11.06	0.94 | 11.42	1.94 | 19.45	1.92 | 19.43	0.94 | 5.10	0.988 | 5.293
$i_b \mid i_{o1} \mid i_{o2}$ (mA)	0.16 | 0.19 | 1.32	0.17 | 0.19 | 1.36	0.30 | 0.36 | 1.94	0.30 | 0.39 | 2.05	0.15 | 0.17 | 0.51	0.16 | 0.18 | 0.54
Compensation capacitor (C_c) (pF)	0.85	0.85	1.3	1.3	0.25	0.25
Equivalent input noise (nV/√Hz)	11.85	12.5	8.32	9.4	11.99	12.7
Product Gain-Bandwidth (MHz)	162	155	219	202	513	494
Phase Margin (degrees)	67.1	66.4	64.6	63.7	15.5	14.6
ENOB (bits)	**8.05**	**7.72**	**12.18**	**12.28**	**10.11**	**10.20**
Power consumption (mW)	**3.82**	**3.82**	**5.88**	**6.21**	**1.81**	**1.91**

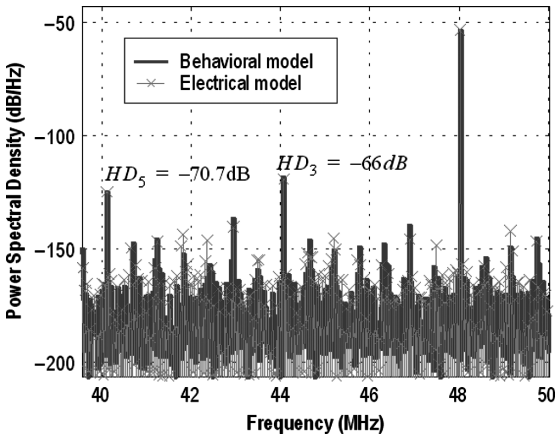

Fig. 11. Output spectrum of the circuit in Fig. 9 for scenario C in the 90-nm technology.

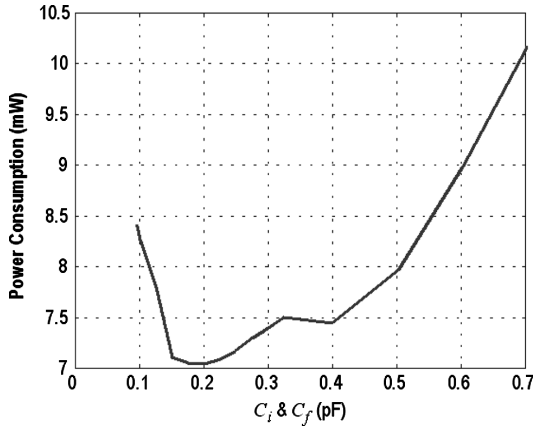

Fig. 13. Power consumption against sampling and feedback capacitances.

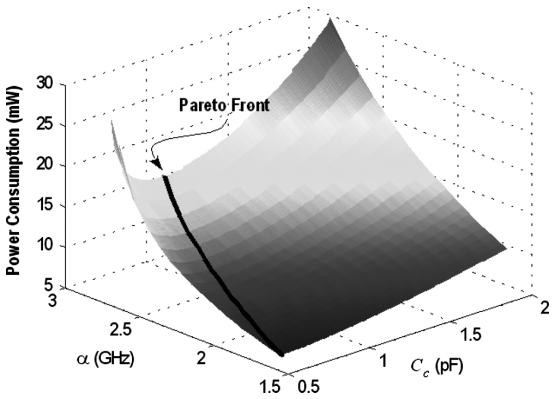

Fig. 12. 3-D view of the optimization procedure.

(even the over-damped one) could be potentially useful to make the design compliant with technology corner variations. To illustrate this point, let us consider again the designs of Tables IV and V (derived under typical operation conditions) and the corners listed in Table VI.

TABLE VI
CORNERS DEFINITION

	Typical	Fast	Slow	Worst ONE	Worst ZERO
MOS models	Typ	Fast *n* Fast *p*	Slow *n* Slow *p*	Fast *n* Slow *p*	Slow *n* Fast *p*
Temperature	27	-40	85	85	85
Cap. models	Typ	Min	Max	Typ	Typ
Volt. supply	1.2	1.2	1.2	1.2	1.2

The data in Table VII collect the values obtained for ENOB at such corners. Each ENOB entry in Table VII includes two numerical data linked by an arrow. They correspond to the two different values of the compensation capacitor shown at the third column of the table. Transistor sizes and biasing conditions of corresponding designs remain as indicated in Tables IV and V. For each duplet, the data at the left corresponds to the original

TABLE VII
ENOB AT THE TECHNOLOGICAL CORNERS BEFORE AND AFTER ADJUSTING THE COMPENSATION CAPACITANCE

Technology	Scenario	Compesation capacitor	*ENOB*				
			Typical	Fast	Slow	Worst ONE	Worst ZERO
130nm	A	1.05 → 0.79	7.86 → 12.42	8.26 → 13.31	7.02 → 10.56	6.18 → 7.95	7.96 → 10.74
	B	1.45 → 1.34	11.97 → 13.01	13.32 → 14.24	10.37 → 11.82	9.80 → 11.74	12.64 → 11.50
	C	0.25 → 0.22	9.78 → 10.86	10.52 → 11.94	8.79 → 9.95	8.51 → 10.01	9.96 → 9.92
90nm	A	0.85 → 0.55	7.72 → 11.17	7.53 → 12.86	7.13 → 9.17	5.59 → 7.96	8.30 → 9.93
	B	1.3 → 0.975	12.28 → 13.22	12.76 → 13.29	11.08 → 11.80	9.34 → 12.22	12.06 → 11.94
	C	0.25 → 0.215	10.20 → 11.96	10.47 → 12.97	9.47 → 10.08	8.47 → 10.49	11.65 → 10.07

value of the compensation capacitor obtained from the synthesis procedure. Note that ENOB requirements (see Table III) are not satisfied in the "Slow" and "Worst ONE" corners. The reason is that the corresponding systems become strongly over-damped. This situation can be corrected by reducing the system damping factor; i.e., by decreasing the value of the compensation capacitance, as indicated at the third column of Table VII. Thus, the system becomes underdamped and the ENOB values at the right of the duplets are obtained. It is now observed that the required resolution is nearly satisfied in all the corners. If this does not suffice, the above heuristic approach could be complemented by slightly increasing the original ENOB requirements. Alternatively, the design before adjustment could focus in one of the worst corners to guarantee that all the rest meet the specifications.

VI. CONCLUSION

A design procedure for sizing arbitrary topologies of two-stage Miller-compensated OTAs embedded in generic SC blocks has been presented. It is based on a detailed study of the closed-loop transient response and an accurate behavioral modeling. The methodology directly maps SC block specifications onto transistor sizes and biasing conditions and identify the optimum open-loop specifications of the OTA to meet such specifications. The procedure has been implemented in a fully functional MATLAB routine which is herein demonstrated with the design of different OTAs in several scenarios. In all cases, close agreement between behavioral and electrical-level simulation results is obtained. Besides, the high computational efficiency makes the procedure suitable for design space exploration and contributes to speed the design cycles from specifications to physical circuits.

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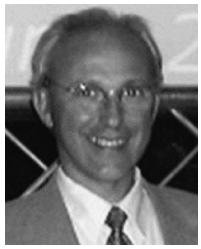

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Dr. Rodríguez-Vázquez has served as Editor, Associate Editor and Guest Editor for different IEEE and non-IEEE journals and as chairman for different international conferences and is on the committee of some international journals and conferences. He has received a number of international awards for his research work (including the IEEE Guillemin–Cauer best paper award) and was elected Fellow of the IEEE for his contributions to the design of chaos-based communication chips and neuro-fuzzy chips.