Current-Mode Building Blocks for CMOS-VLSI Design of Chaotic Neural Networks

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Abstract **-- This paper presents two nonlinear CMOS current-mode circuits that implement neuron soma equations for chaotic neural networks, and another circuit to realize programmable current-mode synapse using CMOS-compatible BJT's. They have been fabricated in a double-metal, single-poly 1.6μm CMOS technology and their measured performance reached the expected function and specifications. The neuron soma circuits use a novel, highly accurate CMOS circuit strategy to realize piecewise-linear characteristics in current-mode domain. Their prototypes obtain reduced area and low voltage power supply (down to 3v) with clock frequency of 500kHz. As regard to the synapse circuit, it obtains large linearity and continuous, linear, weight adjustment by explotation of the exponential-law operation of CMOS-BJT's. The full accordance observed between theory and measurements supports the development of future analog VLSI chaotic neural networks to emulate biological systems and advanced computation.**

I. Introduction

Most artificial neural networks use a simple neuron model where the processing realized by the soma involves a static nonlinear transformation, with either sigmoid or threshold characteristics [1]. However, recent studies on real nerve membranes in neurophysiological experiments have shown that the dynamic behavior of biological neurons is much more complex (including chaotic response) than that exhibited by simple models [2], [3]. Consequently new schemes of artificial neural networks have emerged to more realistically emulate the chaotic responses experimentally observed in biological systems. In particular, some remarkable chaotic neuron models have been reported by Nagumo and Sato [4]; and Aihara, Takabe and Toyoda [5].

Many studies on chaotic neural networks in general, and using the previous models in particular, reveal that such networks serve not only as an experimental vehicle in the study of sensory nerve systems, but also lead to important engineering applications. In this sense, chaotic neural networks have been proposed to solve difficult *optimization* problems [6], [7]; for *dynamical associative pattern classification* [8]; and for *signal detection* and *classification* in *noisy environments* [9], and it is predictable that new applications will arise in the near future.

In spite of the strong economical interest involving these applications, few up-to-date physical implementations of chaotic neural networks have been proposed. Thus, it is advisable to give circuit realizations of these models. Furthermore, due to the technological trend towards system integration, these circuits must be well-suited for VLSI, and, if possible, compatible with standard low cost CMOS technologies.

The purpose of this communication is to report some circuit building blocks for CMOS-VLSI design of chaotic neural networks using analog current-mode techniques. Neuron soma and synapse circuits are proposed and validated using silicon prototypes in a single-poly double-metal 1.6μm CMOS technology. In particular, Nagumo-Sato's and Aihara-Takabe-Toyoda's chaotic neuron models, and a synapse circuit with continuous, linear, programmability which employs CMOS-compatible BJT's. Proposed circuits use innovative current-mode techniques and operate correctly for bias voltage down to 3v.

II. Neuron Models

Fig. 1 is a block diagram for an artificial neuron, where we can distinguish a *dendritic/synaptic* structure and a *soma*. The dendritic structure collects input signals (represented by vector **I**) and signals from other neurons (vector **y**), so that the input strength is given by,

$$A_i(n) = \sum_{j=1}^{M} W_{ij} y_j(n) + \sum_{j=1}^{N} V_{ij} I_j(n) - \theta_i \qquad (1)$$

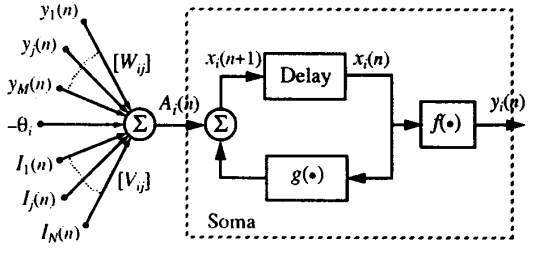

Fig. 1. Analog computer concept for the chaotic neuron circuit. The nonlinear block is given by $g(x) = kx - \alpha f(x)$, according to (1).

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where the first term computes the influence of the M neurons driving the ith neuron; the second, the excitation from the N external inputs, I_j; and θ_i is the threshold of the ith neuron. For convenience, in Fig. 1 and (1) we have assumed that signals are discrete time, with time index represented by n.

In a conventional artificial neuron, processing performed at the soma is a simple nonlinear transformation,

$$\begin{aligned} x_i(n+1) &= f(x_i(n)) + A_i(n) \\ y_i(n+1) &= f(x_i(n+1)) \end{aligned} \qquad ,n = 0, 1, \ldots \qquad (2)$$

where $x_i(n+1)$ and $y_i(n+1)$ are the internal state and the output of the ith chaotic neuron at the discrete time $n+1$, respectively; and $f(\bullet)$ is a threshold function.

In Nagumo-Sato's model that processing also involves dynamic operators,

$$\begin{aligned} x_i(n+1) &= kx_i(n) - \alpha u(x_i(n)) + A_i(n) \\ y_i(n+1) &= u(x_i(n+1)) \end{aligned} \qquad ,n = 0, 1, \ldots (3)$$

where α and k are the scaling and damping factors of refractoriness (residual effect of a neuron once fired), respectively; and $u(\bullet)$ is a unit-step function. Numerical studies realized with this model show that chaotic responses occur only for a set of parameters with zero measure.

To extend the range of parameters for which chaotic behavior can be observed, the *chaotic neural network* reported in [4] constitutes a modification of the Nagumo-Sato's model [5], where instead of following an all-or-none law for the action potential, modelled by an unit step output function $u(\bullet)$, the neuron shows a continuously graded stimulus-response curve, represented by a non-linear function $f(\bullet)$ The model in [4] is defined by the following finite-difference equations:

$$\begin{aligned} x_i(n+1) &= kx_i(n) - \alpha f(x_i(n)) + A_i(n) \\ y_i(n+1) &= f(x_i(n+1)) \end{aligned} \qquad ,n = 0, 1, \ldots (4)$$

where $f(\bullet)$ constitutes the neuron output function and can be represented by the piecewise-linear model,

$$f(x) = \frac{|x+\varepsilon| - |x-\varepsilon|}{2\varepsilon} \qquad (5)$$

where ε is a positive number defining the steepness of the function.

III. Current Mode Implementations

Current-mode techniques have been employed to implement (3) and (4), following the conceptual diagram shown in Fig.1. Summation is easily realized exploiting KCL. The delay operation can be realized as a cascade of two track-and-hold switched-current stages, as proposed by Hughes et al. [9]. Fig. 2 shows the schematics for this block.

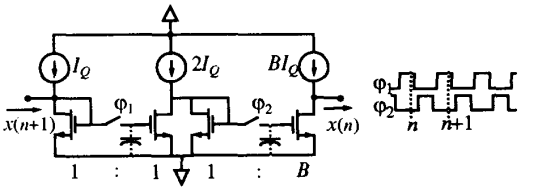
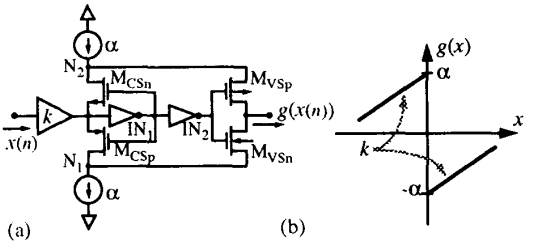


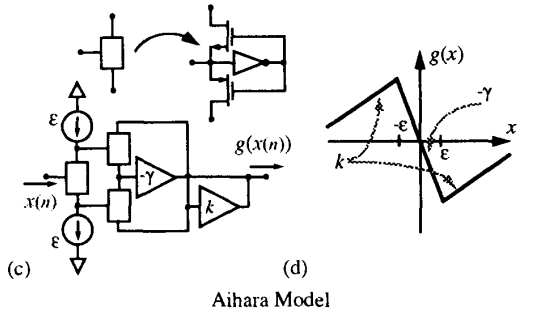
Fig. 2. Current-mode track and hold circuit.

Nonlinearities have been achieved using a novel, highly accurate CMOS circuit strategy to realize piecewise-linear (PL) characteristics in current-mode domain. It is based on the rectifying characteristics of the current switch [10], which provide very high resolution and virtually zero current offset, uninfluenced by transistor mismatches (in fact, minimum size transistors were used in both prototypes). Fig. 3 shows the corresponding schematics for both PL functions. Current amplifiers can be implemented by properly ratioed bilateral current mirrors, whose programmability will be adressed in the next section.

First, let us consider implementation of the nonlinear block, $g(\bullet)$, for the Nagumo-Sato model according to the concept of Fig.1. Fig.3(a), which consists of two current



Nagumo-Sato Model



Aihara Model

Fig. 3. Piecewise linear mapping circuits for the neurons.

sources (realized in practice by current mirror output branches), four transistors, and two digital inverters, shows a conceptual schematic for the realization of the PL characteristics of Fig.3(b). Transistors M_{CSn} and M_{CSp} in Fig.3(a) operate as a current-controlled-current-switch, while transistors M_{VSn} and M_{VSp} operate as voltage-controlled current switches. Any positive input current increases the input voltage, turning the M_{CSp} device ON, and since both devices in the current switch have the same gate voltage, M_{CSn} OFF. Simultaneously, the voltage at the second inverter output evolves to the high logic state, turning M_{VSn} ON and M_{VSp} OFF. Thus, a current $kx(n) - \alpha$ (obtained by KCL at node N_1) is directed to the output node through the transistor M_{VSn} -- the right-hand piece of Fig.3(b) is implemented in this manner. Similarly, negative input currents turn M_{CSn} and M_{VSp} ON, so that a current $kx(n) + \alpha$ circulates through M_{VSp} to the output node. The output response of the neuron can be taken from the voltage at the output of the inverter IN_2 which swings from rail to rail depending on the sign of the input current, thus resembling the required unit step function in voltage mode. Obviously, this binary signal must be combined with analog switches and current sources to properly drive other neurons in the network.

Since current discrimination in the proposed circuit relies on the integration function performed at the input node, resolution is very high, uninfluenced by transistor mismatches (measurements from the CMOS prototype display resolution of 12pA's). Operation speed is also very high, limited mainly by nonlinear transients in the transistors that implement the current sources used to drive nodes N_1 and N_2. Also, the feedback created by inverter IN_1 yields significant reduction of the dead-zone exhibited by the driving point characteristics measured at the input node, that is proportional to $(V_{Tn} + |V_{Tp}|)/ A_{inv}$, where V_{Tn} and V_{Tp} are the threshold voltages for the transistors and A_{inv} is the inverter DC gain. This is an appealing feature that enables reducing the interstage loading errors caused by finite equivalent MOS transistors Early voltages.

Fig. 3(c) shows the corresponding schematic to implement the PL characteristic shown in Fig. 3(d) for the Aihara model, . The current switches, together with the current sources, are used to discriminate the input current into three paths depending on whether $x(n)$ is lower than $-\varepsilon$, greater than ε, or comprised between both values. In the two first cases, the paths are routed to the same node and amplified by k, while if $x(n) \in [-\varepsilon, \varepsilon]$ the current is amplified by $-\gamma$, where $\gamma = \alpha/\varepsilon - k$, according to (1) and (3). In this case, the output of the neuron can be easily taken by replication and scaling the output current of the amplifier with gain $-\gamma$.

IV. Current Mode Synapse and Dendritic Structure

The synaptic structure in Fig.1 involves the operation of analog-weighted summation. Summation is easily performed in current-mode domain by KCL. Digital programmability can be incorporated by analog multiplexing of current contributions from different mirrors. These mirrors can either implement fixed weights (with application, for instance, in cases where well-defined tasks must be sequentially performed), or be binary-weighted (for more general application). Digital programmability provides ease of controllability and accurate results, at the cost of a strong area penalty.

Analog programmability should be considered for reduced area and continuous weight adjustment. A simple way to achieve analog programmability is to use tunable transconductors, like that shown in Fig. 4(a). Fig. 4(b) shows a programmable current mirror using this transconductor. Two different situations arise depending on whether transistors operate in weak or strong inversion. Analysis for both operating conditions shows the following,

$$\left.\frac{i_o}{i_{in}}\right|_{strong} = \sqrt{\frac{\beta_2 I_{B2}}{\beta_1 I_{B1}}} \qquad \left.\frac{i_o}{i_{in}}\right|_{weak} = \frac{I_{B2}}{I_{B1}} \quad (6)$$

As can be seen, the dependence is linear for weak inversion; hence, this latter case provides larger weight adjustment ranges. It is illustrated in Fig. 5, showing the current weight as a function of I_{B2}/I_B for different values of I_{B1}/I_B, where I_B is a normalization factor of 10nA for weak inversion (Fig. 5(a)) and 50μA for strong inversion (Fig. 5(b)). Also, nonlinearity cancellation is exact in weak inversion due to the exponential nature of current

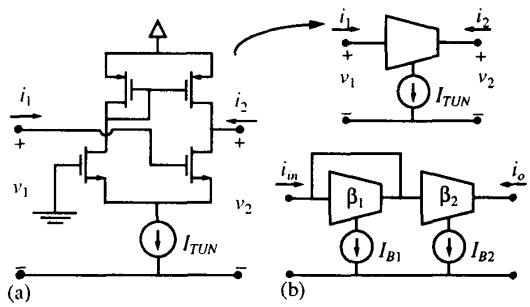
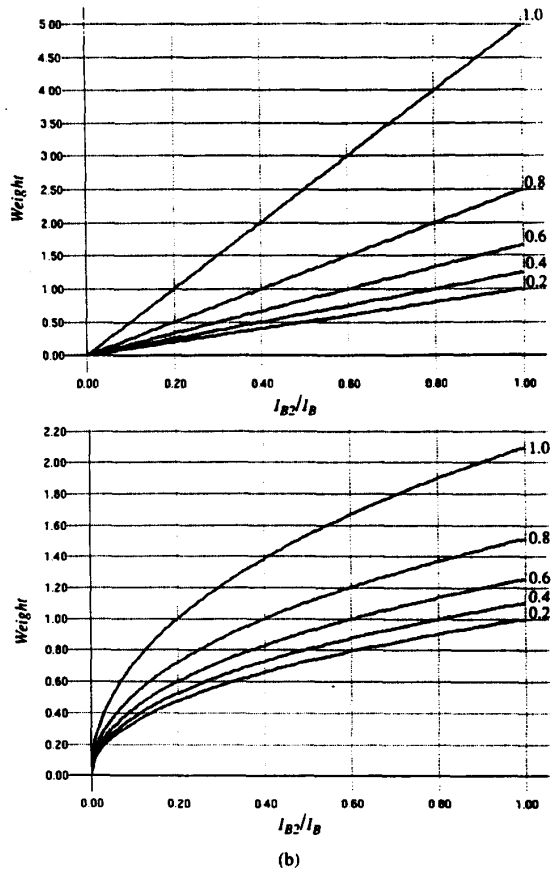


Fig. 4. (a)Tunable transconductor. (b) Programmable current mirror.

to voltage characteristics, while it is only approximate for strong inversion: nonlinearity in the weak inversion case is less than 1% up to $i_o=I_{B2}$, while the corresponding value for strong inversion is $i_o=0.13I_{B2}$. Drawbacks of weak inversion are low accuracy, due to mismatch, and reduced speed. This paper overcomes this drawback using CMOS compatible lateral BJTs, which exhibit exponential feature for larger current ranges, and have excellent matching properties [11].

V. Experimental Results

Both neurons have been fabricated in a double-metal, single-poly 1.6μm CMOS technology. Fig. 6 shows the corresponding microphotographs. Some extra miscellaneous circuitry has been added to both circuits to enable testing the output current and the ability to either open or close the feedback loop. Dummy switches were also added to reduce the influence of clock feedthrough. All



(b)

Fig. 5. Weight (i_o/i_{in}) variation with I_{B2}/I_B for different values of I_{B1}/I_B in Fig. 4(b). (a) Transconductors operating in weak inversion, I_B = 10nA.(b) Transconductors operating in strong inversion, I_B = 50μA.

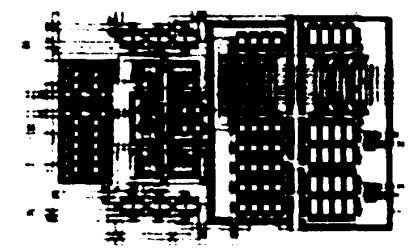
current amplifiers were binary-weighted for the issue of programmability. Bias current I_Q for the delay stages was set to 50μA. Total area occupation is 0.096mm^2 for the Nagumo-Sato neuron, and 0.225mm^2 for the Aihara neuron.

Fig. 7 shows the characteristics measured in open loop for both circuits, using the HP4145 semiconductor analyzer, with a rail-to rail power supply of only 3v. For the Nagumo-Sato neuron (Fig. 7(a)), α = 20μA, k = 1, and the input ranges from −20μA to 20μA. For the Aihara neuron (Fig. 7(b)), ε = 2μA, γ = 10 , k = 1, and the input sweeps from −10μA to 10μA. In both prototypes deviation from linearity is less than 0.2%, and the measured current offset amounts to few pA's.

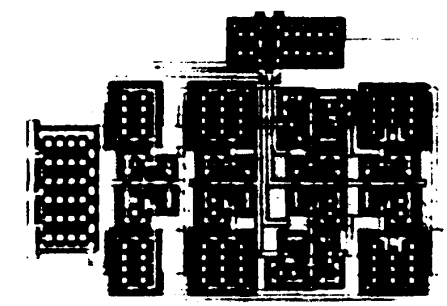
Fig. 8 shows the experimental bifurcation trees for both neurons, where the damping factor k = 0.5 and the neuron excitation A, taken as the bifurcation parameter, varies from −20μA to 20μA. All other parameters were fixed to the values previously cited. Clock frequency was set to 500kHz.

Fig. 9 shows the schematics of a tunable transconductor using CMOS-BJTs for a n-well technology. We have fabricated a programmable current mirror using this transconductor in a 1.6μm technology and have obtained continuous weight variation in four decades range with very low current off set (nA's level).

All these measurements are in full accordance with the theoretical results. Also, given the reduced area, as well as operating with only 3v power supply, we believe

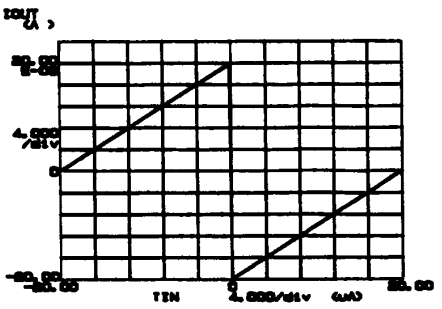


(a) Nagumo-Sato Model

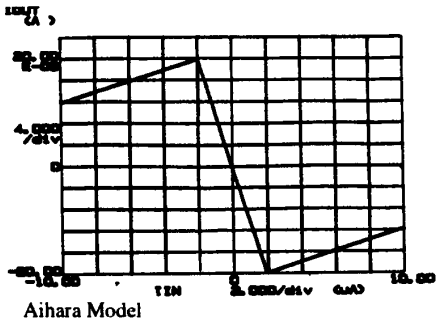


(b) Aihara Model

Fig. 6. Microphotographs of the prototypes.



(a) Nagumo-Sato Model



(b) Aihara Model

Fig. 7. Measured open-loop characteristics.

both neuron implementations are very appropriate for high density chaotic neural networks on a single chip.

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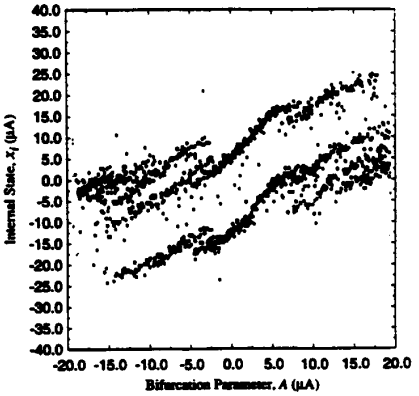
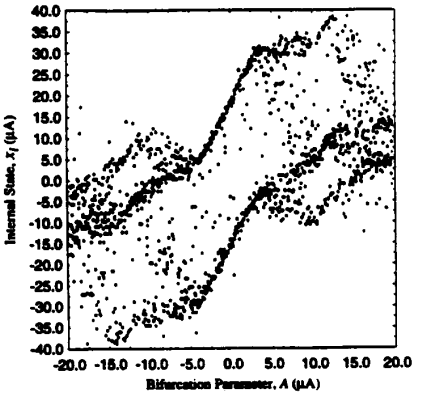


(a) Nagumo-Sato Model



(b) Aihara Model

Fig. 8. Bifurcation diagrams.

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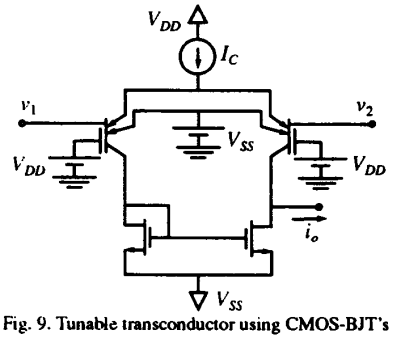

Fig. 9. Tunable transconductor using CMOS-BJT's