Current-Mode Piecewise-Linear Function Generators

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Abstract - We present a systematic design technique for current-mode piecewise-linear (PWL) function generators. It uses two building blocks: a high-resolution current rectifier, and a programmable current amplifier. We show how to arrange these blocks to obtain basic non-linearities from which generic characteristics are built through aggregations. Measurements from a 1.0μm CMOS prototype chip show 10pA resolution in the rectification operation and 0.6% non-linearity errors in the programmable scaling operation for 2μA input current range.

I.Introduction

Function generators realize parametrizable nonlinear functions for given input signal range [1]-[3]. The parameterization may be determined by component ratios (*non-programmable* generators); or through external control signals and electrically-adjustable circuits (*programmable* generators).

Regardless of the programmability issue, the design of electronic function generators encompasses several subproblems (shown conceptually in Fig.1):

- Realization of nonlinear *operators* through the interconnection of primitive components.
- Realization of *elementary functions* as the interconnection of circuit blocks which synthesize nonlinear operators.
- *Approximation* of the target as a combination of elementary functions and its realization as the interconnection of the circuit blocks associated to these functions.

A number of reported solutions to these problems employ *piecewise-linear* (PWL) approximant functions [4]. Their main advantage is simplicity of representation, which eases the calculation of the adjustment parameters. PWL functions are also easily realized at a circuit level. In fact, diverse solution have been proposed parting from different primitive components and assuming distinct physical representations for the electrical variables [5]-[10].

This paper presents a methodology for PWL approximation of arbitrary unidimensional functions (including those with finite jump discontinuities) using current mode techniques. Section II discusses some PWL representation techniques, and present the basic non-linearities involved. Section III presents the building blocks for the basic functions and describes some examples where the global topology of the generator can be simplified by taking advantage of symmetries. Section IV shows experimental results obtained from a chip which has been fabricated in a 1μm standard digital CMOS technology. All the parameters of the circuit are electrically controllable to enable fully programmable operation.

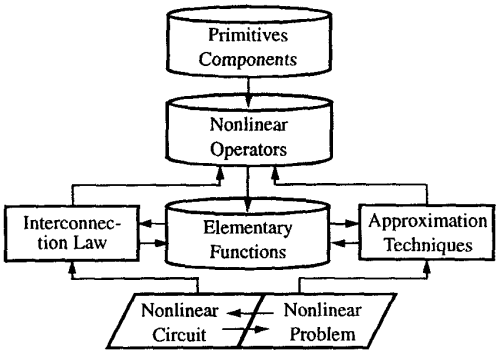

FIGURE 1. Hierarchical decomposition for the synthesis of function generators.

II.Piecewise Linear Representations

Many of the circuit schemes proposed for the implementation of PWL function generators are based on the concept of *extension* operator presented in [9]. Let us consider that the function $y=f(x)$ is defined inside a real interval $[\delta_0, \delta_{N+1}]$ and described by a collection of data measured at the *knots* of a given partition $\Delta = \{\delta_0, \delta_1, \delta_2,...,\delta_N, \delta_{N+1}\}$.

The basic idea behind the concept of an extension operator is to build the approximate function, $g(x)$, following an iterative procedure. At each iteration, the procedure starts from a previous approximation for a subinterval of $f(x)$, and then adds new terms to fit the data associated with the adjacent subintervals. Generally, some pieces are adjusted to the left and others to the right, to yield,

$$g(x) = g^{0}(x) + \sum_{i=1}^{N_+} \Delta^{+} g_i(x) + \sum_{i=-N_-}^{-1} \Delta^{-} g_i(x) \quad (1)$$

where,

$$\Delta^{+} g(x) = w u_{+}(x-\delta) \equiv w(x-\delta)\, sgn(x-\delta)$$

$$\Delta^{-} g(x) = w u_{-}(x-\delta) \equiv w(x-\delta)\, sgn(\delta-x) \quad (2)$$

$$g^{0}(x) = ax + b$$

and $sgn(\bullet)$ denotes the *sign* function. Fig.2(a) shows an example of this procedure.

Based on the extension operator, Chua and Kang have developed a *canonical* representation for unidimensional PWL functions given by [9],

$$g(x) = ax + b + \sum_{i=1}^{N} w_i |x - \delta_i| \quad (3)$$

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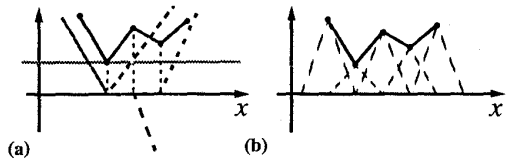

FIGURE 2. Piecewise linear decomposition of a function (a) using the extension operator concept, and (b) using basic linear functions.

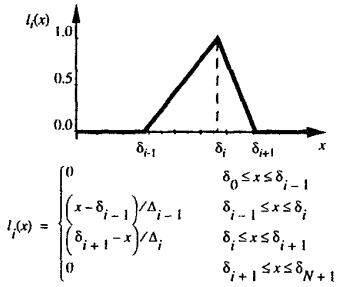

FIGURE 3. Linear basis function (LBF).

which involves only one non-linearity, the *absolute value* function, with the additional advantage that it requires a minimal number of fitting parameters [9].

A different approach for the representation of nonlinear functions is to express the transfer characteristic as a linear combination of *basis* functions, each having compact support over a corresponding subinterval of the partition. In the case of PWL functions, basis functions are called *linear basis functions* (LBF), and lead to the following expression,

$$g(x) = \sum_{i=1}^{N+1} c_i \, l_i(x) \qquad (4)$$

Fig.3 shows the shape of the ith LBF, which equals 1 at δ_i and decreases to 0 at δ_{i-1} and δ_{i+1}.

Fig.2(b) illustrates the representation technique based on LBFs, using the same function $f(x)$ used to describe the extension operator. Note that the LBF representation is more modular than the approximation based on the extension operator. However, this modularity is not for free; their implementation is not the cheapest in terms of components and consequently, may not be optimal for applications in which the target function is fixed. On the contrary, the representation (4) is an excellent option in the design of fully programmable function generators.

III. Current-Mode Linear Basis Functions

The proposed design technique for linear basis functions is based on the interconnection of two basic building blocks: *current switches* and *programmable current amplifiers*.

Current Switch

Fig.4(a) and (b) show respectively the symbol and schematic of the current switch proposed in [10]. This block routes the input current to either the upper or the lower terminal depending on its sign. Besides, it generates a logical signal V_s which codifies the current sign (V_s = '1' for $I_{in} > 0$, and V_s = '0' otherwise).

The circuit exhibits very high resolution (around 10pA), and is insensitive to transistor mismatch. Thus, it can be realized through minimum size devices. Additionally, the feedback loop created by the inverter Inv_1 allows significant reduction of the dead zone non-linearity shown by the input driving-point characteristic, which alleviate loading errors of the circuit with the environment.

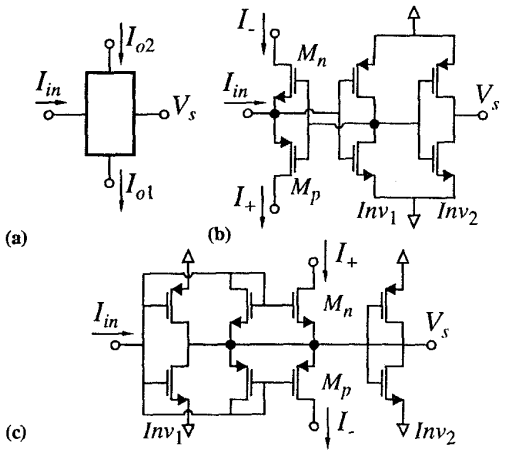

FIGURE 4. (a) Current switch symbol; (b) Proposal in [10]; (c) Alternative design using current mirrors and inverters.

An alternative design for the current switch is shown in Fig.4(c). As opposed to the previous case, positive (negative) currents are now routed to the lower (upper) terminal, as a consequence of the mirrors included in the current path. Simulation results show that the circuit is especially suited for low voltage operation (correct performance has been noted for supply voltages of less than 2 V). The main drawback of this structure is that currents I_+ and I_- are affected by the mismatch of the transistors making up the current mirrors.

Programmable Current Amplifier

Fig.5(a) shows the conceptual block diagram of a programmable current amplifier. It is formed by the series connection of a grounded resistor and a tunable linearized transconductor. The schematics in Fig.5(b) (output stage) and Fig.5(c) (core block) form the complete circuit amplifier. The grounded resistor is realized through a pair of p channel transistors in diode configuration, connected in cascode with the external nodes connected to the rails. As shown in Fig.5(c), the linear I-V conversion is done in the core block. The configuration described in [11] has been chosen for the linearized transconductor, introducing some modifications to increase the gain adjustment range. First, the input PMOS differential pair in [11] has been replaced by a NMOS pair and two p-channel cascode mirrors to increase the variation range of voltages V_1 and V_2. Next, the common-source node of the output differential pair has been connected to a voltage follower of very low output resistance to supply a fairly constant voltage drop, V_F. On one hand, this obtains low current gain values. On the other, gives an increased efficiency for the current flowing through the output stage. Finally a set of analog switches driven by the binary signal V_s has been included in the output pair to determine the sign of the output current.

Using the quadratic law of a MOS transistor in saturation, the gain of the amplifier reads as:

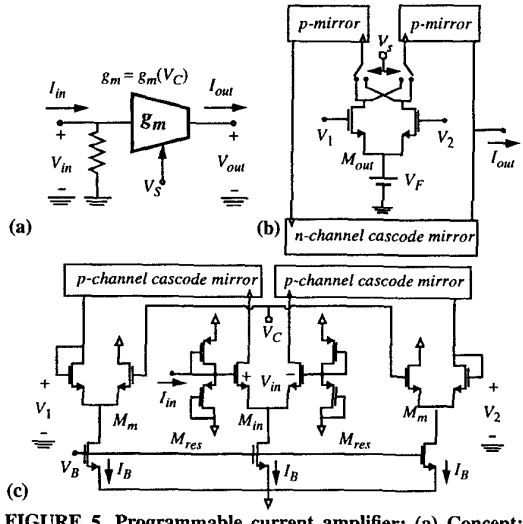

FIGURE 5. Programmable current amplifier: (a) Concept; (b) Amplifier output stage; (c) Core block.

$$A_I = \pm \frac{1}{V_{DD}-|V_{Tp}|}\frac{\beta_{out}}{\beta_{res}}\sqrt{\frac{\beta_m}{\beta_{in}}}\left(V_C - V_F - V_{Tn}\right) \qquad (5)$$

where the sign is defined by the binary signal V_s. As it is seen, the gain depends linearly on the control voltage V_C. Correct performance enforces the following conditions on the electrical variables:

$$|I_{in}| \le 2\beta_{res} min\left\{\left(V_{DD}-|V_{Tp}|\right)\sqrt{\frac{2I_B}{\beta_{in}}}, \left(V_{DD}-|V_{Tp}|\right)^2\right\} \qquad (6)$$

$$V_C \ge V_F + V_{Tn} + \sqrt{\frac{2I_B}{\beta_m}}$$

Current-Mode Basic Functions

Fig.6(a) shows the block diagram for a *LBF* formed by three current switches, two current amplifiers, and four analog switches in the output stage. Note that the central current switch supplies the binary signal that determines the sign of the current amplifiers and the output branch through which I_{out} flows.

The combination of current switches and voltage amplifiers also enables implementing the elementary functions for the other approximation techniques cited in Section II. Thus, Fig.6(b) shows an example of *extension* operator construction and Fig.6(c), the realization of the *absolute value* function.

Fig.6(d) shows the realization of a trapezoidal function, frequently used as a *membership function* in fuzzy logic. Note that instead of using two linear basis function like those in Fig.6(a), the function symmetry enables reducing the number of circuit components. Finally, Fig.6(e) shows an example of construction of functions with finite jump discontinuity, taking advantage of the binary signal generated by the current switches, together with the logic gates.

IV.Experimental Results

Fig.7 presents a microphotograph of the integrated prototype of a programmable linear basis function fabricated in single poly 1.0μm CMOS technology. The current switches used in the design are shown in Fig.4(b). Fig.8(a) shows the transfer characteristics of

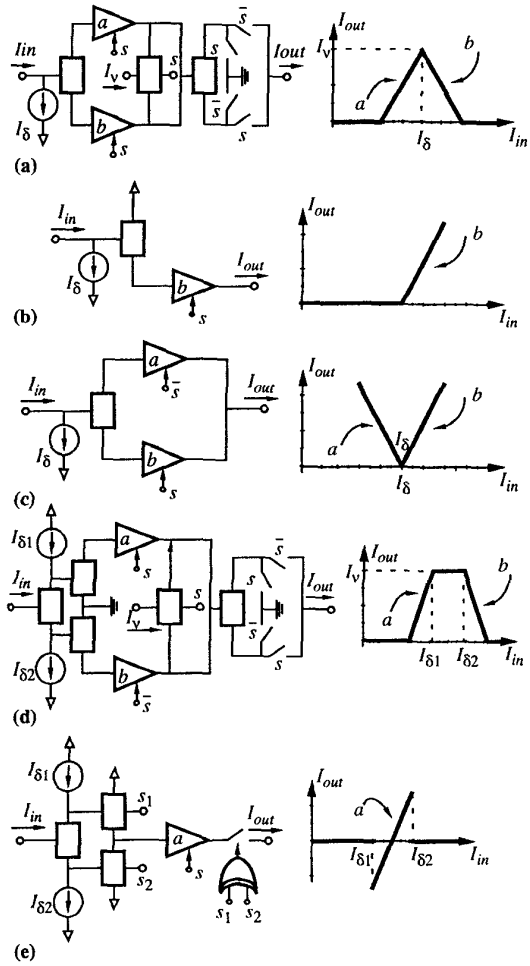

FIGURE 6. Block diagrams of: (a) linear basis function; (b) extension operator; (c) absolute value; (d) trapezoidal function, and (e) discontinuous function.

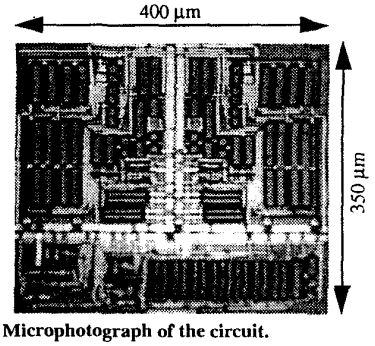

FIGURE 7. Microphotograph of the circuit.

the implemented current amplifier. The amplifier gain ranges from 0 to 25 for input linearity between $\pm 1\mu A m\dot{p}$. This gain variation is given by the control signal adjustment, V_C, whose valid range is between -0.5 V and 1.3 V. Voltage V_F and bias current I_B were set at -1.8 V and15 μAmps, respectively. Fig.8(b) shows the deviations of the linear behavior of the current amplifier for different values of control voltage V_C. The relative error in all cases was less than 0.6%.

Fig.9 shows a group of experimental curves for the transfer function of the whole circuit, obtained through individual variation of each of the Hermite

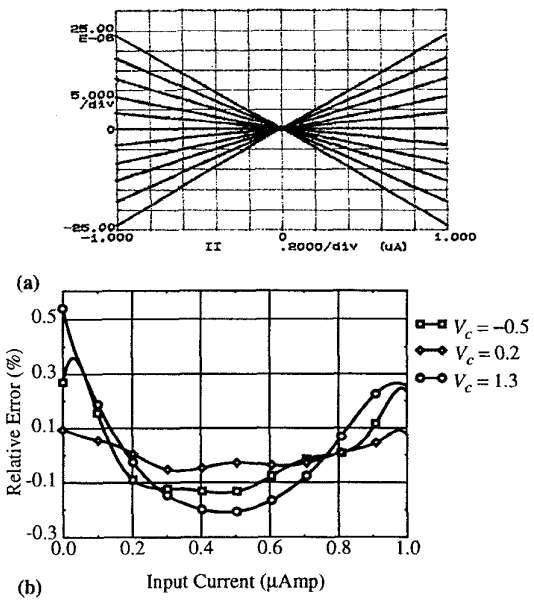

FIGURE 8. Experimental response of a programable current amplifier. (a) Transfer characteristic; (b) Nonlinearity error for different values of the control variable.

operator parameters. Fig.9(a) represents the variation of the height of the basis function for different positive and negative values of I_v. Fig.9(b) shows the curve family obtained through variation of I_δ, maintaining the rest of the parameters constant. Fig.9(c) and (d) show the variation of the linear basis function slopes obtaining by adjusting the gain of the corresponding current amplifiers.

V.References

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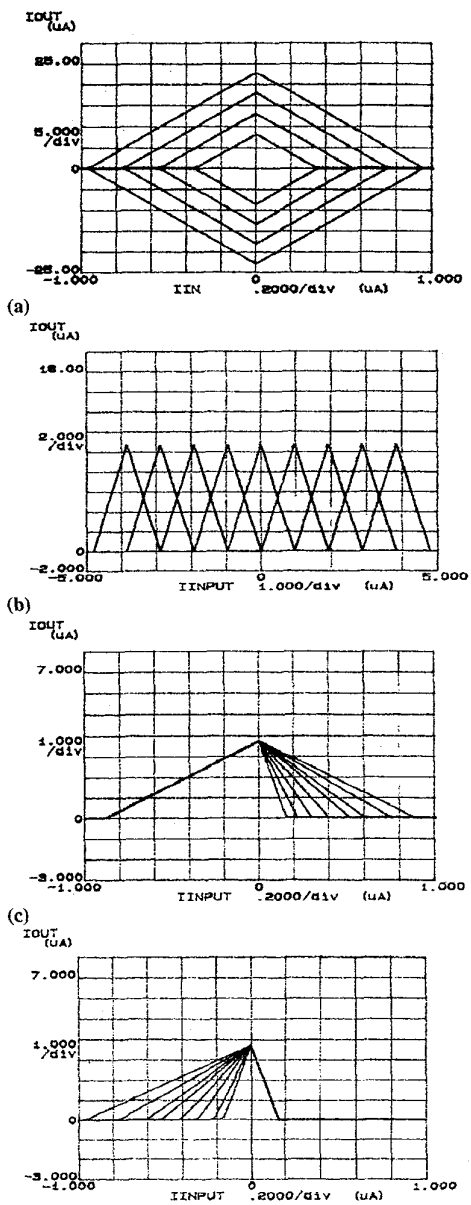

FIGURE 9. Experimental results obtained from the integrated prototype: (a) Variation with I_v; (b) Variation with I_δ; (c) and (d) Variation with slopes.