IEEE Instrumentation and Measurement
Technology Conference
Brussels, Belgium, June 4-6, 1996

A Fourth-Order BandPass ΣΔ Modulator Using Current-Mode Analog/Digital Circuits

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Abstract*- We present a fourth-order bandpass ΣΔ switched-current modulator IC in 0.8 μm CMOS single-poly technology. Its architecture is obtained by applying a lowpass to bandpass transformation ($z^{-1} \rightarrow - z^{-2}$) to a second-order lowpass modulator. It has been realized using fully-differential circuitry with common-mode feedback. Measurements show 8 bit dynamic range up to 5MHz clock frequency and 10KHz bandwidth.

I. INTRODUCTION

ΣΔ converters use oversampling to reduce the in-band power of quantization noise, and feedback to shape this noise and push it out of band. The intrinsic tolerance of ΣΔ converters to analog circuitry inaccuracies renders them very well-suited for the on-chip design of high-resolution interfaces in mixed-signal ASICs.

Applications of ΣΔ converter ICs span from instrumentation to telecommunications. In particular, bandpass ΣΔs are used at the front-end of modern narrow-band communication systems [1][2]. Table 1 summarizes the state-of-the-art on ΣΔ BandPass realizations. [3] and [4] are in BiCMOS technology. The former use "off-chip" LC resonators, while the latter employs sampled-data resonators realized with switched capacitor circuits. Similar design technique is employed in [5] and [6], in CMOS technology. The table displays the center frequencies and bandwidths measured for each realization. They are suitable for broadcast and voice AM, IS-54 cellular telephony, and GSM telephony. However, they are not the best suited for standard VLSI where neither accurate thermal oxide linear capacitors nor high f_T BJT transistors are available.

The trend towards combination of analog and digital circuitry on mixed-signal chips with low production cost has motivated exploring design techniques such as Switched-Currents (SI), which can be manufactured in standard VLSI single-poly technologies without any extra processing steps [7].

SI circuits have already been used for lowpass ΣΔs [8,9]. To the best of our knowledge, this paper reports the first IC realization of an SI bandpass ΣΔ IC. It is a fourth-order architecture and has been designed using fully-differential circuitry in 0.8 μm CMOS single-poly technology. Measurements show 8 bit dynamic range up to 5MHz clock frequency. Since the commercial AM broadcast band is 540 to 1600KHz, with stations occupying a band 10KHz wide, this modulator performs according to digital AM receiver requirements [6].

II. ARCHITECTURE OF THE MODULATOR

The modulator architecture has been obtained by applying a $z^{-1} \rightarrow -z^{-2}$ transformation to the second-order lowpass prototype of Fig. 1 [5]. This transformation maintains the stability properties of the lowpass prototype, whose practical use has been demonstrated in both SC and SI implementations [8].

Because of this transformation, the integrators in the lowpass prototype become resonators with transfer function,

Table 1: State of the Art of BandPass ΣΔ Modulators

Reference	F_s (MHz)	BW (KHz)	SNR (dB)	Technology
Jantzi[6] (1993)	1.852	8	63	CMOS 3μm double poly
Longo[5] (1993)	7.2	30	92	CMOS 1μm double poly
Troster[3] (1993)	26	200	55	BiCMOS 1.2μm/7GHz off-chip LC
Singor[4] (1995)	42.8	200	57	BiCMOS 0.8μm

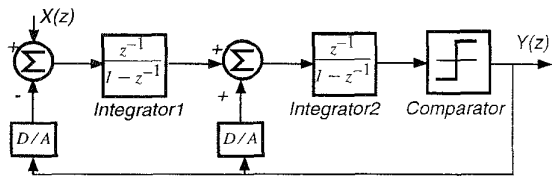

Fig. 1: Initial lowpass block diagram

$$R(z) = \frac{-z^{-2}}{1+z^{-2}} \quad (1)$$

Fig. 2 shows two alternative structures to realize $R(z)$ above in a way compatible with SI design technique. Structure -1 is a cascade of one Forward-Euler integrator and one Forward-Euler differenciator. Structure-2 is a cascade of two Back-Euler integrator blocks.

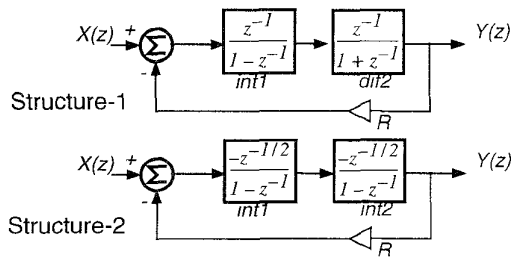

Fig. 2: Alternative structures to implement the resonator block

For both structures in Fig. 2, the nominal value of the feedback coefficient R is 2. In practical realizations, changes in this coefficient degrade the quality of the resonator. Fig. 3 displays the pole movement with R varying around its nominal value, for both structures. It is seen that the poles remain in the circle unit for Structure-2 -- the reason leading us to choose this structure to design the modulator.

Fig. 4 shows the block diagram of the bandpass modulator. The required feedback delay has been realized through two additional delay blocks, as depicted in the figure. Assuming that the 1 bit quantizer in the resulting bandpass modulator can be modelled as an additional white noise source with effective gain of k, the output is given as,

$$Y(z) = z^{-2}X(z) + (1+z^{-2})^2 E(z) \quad (2)$$

where $X(z)$ is the modulator input signal, $Y(z)$ is the modulator output, and $E(z)$ is the additional quantization noise source in the linear model. We see that the transfer

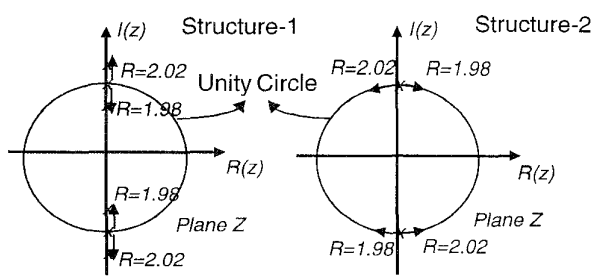

Fig. 3: Displacement of poles with R.

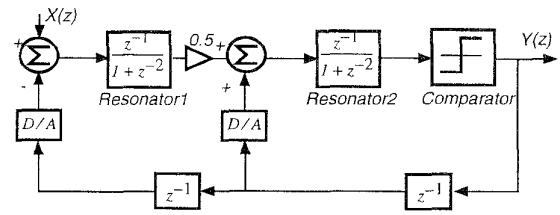

Fig. 4: Block Diagram of the Modulator.

function for the input is a double-delay; on the other hand, the transfer function $NTF(z)$ for the quantization noise has two transmission zeroes at $f_s/4$. This is the equivalent of the two zeroes at DC observed in the lowpass prototype.

Fig. 5 shows simulation results of the modulator architecture obtained using *ASIDES* [10], a proprietary behavioral simulator for ΣΔ modulators. Fig. 5a shows an FFT of the simulated modulator output for a sinusoidal input of –6dB range, centered on 2.5 MHz, and a clock frequency of 10MHz. The use of a scaling factor 0.5 at the output of the first modulator obtains similar dynamic range at the output of both resonators, as shown in the histogram of Fig. 5b. Thus both resonators can be designed identically.

III. DESIGN PROCESS

The methodology used to design the modulator is based on our previous work in [10]. The coefficients of the modulator are chosen through a statistical optimization procedure where the cost function is built using equations to describe the major non-idealities of SI blocks (namely, memory cells and integrators) that degrade the performance bandpass ΣΔ modulators. As regards to the calculation of the dimensions of the transistors in the SI blocks we have used also statistical optimization, and electrical simulations to evaluate the cost function.

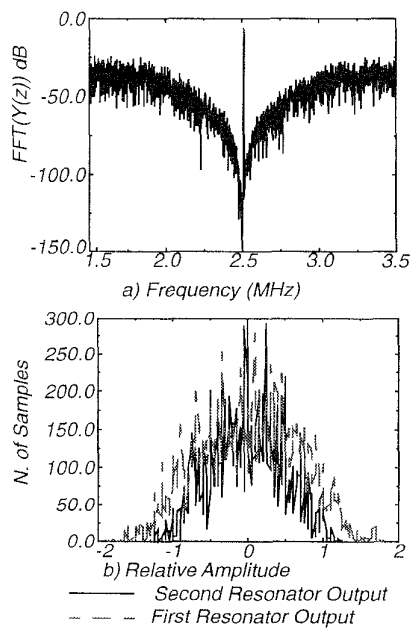

Fig. 5: Behavior Simulations of the Modulator

A.Quantization noise

Previous analysis of SI memory cells and integrators have considered finite output-input conductance ratio (ε_g), charge injection (ε_q) and settling errors (ε_s) [7]. For our purposes, we have also taken into account errors due to changes in the feedback loop gain,

$$\varepsilon_R = 1 - \frac{R}{R_{NOM}} \tag{3}$$

where R_{NOM} is the nominal value of 2. The transfer function of quantization noise when these non-idealities are taken into account is given by,

$$NTF(z) \approx \left(1 + z^{-2}\right)^{-2} + \varepsilon_g(z) + \varepsilon_q(z) + \varepsilon_s(z) + \varepsilon_R(z) \tag{4}$$

where,

$$\varepsilon_g(z) = \varepsilon_q(z) = \left(-4\varepsilon_g\left(1 + z^{-2}\right)\left(1 - z^{-1}\right)\right)$$
$$\varepsilon_s(z) = -4\varepsilon_s\left(1 + z^{-2}\right)\left(20 - 16z^{-1}\right)$$
$$\varepsilon_R(z) = -12\varepsilon_R^2 z^{-2}\left(1 + \frac{4}{3}z^{-2}\right)$$

It is seen that the zeroes of *NTF(z)* are shifted from their nominal positions at $f_s/4$, thereby degrading the filtering performed by the resonators. Each non-ideality produces different amount of degradation. As designers, we would like to have insight about the separate influence of each non-ideality. Fig. 6 illustrates this. There we plot three different families of Bode diagrams for $|NTF(f)|$ with $z = \exp(j2\pi f/fs)$. Each has been obtained by keeping only one error term and nulling the others. It is seen that, for similar error magnitude, the most important shifting in $|NTF(f)|$ is due to settling error ε_s. On the other hand, the gain error ε_R manifests only through shiftings of the signal band around the center frequency.

The quantization noise power P_{EQ} can be obtained by integrating the power spectral density in the signal band,

$$P_{EQ} = \frac{\Delta^2}{12 f_s} \int_{\left(f_s/4 - (BW)/2\right)}^{\left(f_s/4 + (BW)/2\right)} |NTF(f)|^2 df \tag{5}$$

Where Δ is the quantization step and *BW* is the information signal band. After some algebra, and assuming that errors are < 1% (for simplifications) one obtains,

$$P_{EQ} = \frac{\Delta^2}{120}\frac{\pi^4}{M^5} + \frac{\Delta^2}{9}\frac{\pi^2}{M^3}\left(4\varepsilon_g^2 + 4\varepsilon_q^2 + 16\varepsilon_s^2 + 3\varepsilon_R^2\right) \tag{6}$$

where *M* is the oversampling ratio defined as $f_s/(2BW)$. The first term in (6) is the ideal P_{EQ} and the others are the error contributions

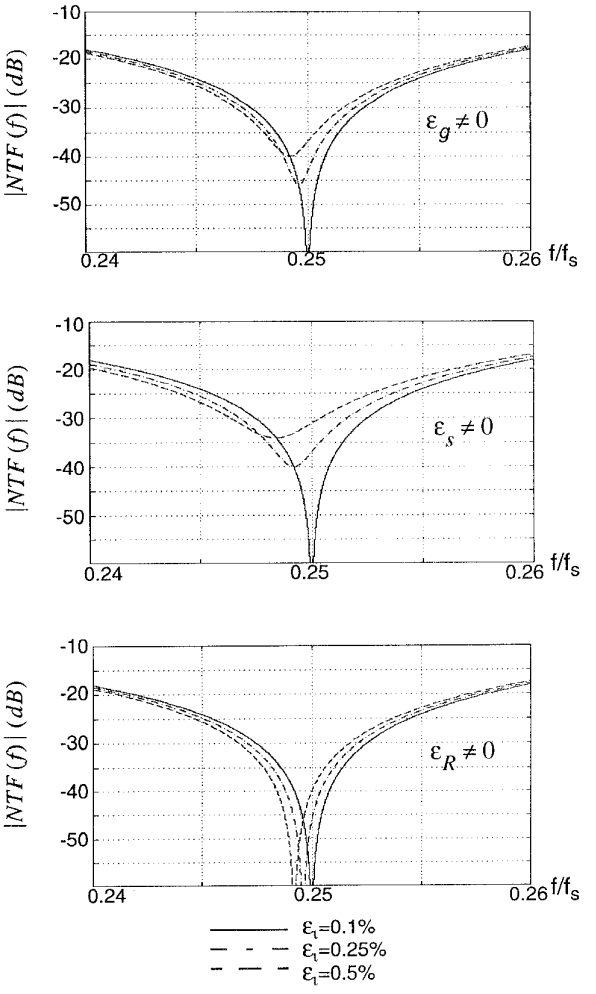

Fig. 6: Influence of non-idealities on *NTF(z)*

B.Thermal Noise

Thermal noise is the ultimate limiting factor in practical realizations of ΣΔ modulators. The most important contribution is due to the first resonator in Fig. 4, whose input-referred current noise Power Spectral Density (*PSD*) is given by [11],

$$S_I(f) = \left(\frac{\tau}{T}\right)^2 Sinc^2(f\tau)\, S_o \frac{2BW_n}{f_{ck}} \tag{7}$$

where BW_n is the noise equivalent bandwidth and S_o is the thermal noise *PSD* before sampling.

The maximum signal to noise ratio for a sinusoidal input of Δ amplitude is given as,

$$SNR = \frac{\Delta^2/2}{P_{EQ} + P_{TH}} \tag{8}$$

where P_{TH} is the thermal noise power obtained after integration of (7) in the signal band.

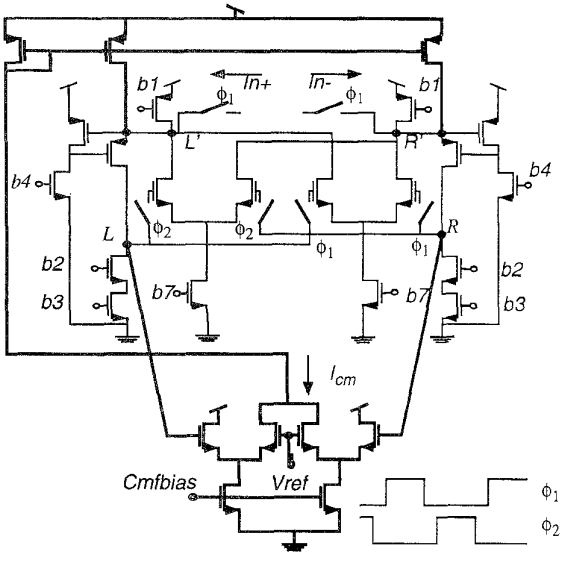

Fig. 7: Regulated Folded-Cascode Integrator with CMFB

IV. MODULATOR BLOCKS

A.SI Integrator

Fig. 7 shows the implementation of the integrator with SI techniques. For maximum reduction of errors, we used a fully-differential regulated folded cascode structure -- inspired in [11]. The thin line in this figure represents the signal path, while the thick lines represent the Common-Mode Feedback path (CMFB). The cell incorporates local feedback in the signal path to increase the input conductance and thus reduce the interconnection loading errors. Minimum size dummy transistors are used to attenuate feedthrough cancellation. Besides, the differential structure of the cell provides first-order cancellation of the residual feedthrough. To avoid transient spikes, the cell output nodes are connected to low-impedance nodes while the steering switches are open. Also, delayed versions have been used for the clock phases that control the steering switches.

B.1-bit D/A Converter

Fig. 8 shows a schematic of the 1-bit D/A converter used in the circuit, consisting of a current source controlled by the comparator output [8]. The stacked cascode current mirror

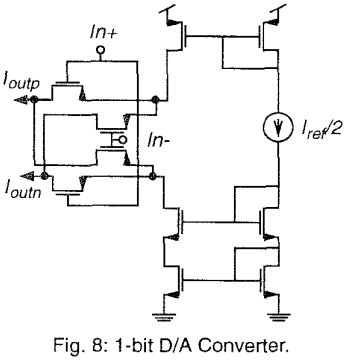

Fig. 8: 1-bit D/A Converter.

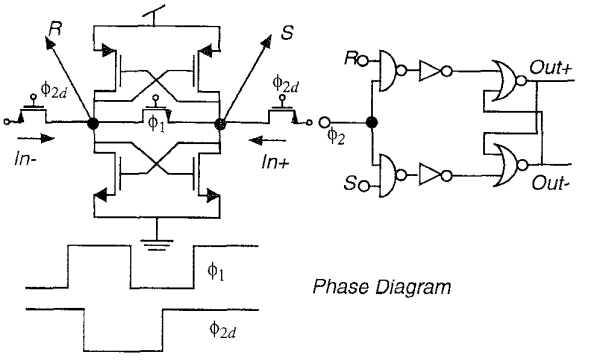

Fig. 9: Block diagram of the Current Quantizer

has been chosen because it resembles the structure of the cell memory. The two output currents change the flow direction depending on the comparator output. A small offset is no serious problem for the modulator. PMOS switches are used due to the input voltage range required in the integrators.

C.1-bit Quantizer

Fig. 9 shows the quantizer block diagram, made up of a regenerative latch [13] and an RS flip-flop that maintains the output value in the phase ϕ_1, which is the phase where the resonators are feedback.

The regenerative latch operates as follows. Since the input switches are PMOS, currents are sampled in the complementary phase ϕ_{2d}, developing a small difference voltage through the NMOS switch. When the NMOS switch opens, the current which flows through it cuts off abruptly, and the latch impedance changes from positive to negative (due to the positive feedback). Consequently, depending on the sign of the small difference of stored voltage, the latch output nodes (R and S) will go to the positive or negative rail. A fast comparison is thus obtained with low input current levels.

D.Input Buffer

If the voltage-to-current conversion needed at the modulator output is realized using an external resistance, the transient behavior of resonator-1 is influenced by the pad capacitance. To avoid this, an input buffer is included in our prototype. Fig. 10 shows the schematics of this block. Input to this block can be either fully differential or single-ended,

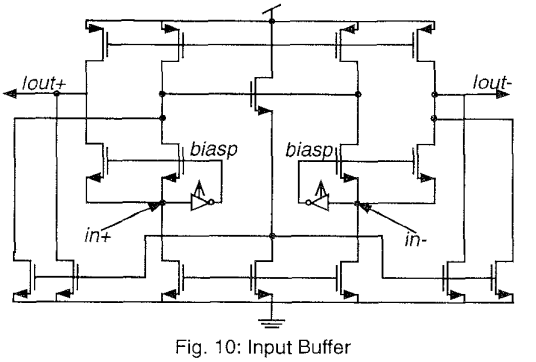

Fig. 10: Input Buffer

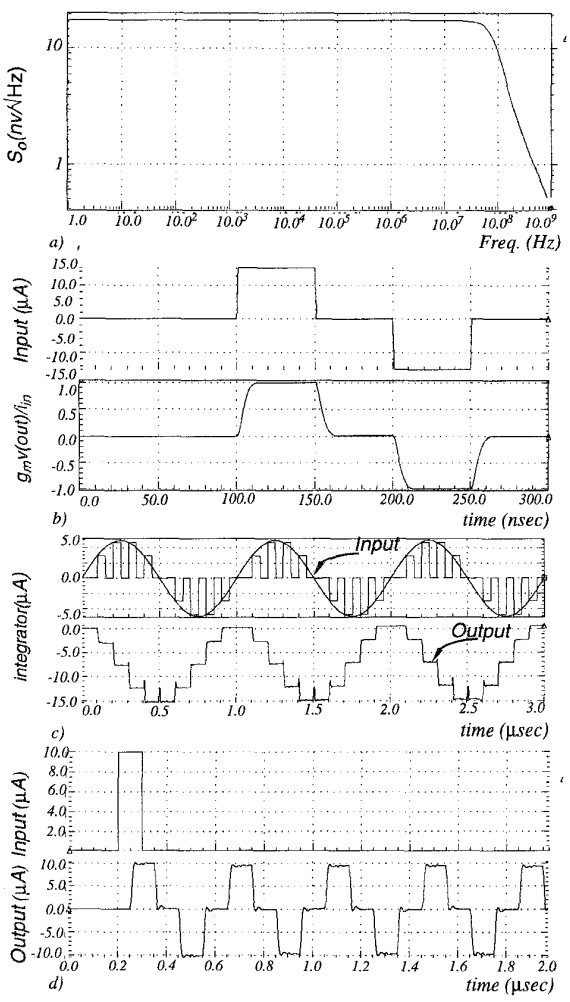

Fig. 11: HSPICE Simulations of the Memory Cell and Resonator.

while output is always fully-differential. The common-mode gain of the blocks is significantly smaller than the differential gain. Any remaining common mode will be rejected by the CMFB circuit of the differential SI integrator.

V. SIMULATION RESULTS

Fig. 11 shows several simulations of the modulator blocks using *HSPICE*. Fig. 11a shows the total noise rms voltage (S_o) of the buffer and integrator cascade.This AC simulation is made with all switches closed and *1/f*-noise removed and results in an equivalent noise PSD of 17.9nV/√Hz at the gates of the memory transistors of the integrator. Fig. 11b shows transient simulation of this cell in the storage phase; *v(out)* is the gate voltage of the memory transistor. Fig. 11c shows the time response of the integrator to a sinusoidal input of 5μA range and 1MHz when sampled to 10MHz. Finally, Fig. 11d shows a simulation of the time response of the resonator when it is excited by an impulse signal of 10μA range. The Resonator output should repeat the values in the ranges 10μA, 0, -10μA, 0 periodically. The observed

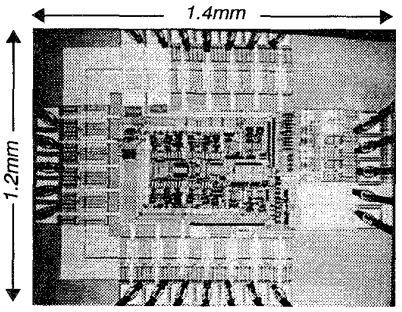

Fig. 12: Chip microphotograph

attenuation is due to non-idealities.

VI. EXPERIMENTAL RESULTS

Fig. 12 is a microphotograph of the prototype, which has been designed in a CMOS 0.8μm single-poly technology. It occupies 0.79x0.54mm^2 (without the interconnection pads), and consumes 15mW from a 5V supply. A clock phase generator is also included.

A.Input Buffer

Table 2 summarizes measurements made on an isolated buffer using a single-ended input. The white output noise has been measured with two external resistances connected to a 4V reference voltage. DC measurements have been realized with the semiconductor parameter analyzer HP4145, while bandwidth have been measured with the network analyzer HP4195.

In order not to constraint the high-frequency performance of the buffer, an external loading device with large bandwidth has been used. Fig.13 shows the measurement set-up. It is based on the AD844, a high speed monolithic operational amplifier implemented as a second generation current conveyor of gain +1 (CCII+) [14]. Fig. 14 shows an experimental Bode plot corresponding to C_{PAD} = 11pF (the whole parasitic capacitance in the experimental board). The measured 3dB frequency is 28MHz, which results approximately equal to the dominant pole $(2\pi R_{in}C_{PAD})^{-1}$, created by the input resistance of the buffer.

B.Modulator

A test board was fabricated following the indications in [15]. Fig. 15(a) shows the measured power spectrum of the modulator output when the clock frequency is 5MHz and the input is a -6dB@1.26MHz single tone. In order to obtain the signal to noise ratio, bit streams were obtained for the modulator at different signal levels by using the HP82000

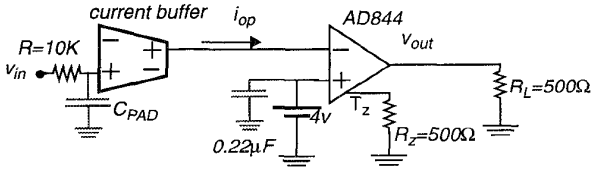

Fig. 13: AC Buffer Measurement Set-Up

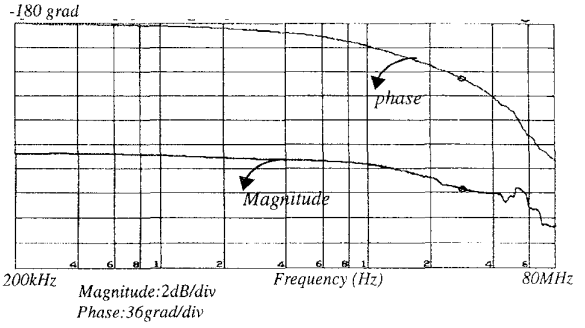

Fig. 14: Experimental Bode plot

data acquisition equipment. Hanning-windowed 32768-point FFTs were performed on each of those bit streams and SNR was calculated from them by varying signal levels. Fig. 15(b) shows the measured SNR versus input for the same modulator evaluated in a bandwidth of ±5KHz around the input frequency.

VII. CONCLUSIONS

A SI bandpass ΣΔ modulator has been designed in a CMOS 0.8μm single-poly technology. The architecture is obtained by applying a lowpass to bandpass transformation to a second order lowpass architecture. The circuit has been realized using switched-current fully differential regulated cascode cells. Measurements show 8 bit dynamic range up to 5MHz clock frequency. Since the commercial AM broadcast band is 540 to 1600Khz, with stations occupying a band 10KHz wide, this modulator performs according to digital AM receiver requirements [6].

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Table 2: Measurements of the current buffer

PARAM.	HSPICE	Experimental	Unit.
Diff. DC-Gain	0.48	0.49	--
Output swing	±20	±12	μA
R_{in}	684	<684	Ω
R_{out}	176	113	KΩ
Common DC-Gain	0.03	0.03	dB
White output Noise	10	50	nV/√Hz
Bandwidth	25	>20	MHz

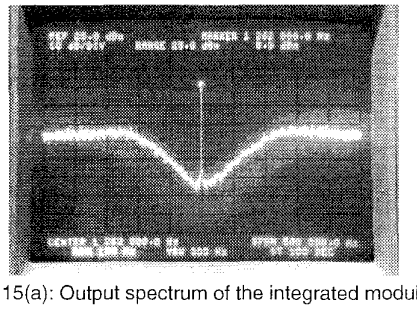

Fig. 15(a): Output spectrum of the integrated modulator

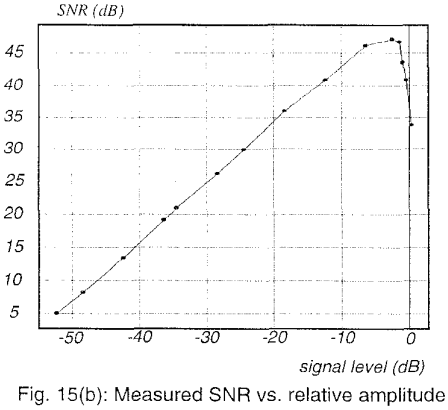

Fig. 15(b): Measured SNR vs. relative amplitude