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Integrated Control and Modulation for Three-Level NPC Rectifiers

Antonio Ventosa-Cutillas [1,*], Pablo Montero-Robina [1], Francisco Umbría [2], Federico Cuesta [1] and Francisco Gordillo [1]

[1] Departamento de Sistemas y Automática, Escuela Técnica Superior de Ingeniería, Universidad de Sevilla, 41092 Sevilla, Spain; pmontero1@us.es (P.M.-R.); fcuesta@us.es (F.C.); gordillo@us.es (F.G.)
[2] ASM Assembly Systems GmbH & Co. KG, 81379 Munich, Germany; francisco.umbria@asmpt.com
* Correspondence: aventosa@us.es; Tel.: +34-95-448-2292

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Abstract: This paper uses a novel approach for the control of three-level neutral-point-clamped (NPC) rectifiers in order to tackle the capacitor voltage balance problem. A distinctive feature of the new control approach is that it is based on a model which is written in terms of the duty ratios for each phase at each level. Hence, the system model presents nine duty cycle variables. Despite the fact that this formulation is different from the usual ones, it is shown that the control problem of currents and dc-link voltage can be formulated in a similar way to conventional methods. Furthermore, the control of the capacitor voltage balance can be expressed by means of equations that are decoupled from the currents and dc-link voltage dynamics, which results in a specific controller for the voltage balancing that does not affect the previous dynamics. A key point of the proposed approach is that part of the modulation stage is implicit in the formulation. Two particular controllers are compared in this paper. The first one fulfills the different control objectives at the expense of a large number of commutations. This problem is overcome in a new proposed controller, which presents similar performance and a satisfactory number of commutations. Experimental results are performed showing the effectiveness compared with a modified virtual space vector modulation with capacitor voltage balance capabilities.

Keywords: synchronous rectifier application; neutral-point-clamped (NPC) converter; voltage balancing; integrated control and modulation (ICM); Grid-connected power converter; multilevel converters

1. Introduction

In the field of energy conversion systems, the advantages that multilevel power electronic converters offer are well known. Bidirectional power flow, increase of the output voltage magnitude, robustness, etc. are only some of the advantages that have made multilevel converters popular in medium and high power applications in the industry [1–3]. Some of the different types of topologies of these converters are neutral-point-clamped, cascaded H-bridge or flying-capacitor [1,2,4]. A Neutral-point-clamped (NPC) converter, which was proposed for the first time in [5], is one of the most used multilevel converter topologies. During normal operation, the voltage that drops across each capacitor must be balanced otherwise, it can result in poor output voltage quality, affecting the performance of the control or even damaging the semiconductor devices. Therefore, NPC converters present an additional objective apart from the usual control objectives in power converters [6] that is the voltage balance between capacitors, which is the main focus in this paper.

Over the last few years, numerous techniques have been developed to correct the voltage unbalance. Some of them use additional circuitry [7–9], but this would lead to an increase in cost, losses and complexity in hardware. Other authors use different control techniques with algorithms of varying difficulty [10–15]. One of these control techniques [13] uses a modification of virtual space

vector [16] (denoted as mVSVPWM in this paper). In [13], the voltage reference vector is obtained by creating virtual vectors where the possible switching states are weighted to generate currents that benefit the voltage balance.

Regarding the modelling, it is usual to work with averaged models where the discrete values of the gating elements are considered as continuous signals [1,17]. In order to implement the control laws obtained with such models, a discretization stage, usually called modulation, needs to be accomplished [18]. Modulation plays an important role in the overall system performance since properties such as number of commutations and harmonic distortion of currents and voltages are affected by the way modulation is carried out. Modulation methods can be classified into three main groups [19]: pulse width modulation (PWM) [20,21], pseudo-modulation [22] and closed-loop control methods with implicit modulator [23–25].

This paper presents a new approach to deal with the control of three-level NPC converters, which is based on [26]. In this paper, the circuit model is formulated in terms of the duty ratios of each phase at each level. In this way, there are nine duty cycle variables (three duty cycles per phase) instead of just three (one duty cycle per phase). This formulation is not new, e.g., a similar model, based on d–q transformation, was presented in [27] to design an LQR controller for an NPC inverter by linearization using a small-signal model. In [26], it is shown that this formulation allows to explicitly consider, in the control design stage, the extra degree of freedom associated with the injection of homopolar component. The increase in the number of variables does not make the design significantly more difficult since, with an appropriate change of variables, the dc-link voltage and active and reactive power control problems can be formulated in a similar way to other usual approaches. As a result, the voltage balance controller can be easily designed at the same time that an important part of modulation is not needed. For this, the proposed approach can be considered as a control method with part of the modulation stage included in the control formulation, therefore, in what follows it would be called "Integrated Control and Modulation" (ICM). The main advantage of the proposed control law is its simplicity in implementation compared to modified versions of space vector modulation (SVM) [16] that also tackle the capacitor voltage unbalance but it still presents some advantages with respect to CB-PWM approaches. This is due to the fact that the modulation stage is simplified without losing part of the flexibility of SVM [28,29]. Once the nine duties are computed, the way they are sequenced can be chosen freely, splitting them up or shifting them among the different phases. This freedom allows the user to achieve secondary control objectives similarly to SVM such as common-mode voltage reduction or avoidance of extra switching losses. For the sake of a fair comparison, this article will use a simple triangular-shaped sequence similar to that of CB-PWM approaches. Furthermore, the problem formulation for power, current and dc-link voltage control is the same as when using other conventional approaches, such as model-based direct power control (DPC) [30–33] or proportional-resonant controller (PR) for currents [34,35].

The drawback of the proposed approach in [26] is that it may lead to an unnecessary increase in the number of commutations. This is due to the fact that, unless some of the duty cycle variables turn out to be zero, the resultant switching signals will commute among all the levels for the three phases every sampling period. This is the case of the first control law considered in this paper (ICM1), whereas with the dc-link voltage, current or power control can be accomplished by switching each phase between two levels [36] when the voltage balance problem is not considered. In this paper, by using a remaining degree of freedom associated with the injection of homopolar component, some commutations are avoided compared to ICM1 presenting a second controller (ICM2) who explodes this capability. The output waveform of ICM2, as it will be shown later on in experiments, is similar to those approaches which inject a third harmonic signal into the output voltage to increase the fundamental signal range without overmodulating [37]. Therefore, ICM2 also has this property inherent without the need of extra computations.

Both control laws are validated by means of experiments and compared with a control technique based on a modified virtual space vector modulation (mVSVPWM) [13], which includes capacitor

voltage balance capabilities. Therefore, the main contributions of this paper in comparison with [26] are the inclusion of a new approach (ICM2) along with experimental verification of both approaches.

The next section is devoted to presenting the converter considered in this paper, as well as its dynamic model. Section 3 presents the controller design for fulfilling the three control objectives: regulation of the currents and the dc-link voltage and capacitor voltage balance. Section 4 proposes two variants for the selection of the remaining degrees of freedom resulting in two different controllers, ICM1 and ICM2. Section 5 presents experimental results. The paper closes with a section of conclusions.

2. Dynamic Model of the System

The configuration of the converter used in this paper is a three-phase three-level NPC converter in rectifier mode with a resistive load, as shown in the scheme of Figure 1.

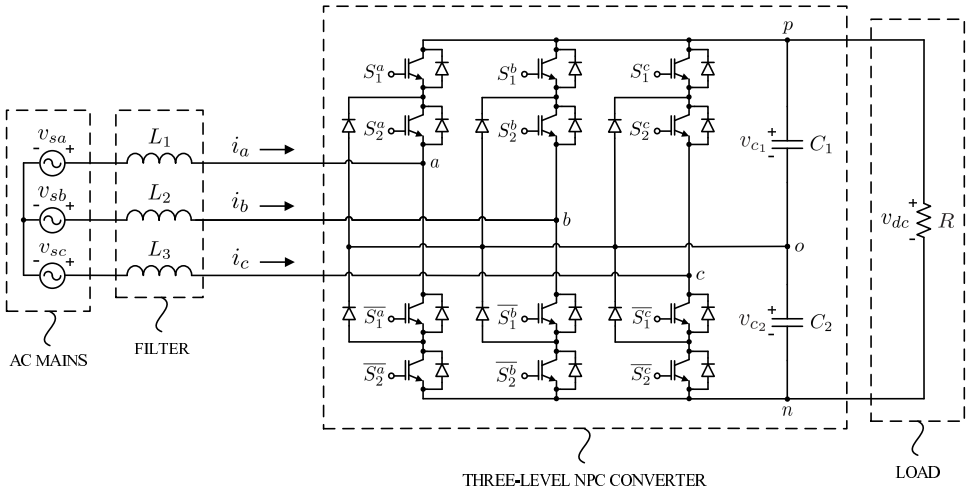

Figure 1. Schematic diagram of the three-phase three-level neutral-point-clamped (NPC) rectifier.

The electrical power grid is considered as a three-phase voltage source, where the phase voltages are represented by v_{sa}, v_{sb} and v_{sc}. The converter is connected to the grid through an inductive filter where inductances have the same value L.

On the dc-link side, capacitors have the same value C and their voltages are denoted by v_{c1} and v_{c2}. Connected to the converter terminals there is a resistive load R. The total dc-link voltage is defined as $v_{dc} = v_{c1} + v_{c2}$.

Considered System Model

The model considered in this paper is described in [26], which is based on a model presented in [27]. This model uses the equations in $\alpha\beta\gamma$ coordinates by introducing the power-invariant form of the Clarke Transform. Furthermore, the switching signals have been replaced by their respective duty ratios in each level [27,38], d_{ij} with $i = \alpha, \beta, \gamma$ and $j = p, o, n$, where p is the positive level when switches S_1^i and S_2^i are closed, o is the zero level when switches $\overline{S_1^i}$ and S_2^i are closed and n is the negative level when switches $\overline{S_1^i}$ and $\overline{S_2^i}$ are closed. This formulism yields

$$L\frac{di_\alpha}{dt} = v_{s\alpha} - (d_{\alpha p} - d_{\alpha n})\frac{v_{dc}}{2} - (d_{\alpha p} + d_{\alpha n})\frac{v_d}{2} \quad (1)$$

$$L\frac{di_\beta}{dt} = v_{s\beta} - (d_{\beta p} - d_{\beta n})\frac{v_{dc}}{2} - (d_{\beta p} + d_{\beta n})\frac{v_d}{2} \quad (2)$$

$$C\frac{dv_{dc}}{dt} = (d_{\alpha p} - d_{\alpha n})i_\alpha + (d_{\beta p} - d_{\beta n})i_\beta - 2\frac{v_{dc}}{R} \quad (3)$$

$$C\frac{dv_d}{dt} = (d_{\alpha p} + d_{\alpha n})i_\alpha + (d_{\beta p} + d_{\beta n})i_\beta, \quad (4)$$

where v_d is the dc-link capacitor voltage difference defined by $v_d = v_{c1} - v_{c2}$. The control inputs $d_{\alpha p}$, $d_{\alpha n}$, $d_{\beta p}$ and $d_{\beta n}$ are the duty ratios in $\alpha\beta\gamma$ coordinates. Control inputs $d_{\gamma p}$ and $d_{\gamma n}$ do not appear in the model, as mentioned in [26], because they are multiplied by i_γ, whose value is zero for a balanced system. Similarly, variables d_{io} do not appear in this model but their values can be retrieved at the final stage of the controller using the following constraints:

$$d_{ap} + d_{ao} + d_{an} = 1 \tag{5}$$

$$d_{bp} + d_{bo} + d_{bn} = 1 \tag{6}$$

$$d_{cp} + d_{co} + d_{cn} = 1 \tag{7}$$

$$d_{ij} \in [0,1], \text{ for } i = a,b,c \text{ and } j = p,o,n.$$

Phase currents i_α and i_β can be expressed in terms of powers as

$$i_\alpha = \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(v_{s\alpha}p - v_{s\beta}q\right) \tag{8}$$

$$i_\beta = \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(v_{s\beta}p + v_{s\alpha}q\right), \tag{9}$$

where p and q are the instantaneous active and reactive powers of the system, respectively. In this way, (3) and (4) could be expressed as

$$C\frac{dv_{dc}}{dt} = \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(d_{\alpha p} - d_{\alpha n}\right)\left(v_{s\alpha}p - v_{s\beta}q\right) + \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(d_{\beta p} - d_{\beta n}\right)\left(v_{s\beta}p + v_{s\alpha}q\right) - 2\frac{v_{dc}}{R} \tag{10}$$

$$C\frac{dv_d}{dt} = \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(d_{\alpha p} + d_{\alpha n}\right)\left(v_{s\alpha}p - v_{s\beta}q\right) + \frac{1}{v_{s\alpha}^2 + v_{s\beta}^2}\left(d_{\beta p} + d_{\beta n}\right)\left(v_{s\beta}p + v_{s\alpha}q\right), \tag{11}$$

where variables v_{dc} and v_d are expressed in terms of the instantaneous power p and q.

3. Controller Design

With the purpose of dealing with the three control objectives (currents, dc-link voltage and capacitor voltage balance control), the system dynamic model (1)–(4) presented previously is considered to design the controllers in this section. It can be seen that the proposed modeling allows to cope with the capacitor voltage balance problem while it does not affect the current and dc-link voltage controllers.

3.1. Total DC-Link Voltage Controller

In order to maintain constant the dc-link voltage and close to its reference (v_{dc}^r), as usual, a PI controller is used [26,30,39],

$$p^r = k_p^{dc}\left({v_{dc}^r}^2 - v_{dc}^2\right) + k_i^{dc}\int_0^t\left({v_{dc}^r}^2 - v_{dc}^2\right)d\tau, \tag{12}$$

where constants k_p^{dc} and k_i^{dc} are controller tuning parameters.

3.2. Current Controller

Observing Equations (1) and (2), two virtual control variables can be defined as

$$u_1 \doteq d_{\alpha p} - d_{\alpha n} \tag{13}$$

$$u_2 \doteq d_{\beta p} - d_{\beta n}. \tag{14}$$

Introducing these variables into the currents dynamic model and assuming that the value of variable v_d is small enough to be neglected,

$$L\frac{di_\alpha}{dt} = v_{s\alpha} - u_1\frac{v_{dc}}{2} \tag{15}$$

$$L\frac{di_\beta}{dt} = v_{s\beta} - u_2\frac{v_{dc}}{2}. \tag{16}$$

These expressions are equivalent to those current dynamics of the conventional two-level converter [26]. Therefore, by the use of the change of variables (13) and (14), the added difficulty inherent for the adopted formulation disappears, at least at this stage. Additionally, introducing the references for the active (p^r) and reactive power (q^r) into (8) and (9), the current references can be retrieved (i_α^r, i_β^r). Once these values are known, a non-ideal proportional-resonant controller [35], tuned at the grid frequency, is used to make the phase currents to track their references. In this way, the tracking error $(i_\alpha^r - i_\alpha, i_\beta^r - i_\beta)$ inputs the resonant controller, providing the value for control variables (u_1, u_2).

$$G_{PR_\omega}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega^2}$$

$$u_1 = \frac{2}{v_{dc}}(-G_{PR_{\omega_g}}(i_\alpha^r - i_\alpha) + v_{s\alpha}) \tag{17}$$

$$u_2 = \frac{2}{v_{dc}}(-G_{PR_{\omega_g}}(i_\beta^r - i_\beta) + v_{s\beta}) \tag{18}$$

where k_p and k_r are the proportional and resonant control parameters; ω_c is the cut-off frequency of the low-pass filter implemented into the resonant part; and ω is the resonant frequency—tuned at the grid frequency ω_g.

3.3. Voltage Balance Controller

The objective of the voltage balance controller is to keep the state variable v_d close to zero, avoiding the unbalance of the dc-link capacitor voltages, and it is based on the definition of two new virtual control variables

$$u_3 \doteq d_{\alpha p} + d_{\alpha n} \tag{19}$$

$$u_4 \doteq d_{\beta p} + d_{\beta n}. \tag{20}$$

Introduction of (19) and (20) into (11) yields

$$C\frac{dv_d}{dt} = \frac{v_{s\alpha}p - v_{s\beta}q}{v_{s\alpha}^2 + v_{s\beta}^2}u_3 + \frac{v_{s\beta}p + v_{s\alpha}q}{v_{s\alpha}^2 + v_{s\beta}^2}u_4. \tag{21}$$

It is important to highlight that the definition of u_3 and u_4 causes a decoupling of the virtual control variables for control purposes. Note that u_1 and u_2 are designed to regulate the state variables p and q, whereas u_3 and u_4 can be used to regulate v_d (21). This is an important benefit of the proposed control approach.

Taking into account (21), the proposed control laws [26] are defined as follows

$$u_3 = k_d \frac{v_{s\alpha}p - v_{s\beta}q}{p^2+q^2}(v_d^r - v_d) + k_{di}\frac{v_{s\alpha}p - v_{s\beta}q}{p^2+q^2}\int_0^t (v_d^r - v_d)\,d\tau \quad (22)$$

$$u_4 = k_d \frac{v_{s\beta}p + v_{s\alpha}q}{p^2+q^2}(v_d^r - v_d) + k_{di}\frac{v_{s\beta}p + v_{s\alpha}q}{p^2+q^2}\int_0^t (v_d^r - v_d)\,d\tau, \quad (23)$$

where positive constants k_d and k_{di} are customary tuning parameters. The reference for v_d is denoted by v_d^r, which is set to zero to ensure a balanced distribution of the dc-link voltage across capacitors C_1 and C_2.

By introducing (22) and (23) into (21), the voltage balance dynamics become linear:

$$C\frac{d^2(v_d^r - v_d)}{dt^2} + k_d\frac{d(v_d^r - v_d)}{dt} + k_{d_i}(v_d^r - v_d) = 0, \quad (24)$$

whose stability is assured provided that parameters k_d and k_{d_i} are positive. A complete schematic block diagram of all controllers is illustrated in Figure 2.

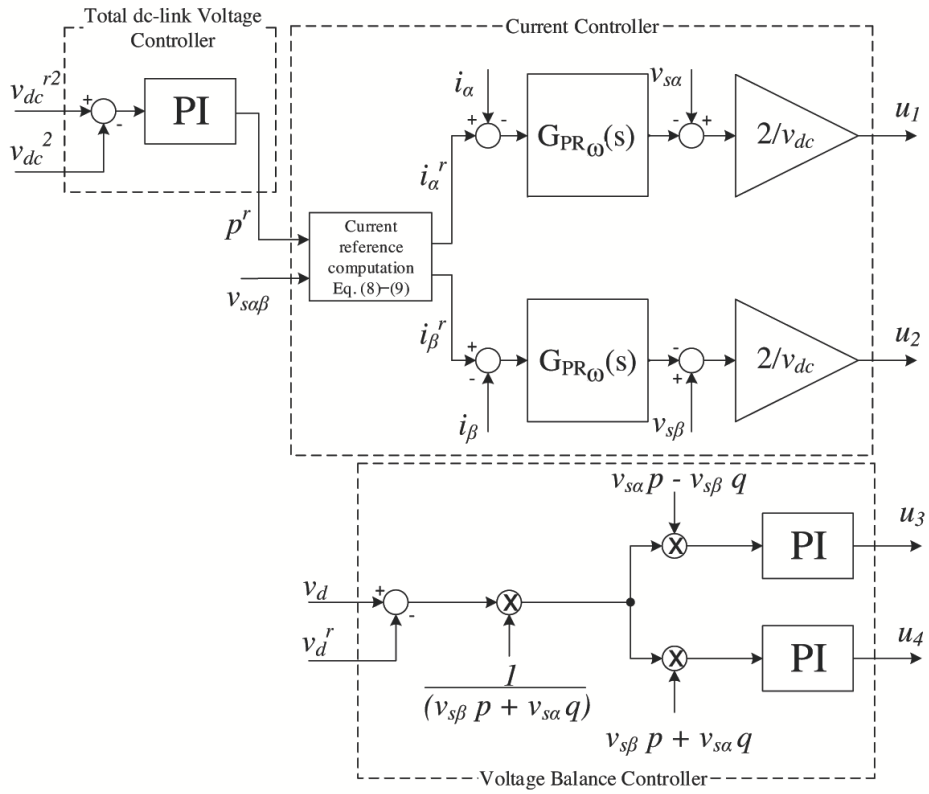

Figure 2. Complete schematic block diagram of the controllers.

4. Modulation Strategy

The controller presented in the previous section provides, at each sampling time, the values for u_1, u_2, u_3 and u_4. The corresponding values for $d_{\alpha p}, d_{\alpha n}, d_{\beta p}$ and $d_{\beta n}$ can be obtained solving the system of Equations (13), (14), (19) and (20) yielding

$$d_{\alpha p} = \frac{1}{2}(u_1 + u_3) \tag{25}$$

$$d_{\alpha n} = \frac{1}{2}(-u_1 + u_3) \tag{26}$$

$$d_{\beta p} = \frac{1}{2}(u_2 + u_4) \tag{27}$$

$$d_{\beta n} = \frac{1}{2}(-u_2 + u_4) \tag{28}$$

In order to compute the actual duty ratios $d_{ij}, i = a, b, c; j = p, n$, the Clarke transformation can be used

$$\begin{bmatrix} d_{aj} \\ d_{bj} \\ d_{cj} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} d_{\alpha j} \\ d_{\beta j} \\ d_{\gamma j} \end{bmatrix}, \quad j = p, n. \tag{29}$$

where $d_{\gamma p}$ and $d_{\gamma n}$ are remaining degrees of freedom. Obviously, the remaining duty ratios, d_{ao}, d_{bo} and d_{co} can be computed using (5)–(7).

4.1. First Proposal, ICM1

The first variant, ICM1, was proposed in [26]. In this variant, $d_{\gamma p}$ and $d_{\gamma n}$ are chosen to be constant and can be considered as tuning parameters. In [26], guidelines are given in order to avoid saturation problems. This approach is a simple way to accomplish the modulation but it presents an important drawback: except by chance, none of the d_{ij} will result in zero. This implies that, in each sampling time, each phase commutes among the three levels, which can be considered too many commutations compared with other controllers, even those including voltage balancing. This fact could yield large switching losses.

4.2. Second Proposal, ICM2

In order to avoid the large number of commutations, a new variant is proposed. This variant takes advantage of the two degrees of freedom associated with $d_{\gamma p}$ and $d_{\gamma n}$ by imposing, at each sampling period, one d_{ip} and one d_{in} to be zero. The two phases for which one of the duty ratios has to be zero need to be chosen carefully, as it is explained below, taking into account that the duty cycles in *abc* coordinates have to be in the interval $[0, 1]$. The result is that these two phases only switch between two levels while the remaining phase commutes among the three levels.

In order to select these phases, the procedure checks if setting one of the $d_{ij}, i = a, b, c; j = p, n$ to zero yields to the fulfillment of the constraints $0 \leq d_{ij} \leq 1$ for the rest of duty cycle variables. Starting with the case $d_{ap} = 0$, Equation (29) for $j = p$ can be considered as a set of equations, where $d_{\alpha p}, d_{\beta p}$ are known, $d_{ap} = 0$ and d_{bp}, d_{cp} and $d_{\gamma p}$ are the unknowns. The resultant system of equations can be solved in order to check if this case is feasible, that is, if d_{bp} and d_{cp} are in the interval $[0, 1]$. Repeating to the other phases, three different cases have to be analyzed for $j = p$ and other three cases for $j = n$. The associated equations are

Case 1: $d_{aj} = 0$

$$d_{bj} = -\frac{\sqrt{6}}{2} d_{\alpha j} + \frac{\sqrt{2}}{2} d_{\beta j} \quad (30)$$

$$d_{cj} = -\frac{\sqrt{6}}{2} d_{\alpha j} - \frac{\sqrt{2}}{2} d_{\beta j} \quad (31)$$

Case 2: $d_{bj} = 0$

$$d_{aj} = \frac{\sqrt{6}}{2} d_{\alpha j} - \frac{\sqrt{2}}{2} d_{\beta j} \quad (32)$$

$$d_{cj} = -\sqrt{2} d_{\beta j} \quad (33)$$

Case 3: $d_{cj} = 0$

$$d_{aj} = \frac{\sqrt{6}}{2} d_{\alpha j} + \frac{\sqrt{2}}{2} d_{\beta j} \quad (34)$$

$$d_{bj} = \sqrt{2} d_{\beta j}, \quad (35)$$

where $j = p, n$. The resultant duty ratios for the considered sampling instant are the corresponding ones to the feasible cases, that is, cases where all the duty cycles are in the interval $[0, 1]$. It will be shown below that, at every instant, there exists at least one (and apart from some border cases, only one) feasible case.

Regarding the computation burden of this approach, after retrieving (25)–(28), the calculation of the duty ratios d_{ij} can be achieved by checking the constraints $d_{ij} \in [0, 1]$ for the $3 \times 2 = 6$ cases. For this, (30)–(35) have to be used twice (for levels p and n). This last stage implies the computation of 20 multiplications and 8 sums as well as 24 comparisons.

Alternatively, a different approach can be used to choose the correct case at every sampling instant with the help of Figure 3. This figure depicts the straight lines that are the boundaries of constraints $0 \leq d_{ij} \leq 1$ using expressions (30)–(35). Consequently, the shaded regions represent the fulfillment of these constraints for each one of the three cases above. As for each level $j = p, n$ there is one d_{ij} that it is equal to zero, there are four of such lines for each case, instead of six. It can be seen that the three shadowed areas do not overlap (except at their borders) and that they cover a whole hexagon. An interesting fact is that this hexagon is related to the well-known hexagon of Space Vector Modulation (SVM), but in this case, there are two such hexagons (one for $j = p$ and one for $j = n$). The interest of Figure 3 is twofold: (1) it shows that, provided the converter does not work in overmodulation region, one of the three cases is always feasible, and (2) Figure 3 can be used as an alternative method to choose the correct case: the working sector can be computed as usual in SVM and once the appropriate case is selected, the corresponding formulae can be applied.

In summary, the ICM2 algorithm, whose data input and output are depicted in Figure 4, can be implemented in two alternative and equivalent ways that only differ in the computational burden, which in alternative B depends on the method used for the computation of the sextant:
Alternative A:

- Computation of u_3 and u_4 using (22) and (23).
- Computation of $d_{\alpha p}, d_{\alpha n}, d_{\beta p}, d_{\beta n}$ using (25)–(28).
- For levels p and n:
  - Computation of Equations (30)–(35) and selection of the case that fulfills the constraints $0 \leq d_{ij} \leq 1$. This procedure gives directly the resultant duty cycles.

Alternative B:

- Computation of u_3 and u_4 using (22) and (23).
- Computation of $d_{\alpha p}, d_{\alpha n}, d_{\beta p}, d_{\beta n}$ (25)–(28).
- For levels p and n:
  - Computation of the sextant inside the hexagon of Figure 3. This step is similar to the corresponding one in SVM (but it must be computed twice, one for level p and one for level n). The sextant gives the corresponding case.
  - Computation of the duties using the corresponding Equations of (30)–(35).

It can be noted that the computational complexity is lower in both ICM1 and ICM2 with respect to SVM strategies that include control of the voltage balance, such as [13].

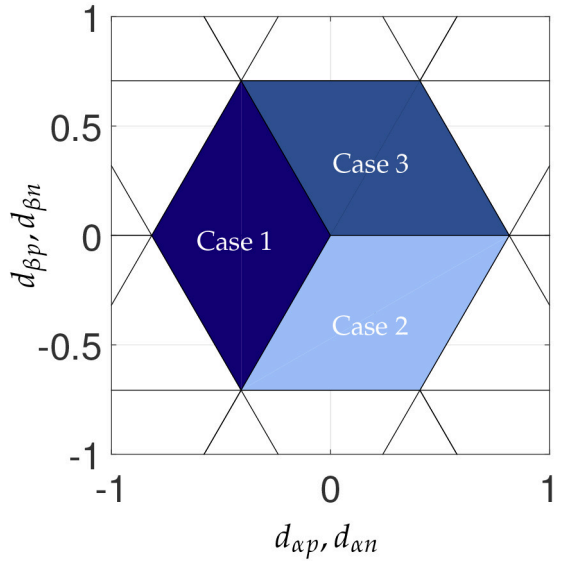

Figure 3. Graphical representation of the limits of each case.

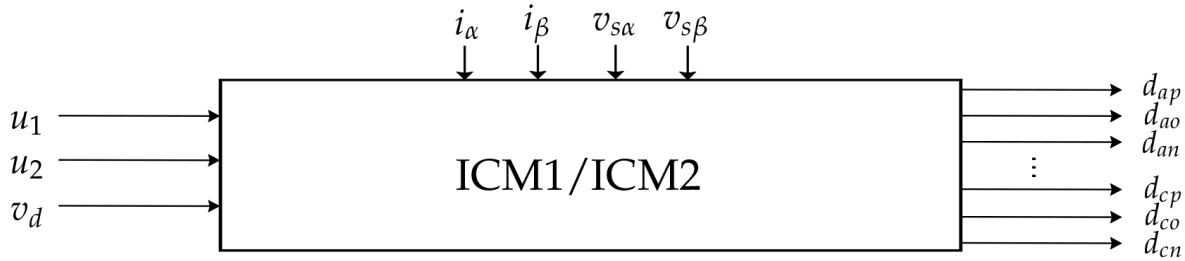

Figure 4. Data input and output of ICM1 and ICM2.

5. Experimental Verification

This section presents the experimental results obtained in the laboratory for the two approaches presented in this paper and the one used as a comparative (mVSVPWM) [13]. To this end, the three-level NPC converter shown in Figure 5 has been used. It has been configured as rectifier and it has the circuit and control parameters provided in Table 1. A first-order low-pass filter has also been added to the proportional part of the total dc-link voltage controller, as it is recommended in [33], tuned at 5 KHz in order to reduce the harmonics presence.

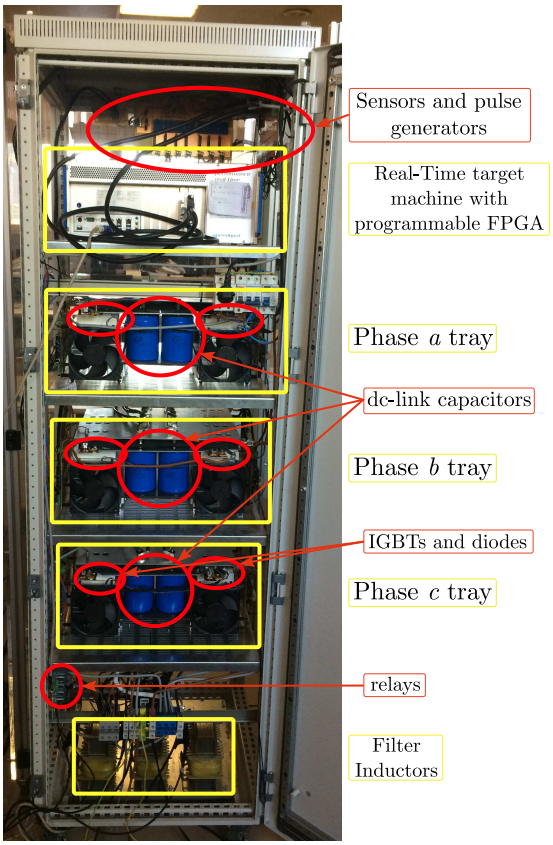

Figure 5. Experimental prototype of the three-level NPC rectifier.

Table 1. Circuit and control parameters.

Parameter	Value	Parameter	Value	Parameter	Value
ω_g	$2\pi 50$ rad/s	Sampling frequency (f_s)	10 KHz	k_i^{dc}	1
v_{sa}, v_{sb}, v_{sc}	230 V_{RMS}	Switching frequency (f_{sw})	10 KHz	k_p	5
L	2 mH	ω_c	1 rad/s	k_r	100
C	3300 µF	v_{dc}^r	700 → 800 V	k_d	0.1
R	120 → 60 → 120 Ω	k_p^{dc}	0.05	k_{di}	1×10^{-2}

In order to show the control system behavior under different conditions, several stages with different resistive load values and reference voltages have been implemented. Starting with $R = 120\,\Omega$ and $v_{dc}^r = 700$ V, a step in the load is applied to make $R = 60\,\Omega$ at t = 0.8 s, then variable v_{dc}^r is modified from 700 to 800 V progressively from t = 1.5 s to t = 2.2 s, and finally the load is changed back to 120 Ω at t = 3.8 s. During the whole experiment, the instantaneous reactive power reference (q^r) has been assumed to be zero in order to guarantee unity power factor.

Figure 6 shows a comparative of the phase currents, system power and switching states of one phase for the three approaches under analysis in this paper. Regarding balancing capabilities, the capacitor voltage evolution starting from an unbalanced condition for the three approaches is depicted in Figure 7. To provide a more accurate analysis of the phase current distortion, a harmonic decomposition of phase *a* current (the blue one depicted in the left graph of Figure 6) is plotted in Figure 8 along with its total harmonic distortion (THD) value. The three approaches achieve a proper power tracking and balancing capabilities from unbalanced conditions, although, some differences can be noted. As it can be seen, approach mVSVPWM offers a similar outcome in terms of current distortion compared to the ICM1 one whereas the ICM2 approach entails a reduction in the current distortion (see current ripple in Figure 6 and THD values in Figure 8). On the other side, the time it takes for the modulation approach to balance the capacitor from the same unbalanced condition varies

increasingly as mVSVPWM is fastest, ICM2 is in the second place and ICM1 is in last position. Despite that, the actual balancing time for ICM1 and ICM2 approaches are still acceptable for real applications. Both approaches have tunable parameters (k_d, k_{di}) that can be increased in the case the application requires a faster balancing solution at the expenses of worsening the transients because of saturation issues, resulting in a trade-off between balancing speed and transient behaviour.

In regard to the number of commutations, the main differences can be noted in the switching states of Figure 6. In this term, ICM1 yields 800 commutations—jumps from one level to another—per grid period at 10 KHz of switching frequency; ICM2 yields 532, which is two thirds of ICM1 commutations; while mVSVPWM yields 375. Therefore, ICM2 presents an improvement in terms of current distortion when compared with ICM1 and mVSVPWM whereas ICM2 presents a commutation reduction when compared only with ICM1. The discussed features are presented in Table 2.

Regarding the computational burden, the execution times for ICM1 and ICM2 (using alternative A) are respectively 67% and 61% less than the time spent for the equivalent stage by the mVSVPWM technique [13], showing the simplicity of the presented methods compared to mVSVPWM. Moreover, the generation of the IGBT gating signals is simpler in the case of ICM1 and ICM2 compared to mVSVPWM as only several comparisons with a carrier wave are required.

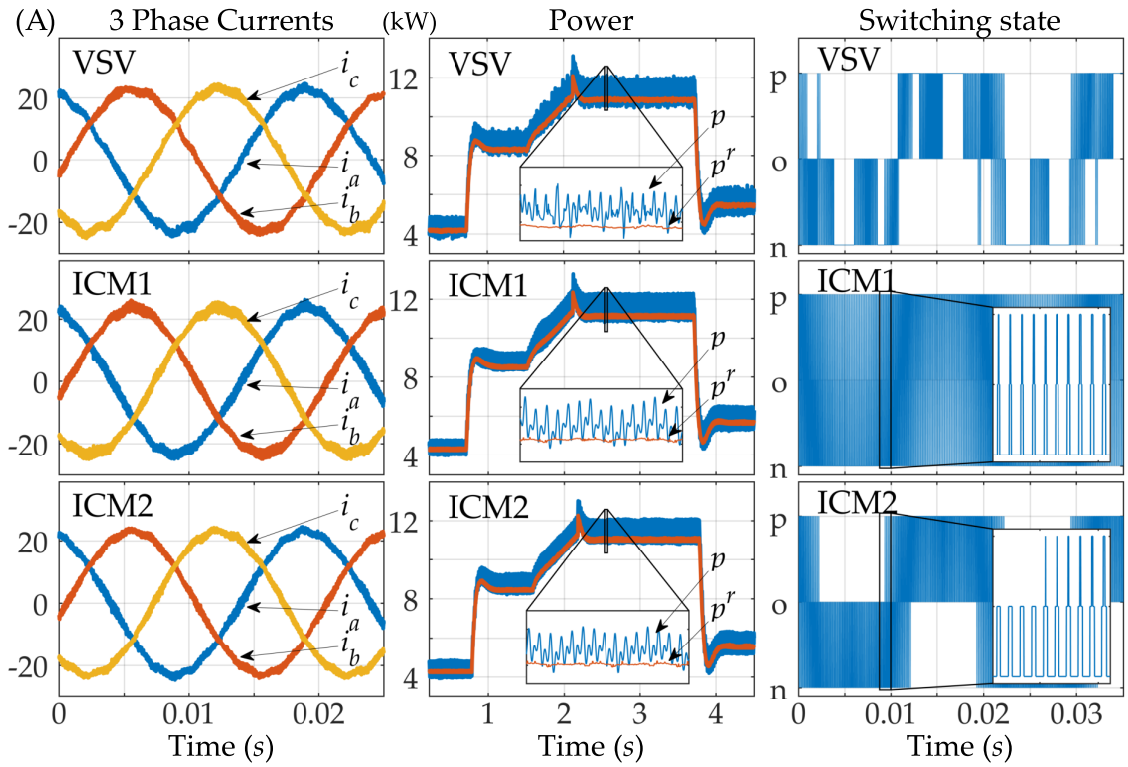

Figure 6. Experimental results: (**Left**) Phase currents at steady state with $v_{dc} = 800\,V$, $R = 60\,\Omega$ for the mVSVPWM (denoted as VSV in the figure legend), ICM1 and ICM2; (**Center**) evolution of the instantaneous power (p) and its reference (p^r) along different operating conditions for the three modulation approaches considered; (**Right**) switching states at steady state with $v_{dc} = 800\,V$, $R = 60\,\Omega$ for the three approaches.

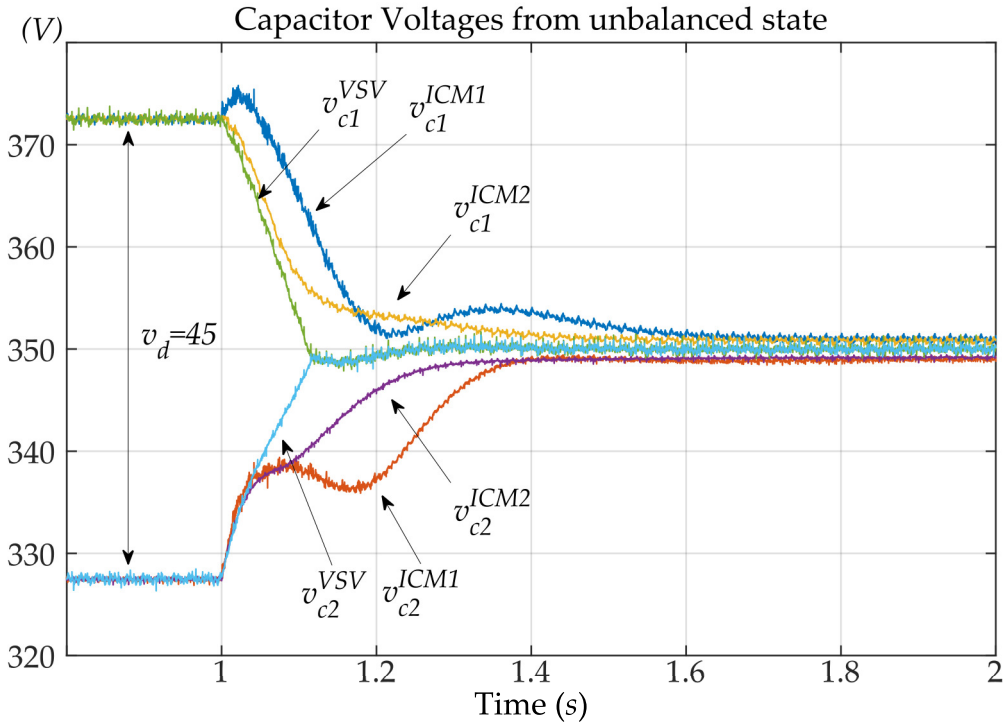

Figure 7. Experimental results: evolution of the capacitor voltages starting from an unbalanced condition, considering mVSVPWM (VSV in the figure), ICM1 and ICM2.

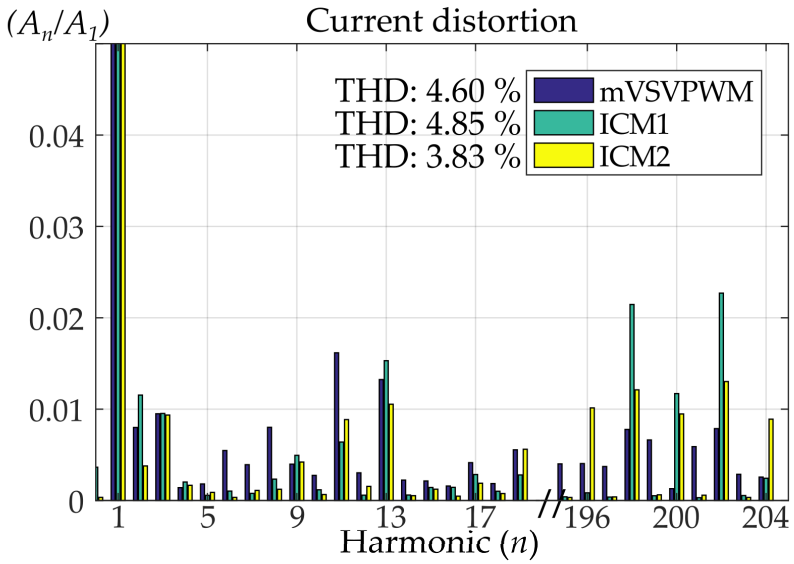

Figure 8. Experimental results: Harmonic spectrum and total harmonic distortion (THD) value of phase *a* current for the three approaches considered: mVSVPWM, ICM1 and ICM2.

Table 2. Main features of the considered approaches.

Approach	THD Value	Number of Conmutations	Balancing Time (Figure 7)	Computational Burden (% Reduction)
mVSVPWM	4.6%	375	0.12 s	–
ICM1	4.85%	800	0.50 s	67%
ICM2	3.83%	532	0.40 s	61%

6. Concluding Remarks

In this paper, the control of a three-level NPC rectifier has been addressed using a modeling approach that considers averaged duty cycle variables for the different levels in each phase. It has been shown that the associated extra degree of freedom can be used to balance the capacitor voltages. At the same time, it is shown that the design of the outer controllers (current and dc-link voltage controllers) is not affected by this approach.

In this way, the control law presented in [26] (ICM1) has been revisited and modified (ICM2) in order to reduce the main problem associated with the proposed approach: the high number of commutations and, therefore, losses. Furthermore, experiments have been made with a three-level NPC rectifier. The results obtained for the designed controllers have been quite satisfactory.

The main novelty of these two control laws is that, in spite of being based on an averaged model, control and modulation are integrated in the same stage. In this way, the controller yields directly the duty cycles for each phase in each level. Therefore, an algorithmic and computational simplification is achieved.

Experiments have been performed showing the benefits of the control laws presented in this paper and a comparison has been made with mVSVPWM [13], obtaining similar results in terms of THD for ICM1. On the other hand, the new approach ICM2 reduces the number of commutations at the same time that it reduces the high-order harmonics components, improving the THD value and the overall efficiency in comparison with ICM1. Both approaches accomplish the control objectives as they reduce the computational time of the control stage compared to mVSVPWM [13].

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Abbreviations

The following abbreviations are used in this manuscript:

NPC	Neutral Point Clamped
PWM	Pulse Width Modulation
SVM	Space Vector Modulation
CB-PWM	Carrier Based Pulse Width Modulation
DPC	Direct Power Control
ICM	Integrated Control and Modulation
ICM1	Integrated Control and Modulation variant 1
ICM2	Integrated Control and Modulation variant 2
mVSVPWM	Modified Virtual Space Vector Modulation
THD	Total Harmonic Distortion

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