A LVDS Serial AER Link

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***Abstract*— Address-Event-Representation (AER) is a communication protocol for transferring asynchronous events between VLSI chips, originally developed for bio-inspired processing systems (for example, image processing). Such systems may consist of a complicated hierarchical structure with many chips that transmit data among them in real time, while performing some processing (for example, convolutions). The event information is transferred using a high speed digital parallel bus (typically 16 bits and 20ns-40ns per event). This paper presents a testing platform for AER systems that allows to analyse a LVDS Serial AER link. The interface allows up to 0.7 Gbps (~40Mev/s, 16 bits/ev). The eye diagram ensures that the platform could support 1.2 Gbps.**

I. Introduction

Address-Event-Representation (AER) was proposed in 1991 by Sivilotti [1] for transferring the state of an array of analog time dependent values from one chip to another. It uses mixed analog and digital principles and exploits spikes for coding information. Figure 1. explains the principle behind the AER basics. The emitter chip contains an array of cells (like, for example, the pixels of a camera or an artificial retina chip) where each cell implements a continuously varying time dependent state that change with a slow time constant (in the order of *ms*). Each cell or pixel includes a local oscillator (VCO) that generates digital pulses of minimum width (a few nano-seconds). The rate of pulses is proportional to the state of the cell (or pixel intensity for a retina), assuming spike rate coding is used. Each time a pixel generates a pulse (which is called "event"), it communicates with the array periphery and a digital word representing a code or address for that pixel is placed on the external inter-chip digital bus (the AER bus). Additional handshaking lines (Acknowledge and Request) are used for completing the asynchronous communication. The inter-chip AER bus operates at the maximum possible speed. In the receiver chip the pulses are directed to the pixels whose code or address was on the bus. In this way, cells with the same address in the emitter and receiver chips are virtually connected with a stream of pulses. The receiver cell integrates the pulses and reconstructs the original low frequency continuous-time waveform. Cells that are more active access the bus more frequently than those less active.

Transmitting the cell addresses allows performing extra operations on the events while they travel from one chip to another. For example in a retina, the activity of the pixels in the array represents the input image. By translating the address of the events during transmission, the image can be shifted or rotated. This translation of the address can be achieved by inserting properly coded EEPROMs. Furthermore, the image transmitted by one chip can be received by many receiver chips in parallel, by properly handling the asynchronous communication protocol. The event-based nature of the AER protocol also allows for very efficient convolution operations within a receiver chip [2].

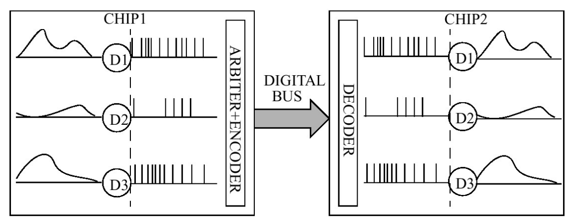

Figure 1. Rate-Coded AER inter-chip communication scheme.

There is a growing community of AER protocol users for bio-inspired applications in vision, audition systems and robot control, as demonstrated by the success in the last years of the AER group at the Neuromorphic Engineering Workshop series [3]. The goal of this community is to build large multi-chip and multi-layer hierarchically structured systems capable of performing complex massively-parallel processing in real time [4][5].

These systems are limited by the number of bits of the AER bus and the bandwidth that parallel cables supports. There are several works [7] that uses ATA100 cables.

In the following sections we present a new Serial AER (SAER) communication scheme and a platform for testing and interfacing Serial AER systems with robots. An experiment to test the SAER communications capabilities and an eye diagram are also presented.

II. LVDS SERIAL AER

Following the next-generation interconnect standards, we present a new SAER scheme, based on the use of high-speed point-to-point serial connections.

The SAER scheme emerges to overcome a number of limitations of the Parallel AER scheme. The most significant limitations are the difficulty in increasing the data rate beyond 100 Mbytes/s (50Mev/s) and the fact that ATA100 cable uses a single-ended signaling system that is prone to induced noise. A signaling at gigabit speeds requires differential signaling. We have chosen a serial wire that uses the Low Voltage Differential Signaling (LVDS) standard, TIA/EIA-644-A-2001[8]. LVDS is designed for high-speed, low-power, and low-noise point-to-point communications. LVDS radiates less noise than single-ended signals due to the canceling of magnetic fields, and is more immune to noise because it is coupled onto the two wires as a common-mode signal.

On the other hand, SAER uses only 4 signal pins, improving pin efficiency over the Parallel AER interface which uses more than 18 signal pins going between devices.

So, this new point-to-point connection (SAER) provides greater dedicated bandwidth and smaller connectors.

Furthermore, SAER increases the flexibility and the scalability. Parallel AER is limited in scalability because of an increment of the number of neurons within a system requires an increment of the number of wires in parallel bus. Increasing bus width reduces the maximum achievable frequency due to skew between signals. More signals also requires more pins on a device, traces on boards and larger connectors.

SAER saves a significant large amount of space and does not limit on the physical length of the wire.

In addition, LVDS serializers and deserializers also contribute significant space and cost savings to designs. To transmit the parallel data, Address Event, as a serial data stream, it is necessary a parallel-to-serial conversion at the emitter chip, and a corresponding serial-to-parallel conversion at the receiver chip. The MAX9205 LVDS serialiser [9] and the MAX9206 LVDS deserialiser [10] are used, in our design, to convert 11 TTL lines (10 data + 1 clock) into one high-speed LVDS pair. The MAX9205 serializer converts 10bit wide parallel LVTTL/LVCMOS data into an LVDS serial data stream. A high-state start bit and a low-state stop bit are added internally and frame the 10bit parallel input data and ensure a transition in the serial data stream. Therefore, 12 serial bits are transmitted for each of the 10bit parallel input bits. The MAX9205 accepts a wide 16-40MHz reference clock to produce a serial data rate from 192Mbps (12bits x 16MHz) to 480Mbps (12 bits x 40MHz). However, since only 10 bits are from input data, the actual throughput is 10 times the reference clock frequency. The MAX9206 deserializer receives the serial output from the MAX9205 and converts it back to 10bit-wide parallel data. Because the deserializer recovers both clock and data from the serial data stream, clock-to-data and data-to-data skew, that would be present with a parallel bus, are eliminated.

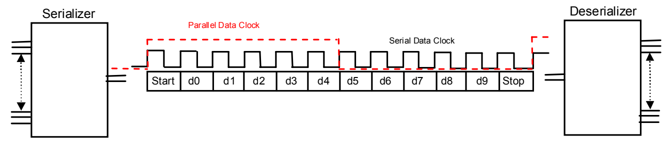

Figure 2. Clock embedded into serializer output.

In the previous Parallel AER scheme, an asynchronous communication, data is sent without a timing clock using a handshake protocol. This involves two additional lines and additional delay for control signals manipulation at the VHDL level (hard to get 100mev/s with 100Mhz clock). However, our SAER scheme, a synchronous communication, data is sent with a timing clock, Figure 2. This allows to eliminate the acknowledgment signal. In the handshake protocol, it is necessary to wait for acknowledgment before sending the next events. This could imply a delay in the next events. In Address-Event-Representation are important both data (Address) and the time when this data appears on the bus (Event). So, the handshake protocol could generate errors in the timing information of the events. It is true that SAER scheme could generate events leak. But this error is not as important as receiving data without correct timing information.

In the biological neural communications do not exist any confirmation mechanism. Neurons send pulses to next layer and do not mind about if the pulses are received or not.

So, for these reasons, Serial synchronous AER scheme is more similar to biological neural communication and AER philosophy than Parallel handshake AER scheme.

III. AER TESTING PLATFORM

This section describes in detail the AER platform called AER-Robot. This new interface is an improved version of a prototype designed to control an anthropomorphic AER hand [6]. This platform has been designed around a Spartan 3 400 FPGA with 4 parallel AER connectors (2 input and 2 output), 4 power stages to manage 4 DC motors with two encoder channels and 4 hall effect current sensor to measure the power consumption of the motors. The interface also has 12 analog sensor inputs and 36 general purpose digital ports.

With this FPGA, the interface is able to receive high speed Address Event rates, process them together with robot sensors and encoders and give orders to the motors of the robot.

This interface has been developed to communicate AER systems with robots using two AER buses: one for incoming events and another for outgoing information (events) about the state of the motors and the sensors. The input AER bus could be replicated into the output AER bus, called AER IN pt, to allow a chain connection of several boards. There is another input AER bus, called AER OUT pt, that is arbitrated with the AER output of the FPGA before sending events to the AER system (through AER OUT port). This configuration allows connecting several AER-Robot boards into a chain to the AER system or inserting the board in between an AER communication. Figure 3. shows the block diagram of the AER-Robot platform.

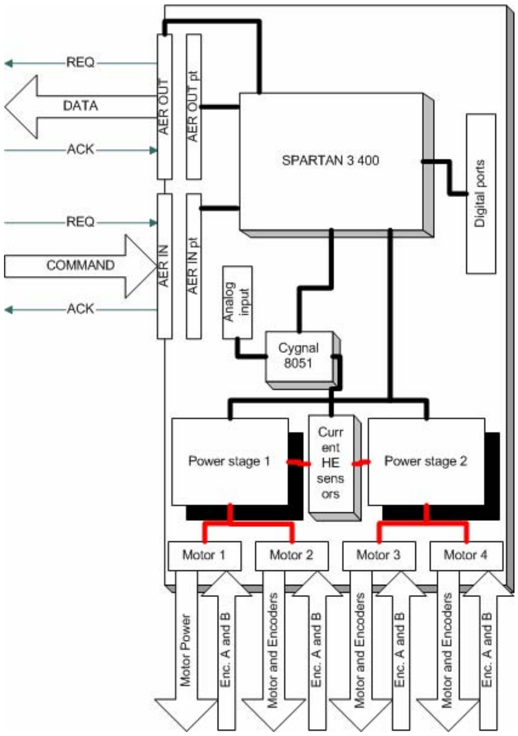

Figure 3. Block diagram of the AER-Robot platform.

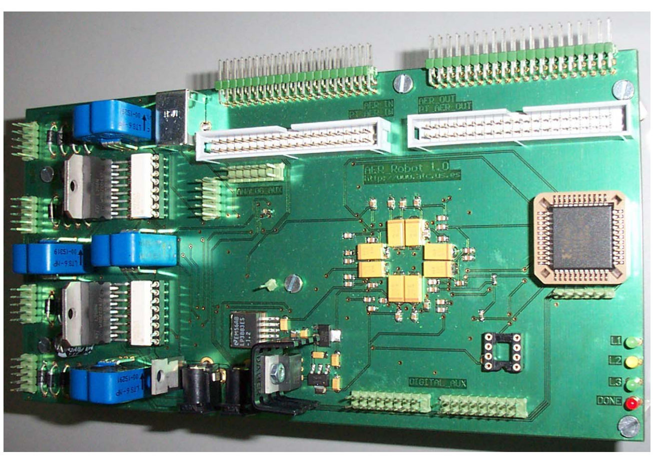

Figure 4. AER-Robot board photograph.

Figure 4. shows a photograph of the AER-Robot Interface PCB. The digital part of the PCB is in the middle. The board has a Cygnal 80C51F320 microcontroller for the analog to digital conversion (200Ksamples/second and 10-bits) of the sensor measurements and 1 USB port for the PC connectivity.

An external plug-in, based on the MAX9205 LVDS serializer, can be connected to an output AER port for the parallel-to-serial conversion. In the same way, another external plug-in, based on the MAX9206 LVDS deserializer, can be connected to an input AER port for the serial-to-parallel conversion.

IV. Experiment

We propose a simple experiment to probe that the SAER is possible and it has a lot of possibilities from the point of view of speed, scalability, and easier to implement. This experiment consists on programming a simple VHDL code, for the Spartan 3 400 FPGA of the AER-Robot platform, for testing the maximum speed supported by this slow version of the MAXIM LVDS serializer and deserializer transceivers. The VHDL code describes a simple state machine that generates continuously 10-bit word to transmit them through the external serializer plug-in board. The external serializer can work with a clock frequency of up to 66 MHz. We have used a 25MHz clock. The serial output of the plug-in board, a LVDS signal, is sent using a 30cm SATA cable connected to another plug-in board with a deserializer MAXIM interface. This second plug-in is connected to the AER IN connector of the AER-Robot interface. The VHDL code is receiving the 10 bits data continuously and is comparing the transmitted word with the received one. Figure 5. shows the experiment block diagram.

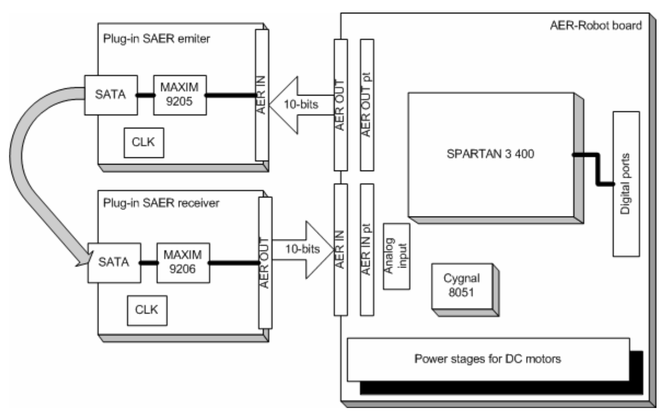

Figure 5. SAER link experiment block diagram

These two MAXIM chips transmit both data and clock into the same differential signal.

Figure 6. shows the oscilloscope LVDS signal and the clock extracted by the oscilloscope. The transmission works at 300 Mbps.

Figure 7. and Table 1 show the eye diagram and its parameters of the differential pair when the experiment is running. It can be seen that for this cable length (30 cm) the speed transmission can be almost three times higher.

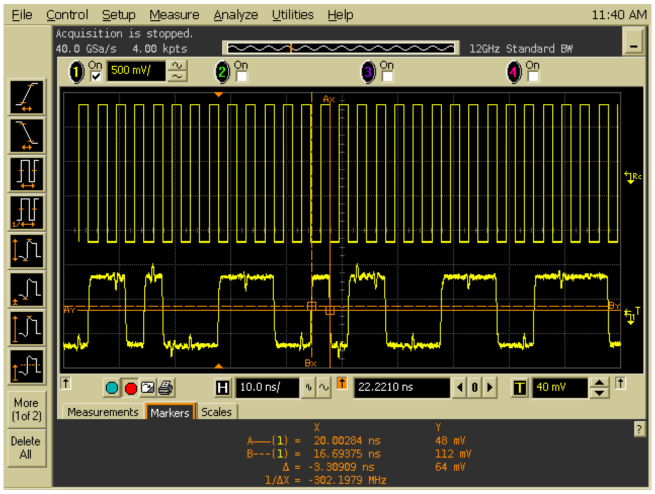

Figure 6. SAER link oscilloscope with clock extraction.

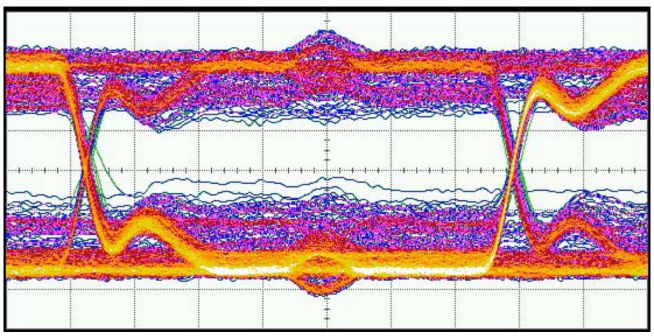

Figure 7. SAER link eye diagram.

Parameter	Value
Total Jitter	150 ps
Marginal Jitter	720 ps
Symbol duration	3,3 ns
Bit rate	302 Mbps
Reference clock	25 MHz
Event rate (16-bits)	15 Mev/sec

Table 1. SAER link eye diagram parameters.

V. CONCLUSIONS

This paper presents a Serial Address-Event-Representation (SAER) synchronous proposal for high speed inter-chip neuro-inspired communications. A simple serializer and deserializer plug-in boards, based on MAXIM chips, are presented to convert a conventional parallel AER bus into serial and vice-versa.

An AER testing platform is also presented and used to test the LVDS transmission characteristics through SATA cable. The eye diagram ensures that the communication could work up to four times higher, what implies 1.2Gbps. If you suppose 2 bits for command and 8 for x or y event information for this 10-bit MAXIM interface, you will need two 10-bit word to transmit an AER 16-bit word. Therefore, the SAER bandwidth could be up to 60Mev/sec. A new and faster version of the MAXIM is needed to test the 1.2Gbps and to get an shorter eye diagram.

The future work is focussed on characterize the LVDS signal parameters for different cable lengths and higher bandwidths using faster reference clocks (60MHz). We will characterize also the BER and power consumption for the different versions.

ACKNOWLEDGMENTS

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REFERENCES

[1] M. Sivilotti, Wiring Considerations in analog VLSI Systems with Application to Field-Programmable Networks, Ph.D. Thesis, California Institute of Technology, Pasadena CA, 1991.

[2] Teresa Serrano-Gotarredona, Andreas G. Andreou, Bernabé Linares-Barranco. "AER Image Filtering Architecture for Vision-Processing Systems". IEEE Transactions on Circuits and Systems. Fundamental Theory and Applications, Vol. 46, N0. 9, September 1999.

[3] A. Cohen, R. Douglas, C. Koch, T. Sejnowski, S. Shamma, T. Horiuchi, and G. Indiveri, *Report to the National Science Foundation: Workshop on Neuromorphic Engineering*, Telluride, Colorado, USA, June-July 2004. [www.ini.unizh.ch/telluride]

[4] Kwabena A. Boahen. "Communicating Neuronal Ensembles between Neuromorphic Chips". Neuromorphic Systems. Kluwer Academic Publishers, Boston 1998.

[5] Misha Mahowald. VLSI Analogs of Neuronal Visual Processing: A Synthesis of Form and Function. PhD. Thesis, California Institute of Technology Pasadena, California, 1992.

[6] A. Linares-Barranco, R. Paz-Vicente, G. Jimenez, J.L. Pedreño-Molina, J. Molina-Vilaplana, J.L. Coronado. "AER Neuro-Inspired interface to Anthropomorphic Robotic Hand". IEEE World Conference on Computational Intelligence. International Join Conference on Cellular Neural Networks. Vancouver, July-2006.

[7] R. Serrano-Gotarredona, M. Oster, P.. Lichtsteiner, A. Linares-Barranco, R. Paz, F. Gomez-Rodriguez, H. Kolle Riis, T. Delbrück, S.C. Liu, S. Zahnd, A.M. Whatley, R. Douglas, P. Häfliger, G. Jimenez, A. Civit, T. Serrano-Gotarredona, A. Acosta, B. Linares-Barranco. AER Building Blocks for Multi-Layer Multi-Chip Neuromorphic Vision Systems. Accepted at NIPS 2005. Vancouver.

[8] ANSI/TIA/EIA-644-A Telecommunications Industry Association, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS)", 2001.

[9] MAXIM 10-bit Bus LVDS Serializers. Rev 0;5/01. http://para.maxim-ic.com

[10] MAXIM 10-bit Bus LVDS Deserializers. Rev 0;8/01. http://para.maxim-ic.com