A 14-bit 4-MS/s Multi-bit Cascade ΣΔ Modulator in CMOS 0.35-μm Digital Technology

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Abstract

This paper presents a 4th-order 3-stage cascade ΣΔ modulator that achieves 14-bit dynamic range at 4MS/s using low oversampling ratio. It includes a programmable multi-bit quantizer in the last stage, providing 2-, 3-, or 4-bit internal resolution. The modulator is implemented with fully-differential switched capacitor circuits in a CMOS 0.35-μm digital technology. The estimated power consumption is 78mW, from a 3.3-V supply.

1. Introduction

Cascade ΣΔ modulators (ΣΔMs) are being successfully employed for high-speed, high-resolution A/D conversion in xDSL applications [1]-[4]. These architectures perform a high-order filtering by cascading low-order (1st- and 2nd-) ΣΔMs to guarantee unconditional stability. Moreover, the use of multi-bit quantization at the last stage of the cascade reduces the oversampling ratio required for a given modulator resolution. These modulators also exhibit low sensitivity to the DAC non-linearities [5], so that neither correction nor calibration are required. This makes cascade multi-bit ΣΔMs good candidates to achieve high performance with a reduced power consumption.

This paper presents the design of a ΣΔM using a 4th-order 3-stage cascade multi-bit architecture – the 2-1^2*mb* modulator [1] shown in Fig.1. A detailed discussion on the benefits of the selected topology, as well as on the selection of integrator weights (summarized in Table 1) can be found in [6] [7].

The modulator presented here can operate with different oversampling ratio M and last-stage quantizer resolution B:

- $M = 12$, $B = 4$ and $M = 16$, $B = 2$, providing 13bit@4MS/s,
- $M = 16$, $B = 3$, providing 14bit@2MS/s, and
- $M = 16$, $B = 4$, achieving 14bit@4MS/s.

These M, B alternatives have been implemented together including programmability in the last-stage quantizer, whose resolution can be set to 2, 3, or 4bit. Such performance places this modulator in the state-of-the-art on high-resolution, high-speed ΣΔMs [1]-[5], especially considering its implementation in a CMOS digital process, unlike the former ones.

The paper is organized as follows. Section 2 covers the synthesis of the 2-1^2*mb* modulator. Sections 3 to 7 describe the design of the modulator building blocks. Finally, Section 8 is dedicated to layout and prototyping considerations.

2. Modulator Sizing

The evaluation of the circuit requirements for the 2-1^2*mb* ΣΔM has been done using SDOPT [8], a sizing tool for SC ΣΔMs. This tool combines accurate analytical expressions for each error contribution degrading the modulator performance and statistical optimization, which allows us to find optimized, non-oversized specifications for the building blocks. Table 2 summarizes the circuit requirements providing 14bit@4MS/s. Most significant error contributions are also shown. Note that quantization noise is the main in-band error source (-85dB). This includes the effect of integrator leakage and weights mismatch. Both non-idealities cause incomplete cancellation of the quantization error in the first and second stages [8], which may degrade the modulator performance. According to SDOPT results, this limits the minimum amplifier DC-gain to 68dB and the maximum standard deviation in capacitors to 0.12%.

The unitary capacitor value (0.5pF) is set according to thermal noise and dynamic considerations. Both error powers are well below the limit imposed by the modulator resolution.

The requirements in Table 2 for the integrator and the

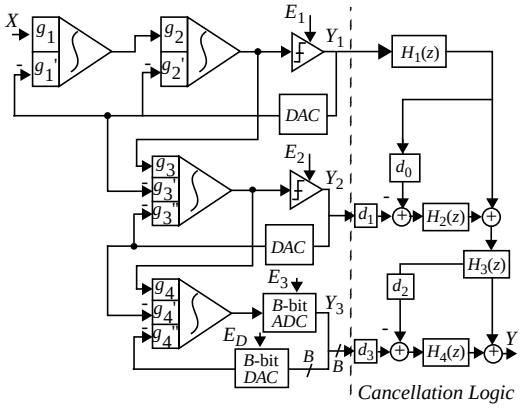

Fig. 1: Block diagram of the 2-1^2*mb* ΣΔM.

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Table 1: Integrator weights for the 2-1^2*mb* ΣΔM.

g_1	0.25	g_3	1	g_4	2
g_1'	0.25	g_3'	0.5	g_4'	1
g_2	1	g_3''	0.5	g_4''	1
g_2'	0.5				

Table 2: Modulator sizing results.

SPECS: 14bit@4MS/s@1.1V$_p$		2-1^2*mb*
Modulator	Oversampling ratio	16
	Sampling frequency	64MHz
	Reference voltages	±2V
Integrators	Sampling capacitor	0.5pF
	Unitary capacitor	0.5pF
	Sigma	0.12%
	Capacitor non-linearity ≤	25ppm/V
	Bottom parasitic capacitor	20%
	Switch ON-resistance ≤	250Ω
Opamps	DC-gain	68dB
	DC-gain non-linearity ≤	20%V^{-2}
	Transconductance ≥	2.5mA/V
	Maximum output current ≥	±0.95mA
	Output swing ≥	±2V
Comparators	Hysteresis ≤	30mV
A/D/A Converter	Resolution	4bit
	Non-linearity (*INL*) ≤	0.4%FS
Dynamic range		87.2dB 14.2bit
Quantization noise		-85.0dB
Thermal noise		-94.8dB
Incomplete settling noise		-96.9dB
Harmonic distortion		-99.4dB

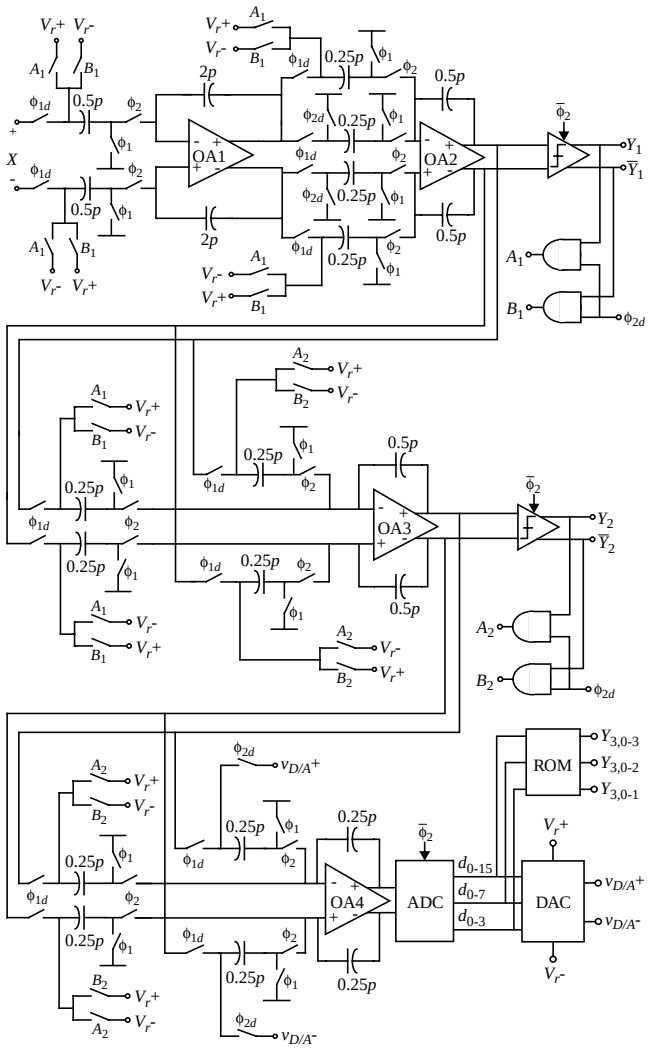


Fig. 2: SC implementation of the 2-1^2*mb* ΣΔM.

amplifier apply only to the first integrator in the cascade. However, some specifications, as amplifier DC-gain, transconductance and output current, can be relaxed for the second, third, and fourth integrator, because their in-band error power contributions are attenuated by increasing powers of *M*. The same applies for thermal noise, which allows reduction of the unitary capacitor to 0.25pF for these integrators.

Fig.2 shows the fully-differential SC implementation of the 2-1^2*mb* ΣΔM. The first stage is formed by two SC integrators, with one and two input branches, respectively. A single-bit quantizer (comparator) at the end of the first stage, together with two AND gates, provides the feedback signals A_1,B_1 to switch the integrator sampling capacitors to either V_r+ = +1V or V_r- = -1V. Since the circuit is fully differential, the resulting reference voltages are ±2V. The second stage has a two-branch integrator. Although three different weights are needed in this integrator – g_3, g_3', and g_3'' – weight in Table 1 allows splitting of g_3 between the two branches. The same applies for weight g_4 in the fourth integrator. This integrator drives the programmable ADC and the third-stage loop is closed through the DAC. The 1-of-16 output code of the ADC (alternatively 1-of-8 if $B = 3$ or 1-of-4 if $B = 2$) is converted to binary code using a ROM memory, providing outputs $Y_{3,0\text{-}3}$ ($Y_{3,0\text{-}2}$ if $B = 3$ or $Y_{3,0\text{-}1}$ if $B = 2$).

The modulator is controlled by two non-overlapped clock-phases. The integrator input signals are sampled during phase ϕ_1 and the algebraic operations are performed during ϕ_2. The comparators and the ADC are activated at the end of ϕ_2 – using $\overline{\phi}_2$ as strobe – to avoid any possible interference from the integrator outputs in the beginning of ϕ_1. This timing guarantees a single delay per clock-cycle. In order to attenuate the signal-dependent clock-feedthrough, delayed versions of the phases, ϕ_{1d} and ϕ_{2d}, are also provided.

The modulator has been extensively evaluated in ASIDES [8], a behavioural simulation tool for ΣΔMs. Simulations have been carried out including the non-idealities derived from the final implementation of the building blocks. Fig.3*(a)* shows the signal-to-(noise+distortion)-ratio *SNDR* of the modula-

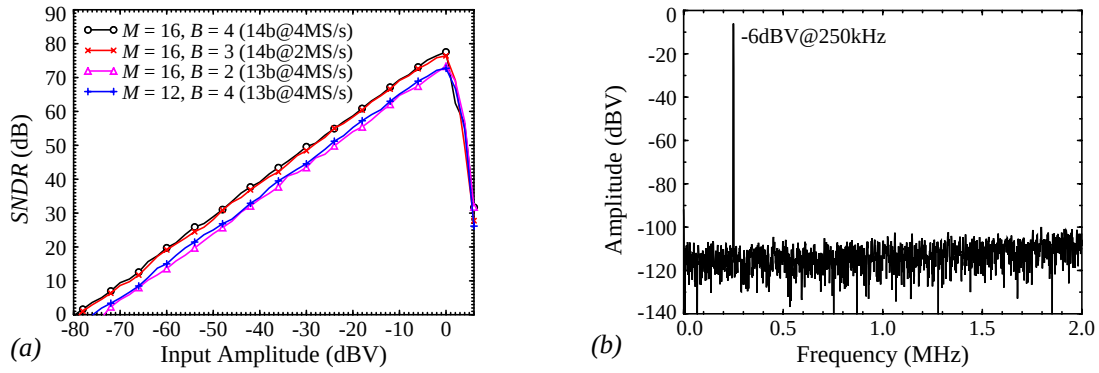


Fig. 3: 2-1^2*mb* ΣΔM: *(a) SNDR* curves for different *M*,*B* pairs, *(b)* Output spectrum operating with $M = 16$ and $B = 4$.

tor as a function of the input level, when operating with $M = 16$ and $B = 4$. The additional operation modes are also depicted. The modulator achieves a dynamic range *DR* of 85.5dB with $M = 16$, $B = 4$ and $M = 16$, $B = 3$. *DR* is 80.5dB with $M = 16$, $B = 2$ and $M = 12$, $B = 4$. Fig.3*(b)* shows its output spectrum for a -6dBV@250kHz input tone, operating with $M = 16$ and $B = 4$.

3. Amplifiers

According to the results in Table 2, the amplifier design should concentrate in the following aspects:

- *Required output swing*, which must be feasible in a 3.3-V implementation. The output swing requirement strongly depends on the value of integrator weights selected for the ΣΔM [8]. With the weights in Table 1, the integrator output swing demands are reduced to only the reference voltages – i.e., ±2V –, so that they do not become tight for a fully-differential amplifier with 3.3-V supply.
- *Open-loop DC-gain*: Although the SDOPT result for the DC-gain is 68dB, simulations with ASIDES show that this can be relaxed for amplifiers in the second (OA2), third (OA3), and fourth (OA4) integrator down to 62dB, 54dB, and 54dB, respectively.
- *Dynamics*, which critically depend on the equivalent capacitive load of the amplifier C_{eq} and is rather different for each integrator. C_{eq} also changes from the sampling phase to the integration phase. They can be calculated as [9]:

$$C_{eq,\phi_1} = C_p + (C_l + C_{n,\phi_1})\left(1 + \frac{C_p}{C_o}\right)$$
$$C_{eq,\phi_2} = C_i + C_p + (C_l + C_{n,\phi_2})\left(1 + \frac{C_i + C_p}{C_o}\right) \quad (1)$$

where C_i and C_o are the sampling and feedback capacitors of the integrator, respectively, C_p and C_l refer to the parasitics at the amplifier input and output nodes,

Table 3: Basic amplifier requirements.

	DC-gain	C_{eq,ϕ_1}	C_{eq,ϕ_2}	DC-gain	Driving Capabilities
OA1	68dB	1.49pF	1.51pF	*high*	*medium*
OA2	62dB	1.24pF	1.32pF	*medium*	*medium*
OA3	54dB	1.24pF	1.32pF	*low*	*medium*
OA4	54dB	0.56pF	4.89pF	*low*	*high*

Table 4: Simulation results for the amplifiers.

	OA1	OA2	OA3	OA4
DC-gain	80.0dB	62.8dB	55.7dB	62dB
GB	250MHz	311MHz	261MHz	167MHz
PM	67° (1.6pF)	65° (1.4pF)	71° (1.4pF)	79° (4.5pF)
Output swing	±2.5V	±3.1V	±2.9V	±3.1V
Transconductance	9.6A/V	4.2mA/V	2.6mA/V	5.4mA/V
Max. output current	±40mA	±0.57mA	±0.45mA	±0.84mA
Power consumption	38.5mW	4.5mW	4.0mW	6.6mW

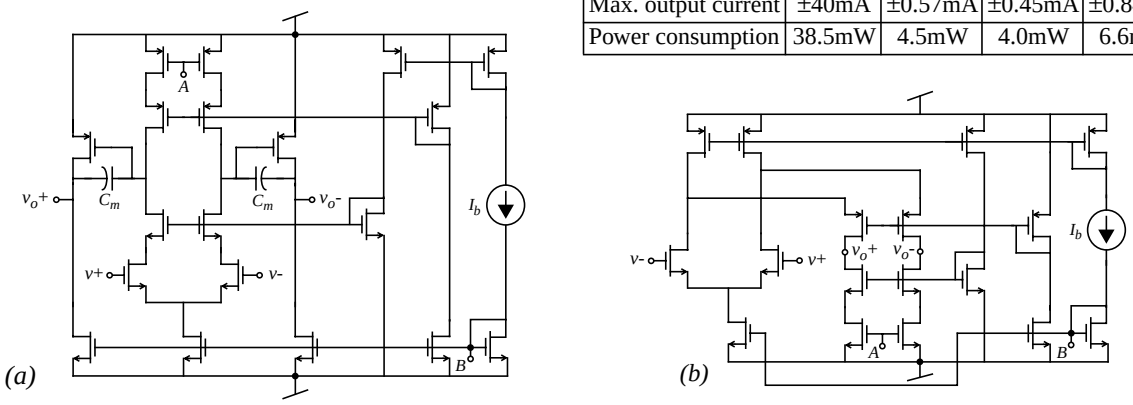


Fig. 4: Schematics of the amplifiers: *(a)* Two-stage amplifier, *(b)* Folded-cascode OTA.

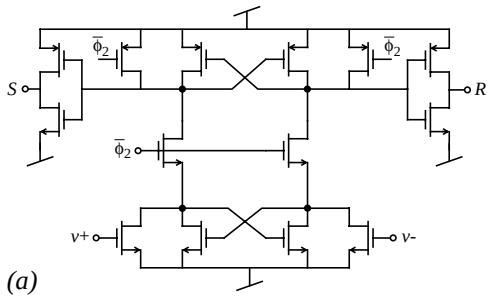


Fig. 5: Comparator: *(a)* Regenerative latch, *(b)* RS flip-flop.

Table 5: Simulation results for the comparators.

Hysteresis	<10mV
TPLH	2.5ns
TPHL	2.3ns
Power consumption	0.65mW

C_{n,ϕ_1} stands for the sampling capacitors of the next integrator in the cascade, and C_{n,ϕ_2} refers to capacitors in the ADC for the fourth amplifier.

Table 3 shows the equivalent loads for the four amplifiers, as well as their DC-gain requirements. Note that C_{eq} is similar for the first three ones during both clock-phases, but becomes considerably larger for OA4 during ϕ_2, since it must drive the ADC. The diversity of specifications for the amplifiers recommends a dedicated design for each of them to avoid over-sizing and optimize the power consumption.

A two-stage architecture, shown in Fig.4*(a)*, was selected for OA1 in order to fulfil its DC-gain requirement. It uses a telescopic first stage and Miller compensation. A single-stage folded-cascode OTA, shown in Fig.4*(b)*, has been used in OA2, OA3, and OA4 – enough to accomplish their medium-, low-DC-gain requirements. Although these amplifiers use the same structure, different sizings have been obtained for each of them, in order to fulfil their specifications with a reduced power consumption. The common-mode feedback net (not shown) is of dynamic type for all amplifiers, because it yields smaller power consumption than static ones for high-frequency operation.

The main features of the four amplifiers are summarized in Table 4. Note OA1 and OA4 DC-gains are larger than required. Nevertheless, further re-fining of the sizing of these amplifiers did not imply significant reduction of their power consumption.

4. Comparators

Comparators at the end of the first and second stages of the ΣΔM demand a low resolution time, while hysteresis as large as 30mV can be tolerated. The same applies for comparators in the last-stage flash ADC. This recommends the use a dynamic comparator based on a regenerative latch, with no need of a pre-amplifying stage. Fig.5 shows the schematic of comparators, widely used in ΣΔM design. The main features of the comparator are shown in Table 5.

5. Switches

Due to the high-speed operation of the ΣΔM, finite switch ON-resistance R_{on} is mainly constricted by dynamic considerations. The influence of R_{on} in the incomplete charge transferring in combination with the finite opamp dynamics must be carefully evaluated, because it leads to a further degradation of the integrator response. Fig.6 shows the effect of R_{on} on the first integrator output voltage during a clock-cycle. Note that, as R_{on} increases, charge-transfer at the beginning of the phases is no more instantaneous and the integrator dynamic is slowed down. Nevertheless, R_{on} in the range of 250Ω - 300Ω can be tolerated, with a minor degradation of the modulator performance. This value is not too demanding for a CMOS transfer gate in the intended technology – operating with a 3.3-V supply –, so that clock-boosting stages or similar techniques can be avoided [10]. CMOS switches, with aspect of 8/0.35 for the NMOS transistor and 29.5/0.35 for the PMOS, have been used.

6. Capacitors

Capacitor ratios giving the integrator weights in the ΣΔM have been implemented using unitary capacitors. The value of the unitary is selected according to matching and thermal noise requirements. As formerly stated, this results in a 0.5-pF unitary capacitor for the first integrator and 0.25-pF unitary capacitors for the second, third, and fourth integrator.

Besides this, the set of integrator weights in Table 1 has the advantage of requiring only two-branch integrators. This makes the total number of unitaries to be only 16 – smaller than in other cascade ΣΔMs: 29 capacitors in [2] and [3], and 44 in [4].

Unitary capacitors have been implemented with a multi-metal sandwich structure, using the five metal layers available in the intended technology. The

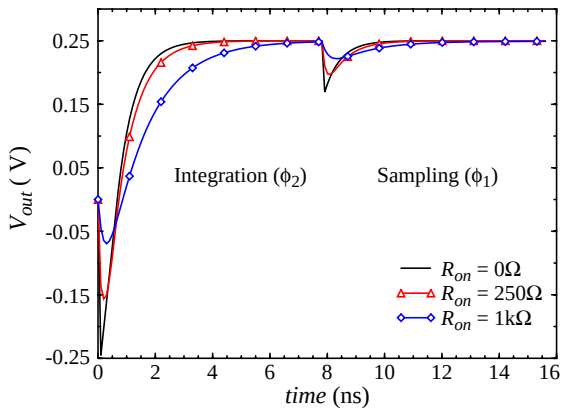


Fig. 6: Evolution of the first integrator output.

0.5-pF unitary capacitor is 52x52μm^2 size and the 0.25-pF unitary is 36x36μm^2. The bottom-plate parasitic capacitor, especially important for evaluating the amplifier dynamic requirements, is around 20% - 25% of the nominal capacitance.

7. Programmable A/D/A Converter

The different *M*, *B* alternatives have been implemented by means of a selectable-resolution A/D/A converter, capable of 2bit-, 3bit-, or 4bit-quantization. Its SC implementation, depicted in Fig.7, corresponds to that of a 4bit fully-differential flash converter with an adaptable output code driving the DAC input.

The latter consists of a simple resistor string of 30 unitaries (R = 50Ω) connected between the reference voltages V_r+ = +1V and V_r- = -1V. The value selected for R ensures that settling errors in the voltage references transferred to the ADC during phase ϕ_1 and in the input capacitors of the fourth integrator during phase ϕ_2 are low enough. Resistors have been implemented using unsalicided *p*+ poly.

The ADC uses 0.25-pF multi-metal sandwich capacitors and CMOS switches identical to that used in the SC integrators. The timing scheme of the switches has been adapted to reduce the capacitive load of the fourth integrator, driving the ADC. Nevertheless, it suffers from input-dependent feedthrough from switches controlled by ϕ_2. This problem has been overcame by making these switches considerably smaller (1/0.35 for both NMOS and PMOS transistors), without degrading the ADC performance.

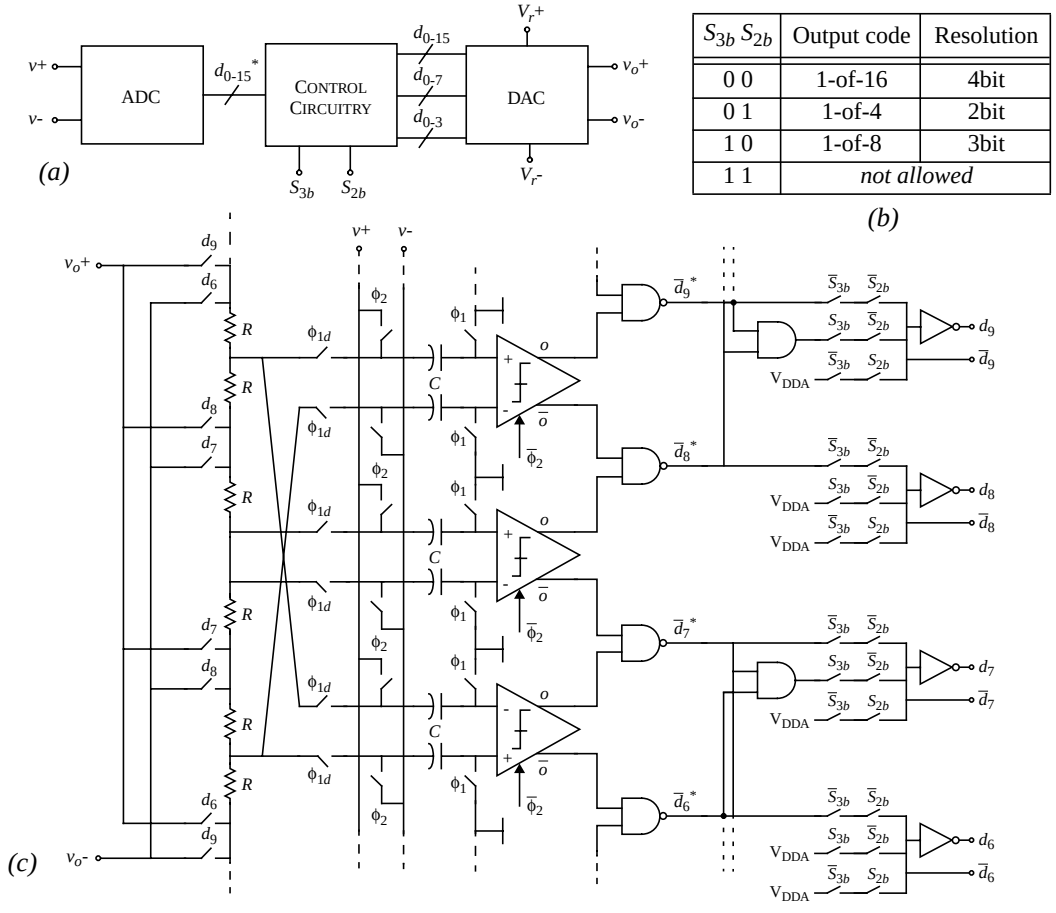
The 4bit ADC output is digitally combined, as illustrated in Fig.7, to provide 2bit-, 3bit-, or 4bit-resolution. The resolution selection is done by input signals S_{2b} and S_{3b}, as shown in Fig.7*(b)*.

The functionality of this circuitry, shown in Fig.8, basically consists in the OR operation of the appropriate digital outputs $d_{0\text{-}15}{}^*$ of the 4bit ADC in order to accommodate them to a 1-of-4 or 1-of-8 code. Note in Fig.8*(a)* that, since $(2^4\text{-}1)/(2^2\text{-}1) = 5$ is an integer, the 4bit-to-2bit conversion leads to a regular 2bit A/D/A converter with full-scale range $FS = \pm 2\text{V}$. For the 4bit-to-3bit conversion, since $(2^4\text{-}1)/(2^3\text{-}1) = 2.14$ is not an integer, a 3bit A/D/A converter with $FS = \pm 1.87\text{V}$ and an offset error of 133mV (0.25LSB) is obtained. Nevertheless, cascade multi-bit ΣΔMs present very low sensitivity to offset errors in the DAC [8], so that the overall modulator performance is not degraded.

8. Layout and Prototyping

For the layout of the 2-1^2*mb* ΣΔM, in Fig.9, the following considerations were taken into account:

• Centroid techniques with unitary transistors have



S_{3b} S_{2b}	Output code	Resolution
0 0	1-of-16	4bit
0 1	1-of-4	2bit
1 0	1-of-8	3bit
1 1	*not allowed*	

Fig. 7: A/D/A converter: *(a)* Block diagram, *(b)* Resolution selection, *(c)* Partial view of the SC implementation.

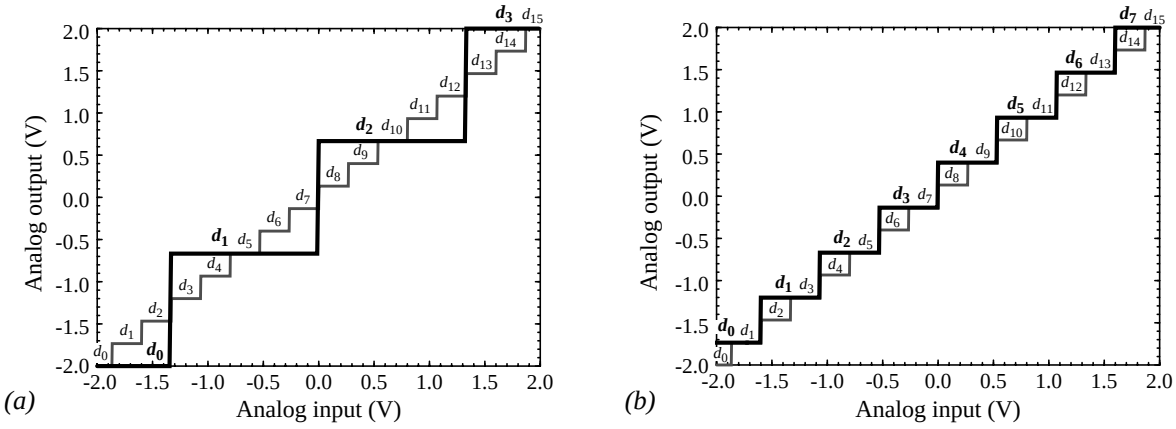


Fig. 8: Programmable A/D/A converter: *(a)* 4bit-to-2bit conversion, *(b)* 4bit-to-3bit conversion.

been employed for matched transistors in the amplifiers and in the regenerative latches.

• Separate analog and digital power supplies have been used. Analog supplies (V_{DDA}, V_{SSA}) have been employed for the voltage biasing of the substrate and the well rings and for the current biasing of the analog blocks. Separated routing lanes have been assigned for that purpose. Digital supplies (V_{DDD}, V_{SSD}) have been used for the biasing of internal digital blocks.

• In order to reduce the digital switching noise, digital supplies will eventually be reduced during testing. To enable this without affecting the modulator performance, the output stages of digital blocks driving analog parts have been biased with the analog supplies.

• Powerful digital buffers have been designed for the high-speed digital outputs (Y_1, Y_2, $Y_{3,0\text{-}3}$) of the ΣΔM. Dedicated power supplies (V_{DDD2}, V_{SSD2}) have been used for them, in order not to affect the performance of the remaining digital circuitry.

The complete modulator occupies an area of 1.32mm^2 without pads (4.30mm^2 pads included). The modulator power consumption – estimated through electrical simulation – is 78.3mW: 60.2mW for the analog blocks, 4.5mW for the digital part, and 13.6mW for the output drivers.

The circuit is being processed by the silicon foundry and experimental results are expected to be available for the presentation at the Conference.

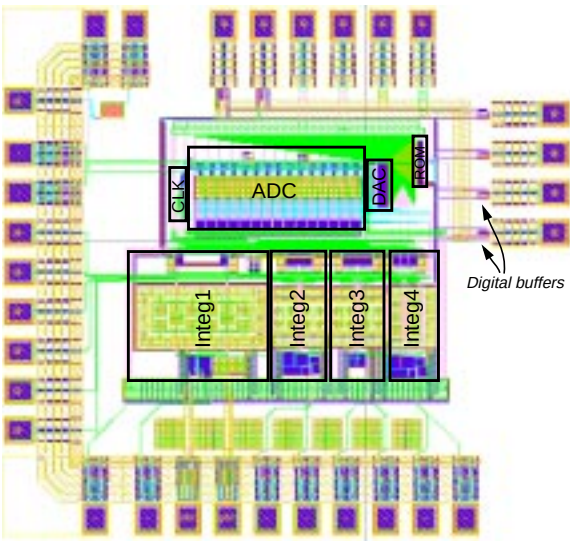


Fig. 9: Layout of the 2-1^2*mb* ΣΔM.

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