A New Reconfigurable Cascade ΣΔ Modulator Architecture with Inter-Stage Resonation and no Digital Cancellation Logic

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***Abstract* – This paper presents a new two-stage cascade ΣΔ modulator architecture that uses inter-stage resonation to increase its effective resolution as compared to conventional cascades and avoids the need for digital filtering in the error cancellation logic. The combination of these two strategies, together with the use of unity signal transfer function in all stages, make the presented modulator highly tolerant to noise leakages, very robust to non-linearities and mismatches of the loop-filter circuitry, and especially suited for low-voltage implementations at low oversampling ratios. In addition, the use of loop filters based on Forward-Euler integrators, instead of Backward-Euler integrators, simplifies the switched-capacitor implementation of the resonation and makes the presented architecture very suited for reconfigurable multi-standard applications. Besides, several practical details about the implementation of the modulator are given throughout the paper. As an illustration, a Beyond-3G case study is shown to demonstrate the benefits of the presented approach.** †1

I. INTRODUCTION

Beyond-3G wireless telecom systems require efficient CMOS multi-standard transceivers capable to operate over different co-existing standards, signal conditions and battery status, while minimizing their power consumption [1]. One of the most challenging parts in these systems is the Analog-to-Digital Converter (ADC), because of the varying sampling rates and resolutions required to handle the wide range of signals corresponding to each individual operation mode [2].

The majority of reported multi-standard ADCs uses the ΣΔ Modulation (ΣΔM) technique [3]-[9], being the most commonly applied reconfiguration strategy just changing the OverSampling Ratio (*OSR*) according to the operation standard. However, the increasing demand for high data rates in new standards restricts oversampling to low values, what forces to increase the noise-shaping filter order and/or the number of bits of the internal quantizers.

A usual design choice is to employ cascade (MASH) topologies in order to circumvent the stability problems of high-order loops. However cascade topologies are more sensitive to quantization noise leakages caused by mismatches between the analog and digital signal processing in the cascade. These problems can be alleviated by using the so-called *sturdy* MASH (SMASH) architecture, which eliminates the need of digital filtering in the error cancellation logic [10]. Moreover, the use of cascade ΣΔM topologies can be combined with loop-filter resonation in order to optimally distribute the zeroes of the Noise Transfer Function (NTF), so that the in-band noise can be reduced without increasing the filter order. Recently, a new kind of resonation strategy, called *global or inter-stage resonation*, has been applied to cascade ΣΔMs [11]. Traditionally, the implementation of the in-loop resonators requires Backward-Euler (BE), which makes its Switched-Capacitor (SC) implementation more difficult and less robust. In addition, it requires extra Digital-to-Analog Converters (DACs) in the resonation inter-stage paths.

This paper contributes to this topic and presents a novel ΣΔM architecture intended for low-voltage broadband applications, which extends the underlying principle of SMASH ΣΔMs to the implementation of global resonation in an efficient mode. It uses only Forward-Euler (FE) integrators, with neither digital cancellation logic filter nor extra DACs required. In addition, unity Signal Transfer Function (STF) [12] is used in all stages of the modulator, thus relaxing the requirements of amplifier gain non-linearity and output swing. Moreover, the modulator incorporates reconfiguration strategies at both architectural- and circuital-level, thus making it very suited for multi-standard telecom systems. Besides, several practical considerations, including both architecture timing issues and solutions, and an in-depth study of Dynamic Element Matching (DEM) for the multi-bit modulator front-end DAC, are pointed out. As an application, time-domain behavioral simulations including main circuit limitations are shown for different standard requirements included in Beyond-3G wireless telecom systems. The effect of the DEM operation over the modulator performance will be verified based on behavioral simulations as well.

II. PROPOSED MODULATOR ARCHITECTURE

Fig. 1 shows the proposed modulator architecture. It consists of a 2-2 cascade ΣΔM including Unity STF (USTF) and multi-bit quantization in both stages. Global resonation is implemented through the two inter-stage paths (highlighted in Fig. 1) that feed back a delayed version of the last-stage quantization error at the input of the first-stage quantizer. One advantage of this scheme is

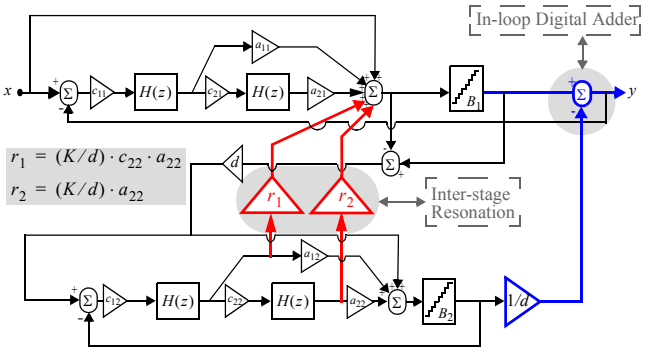

Figure 1. Proposed ΣΔM architecture.

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that, contrary to the one reported in [11], only FE integrators are used. This simplifies the SC implementation and reduces sensitivity to circuit non-idealities.

Besides, the proposed modulator removes the matching requirements between analog and digital filtering. This is achieved by a modified version of the SMASH concept, implemented in Fig. 1 as a digital subtraction of the quantizer outputs inside the first-stage loop [13]. This strategy eliminates the need of additional feedback paths as originally proposed in [10], so that the number of linear DACs required is not increased as compared to a conventional MASH ΣΔM. Note that, the location of the digital adder helps to increase considerably the robustness to capacitor mismatches [13].

Another advantage of the proposed topology as compared to conventional SMASH consists of the beneficial use of an inter-stage scaling factor d that helps to reduce the power of the second-stage quantization error at the output [13]. This factor together with the rest of coefficients, listed in Table I, have been properly selected in order to minimize the amplifiers output swings.

In case that resonation is enabled and considering a linear model for the embedded quantizers, it can be shown that the NTF of the proposed architecture is given by:

$$NTF(z) = \frac{-(1-z^{-1})^2 \cdot [1-(2-K)\cdot z^{-1}+z^{-2}]}{d} \qquad (1)$$

where two of the NTF zeroes are a function of K, whose value can be optimally chosen to maximize the Signal-to-(Noise+Distortion) Ratio (*SNDR*). Note that an increase of d (to reduce the quantization noise) yields a reduction of the feedback coefficient K/d. In practice, this results in a smaller capacitor ratio, which complicates its electrical implementation while reducing capacitor matching. However, the value of K/d can be easily implemented if the oversampling ratio is low enough because —as shown in [11]— a reduction of *OSR* means an increase of K. Therefore, the resonation provided by the proposed modulator is specially suited for wideband applications with low *OSR*.

III. SWITCHED-CAPACITOR IMPLEMENTATION

Fig. 2 shows the conceptual SC schematic of the modulator in Fig. 1, in which the required analog additions are implemented by passive SC networks in order to save power. The desired analog coefficients are implemented as capacitor ratios as shown in Table II. Note that a number of capacitors in Fig. 2 have negative values; in the actual fully differential implementation, these negative values would be implemented by swapping the corresponding capacitors in the positive and negative signal branches.

The use of passive SC analog additions involves a reduction of the full scale at the quantizer input and, consequently, a compression of the references and the quantizers voltage levels to be used [14]. For instance, considering charge redistribution in the capacitors of the first-stage analog adder, the resulting scaling factor is

$$\frac{C_{\text{in1}}}{13C_{\text{in1}} + 8K/d \cdot C_{\text{in1}} + C_{\text{quant}}} \qquad (2)$$

where C_{quant} stands for the input capacitance of the quantizer.

In order to get a robust modulator implementation it is desirable to have the same factor regardless of the use of resonation. However, note from (2) that the denominator term $8K/d \cdot C_{\text{in1}}$ equals zero in case resonation is not employed, and thus the scaling factor varies from the one obtained with resonation. Let us assume that $C_{\text{in1}} = 0.4\text{pF}$, $d = 2$, $K = 0.1$, a 1.5-bit quantizer and 40-fF input capacitance for the quantizer comparators; then the corresponding scaling factor would be 0.065, being 0.067 when resonation is not employed ($K = 0$). This former value can be implemented via a resistor ladder with a 2 to 30 ratio. The second-stage quantizer scaling factor can not be analytically obtained since this stage only processes the quantization error of the previous one. Therefore a simulation-based approach is used to determine this value as depicted in Fig. 3 for two different modes of the case study in next section. An acceptable value is 0.025 which can be realized with a resistors ratio of 4 to 160. Unfortunately, small scaling factors —as those employed in this example (0.067 and 0.025)— impose strict requirements on the comparators input offset. For instance, the first- and second-stage comparators offset requirements are 40 and 7.5mV respectively in this case. This issue can be relieved by design and/or using auto-zero techniques.

TABLE I. MODULATOR COEFFICIENTS

$a_{11} = 8$	$a_{21} = 4$	$a_{12} = 8$	$a_{22} = 4$	$d = 2$
$c_{11} = 1/4$	$c_{21} = 1$	$c_{12} = 1/4$	$c_{22} = 1$	

The digital adder performs the substraction of a 3-level input and a 5-level one (coming from the first- and second-stage respective quantizers), being the later input digitally scaled by $1/d$ in this operation. The output of this substraction is directly given to the 13-level DAC embedded in the front-end loop. As a consequence of this digital operation ($out = y_1 - y_2/d$), the fed back signal in this loop is implicitly scaled by a factor that depends on the quantizers full-scale —this full-scale is the same employed by the front-end DAC— and the inter-stage scaling factor, d. Since the full-scale of both quantizers is the same, given by the reference voltages, the range of this scaling factor is fully determined by d; being $1/2$ and $2/3$ for d equal to 1 and 2, respectively.

Besides, the modulator includes different reconfiguration strategies. On the one hand, the order can be configured to be either 2 or 4, by using the control signal SL in Fig. 2. On the other hand, several SC networks (highlighted in Fig. 2) are enabled or disabled depending on whether the global resonation is used or not. All these reconfiguration strategies (adaptive global resonation and NTF order) can be used independently, thus giving more flexibility to the ΣΔM to adjust its functionality to the required performance. In a practical application, those components that are not used can be turned off by using a power-down control in order to save power consumption.

TABLE II. SC IMPLEMENTATION OF THE ΣΔM COEFFICIENTS

In-loop Capacitors
$a_{11} = C_{a11}/C_{in1}$; $a_{12} = C_{a12}/C_{in2}$; $a_{21} = C_{a21}/C_{in1}$; $a_{22} = C_{a22}/C_{in2}$
$c_{11} = C_{s11}/C_{i11}$; $c_{12} = C_{s12}/C_{i12}$; $c_{21} = C_{s21}/C_{i21}$; $c_{22} = C_{s22}/C_{i22}$
Inter-stage Capacitors
$C_{r1} = c_{22}\cdot a_{22}\cdot (K/d)\cdot C_{in1}$; $C_{r2} = a_{22}\cdot (K/d)\cdot C_{in1}$
$C_{s12d} = d\cdot C_{s12}$; $C_{in2d} = d\cdot C_{in2}$;
$C_{r1d} = c_{22}\cdot a_{22}\cdot K\cdot C_{in2}$; $C_{r2d} = a_{22}\cdot K\cdot C_{in2}$
$C_{r1s12d} = c_{22}\cdot a_{22}\cdot K\cdot C_{s12}$; $C_{r2s12d} = a_{22}\cdot K\cdot C_{s12}$
Adder Capacitors
$C_{a12} = a_{12}\cdot C_{in2}$; $C_{a22} = a_{22}\cdot C_{in2}$
$C_{s12d} = d\cdot C_{s12}$; $C_{a11s12d} = d\cdot a_{11}\cdot C_{s12}$; $C_{a21s12d} = d\cdot a_{21}\cdot C_{s12}$
$C_{in2d} = 2\cdot C_{in2}$; $C_{a11in2d} = d\cdot a_{11}\cdot C_{in2}$; $C_{a21in1d} = a_{21}\cdot C_{in2d} = d\cdot a_{21}\cdot C_{in2}$

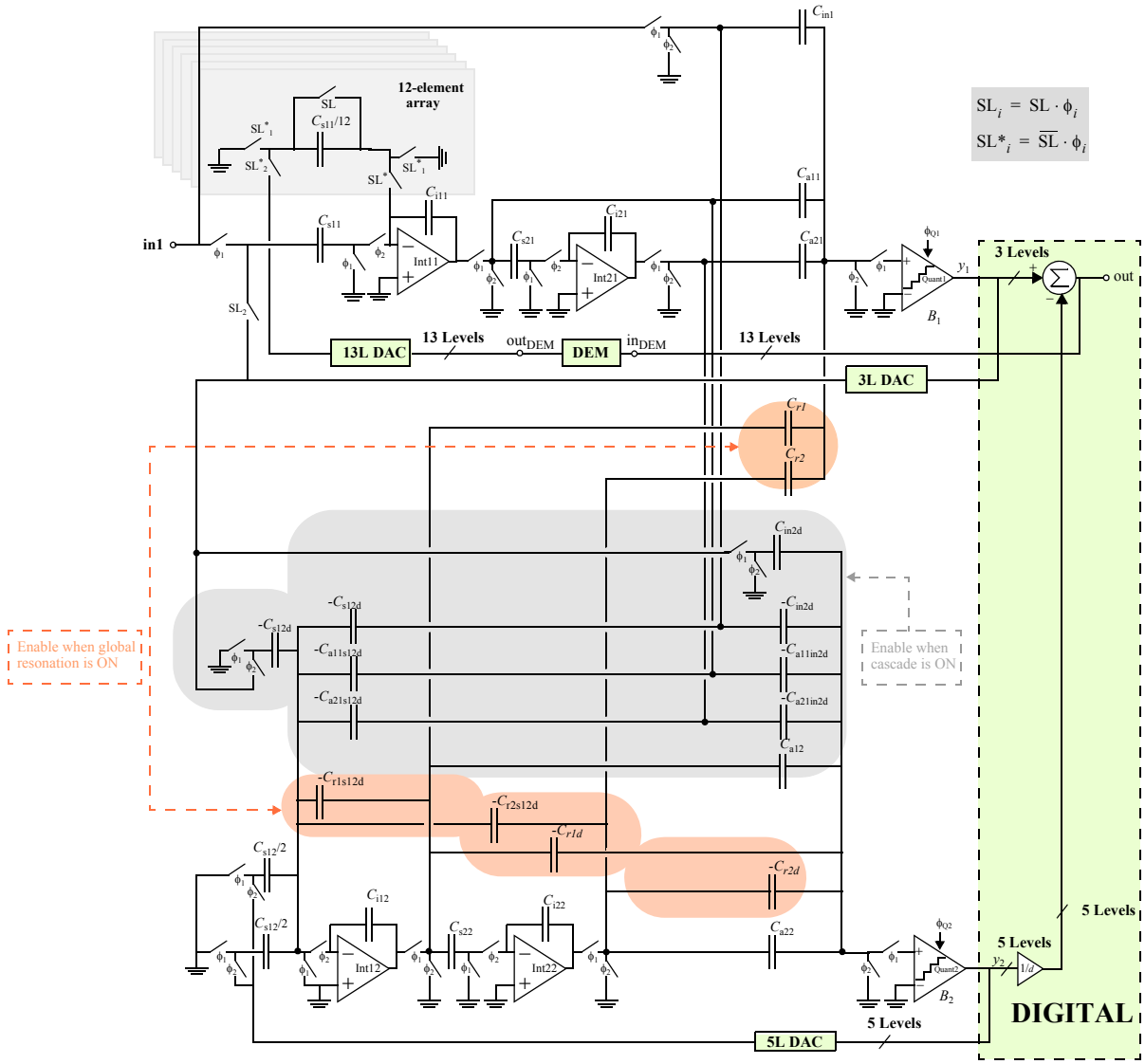

Figure 2. SC schematic of the proposed reconfigurable ΣΔM (single-ended version).

III.A. Timing Issues and Solutions

The timing constraints of the modulator operation are quite demanding due, mainly, to the use of USTF in all stages and the topological innovations included in the employed modulator architecture. On the one hand, the input signal is directly fed to the second-stage analog adder in Fig. 1 after being only added in the 1st-stage adder and quantized. On the other, the front-end analog adder output is quantized, digitally added to the 2nd-stage quantizer output, scrambled by the DEM block and finally fed back to the first integrator by a 13-level DAC. All these operations must in practice be performed in only one half of the clock cycle. Indeed, excessive delay in any of these two paths will modify the signal and noise modulator transfer functions and degrade the SNR. The solution proposed to relax timing issues in these two critical paths is to trigger the 1st-stage quantization before the end of phase ϕ_1. If this operation is done later, there will be an additional delay z^{-1} either in the inter-stage input of the 2nd-stage analog addition in Fig. 1 —or, equivalently, in the 3-level inter-stage DAC in Fig. 2— or, alternatively, in the feed-back operation of the front-end loop.

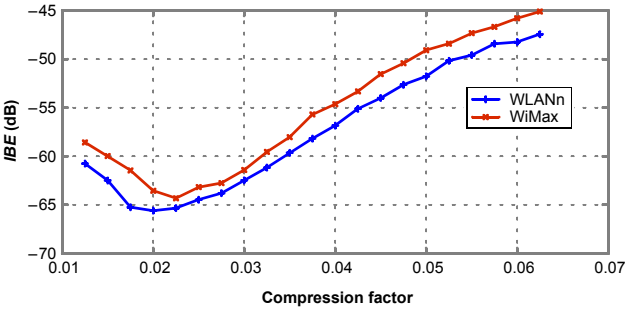

Figure 3. Evolution of the In-Band Error (*IBE*) versus the 2nd-stage quantizer compression factor (-6dBFS input signal).

Fig. 4 shows the timing trade-offs for the proposed solution in the two critical paths. In both cases, a fast operation time for the 1st-stage analog addition (t_{aadd1}) is essential. Then, the 1st-stage quantization (t_c) is followed by either the inter-stage DAC (t_{dac2}) and the 2nd-stage analog addition (t_{aadd2}); or the digital adder (t_{di-}

$_{gadd}$), the DEM processing (t_{DEM}) and the front-end 13-level DAC (t_{dac1}). The values of t_c, t_{dac1}, t_{dac2} and t_{digadd} are expected to be very small since the comparators —main building blocks of the quantizers— can be based on very fast regenerative latches, and both the digital adder and the DACs can be implemented with few digital gates. Therefore, the bottleneck for timing issues comes from the time required by the analog adders and by the DEM block for proper operation. That required by the analog adders can be significantly reduced by properly sizing the switches and capacitors in the adders; that is, the RC time constant associated to each switched-capacitor branch in the adder can be made small enough compared to the available time slot for the respective analog additions. On the other hand, the DEM algorithm to be used must be mapped onto a practical implementation with reduced propagation delay in order not to degrade the modulator performance. The details on this time-saving DEM implementation are provided in the in the next section.

III.B. Dynamic Element Matching Implementation

A widely used and efficient algorithm for performing the DEM operation is Data Weighed Averaging (DWA). DWA is based on the sequential selection of elements from a DAC array, beginning with the next available unused element[†2] [15]. A first-order noise shaping of the mismatch errors associated to the DAC elements is obtained with this algorithm [16]; pushing, thus, the error power to high frequencies, where it will be filtered out by the decimation filter.

Fig. 5 shows three possible implementations of the DWA algorithm. The first implementation is the one traditionally selected, but it is not very time-efficient; on the contrary, the second approach, depicted in Fig. 5(b), presents an improvement in timing performance [17]. The reason for this is that the first approach performs the full addition in the critical path, while only the carry outputs of that addition are needed for performing the DEM scrambling operation. The second approach takes full advantage of this feature and makes the element rotation, G and P signal generation —needed for the carry generation—, and register loading in a non-critical time slot. This topology replaces the full digital adder with an element rotator in order to reduce the number of flip-flops. Note that the third approach, proposed in this work and depicted in Fig. 5(c), consists of changing the rotator in the former implementation with a full adder, this results in a significant reduction of the number of flip-flops in the registers. For the sake of simplicity, the encoding of the elements into bits at the DEM input is not shown in the figure.

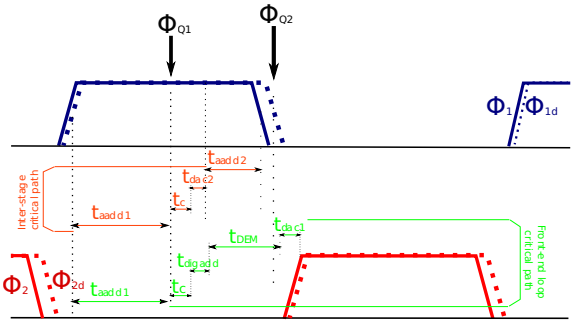

Figure 4. Timing operation in the modulator critical paths.

As aforementioned, an additional advantage of the approach in Fig. 5(c) is its reduced area occupation, since ultra-simplified registers can be used. For the 13-level DEM block shown in Fig. 2, the DWA approach in Fig. 5(a) would require 4×13 (52) flip-flops, since 4 bits are needed to codify 13 levels. The implementation presented in Fig. 5(b) [17] makes use $1 + 2 + 4 + 8$ (15) flip-flops for 4 bits. Based on the data contained in those registers, it is very simple to obtain that of the remaining elements. However, this can not be directly applied in our specific case because the number of levels of the front-end DAC (13) is not a power of two. There are two possible solutions, namely: to keep all the data in the flip-flops as done in Fig. 5(a); or, alternatively, to store only one element per bit; reducing, thus, the numbers of registers to only 4. We have selected the second option, depicted in Fig. 5(c), in order to diminish the area devoted to registers at the price of a small increase in combinational logic —and, thus, in the delay times as well— for the generation of the G and P signals for the carry look-ahead operation. Note however that this additional combinational block does not penalize the speed of the DEM since it is outside the critical path.

On the other hand, the front-end DAC is usually implemented by a set of digital gates, which enable the feed-back of either the positive or the negative reference voltage to each feed-back sampling capacitor in the integration phase as shown in Fig. 6(a). An alternative implementation is depicted in Fig. 6(b), in which the common mode is used as an additional voltage for the DAC feed-back. In our specific case, this will result in a reduction of 12 capacitors to only 6 in the first integrator. These two alternatives for the front-end DAC will be called “2-level” and “3-level” DAC implementations, respectively.

In order to verify the correct operation of the DWA implementation and to know the influence of both front-end DAC alternative implementations in our modulator topology, a set of behavioral simulations have been performed as presented in next section.

†2. Note that when the end of the array is reached, rotation occurs, thus continuing with the first element of the array.

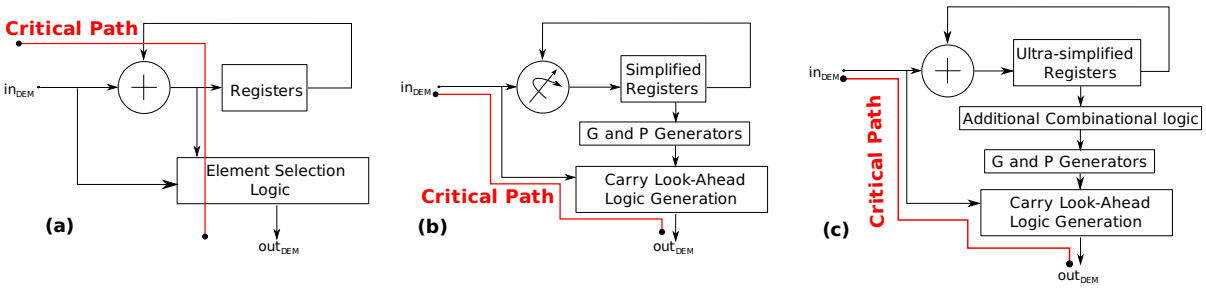

Figure 5. DWA Implementation: (a) Standard, (b) proposed approach in [17], and (c) employed topology.

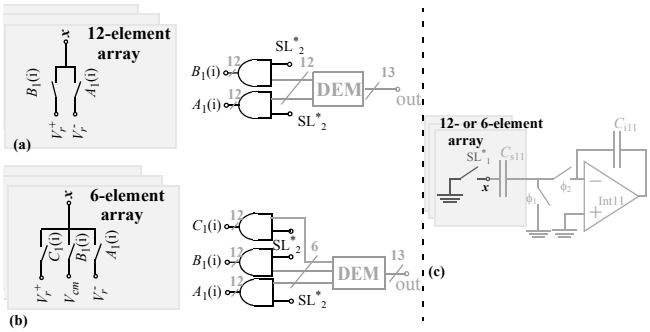

Figure 6. DAC implementations: (a) 2-level, (b) 3-level; and (c) detail of the first integrator DAC connection.

IV. CASE STUDY: APPLICATION TO BEYOND-3G SYSTEMS

In order to show the benefits of the proposed ΣΔM architecture, a case study is presented considering the seven standards and specifications listed in Table III. This table also shows the values of the modulator design parameters that are reconfigured for the different operation modes, namely: NTF order (L) and *OSR*. Different oversampling ratios —and their corresponding sampling frequencies (f_s)— are employed in order to cope with the required resolution for each signal bandwidth. Besides, global resonation is used only in WLANn mode with a feedback coefficient of $K/d = 0.05$, resulting in a shift of two zeroes of the NTF from 0 to $0.95 \pm j0.32$. This zeroes distribution reduces in approximately 9.5dB the quantization noise within a 20-MHz bandwidth.

Several behavioral simulations have been performed using SIMSIDES, a SIMULINK-based time-domain simulator for ΣΔ modulators [18]. The main circuit non-ideal effects were taken into account considering the quantizer scaling factors given in the example of Section III. The first-stage feedback DAC is initially assumed to be linear, since the DEM algorithm will be evaluated separately at the end of this section.

Since there are no noise leakages due to mismatching between analog and digital processing in the cascade in Fig. 1, the DC gain amplifiers requirements are clearly relaxed compared to traditional cascades, as illustrated in Fig. 7 for WiMax mode. In fact, amplifier DC gains of 35dB are enough to fulfil specifications in the seven standards of operation. This low-gain value is specially beneficial in a low-voltage scenario, in which technology scaling degrades the transistor gain, and subsequently that of the amplifier. Note from Fig. 7 that, except for the 3rd opamp, the amplifiers DC gain can be lowered much more for WiMax mode. Contrary to conventional cascades, in which the most demanding requirements are associated to the front-end amplifiers, this is not the case in the proposed modulator topology as a result of the elimination of the digital processing. The same applies for the opamp dynamic requirements, which will be also larger for the 3rd integrator.

Fig. 8 shows the output spectra and the integrated *IBE* powers over frequency for the cascade in Fig. 1 for the operation modes of WiMax, WLANa and WLANn. Note that an increase of f_s implies a reduction of the *IBE* power for WLANa when compared to WiMax for a 10-MHz bandwidth. On the other hand, the effect of the optimal distribution of two NTF zeroes —thanks to the use of inter-stage resonation— in WLANn mode diminishes the *IBE* power when compared to WLANa in its 20-MHz bandwidth. In fact, the notch created by the use of resonation is clearly visible in the figure for the spectrum in WLANn mode.

Fig. 9 depicts the *SNDR* curves for all operation modes. It can be observed that the modulator fulfils the requirements in Table III. Additionally, as Fig. 9 shows, the ΣΔM overloads close to the reference voltage (1.2V) for all modes[†3] as a consequence of the large robustness of the modulator topology to amplifier non-linearities.

TABLE III. STANDARDS SPECIFICATIONS AND ΣΔM PARAMETERS.

Standard	GSM	BT	UMTS	DVB-H	WiMax	WLANa	WLANn
***SNDR* (dB)**	80	75	65	55	60	65	50
***BW* (MHz)**	0.2	0.5	1.96	3.8	10	10	20
L	2				4		
OSR	200	80	40	20	12	16	8
***fs* (MHz)**	40	80	160		240	320	

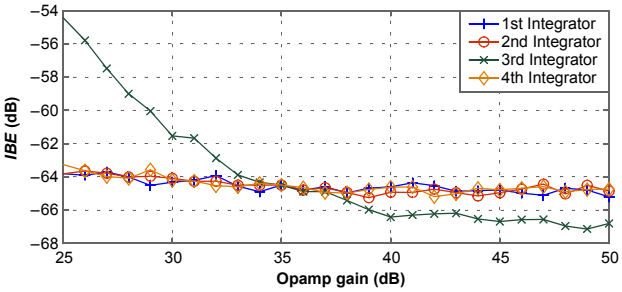

Figure 7. *IBE* vs. amplifier DC gain for WiMax (-6dBFS input level).

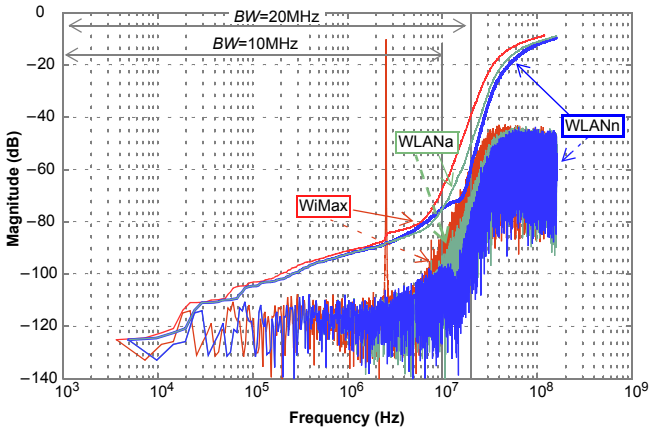

Figure 8. Spectra for WiMax and WLAN modes (-6dBFS input level).

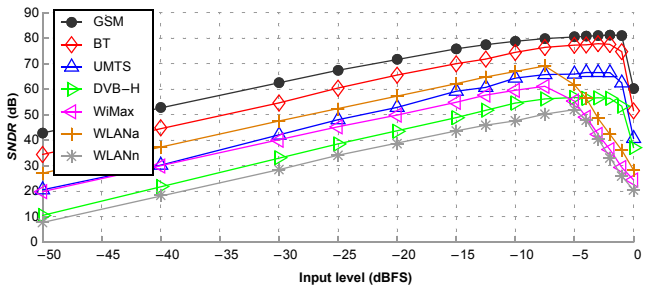

Figure 9. *SNDR* vs. input signal level.

†3. Note that the implicit in-loop scaling factor of $2/3$ makes the modulator overload 3.5dB earlier in the cascade configuration.

This translates into very low requirements for the amplifier output swings, being always lower than 0.3V.

In order to evaluate the performance of the DWA algorithm, several simulations are done for the operation modes that need a front-end multi-bit DAC in this multi-standard case study (WiMax, WLANa and WLANn). These simulations allow to make a comparison between the 2- and 3-level implementation of the front-end DAC as well.

Fig. 10 depicts *SNDR* versus the input level when the capacitors of the front-end DAC present mismatches with a standard deviation of 0.5%. The cases with no DEM and no mismatches are also depicted for comparison purposes. Note the noteworthy degradation of the performance when no DEM is employed, specially for WLANa. The figure shows that there is no appreciable *SNDR* degradation due to mismatch errors as large as 0.5% if the 2-level DAC implementation is used together with a DWA scrambling operation (DWA 2L). However, a *SNDR* degradation larger than 10dB comes out for a 3-level implementation of the DAC (DWA 3L) in WLANa mode, being the degradation also highly dependent on the input level.

CONCLUSIONS

A new resonation-based cascade ΣΔM architecture is presented. This modulator is capable to reconfigure the order of the quantization noise filtering and to resonate through switchable feedback inter-stage paths. These figures are combined with unity STFs in both cascade stages, thus achieving high linearity with reduced output swing requirements. Moreover, no digital cancellation logic filtering is required, removing thus noise leakages given by analog and digital processing mismatches. All these characteristics make the presented architecture very suited to the implementation of low-voltage multi-standard ADCs with very relaxed opamp requirements. Additionally, timing issues arising for the proposed modulator architecture are discussed and solutions are proposed, including different alternatives for the practical implementation of the feedback DAC and the DWA DEM algorithm. Finally, in order to demonstrate the capabilities of the proposed modulator, a case study covering a number of standards, including GSM, Bluetooth, UMTS, DVB-H, WiMax and WLAN is shown.

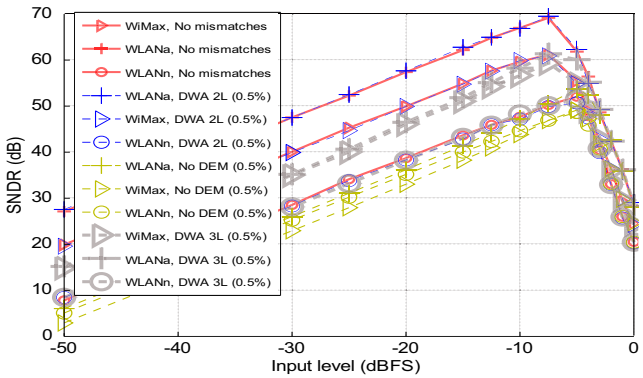

Figure 10. SNDR vs. input level with DWA algorithm and different DAC implementations.

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