A CMOS 0.8-μm Transistor-Only 1.63-MHz Switched-Current Bandpass $\Sigma\Delta$ Modulator for AM Signal A/D Conversion

José M. de la Rosa, Belén Pérez-Verdú, Rocío del Río, and Angel Rodríguez-Vázquez

***Abstract*—This paper presents a CMOS 0.8-μm *switched-current* (SI) fourth-order bandpass $\Sigma\Delta$ modulator (BP-$\Sigma\Delta$M) IC capable of handling signals up to 1.63 MHz with 10.5-bit resolution and 60-mW power consumption from a 5-V supply voltage. This modulator is intended for direct A/D conversion of narrowband signals within the commercial AM band, from 540 kHz to 1.6 MHz. Its architecture is obtained by applying a lowpass-to-bandpass transformation ($z^{-1} \rightarrow -z^{-2}$) to a 1-bit second-order low-pass $\Sigma\Delta$ modulator (LP-$\Sigma\Delta$M). The design of basic building blocks is based upon a detailed analysis of the influence of SI errors on the modulator performance, followed by design optimization. Memory-cell errors have been identified as the dominant ones. In order to attenuate these errors, fully differential regulated-folded cascode memory cells are employed. Measurements show a best SNR peak of 65 dB for signals of 10-kHz bandwidth and an intermediate frequency (IF) of 1.63 MHz. A correct noise-shaping filtering is achieved with a sampling frequency of up to 16 MHz.**

***Index Terms*—Analog-to-digital conversion, bandpass sigma–delta modulation, switched-current circuits.**

I. Introduction

THE TREND toward the realization of complete *mixed-signal* systems *on chip* has motivated the exploration of analog design techniques compatible with standard digital CMOS technologies. This is the case of *switched-current* (SI) circuits [1], which during the last few years have been explored for the construction of different analog functions, including *filtering* and *analog-to-digital conversion* (ADC) [2]–[5].

Many of the SI ADC's reported in literature use *low-pass* $\Sigma\Delta$ modulator (LP-$\Sigma\Delta$M) architectures for handling audio-frequency signals. Particularly, a CMOS 0.9-μm prototype that features 13-bit effective resolution and 300–3400 Hz signal band using a single-loop second-order modulator has been presented in [2]. The use of SI circuits to design *cascade* LP-$\Sigma\Delta$M's capable of handling larger operating frequencies has also been explored in [3]; however, the achieved frequencies are well below the MHz range. Reported SI ADC's for signal frequency in the MHz range employ a Nyquist-type architecture [4]–[5]. Specifically, the CMOS 0.8-μm converter in [4] features 8 bit at 7.5 MHz with 350-mW power consumption; while that in [5], also in CMOS 0.8-μm, features 7.2 bit at 20 MHz and dissipates 82.5 mW.

This paper presents a CMOS 0.8-μm SI $\Sigma\Delta$ modulator circuit capable of handling signals up to 1.63 MHz with 10.5-bit resolution and 60-mW power consumption from a 5-V supply voltage. This modulator is of the bandpass type (BP-$\Sigma\Delta$M) and has been designed to handle narrowband signals within the commercial AM band, from 540 kHz to 1600 MHz. The advantages of BP-$\Sigma\Delta$M's, as compared to wideband Nyquist-rate converters, for digitizing narrowband signals have been discussed elsewhere [6], and a number of standard CMOS *switched-capacitor* prototypes have been reported [7]–[8]. The SI BP-$\Sigma\Delta$M in this paper features a best SNR peak of 65 dB for signals of 10-kHz bandwidth and an intermediate frequency (IF) of 1.63 MHz. Correct *noise-shaping* filtering is achieved with a sampling frequency of up to 16 MHz, thus demonstrating the possibility of using SI BP-$\Sigma\Delta$M's in narrowband high-frequency communication systems.

Circuit design is based upon a detailed analysis of the influence of SI errors, followed by design optimization. Memory-cell errors have been identified as the dominant ones. However, unlike LP-$\Sigma\Delta$M's, S^2I memory cells [9] cannot be employed to attenuate these errors because signals are sampled at a rate close to the signal frequency; hence they change quite significantly during sampling, thereby destroying the S^2I performance. Instead, fully differential regulated-folded cascode memory cells are employed for error attenuation in our circuits. Another consequence of the high-frequency operation is the increased influence of bonding-pad parasitics, which in our circuit is handled through the use of fully differential current-mode buffers [10].

Section II of the paper describes the modulator architecture. Section III describes the design process of the memory cell and outlines other modulator subcircuits. Section IV presents experimental results. Finally, conclusions are given in Section V.

II. Modulator Architecture

Fig. 1 shows the block diagram of the modulator. It is a single-loop fourth-order BP-$\Sigma\Delta$M with a 1-bit quantizer. On the one hand, this choice renders the modulator easy to understand and simple to design. On the other hand, such a simple architecture is capable of achieving high resolution together with robust stable operation; actually, 1-bit quantization and fourth-order filtering suffices to accomplish the specifications intended in this paper.

Note that Fig. 1 is obtained by applying a $z^{-1} \rightarrow -z^{-2}$ transformation to a single-loop second-order LP-$\Sigma\Delta$M. Such a transformation keeps the stability properties of the latter, and hence allows us to exploit the knowledge already available for the low-pass modulator [11] in order to design the bandpass one—another reason for choosing such an architecture. Fig. 1 includes two resonators, resulting from the transformation of the integrators in the LP-$\Sigma\Delta$M, two additional delay blocks, needed to achieve the required delay in the feedback loop, and three

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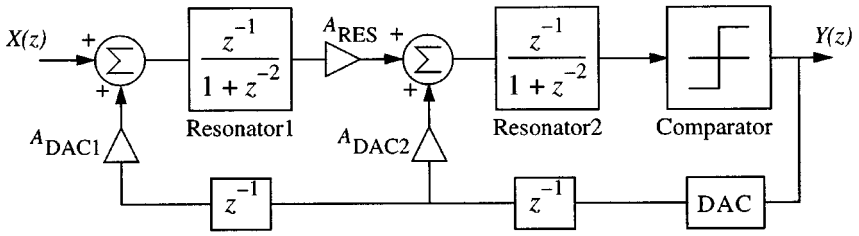

Fig. 1. Block diagram of the modulator.

scaling factors. The values of the latter have been optimized to obtain similar signal ranges for both resonators, giving

$$A_{\mathrm{DAC2}} = -A_{\mathrm{DAC1}} = 1; \quad A_{\mathrm{RES}} = 1/2. \tag{1}$$

Assuming that the quantization error is modeled as white additive noise [6], the z-domain output can be expressed as

$$Y(z) = S_{\mathrm{TF}}(z)X(z) + N_{\mathrm{TF}}(z)E(z) \tag{2}$$

where $S_{\mathrm{TF}}(z)$ and $N_{\mathrm{TF}}(z)$ represent the signal transfer function and the noise transfer function, respectively,

$$S_{\mathrm{TF}}(z) = z^{-2} \quad N_{\mathrm{TF}}(z) = (1+z^{-2})^2. \tag{3}$$

By making $z = \exp(j2\pi f/f_{\mathrm{S}})$, where f_{S} is the sampling frequency, it can be seen that $N_{\mathrm{TF}}(f)$ has 2 transmission zeros at $f_{\mathrm{S}}/4$, and that the filtering around this frequency is actually of the band-stop type.

The *in-band* quantization noise power can be calculated by integrating the output power spectral density within the signal bandwidth, as follows:

$$P_{\mathrm{Q}} = \int_{f_{\mathrm{S}}/4-B_{\mathrm{W}}/2}^{f_{\mathrm{S}}/4+B_{\mathrm{W}}/2} 2S_{\mathrm{Q}}|N_{\mathrm{TF}}(f)|^2\, df \cong \frac{\Delta^2\pi^4}{60M^5} \tag{4}$$

where $S_{\mathrm{Q}} = \Delta^2/(12f_{\mathrm{S}})$ is the power spectral density of the quantization noise, Δ is the quantization step, B_{W} is the signal bandwidth, and $M \equiv f_{\mathrm{S}}/(2B_{\mathrm{W}})$ is the *oversampling ratio*. From (4), and assuming that the modulator input is a sinewave of amplitude $A \leq \Delta/2$, the signal-to-noise ratio (SNR) and the dynamic range (DR) are given by

$$\begin{aligned} \mathrm{SNR} &= \frac{A^2}{2P_{\mathrm{Q}}} = \frac{30A^2M^5}{\pi^4\Delta^2} \\ \mathrm{DR} &= \frac{(\Delta/2)^2}{2P_{\mathrm{Q}}} = \frac{15M^5}{2\pi^4}. \end{aligned} \tag{5}$$

This shows that the modulator resolution increases with M at a rate of about 2.5-bit/octave. However, such an ideal feature can only be achieved provided that the scaling coefficients and the resonator transfer functions in Fig. 1 are realized without errors. Modeling of these errors and circuit optimization are needed to cope with the SNR and DR degradation observed in actual SI circuits.

III. Switched-Current Implementation

Fig. 2(a) shows the block diagram of the resonators in Fig. 1. It consists of a feedback cascade of two lossless discrete integrators (LDI).[1] Fig. 2(b) shows a conceptual SI realization of this resonator employing second generation SI memory cells. As shown in [1], the major error sources of SI memory cells are three, namely: *conductance error* (represented by parameter ε_g) due to finite input/output conductances, *incomplete settling error* (represented by ε_s), and *switch charge injection error* (represented by ε_q). Besides, the resonator behavior becomes degraded by the finite conductances [g_{oF} and g_{oFB} in Fig. 2(b)] of the current mirrors employed to realize the scaling coefficients. Their associated errors are defined respectively by

$$\varepsilon_{\mathrm{F}} = r_{\mathrm{on}}g_{\mathrm{oF}} \quad \varepsilon_{\mathrm{FB}} = r_{\mathrm{on}}g_{\mathrm{oFB}} \quad \varepsilon_{g_{\mathrm{F}}} = \frac{g_{\mathrm{oF}}}{g_{\mathrm{in}}} \quad \varepsilon_{g_{\mathrm{FB}}} = \frac{g_{\mathrm{oFB}}}{g_{\mathrm{in}}} \tag{6}$$

where g_{in} is the input conductance of the memory cells and r_{on} is the on-resistance of the steering switches.

The above-mentioned errors modify the noise-transfer function N_{TF}. Thus the zeros of this function are shifted from their nominal positions—located at $f_{\mathrm{S}}/4$—degrading noise shaping and making the in-band quantization noise power increase. As we demonstrated in [13], the dynamic range of a fourth-order BP-$\Sigma\Delta$M degraded by SI errors is

$$\mathrm{DR} \cong \frac{15M^5}{2\pi^4\left[1+\dfrac{10}{3}(3\xi_1^2+\xi_2^2)\left(\dfrac{M}{\pi}\right)^2+5(\xi_1^2+\xi_2^2)^2\left(\dfrac{M}{\pi}\right)^4\right]} \tag{7}$$

where

$$\begin{aligned} \xi_1 &= -(2\varepsilon_{\mathrm{F}} + 2\varepsilon_{\mathrm{FB}} + 4\varepsilon_s + \varepsilon_{g_{\mathrm{F}}} + \varepsilon_{g_{\mathrm{FB}}}) \\ \xi_2 &= 4\varepsilon_s + 4\varepsilon_g + 4\varepsilon_q + \varepsilon_{g_{\mathrm{F}}} + \varepsilon_{g_{\mathrm{FB}}}. \end{aligned} \tag{8}$$

Note that SI errors do not affect DR in the same way, the largest degradation being produced by ε_s. Equation (7) was used to find the maximum value for each error in order to fulfill digital AM radio receiver specifications, i.e., DR $=$ 60 dB at 2.16 MHz $\leq f_{\mathrm{S}} \leq$ 6.4 MHz at $B_{\mathrm{W}} =$ 10 kHz. This yields $\varepsilon_s \leq$ 0.25%, $\varepsilon_{g,\,q} \leq$ 0.35%, $\varepsilon_{\mathrm{F,\,FB}} \leq$ 0.5% and $\varepsilon_{g_{\mathrm{F,\,FB}}} \leq$ 1%. Modulator building blocks were designed to satisfy these conditions as detailed in the next section.

[1]This structure has been chosen because it keeps the poles inside the unit circle upon changes due to errors of the feedback loop gain. However, as demonstrated in [12] for lowpass modulators, it may happen that unstable resonators result in stable modulators.

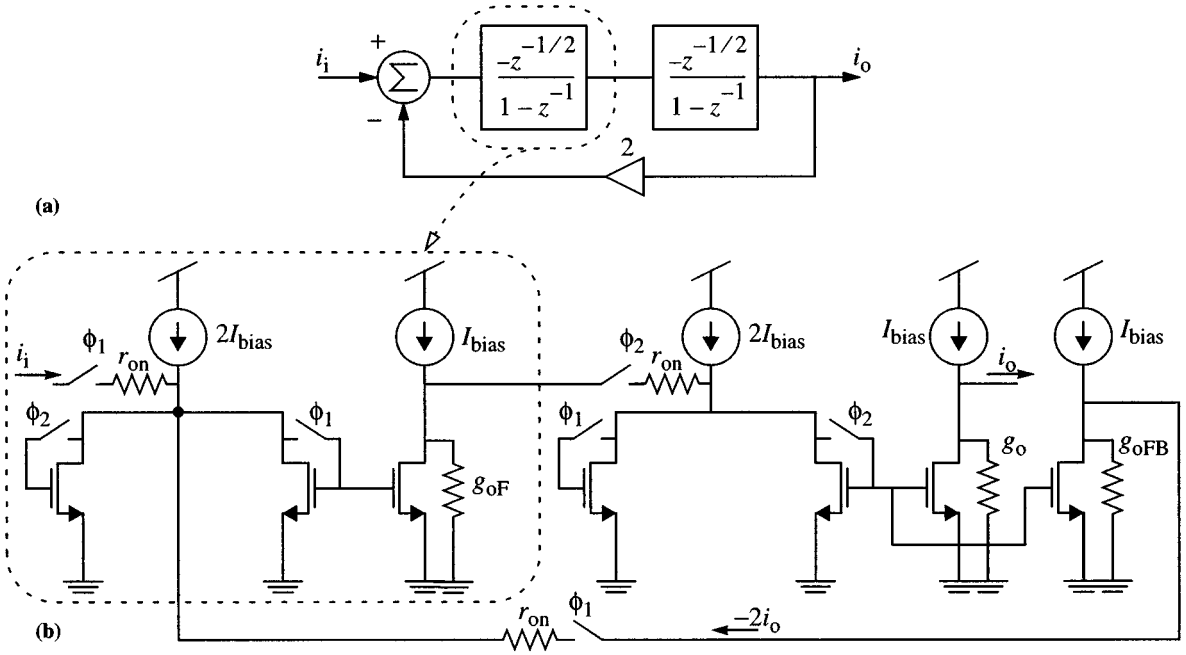

Fig. 2. Implementation of the resonator. a) Block diagram. b) Conceptual schematic considering SI errors.

A. Design of the Memory Cell and the Resonator

A second generation regulated-folded-cascode (RFC) memory cell [14] was used to reduce ε_g. This cell increases the input conductance through the incorporation of a local feedback in the signal path, thus reducing both ε_g and $\varepsilon_{g_{\mathrm{F,FB}}}$. Fig. 3 shows the schematic of the fully differential RFC memory cell including the common-mode feedback circuit (CMFB) (M_{16-24}). The local feedback stage is formed by transistors M_{3-6}, the memory transistors are $M_{1,2}$ and the current source transistors are M_{7-15}. The steering switches are pMOS while the memory switches are nMOS with minimum size; the latter include dummy devices which, in combination with fully differential circuitry, attenuate ε_q. Although there are other approaches to reduce ε_q, we have not used them for different reasons. That in [15] uses zero-voltage switching to attenuate the signal-dependent component of ε_q. However, its power dissipation is penalized by the amplifier employed to create the virtual ground. The alternative is using the so-called S^2I memory cell [9]. However, this cell is not well suited for BP-$\Sigma\Delta$M's because the input signal is not stationary during the sampling phase since is located at $f_S/4$. Hence, unless a sampling-and-hold (S/H) is placed at the front end of the modulator, the advantages of using the S^2I memory cell are destroyed.

Because of the local feedback, the memory cell exhibits third-order dynamics with a single pole at $g_{m1,2}/C_{\mathrm{gs1,2}}$ (where g_m is the small-signal transconductance and C_{gs} is the gate–source capacitance) and a pair of complex conjugate poles whose values depend on the transconductances and the parasitic capacitances of M_{3-6} and the steering switches. Two additional MOSFET capacitors, C_{H}, are connected to the memory transistor gates (see Fig. 3) to create a dominant pole at $g_{m1,2}/(C_{\mathrm{gs1,2}}+C_{\mathrm{H}})$. Thus, ε_s can be controlled by sizing the memory transistor. These extra capacitances also reduce the common-mode component of ε_q.

The memory cell has been designed by using the transistor-level optimizer reported in [11] to attain the specifications required for AM digital radio receivers and, at the same time, optimize the trade-off between speed and dynamic range. The resulting bias currents are $I_{\mathrm{bias}}=212.6\ \mu$A, $I_{\mathrm{biasR}}=20\ \mu$A and $C_{\mathrm{H}}=2.8$ pF (realized through a 36-μm/36-μm nMOS transistor). Table I summarizes the simulated performance of the memory cell. This table also includes the memory-cell errors. Their values are low enough to achieve the targeted modulator resolution. On the other hand, the in-band integrated thermal noise is given by

$$P_{\mathrm{Th}}=\int_{f_S/4-B_W/2}^{f_S/4+B_W/2}\cdot S_{\mathrm{cell}}\left[\left(\frac{\tau}{T_S}\right)+\left(\frac{\tau}{T_S}\right)^2\mathrm{Sinc}^2(f\tau)\frac{2BW_n}{f_S}\right]df \quad (9)$$

where τ/T_S is the fraction of the clock period (T_S) during which the noise is being sampled, $\mathrm{Sinc}(f\tau)$ is the sample-and-hold transfer function, and $BW_n\cong g_{m_{1,2}}/(4C_H)$ is the equivalent noise bandwidth. Assuming that the reference current level of the digital-to-analog converter (DAC) is $\Delta/2$, the thermal dynamic range of the cell is $\mathrm{DR_{Th}}=\Delta^2/(8P_{\mathrm{Th}})$. In our design, $\Delta=100\ \mu$A, and the worst case is obtained for the minimum AM sampling frequency, $f_S=2$ MHz, giving $\mathrm{DR_{Th}}=86$ dB, which clearly does not limit the performance of the modulator.

The SI resonator is implemented by replacing the memory cells in Fig. 2(b) by Fig. 3. The scaling stages are realized through simple current mirrors. Note that the required gain inversion is straightforward because of the fully differential structures. Current steering switches (realized through pMOS transistors) are sized such that $r_{\mathrm{on}}=472\ \Omega$, which bounds

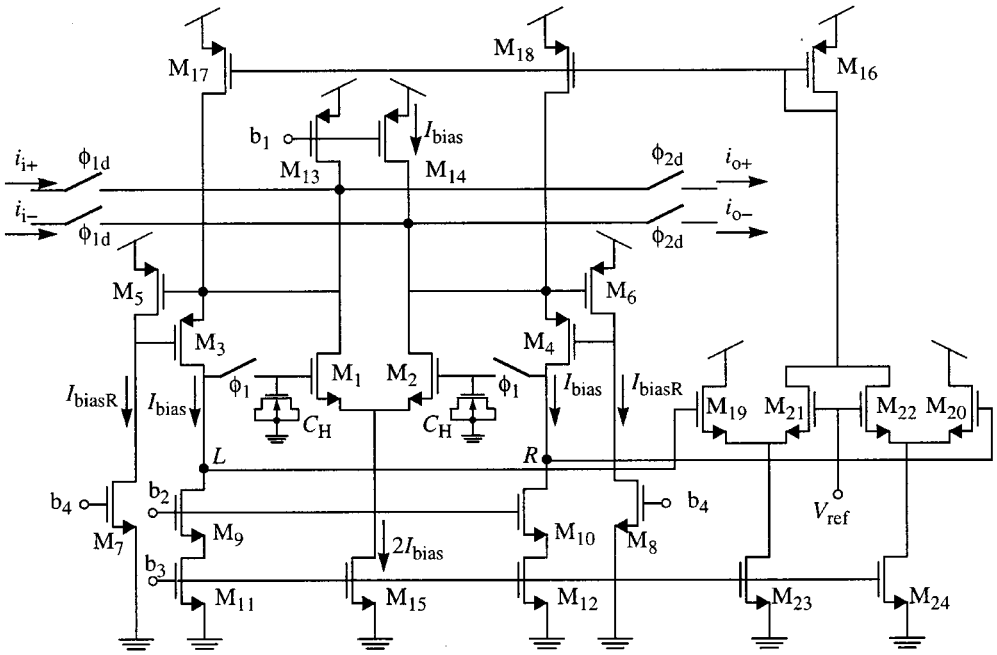

Fig. 3. Schematic of the memory cell.

TABLE I
SIMULATED PERFORMANCE (HSPICE) OF THE MEMORY CELL

dc Parameters	Mean Value	Units
Input resistance	2.9	Ω
Output resistance	204	kΩ
3rd Order Non-Linearity at $I_{in} = 0.9\ I_{bias}$	-105	dB
ac Parameters	**Mean Value**	**Units**
-3dB-frequency	20.7	MHz
1st-Pole frequency	20.5	MHz
2nd-Pole frequency	64.6±196.5j	MHz
SI Errors	**Mean Value**	**Units**
ε_g	28	ppm
ε_q	100	ppm
ε_s ($f_s < 6.67$MHz@$I_{step} = 0.5\ I_{bias}$)	<200	ppm
Thermal noise mean square value, $\sqrt{S_{cell}}$	6.1	pA/$\sqrt{\text{Hz}}$

$\varepsilon_{\mathrm{F,FB}}$ and $\varepsilon_{g_{\mathrm{F,FB}}}$ according to AM digital radio receiver requirements.

B. Other Modulator Subcircuits

Other building blocks of the modulator in Fig. 1 are the quantizer and the DAC. The 1-bit quantizer is made up of a regenerative latch [16] and a NOR flip-flop which maintains the output value in the phase in which the resonators are fed back. A fast comparison is obtained with low input-current levels. Layout extracted simulations show 4% hysteresis—which is not problematic because the power of the in-band noise remains virtually unchanged for hysteresis as large as 10% of the full-scale converter input [11].

The 1-bit DAC used in the modulator consists of a current source controlled by the comparator output [3]. A stacked-cascode current mirror was chosen because it resembles the structure of the memory cell. The differential output current, with values $\pm I_{\mathrm{ref}} = \pm\ 50\ \mu$A $(=\pm\Delta/2)$, change the flow direction depending on the comparator output.

In addition to the mentioned blocks, other circuits have been included for practical reasons. On the one hand, a fully differential current-mode buffer has been incorporated at the front end of the modulator [10]. This buffer is used to isolate the on-chip circuitry from the parasitic time constants at the chip input pads, thus allowing us to take full advantage of the speed capabilities of SI circuits. Apart from this function, this circuit also converts the single-ended external input voltage into a fully differential current through the use of an external resistance.

On the other hand, we have included an internal clock phase generator that provides a 4–phase clock diagram in order to avoid transient current spikes. Thus, overlapping clock phases ($\phi_{1\mathrm{d}}$ and $\phi_{2\mathrm{d}}$) are used for current-steering switches and nonoverlapping clock phases (ϕ_1 and ϕ_2) are used for memory switches (see Fig. 3).

IV. EXPERIMENTAL RESULTS

The fourth-order SI BP-ΣΔM was fabricated in a CMOS 0.8-μm double-metal single-poly technology. Fig. 4 shows the microphotograph of the modulator chip. It occupies an active area of 0.48 mm^2 and consumes 60 mW from a 5-V power supply.

For testing purposes, the modulator chip has been attached to a two-layer PCB, which has been designed following the indications in [17]. The input is applied using the HP3341A single-ended sinusoidal signal source with an off-chip resistor (for V/I conversion) connected to the input pad and then to the on-chip current buffer. The output bit streams were captured with the HP82000 data system. Kaiser ($\beta = 20$)-windowed 32 768-point FFT's were performed on each of those bit streams using MATLAB [18].

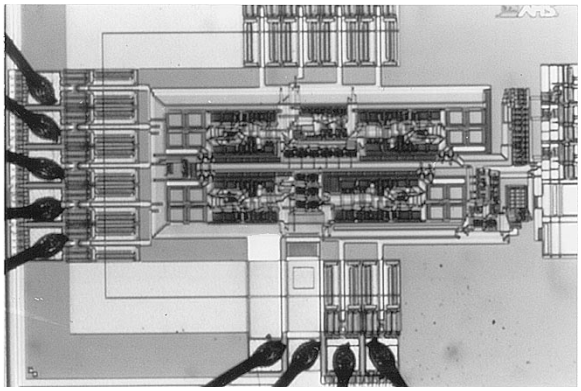

Fig. 4. Microphotograph of the modulator.

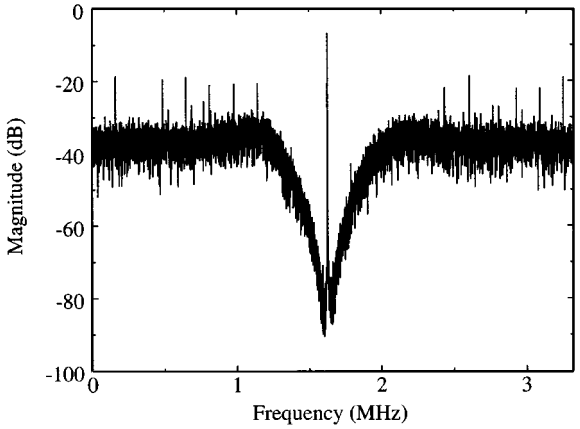

Fig. 5. Measured modulator output spectrum for a sinusoidal signal of $-$ 6 dB input level and 1.63 MHz frequency (6.67 MHz sampling frequency). 0 dB represents $\pm$ 50 μA.

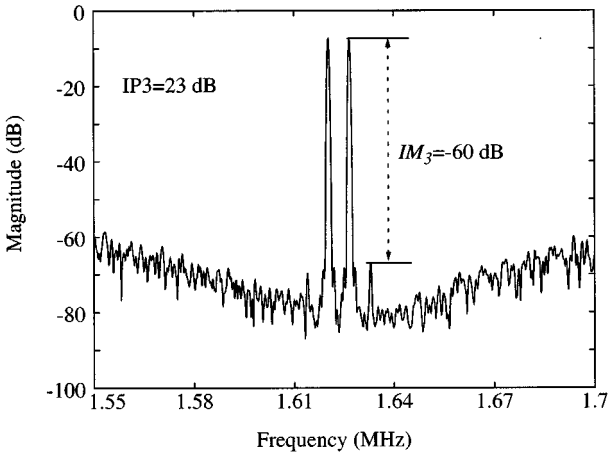

Fig. 6. Measured intermodulation distortion.

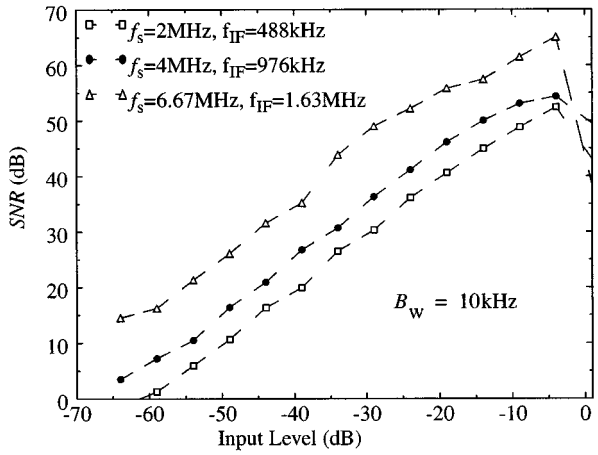

Fig. 7. Measured SNR versus input level for an input tone with different AM IF frequencies and $B_{\mathrm{W}} = 10$ kHz.

Fig. 5 shows the measured modulator output spectrum for a sinusoidal input signal of $-$6 dB input level[2] and 1.63 MHz frequency—maximum frequency in the AM range—($-$ 6 dB at 1.63 MHz) with the sampling frequency being 6.67 MHz. A correct noise shaping is obtained. The presence of out-of-band spikes suggest that the quantization error is not a white noise. However, this behavior does not degrade the modulator performance. To demonstrate this, the harmonic distortion at the modulator output has been measured at the maximum AM sampling frequency of 6.67 MHz. The input signal consisted of two $-$ 7 dB tones at 1.62 MHz and 1.63 MHz. Fig. 6 shows the central part of the output spectrum. Two third-order intermodulation products appear at both sides of the signals with amplitudes of $-$ 69.6 dB and $-$ 67 dB respectively, which corresponds to an IM_3 of $-$ 60 dB. This results in an IP_3 of 23 dB, which is low enough for digital AM receivers.

Fig. 7 shows several measured SNR versus input level curves obtained in a 10 kHz bandwidth (commercial AM bandwidth). The measurements were made with a single input tone centered at several AM frequencies. Note that, as a consequence of the larger oversampling, the best SNR peak in the AM bandwidth is 65 dB for a 6.67 MHz sampling frequency.

[2]Input level is defined as the input signal amplitude referred to the DAC output level, $\pm I_{\mathrm{ref}} = \pm$ 50 μA (= 0 dB in Fig. 5).

Table II summarizes the modulator performance when clocked at 2, 4, and 6.67 MHz for the conversion of commercial AM signals centered at 488, 976, and 1.63 MHz respectively. The DR is larger than 57 dB in all the frequency range, in accordance with the requirements of digital AM receivers.

The modulator also operates correctly at clock frequencies above AM frequencies. As an illustration, Fig. 8 shows the modulator output spectrum for a $-$ 6 dB at 3.8 MHz input tone when clocked at 16 MHz. Observe that, as a consequence of the sampling frequency increase, the settling error dominates the in-band error power, thus degrading the performance of the modulator.

Finally, Fig. 9 compares measured and predicted results. In order to separate the effect of SI errors, the half-scale SNR (corresponding to a $-$ 6 dB input level signal) was obtained for different clock rates and a 50 kHz bandwidth. Note that, for clock frequencies below about 3 MHz, the SNR increases with f_{S} at a rate of about 15 dB/octave, which corresponds to a dependence on M^5 as predicted in (7). This means that the quantization noise dominates the performance of the modulator. However, for clock frequencies above 3 MHz, the SNR increases with f_{S} at a rate of only 3 dB/octave, which reflects a dependence on

TABLE II
MEASURED PERFORMANCE OF THE MODULATOR

Parameter	f_s = 2MHz	f_s = 4MHz	f_s = 6.67MHz
SNR-peak (dB) (B_w = 10kHz)	52	54	65
DR(dB)	57	63	71
Carrier Frequency (MHz)	488kHz	976kHz	1.63MHz

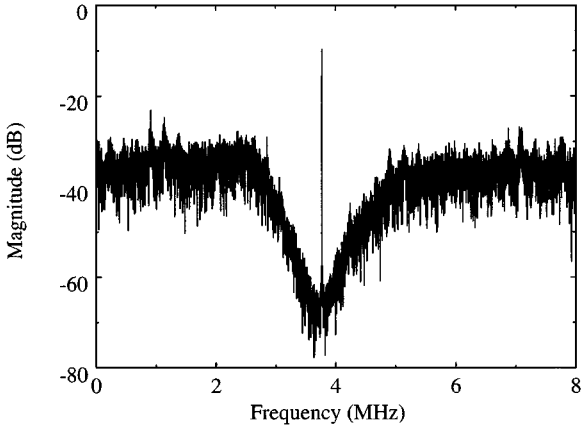

Fig. 8. Measured modulator output spectrum for a $-$ 6 dB at 3.8 MHz input tone when clocked at 16 MHz.

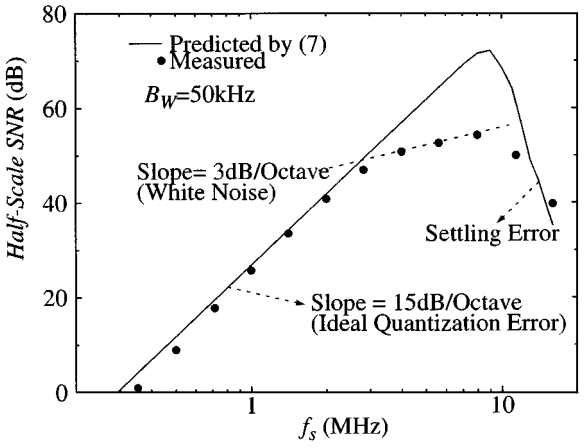

Fig. 9. Measured and theoretical Half-Scale SNR versus f_S obtained in a 50 kHz band centered at $f_S/4$.

M, and therefore, white noise is the dominant error source. Finally, for clock frequencies exceeding 10 MHz, the settling error dominates and the noise power in the signal band increases very rapidly, as predicted by theory.

Fig. 9 demonstrates that the dynamic range of the prototype modulator is limited by circuit noise, not by quantization noise. However, as shown in Section III, thermal noise of memory cells is below the measured noise floor. A possible explanation for the noise increase may be digital switching noise which is coupled to sensitive nodes via the additional MOST capacitance, C_H, connected between the substrate and the gate of the memory transistor (see Fig. 3).

V. CONCLUSIONS

A current-mode bandpass $\Sigma\Delta$ modulator has been designed in a CMOS 0.8-μm single-poly double-metal technology. The circuit has been realized using switched-current fully differential regulated-folded cascode cells. Measurements show DR > 57 dB within a 10 kHz bandwidth for signals centered on 540–1600 kHz (commerical AM bandwidth). A correct noise-shaping filtering is shown for a sampling frequency of up to 16 MHz, thus demonstrating the possibility to use SI BP-$\Sigma\Delta$M's in narrowband high frequency communication systems.

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