Analysis of Error Mechanisms in Switched-Current Sigma-Delta Modulators

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ABSTRACT

This paper presents a systematic analysis of the major *switched-current* (SI) errors and their influence on the performance degradation of ΣΔ Modulators (ΣΔMs). The study is presented in a hierarchical systematic way. First, the physical mechanisms behind SI errors are explained and a precise modeling of the memory cell is derived. Based on this modeling, the analysis is extended to other circuits of higher level in the modulator hierarchy such as integrators and resonators. After that, the study is extended to the modulator level, considering two fundamental architectures: a 2nd-order LowPass ΣΔM (2nd-LPΣΔM) and a 4th-order BandPass ΣΔM (4th-BPΣΔM). The *noise shaping* degradation caused by the linear part of SI errors is studied in the first part of the paper. This study classifies SI non-idealities in different categories depending on how they modify the zeroes of the quantization noise transfer function. As a result, closed-form expressions are found for the degradation of the signal-to-noise ratio and for the change of the *notch* frequency position in the case of 4th-BPΣΔMs. The analysis is treated considering both the isolated and the cumulative effect of errors. In the second part of the paper the impact of non-linear errors on the modulator performance is investigated. Closed-form expressions are derived for the third-order harmonic distortion and the third-order intermodulation distortion at the output of the modulator as a function of the different error mechanisms. In addition to the mentioned effects, thermal noise is also considered. The most significant noise sources of SI ΣΔMs are identified and their contributions to the input equivalent noise are calculated. All these analyses have been validated by SPICE electrical simulations at the memory cell level and by time-domain behavioural simulations at the modulator level. As an experimental illustration, measurements taken from a 0.8μm CMOS SI 4th-BPΣΔM silicon prototype validate our approach.

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I. Introduction

The 'vertiginous' scaling-down of CMOS VLSI technologies and the tendency towards *systems-on-chip* are prompting the development of new digital telecommunication devices spanning from portable gadgets (cellular phones, digital radio receivers, personal digital assistants) to modems for digital subscribe line (xDSL). In such systems, ΣΔ Modulators (ΣΔMs) have been demonstrated that are very well suited to implement the Analog-to-Digital (A/D) interface. This type of A/D Converters (ADCs), composed of a low-resolution quantizer embedded in a feedback loop, uses *oversampling* (a sampling frequency much larger than the Nyquist frequency) to reduce the quantization noise and ΣΔ modulation [1] to push this noise out of the signal band. The combined use of redundant temporal data (oversampling) and filtering (ΣΔ modulation) results in high-resolution, robust ADCs, which have lower sensitivity to circuitry imperfections and are more suitable than traditional Nyquist-rate ADCs for the implementation of A/D interfaces in modern standard CMOS technologies [2][3].

In last years, the principle of ΣΔ modulation has been extended to bandpass signals, leading to another type of ΣΔM ADCs, named BandPass ΣΔM ADCs (BPΣΔM-ADCs) [4]. These new converter architectures make it possible an early A/D conversion at Radio-Frequencies (RF) or Intermediate-Frequencies (IF) in radio systems, thus allowing digital control and programmability of both the gain and the filter coefficients of the IF stage. On the one hand, this enables the receiver to support multiple communication standards, as has been shown by a large number of CMOS BPΣΔM Integrated Circuits (IC's) [5]-[10]. On the other hand, the use of such ADCs facilitates the integration of a whole digital radio receiver onto a *mixed-signal* chip.

The analog portion of these chips must feature the required analog performance levels in standard 'digital-oriented' VLSI, what has motivated exploring analog design techniques compatible with standard CMOS. This is the case of *switched-current* (SI) circuits [11], which during the last decade have been explored for the construction of different analog functions, including filtering [12] and ADCs [13][14], in digital CMOS.

The SI technique is based on the principle that, by storing the gate voltage of an MOS transistor, the current flowing through it can be memorized. In addition to its obvious compatibility with a standard process (poly-poly capacitors are not needed), the SI technique offers other advantages. On the one hand, as signal carriers are currents instead of voltages, the signal range

is not limited by supply voltages. This fact makes SI a suitable technique for low-voltage supplies. On the other hand, as operational amplifiers are not needed, fast operation can be achieved with low power consumption [12].

The mentioned advantages have been barely demonstrated through actual practical circuits. Thus, in the case of ΣΔMs, performances featured by reported SI ICs are well bellow those of Switched-Capacitor (SC) counterparts, even if the latter are realized in standard technologies without good passive capacitors. Such poorer performances are partly due to the larger influence of SI non-idealities, as well as to the incomplete modeling of their influence on the performance of ΣΔMs.

This paper aims at solving these problems by means of a systematic analysis of error mechanisms in SI ΣΔMs. The study is treated with two well-different objectives: on the one hand, the obtainment of behavioural models that support a fast and precise time-domain simulation; on the other hand, the attainment of approximate equations which, in closed-form, express the effect of each non-ideality at different levels of the modulator hierarchy as a function of itself and other design variables. As a result, closed-form expressions are found for the quantization noise transfer function deviations, the in-band noise power, and the harmonic distortion. This allows the designer to control the non-idealities either through the choice of MOS transistor sizes and bias currents (sizing) or by means of proper circuit techniques.

The analysis described here will focus on two fundamental single-loop architectures: a 1-bit 2nd-order LowPass ΣΔM (2nd-LPΣΔM) and a 1-bit 4th-order BPΣΔM (4th-BPΣΔM). These modulators are easy to understand and simple to design, are capable of providing high resolution together with large tolerance to imperfections and robust stable operation [2]. Nevertheless, this study can be easily extended to other architectures such as multi-stage cascade modulators [2][5]. In these architectures, the error contributions due to the first stage – usually a single loop ΣΔM like those treated in this work – constitute the most significant degrading factor of the overall modulator performance.

The paper is organized as follows. Section II describes the modulator architectures under study. Section III analyses the non-idealities of SI memory cells, putting special emphasis on signal-dependent error mechanisms. In particular, a new model for the non-linear transient behaviour is presented. Section IV extends the analysis to other higher hierarchical level SI circuits – integrators and *resonators* – in order to study the effect of SI errors on the in-band noise power of ΣΔMs. The impact on the harmonic distortion is carried out in Section V and Thermal noise is treated in Section VI. Section VII validates the study through measurements taken from

a 4th-BPΣΔM IC realized using fully differential SI regulated-folded cascode circuits in a standard 0.8μm CMOS technology. Finally, conclusions are given in Section VIII.

II. Modulator Architectures

Fig.1 shows the Z-domain block diagram of the ΣΔMs under study: Fig.1(a) is a 1-bit 2nd-LPΣΔM and Fig.1(b) is a 1-bit 4th-BPΣΔM. The latter has been obtained by applying the transformation $z^{-1} \rightarrow -z^{-2}$ to the former. Assuming that the quantization error is modelled as a white, additive noise, the Z-domain output of both modulators is given by [2]:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \tag{1}$$

where $X(z)$ and $E(z)$ are respectively the Z-transform of the input signal and the additive quantization noise source. The ideal Signal Transfer Function, ($S_{TF}(z)$) is of the *all-pass* type for both modulators. On the other hand, the ideal quantization Noise Transfer Function (N_{TF}) is of the *high*-pass type for the 2nd-LPΣΔM and *bandstop* type for the 4th-BPΣΔM, respectively,

$$N_{TF}(z) = \begin{cases} (1 - z^{-1})^2 & \text{for the lowpass modulator} \\ (1 + z^{-2})^2 & \text{for the bandpass modulator} \end{cases} \tag{2}$$

By making $z = \exp(j2\pi f / f_s)$ – with f_s being the sampling frequency – it can be seen that $N_{TF}(f)$ has 2 transmission zeroes at dc for the 2nd-LPΣΔM which are shifted to $f_s/4$ for the 4th-BPΣΔM – a consequence of the transformation $z^{-1} \rightarrow -z^{-2}$. Fig.2(a)-(b) illustrate the filtering performed by both modulators. The input signal is allowed to pass while, at the same time, most of the quantization noise power is "shaped" so that it is pushed out of the signal band. In both cases, the quantization noise is rejected with a second-order filter.

The *in-band* quantization noise power can be calculated by integrating the output noise Power Spectral Density (PSD) within the signal band, B_w,

$$P_Q = \left\{ \begin{array}{l} \int_0^{B_w} 2S_Q \left|N_{TF}(f)\right|^2 \Big|_{\text{lowpass}} df \\ \int_{f_s/4 - B_w/2}^{f_s/4 + B_w/2} 2S_Q \left|N_{TF}(f)\right|^2 \Big|_{\text{bandpass}} df \end{array} \right\} \cong \frac{\Delta^2 \pi^4}{60 M^5} \tag{3}$$

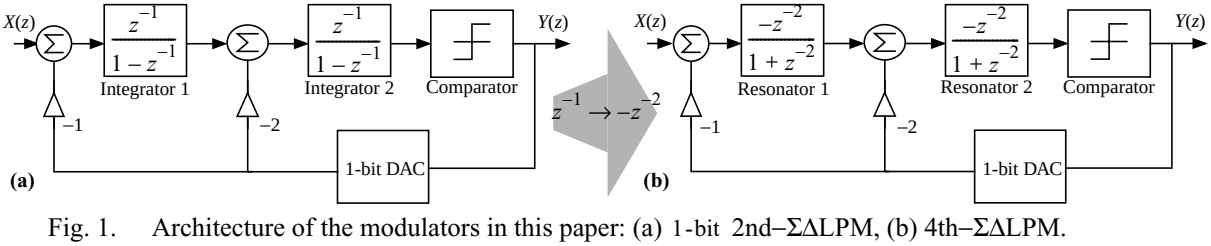

Fig. 1. Architecture of the modulators in this paper: (a) 1-bit 2nd–ΣΔLPM, (b) 4th–ΣΔLPM.

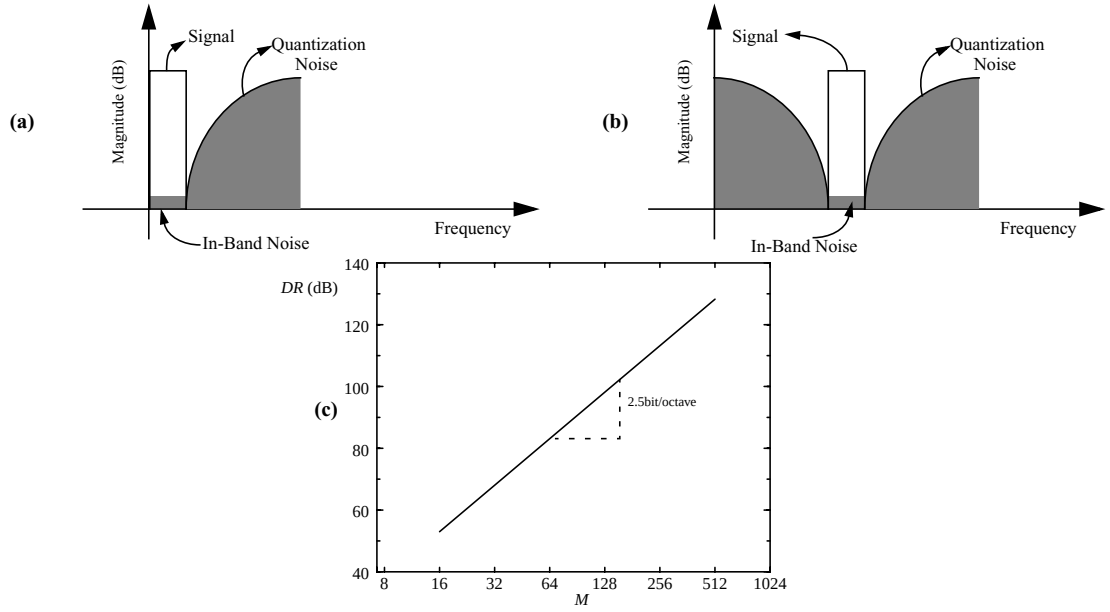

Fig. 2. Filtering functions in: (a) 2nd-LP-ΣΔMs; (b) 4th-BPΣΔMs. (c) DR vs. M.

where $S_Q = \Delta^2/(12 f_s)$ is the PSD of the quantization noise error, Δ is the quantization step, and $M \equiv f_s/(2B_w)$ is the *oversampling ratio.* From (3), and assuming that the modulator input is a sinewave of amplitude A_x, the Signal-to-Noise Ratio (SNR) at the output results in:

$$SNR = \frac{A_x^2}{2P_{\mathrm{Q}}} = \frac{30A_x^2M^5}{\pi^4\Delta^2} \tag{4}$$

The modulator Dynamic Range (DR) is obtained by making $A_x = \Delta/2$ in the above expression. In this ideal scenario, the resolution increases with M at a rate of about 2.5-bit/octave as illustrated in Fig.2(c) where DR is displayed as a function of M.

The first step towards the design of ΣΔMs is choosing a suitable architecture to realize the integrators and resonators. Regarding the latter, several alternatives have been described in the literature [4]-[10]. Among the others, we will adopt a structure consisting of a feedback cascade of two *Lossless Discrete Integrators* (LDIs) because it keeps the poles inside the unit circle upon changes due to errors of the feedback loop gain. For that reason, this has been the resonator – and consequently the integrator – structure chosen to implement the modulators in this paper[†1], whose architectures are depicted in Fig. 3. Note that, in both modulators, the required feedback loop delay has been realized through two additional delay blocks. Also, the scaling factors have been optimized to obtain a similar signal range for both integrators (resonators), giving

$$A_{\mathrm{DAC2}} = -A_{\mathrm{DAC1}} = 1\,;\; A_{\mathrm{INT1}} = A_{\mathrm{RES1}} = 1/2 \tag{5}$$

[†1] All analyses described in this paper for LD integrators can be extended to FE integrators following the same methodology described here.

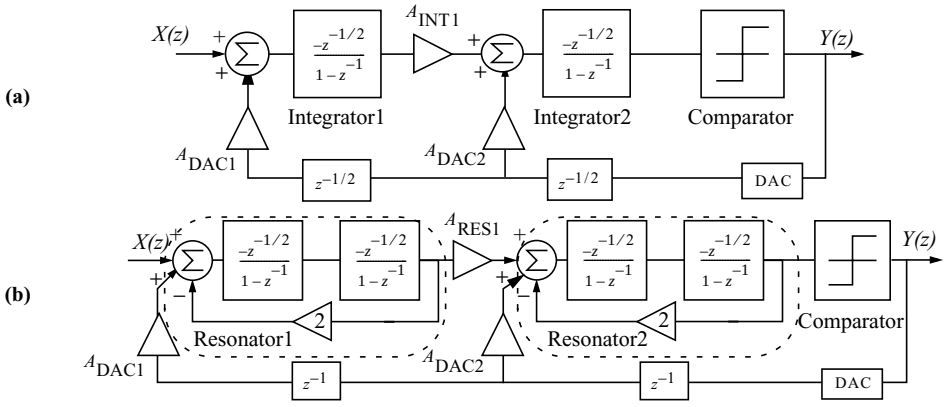

Fig. 3. Block diagram of the LDI-based ΣΔMs. (a) 2nd-LPΣΔM. (b) 4th-BPΣΔM.

The modulators in Fig. 3 present the *SNR* given in (4). However, such an ideal feature can only be achieved provided that the building blocks in Fig.3 are realized without errors. Modeling of these errors and circuit optimization are needed to cope with the *SNR* degradation observed in actual circuits realized using SI memory cells.

III. Fundamental limitations in SI memory cells

According to [11], the main errors responsible for the non-ideal behaviour are: *finite output-input conductance ratio error*, *charge injection error*, *incomplete settling error*, *mismatch error*[†2] and *thermal noise*. Although the physical mechanisms behind all of them have been described in literature [12]-[17], their influence has been studied only at the memory cell level. Bearing this in main, this section analyses the effect of each of the above-mentioned errors with two objectives; on the one hand, to provide precise closed-form expressions for the offset, linear gain error and Harmonic Distortion (HD) caused by SI non-idealities at the memory cell level; on the other hand, to build analytical models which allow us to extend this analysis to other circuits of higher hierarchy level in ΣΔMs such as integrators and resonators.

A. Finite output-input conductance ratio error

Let us consider the second-generation SI memory cell shown in Fig.4(a). The drain node of the memory transistor, M, will be at different voltages on both clock phases, ϕ_1 and ϕ_2. This voltage variation, v_{ds}, is translated into an error on the memorized drain-source current, i_{ds}, basically through two mechanisms [15]. The first is caused by the channel length modulation

[†2] The study described here is based on second-generation memory cells [11]. These cells do not exhibit mismatch errors because the same transistor is used to implement both the sink and source currents. However, general SI circuits require scaling coefficients which are implemented by current mirrors thus being subject to mismatches in the large signal transconductance and the threshold voltage. Their effects, analysed in [34], will be taken into account in the study of SI integrators and resonators of the next section.

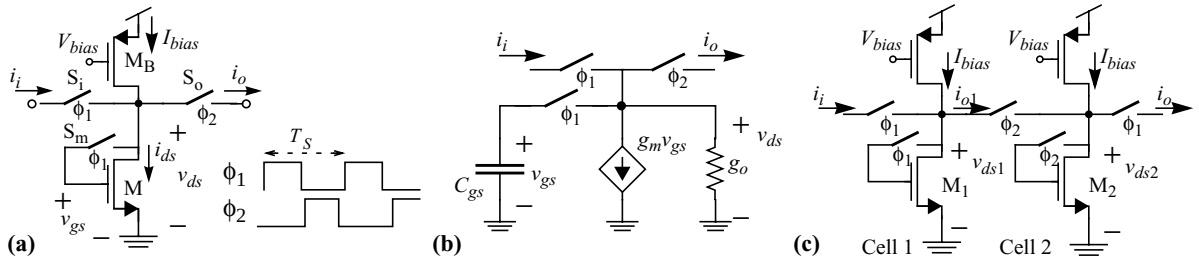

Fig. 4. Linear model for the memory cell with finite output-input conductance error. a) Simple second-generation memory cell. b) Equivalent circuit. c) Connection of two cells in series.

effect of both M and the bias current source transistor, M_B. The second one is due to the charge which flows through the drain-gate overlap capacitance, C_{dg}, into the gate-source capacitance, C_{gs}, thus causing an error on the gate-source voltage, v_{gs}, and consequently on i_{ds}. These two mechanisms of error can be modelled as a finite output conductance, g_o, connected in parallel with the memory transistor [11][15].

Assuming ideal switches, a memory cell can be modelled by the equivalent circuit shown in Fig.4(b). In this circuit g_m and g_o represent the input and output conductances of the cell, respectively given by [16][17]:

$$\begin{aligned} g_m(m_i(t)) &= g_{mQ}\sqrt{1 + m_i(t)} \\ g_o(m_i(t)) &= g_{dsnQ}[1 + m_i(t)] + g_{dspQ} + k_C g_{mQ}\sqrt{1 + m_i(t)} \end{aligned} \tag{6}$$

where $k_C = C_{dg}/(C_{dg} + C_{gs})$; $g_{mQ} \equiv \sqrt{2\beta I_{bias}}$ and $\beta \equiv \mu_o C_{ox} W/L$ are the small-signal and large-signal transconductances of M, respectively; $g_{dsnQ} = \lambda_n I_{bias}$ and $g_{dspQ} = \lambda_p I_{bias}$ are the small-signal output conductances of M and M_B respectively; λ_n and λ_p are respectively the channel length modulation parameter for M and M_B; and $m_i(t) \equiv i_i(t)/I_{bias}$, with i_i and I_{bias} being the input and bias current, respectively.

Let us consider the connection of two cells in series shown in Fig.4(c). Assuming that both cells are modelled by Fig.4(b), and that the stationary state is reached during the sampling phase (C_{gs} is neglected), it can be shown that the equation governing the behaviour of cell1 is:

$$i_{o1,n} = \frac{-i_{i,n-1/2}}{\left(1 + \dfrac{g_o(m_{i,n-1/2})}{g_m(m_{i,n-1/2})}\right)\left(1 + \dfrac{g_o(m_{i,n-1/2})}{g_m(m_{o,n}) + g_o(m_{o,n})}\right)} \tag{7}$$

where $m_{o,n} = i_{o1,n}/I_{bias}$ [†3].

Assuming that the memory cell operates under mild distortion conditions [18], i.e, $|m_{i,n-1/2}| = |m_{o,n}| \ll 1$, and performing a Taylor series expansion of (7), yields[†4]:

[†3] The notation $i_{o,n}$ is used to represent $i_o(nT_s)$, where $n = 1, 2, \ldots$ and T_s is the sampling period.

[†4] In the ideal case $i_{o,n} = -i_{n-1/2}$. On the other hand, in the regime of mild distortion, $|i_{o,n}| \cong |i_{i,n-1/2}|$.

$$i_{o1,\,n} \cong -(1-\varepsilon_g) i_{i,\,n-1/2} + \varepsilon_{g2} i_{i,\,n-1/2}^2 + \varepsilon_{g3} i_{i,\,n-1/2}^3 + \ldots + \varepsilon_{gk} i_{i,\,n-1/2}^k \tag{8}$$

where

$$\varepsilon_g \equiv 2 g_{oQ} / g_{mQ} \tag{9}$$

(with $g_{oQ} \equiv g_{dsnQ} + g_{dspQ} + k_C g_{mQ}$) is defined as the *linear finite output-input conductance ratio error* and ε_{gk} for $k > 1$ represents the k-order non-linear gain error, the most significant being:

$$\varepsilon_{g2} \cong \frac{(1-\varepsilon_g)(2 g_{dsnQ} + k_C g_{mQ})}{g_{mQ} I_{bias}} \qquad \varepsilon_{g3} \cong \frac{(1-\varepsilon_g)(3 g_{dsnQ} + 3 g_{dspQ} + 2 k_C g_{mQ})}{4 g_{mQ} I_{bias}^2} \tag{10}$$

Assuming that i_i is a sinewave of amplitude I_i, the output current will contain harmonics of the input signal frequency f_i. The most significant HD terms are the second- and the third-order, respectively given by:

$$HD_2 \equiv \frac{\varepsilon_{g2}}{2(1-\varepsilon_g)} I_i \cong \frac{\varepsilon_g}{2} M_i \qquad HD_3 \equiv \frac{\varepsilon_{g3}}{4(1-\varepsilon_g)} I_i^2 \cong \frac{3}{32} \varepsilon_g M_i^2 \tag{11}$$

where $M_i = I_i / I_{bias}$ is the modulation index and $k_C \ll 1$ has been assumed – as it occurs in most practical cases. Note that, as HD_2 and HD_3 are proportional to ε_g, they can be reduced by using the same strategies to attenuate ε_g: either by increasing g_m [20] or by reducing g_o [21].

The above analysis has been verified through a transient simulation of the series connection of two memory cells using HSPICE with BSIM3v2 MOS transistor models [19]. Fig.5(a) represents HD_2 and HD_3 vs M_i for $W/L = (10/2)\mu\text{m}/\mu\text{m}$, $g_{mQ} = 268\mu\text{A/V}$, $g_{dsnQ} = 1.83\mu\text{A/V}$, $C_{dg} = 56\text{fF}$, $C_{gs} = 1\text{pF}$ and ideal bias current sources of $100\mu\text{A}$. The effect of g_{dsn} is shown in Fig.5(b) by plotting HD_2 vs L for $W = 5L$ and $I_i = I_{bias}/2$. A good agreement is obtained between electrical simulation and (11).

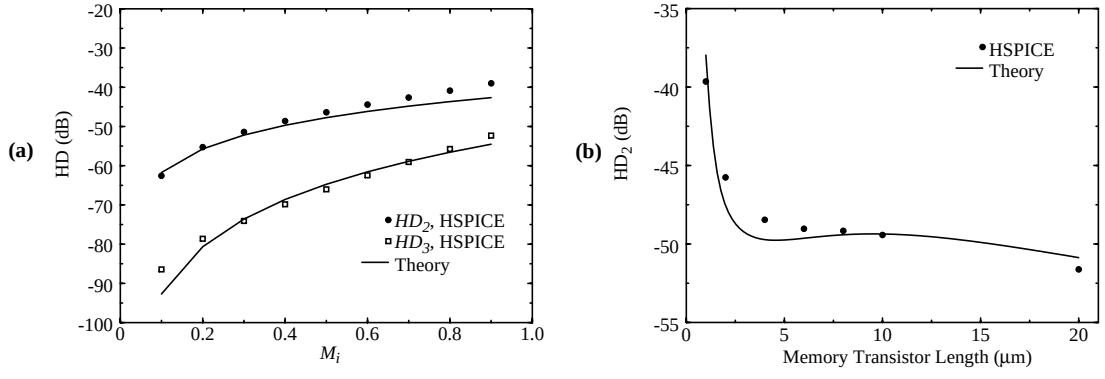

Fig. 5. Harmonic distortion due to the non-linear output-input conductance ratio error. a) HD_2 and HD_3 vs. the modulation index. b) HD_2 vs. memory transistor length for $I_i = 0.5 I_{bias}$.

B. Charge injection error and clock feedthrough

In practice, switches in Fig.4(a) are realized through MOS transistors. During the turn-off transient of ϕ_1, the channel mobile charges of the memory switch, S_m, (see Fig.4(a)) flow out of its drain, substrate, and source. Part of this charge is dumped on the memory transistor gate-source capacitance, C_{gs}. In addition, the fast changing of the gate voltage causes the channel charge to flow through the gate-diffusion overlap capacitances, C_{ol}, into both the source and drain of S_m. These two phenomena cause a variation on the memory gate-source voltage of M – often known as *charge injection* or *clock feedthrough error* – which can be expressed as [11][23],

$$\Delta v_q \equiv \frac{\Delta q_{inj}}{C_{gs}} = \Delta V_{q_{off}} - \xi_q v_{gs} \tag{12}$$

with

$$\Delta V_{q_{off}} = \frac{\alpha_q}{C_{gs}}[C_{ox} W_{s_{eff}} L_{s_{eff}} (V_H - V_T)] + \frac{C_{ol}}{C_{gs}}(V_H - V_L);\ \xi_q = \frac{\alpha_q C_{ox} W_{s_{eff}} L_{s_{eff}}}{C_{gs}}\left(1 + \frac{\gamma}{3}\right) \tag{13}$$

where V_H and V_L are the switch-on and switch-off voltages of S_m; α_q is the fraction of channel charge injected into C_{gs} (typically $\alpha_q = 1/2$)[†5]; γ is the body effect coefficient; and $W_{s_{eff}}$ and $L_{s_{eff}}$ are the effective width and length of S_m, respectively.

Assume that the cell in Fig.4(a) is ideal except for the charge injection error. At the end of clock phase ϕ_1 of period $(n - 1/2)T_s$, the gate-source voltage of M can be expressed as

$$v_{gs,\, n-1/2} = V_T + (V_{gs} - V_T)\big|_Q \sqrt{1 + m_{i,\, n-1/2}} \tag{14}$$

where $(V_{gs} - V_T)\big|_Q$ stands for the operating-point overdrive voltage.

When S_m turns off, its channel charge causes an error Δv_q in the gate voltage memorized at the end of clock phase ϕ_1. In the clock phase ϕ_2 of period nT_s, the output current is given by:

$$i_{o,\, n} = I_{bias} - \frac{\beta}{2}(v_{gs,\, n-1/2} + \Delta v_q - V_T)^2 = -i_{i,\, n-1/2} - g_{mQ}\sqrt{1 + m_{i,\, n-1/2}}\,\Delta v_q - \frac{\beta}{2}(\Delta v_q)^2 \tag{15}$$

Substituting (12) in (15) and performing a Taylor expansion series for $m_i \ll 1$ yields:

$$i_{o,\, n} \cong I_{q_{off}} - (1 - \varepsilon_q) i_{i,\, n-1/2} + \varepsilon_{q_2} i^2_{i,\, n-1/2} + \varepsilon_{q_3} i^3_{i,\, n-1/2} + \ldots \tag{16}$$

where

$$\varepsilon_q \cong 2\xi_q - \frac{(\Delta V_{q_{off}} - \xi_q V_T)}{(V_{gs} - V_T)\big|_Q} = \frac{I_{q_{off}}}{2 I_{bias}} + \xi_q \tag{17}$$

[†5] Assuming fast clock transitions, the channel charge splits equally between source and drain [23].

is the *linear charge injection error,* and

$$I_{q_{off}} \cong 2I_{bias}\left[\xi_q - \frac{(\Delta V_{q_{off}} - \xi_q V_T)}{(V_{gs} - V_T)\big|_Q}\right]; \varepsilon_{q2} \cong \frac{(\Delta V_{q_{off}} - \xi_q V_T)}{4I_{bias}(V_{gs} - V_T)\big|_Q}; \varepsilon_{q3} \cong \frac{-(\Delta V_{q_{off}} - \xi_q V_T)}{8I_{bias}^2(V_{gs} - V_T)\big|_Q} \quad (18)$$

represents the output offset current, the second- and the third-order gain error, respectively. Assuming $\xi_q \ll 1$, the corresponding HD coefficients can be approximated by:

$$HD_2 \cong \frac{-\varepsilon_q}{8} M_i \qquad HD_3 \cong \frac{\varepsilon_q}{32} M_i^2 \quad (19)$$

which, as in the case of ε_g, can be attenuated by reducing ε_q. For this purpose, several compensation techniques have been proposed in literature [24]-[27]. Among the others, the so-called S^2I [28] has been the most extensively used by SI designers. The S^2I cell divides the sampling time into two steps; in the first step, the input current is memorized with an error Δi_q by a coarse memory transistor; in the second step, that error is sampled by a fine memory transistor with an error $\Delta(\Delta i_q) \cong (\Delta i_q)^2$.

The S^2I technique is not well suited for BP-ΣΔMs because the input signal is not stationary during the sampling phase since is typically located at $f_s/4$. Hence, unless a Sampling-and-Hold (S/H) circuit is placed at the modulator front-end, the advantages of S^2I memory cells are destroyed. An alternative is using Fully Differential (FD) cells which, in combination with dummy switches, notably reduce ε_q as compared to the single-ended case [11]. FD cells also cancel even-order harmonics, thus achieving higher level of performance than their single-ended counterparts. For that reason, in what follows, special emphasis will be put on FD cells.

C. Incomplete settling error

During the sampling phase the input current which is applied to a memory cell charges (or discharges) C_{gs}. This transient evolution reaches the steady state when the value of v_{gs} is such that i_{ds} is equal to $(I_{bias} + i_i)$. However, if the charging process is not completed during the sampling period, an error voltage is stored into C_{gs}, thus causing an error in the memorized i_{ds}, which is often referred to as an *incomplete settling error* – represented in the SI context by ε_s.

There have been several attempts to analyse ε_s [29]-[32]. Among the others, a precise study was presented in [32], but its mathematical complexity precludes to extend its usage to ΣΔMs. The approach in this section enables hierarchical systematic analysis of SI circuits containing heavily coupled memory cells as will be demonstrated in Section V.

Fig.6(a) shows a FD SI memory cell. In the analysis that follows, it will be assumed that

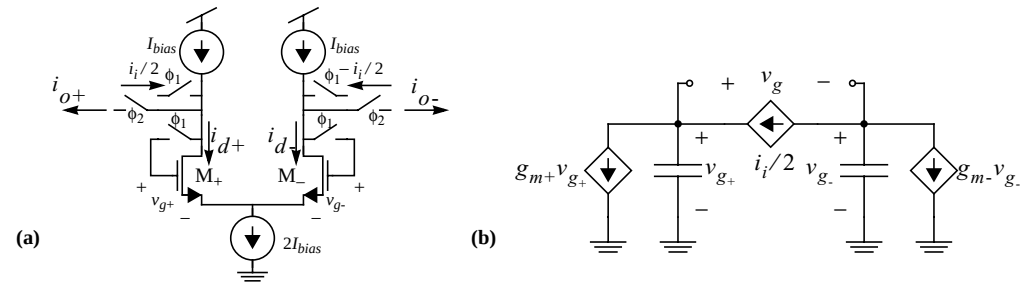

Fig. 6. FD memory cell with settling error. a) Schematic. b) Equivalent circuit during the sampling phase.

the cell is ideal except for ε_s. Besides, in most practical cases the time constant formed by the drain-source capacitance and the switch-on resistance is much smaller than $\tau = C_{gs}/g_{mQ}$. In such a case, the cell can be modelled by the equivalent circuit in Fig.6(b) during the sampling phase, ϕ_1. In this circuit, the large-signal behaviour is modelled by $g_{m+,-}$, which represents the transconductances of $M_{+,-}$, given by $g_{m+,-} = g_{mQ}\sqrt{1 + m_{i+,-}}$, where $m_{i+,-} = i_{i+,-}/I_{bias}$ and $i_{i+,-} = \pm i_i/2$ [30].

Assuming that i_i keeps stationary during ϕ_1, and that the switch becomes OFF at $(n-1/2)T_s$ the differential drain current, $i_d = i_{d+} - i_{d-}$, can be calculated by solving the circuit in Fig.6(b) for the initial condition $v_{g_{+,-}} = v_{g_{+,-},\,n-1}$, giving:

$$i_{d,\,n-1/2} = i_{i,\,n-1/2}[1 - \Psi(m_{i,\,n-1/2})] + i_{d,\,n-1}\Psi(m_{i,\,n-1/2}) \tag{20}$$

where $\Psi(m_{i,\,n}) = \frac{1}{2}\left[\exp\left(-\frac{T_s}{2\tau}\sqrt{1+m_{i,\,n}}\right) + \exp\left(-\frac{T_s}{2\tau}\sqrt{1-m_{i,\,n}}\right)\right]$ and $m_{i,\,n} = i_{i,\,n}/(2I_{bias})$. At the end of the n-th hold phase, ϕ_2, the differential output current, $i_o = i_{o+} - i_{o-}$, is given by:

$$i_{o,\,n} = -i_{d,\,n-1/2} = -i_{i,\,n-1/2}[1 - \Psi(m_{i,\,n-1/2})] + i_{o,\,n-1}\Psi(m_{i,\,n-1/2}) \tag{21}$$

where $i_{d,\,n-1} = i_{d,\,n-3/2}$ has been considered.

To calculate the HD, the function $\Psi(\cdot)$ could be approximated by a polynomial inside a given interval. For that purpose, we have combined Taylor series expansion for $m_i \ll 1$ and numerical fitting for $-0.5 \le m_i \le 0.5$, $0.01\% < \varepsilon_s < 10\%$, to obtain:

$$\Psi(i_{i,\,n-1/2}) \cong \varepsilon_s + \varepsilon_{s2} i^2_{i,\,n-1/2} \tag{22}$$

where

$$\varepsilon_s = e^{-k_s} \tag{23}$$

is the *linear settling error*, $\varepsilon_{s2} = \alpha_s \varepsilon_s k_s[(1+k_s)/(32I^2_{bias})]$ with $k_s = T_s/(2\tau)$, and $\alpha_s = 3/2$ is a fitting parameter. Fig.7(a) shows a good agreement between (22) and the exact expression of $\Psi(\cdot)$ for different values of ε_s. From (21) and (22):

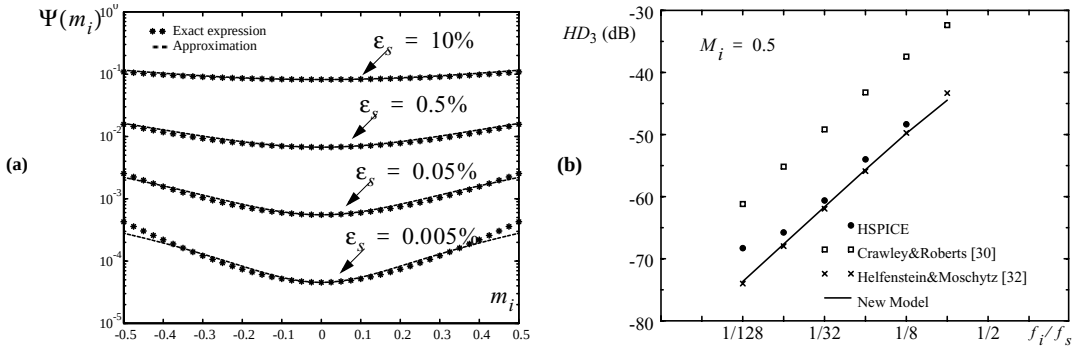

Fig. 7. Settling error. a) Approximation of $\Psi(m_i)$ .b) Comparison with HSPICE and previous models.

$$i_{o,n} \cong -(1-\varepsilon_s)[i_{i,n-1/2} - \varepsilon_{s2}(i^3_{i,n-1/2} + i^2_{i,n-1/2} i_{o,n-1})] + \varepsilon_s i_{o,n-1} \tag{24}$$

The analysis of HD_3 (the dominant HD coefficient in FD circuits) can be simplified if i_o is approximated by its first-order harmonic, such that $i_{o,n} \cong -I_i \sin(2\pi f_i n T_s)$. Thus, performing a Fourier series expansion of (24) it can be shown that

$$HD_3 \cong \frac{\alpha_s \varepsilon_s k_s (1+k_s)}{16(1-\varepsilon_s)} M_i^2 \sin\left(\pi \frac{f_i}{f_s}\right) \tag{25}$$

where $M_i = I_i/(2I_{bias})$.

Predictions given by (25) agree with HSPICE and the model in [32] as shown in Fig.7(b) where HD_3 vs. f_i/f_s is plotted for $g_{mQ} = 82.8\mu A/V$, $C_{gs} = 22.1pF$, $I_{bias} = 20\mu A$, $M_i = 0.5$ and $f_s = 512kHz$ – the same example as in [30][32]. However, as a difference to [32], the approach here can also be used for predicting the HD of higher-level SI blocks as will be demonstrated in Section V.

D. Non-linear sampling process

In the previous analysis it has been assumed that the input signal remains constant during the sampling phase. This assumption applies in the following cases:

- The input signal is supplied by another cell.
- The memory cell follows a S/H circuit.
- The ratio f_i/f_s is small (less than $1/10$).

Let us consider that i_i is a continuous-time sinewave with $I_i = I_{bias}/2$ and $f_i \cong f_s/4$ [†6]. Fig.8(a) shows the transient evolution of i_d for the FD cell of Fig.6. Observe that, in this case, i_i will change during the sampling phase up to $I_i/\sqrt{2}$ [†7], thus causing an additional error to ε_s. This additional error, dominantly non-linear, will cause an extra HD which cannot

[†6] This is the typical case of a front-end cell in a BP-ΣΔM.

[†7] The maximum signal variation during sampling phase is given by: $I_i\left|\sin[2\pi f_i(t+T_s/2)] - \sin[2\pi f_i t]\right|\Big|_{f_i = f_s/4} \le I_i/\sqrt{2}$.

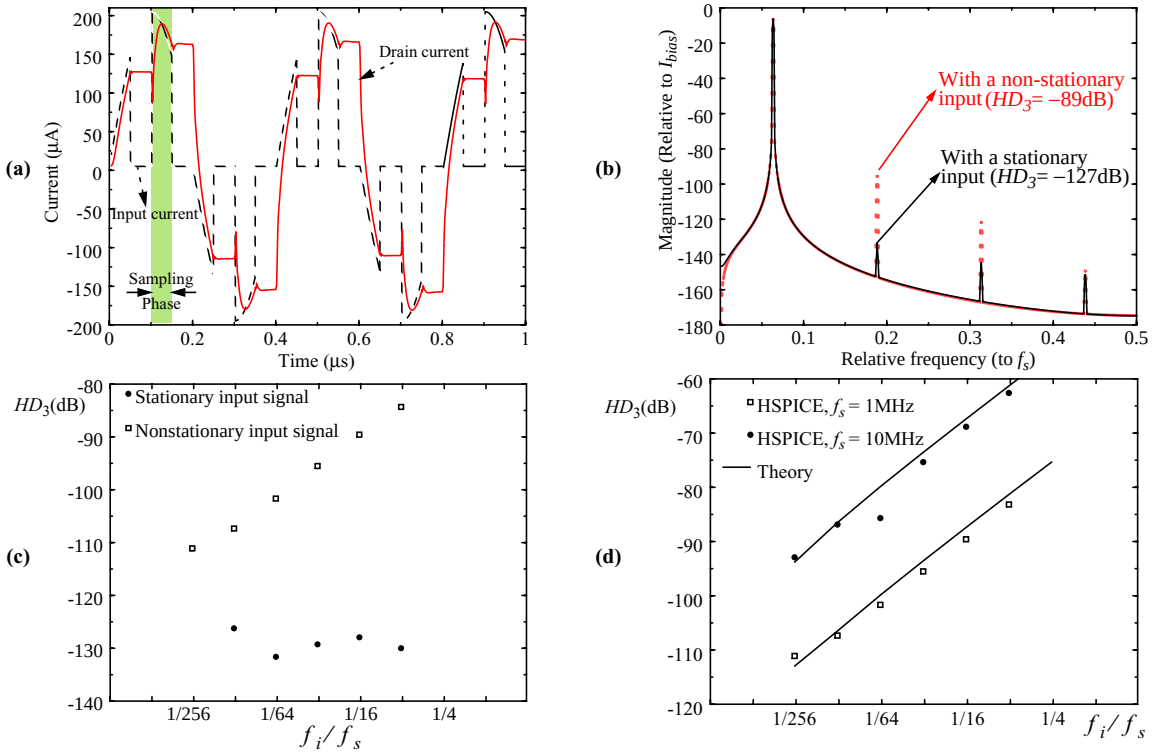

Fig. 8. Non-linear sampling error. a) Transient evolution of i_d for an input sinewave with $I_i = I_{bias}/2$, and $f_s = 10\text{MHz}$. Comparison between HD_3 caused by a non-stationary input signal and a stationary input signal. b) Output spectra for $f_i = f_s/16$. c) HD_3 vs. f_i/f_s (HSPICE). d) Theory vs HSPICE.

be explained by analysing the step-response of the cell, i.e, considering stationary input signals during the sampling phase. This is shown in Fig.8(b) by comparing the simulated (HSPICE) output spectra of the FD cell in Fig.6 (with $I_{bias} = 100\mu\text{A}$, $I_i = I_{bias}/2$, $f_i = f_s/16$, $g_{mQ} = 268\mu\text{A/V}$, $C_{gs} = 1\text{pF}$ and $f_s = 1\text{MHz}$), corresponding to both a sampled-and-held (stationary) and a continuous-time (non-stationary) input tone. It is clear that the latter presents much more HD ($HD_3 = -89\text{dB}$) than the former ($HD_3 = -127\text{dB}$). However, in both cases ε_s is negligible ($\tau = 3.7\text{ns}$, and $T_s = 1\mu\text{s}$), meaning that the extra HD_3 is caused by the non-linear sampling process and, as illustrated in Fig.8(c), becomes lower as f_i/f_s is reduced. This phenomenon is analysed in Appendix I by using the Volterra series method [33], showing that HD_3 due to the non-linear sampling is approximately given by:

$$HD_3(f_i) \cong \frac{-3}{16} j\pi f_i \tau M_i^2 \tag{26}$$

which is in close agreement with HSPICE as shown in Fig.8(d) where HD_3 is plotted vs. f_i/f_s and different values of f_s. Note that, although $\varepsilon_s \cong 6 \cdot 10^{-59}$ for $f_s = 1\text{MHz}$, high levels of HD appear: $HD_3 \in (-95, -60)\text{dB}$.

E. Thermal noise

The electrical noise of a MOS transistor can be modelled by a noisy current source, i_n, connected in parallel with a noiseless transistor, with a PSD given by:

$$S_{i_n}(f) = \frac{8}{3}kTg_{mQ} + \frac{k_f g_{mQ}^2}{C_{ox}WL|f|} \qquad 0 < f < \infty \tag{27}$$

where the first term in the right-hand side represents the thermal noise PSD and the second term is the flicker noise with k_f being a technology-dependent parameter. Fig.9(a) shows a simple second-generation memory cell including its noise sources. The equivalent noise current at the output of the cell can be derived by determining the equivalent noise voltage at the gate of M_1, v_{neq}, and multiplying its PSD by g_{m1}^2, where g_{m1} stands for the small-signal transconductance of M_1. To do this, the equivalent PSD of each noise source at the gate of M_1 is derived by computing the transfer function from said noise source to the gate of M_1. Assuming that they are not correlated they can be added to obtain the PSD of v_{neq}. However, because of the discrete-time nature of memory cells, the transfer function from each noise source to the gate of M_1 will differ from one clock phase to the other. Hence, the output equivalent noise is found by analysing the equivalent circuit in Fig.9(b) for each clock phase and adding them – assuming they are not correlated . Doing this, it is shown that the total output noise PSD of the cell is given by [27]:

$$S_{i_{neq}}(f) \cong S_{i_{nm}} \begin{cases} \left(\frac{\tau_s}{T_s}\right)^2 + \left(\frac{\tau_H}{T_s}\right)^2 \sin c^2(\pi f \tau_H), & f_s \geq 2BW_n \\ \left(\frac{\tau_s}{T_s}\right) + \frac{2BW_n}{f_s}\left(\frac{\tau_H}{T_s}\right)^2 \sin c^2(\pi f \tau_H), & f_s < 2BW_n \end{cases} \tag{28}$$

where $S_{i_{nm}} = (8/3)kT(g_{m1} + g_{m2})$; τ_s and τ_H are the duration of the sampling and the hold phases, respectively; BW_n represents the equivalent noise bandwidth and it has been assumed that flicker noise sources are removed as a consequence of the *autozero effect* [11].

The above result is valid not only for basic memory cells like that shown in Fig.9, but also to more advanced cells by simply replacing the corresponding value of $S_{i_{nm}}$ in (28).

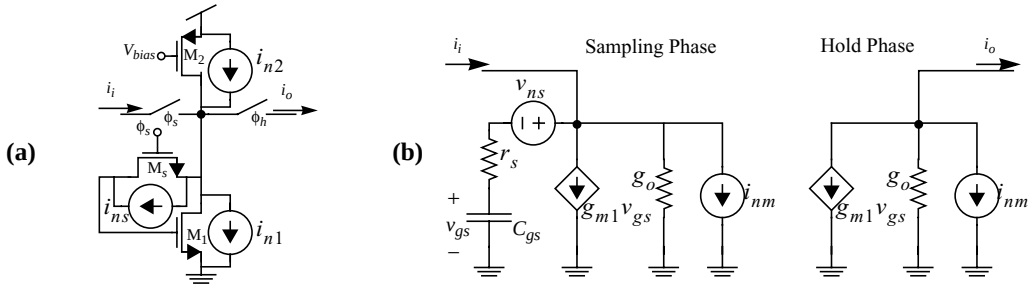

Fig. 9. Noise analysis of a memory cell. a) Noise sources of the cell. b) Equivalent circuit.

IV. Effect of SI errors on the noise-shaping of ΣΔ modulators

In the following sections, the previous analysis will be extended from the memory cell level to other higher hierarchical level circuits such as integrators, resonators and finally, ΣΔMs. This study will be separated into two parts. In the first part, shown in this section, only the contribution of linear errors will be considered and closed-form expressions will be derived for the SNR degradation. In the second part, described in Section V, the non-linear contribution of the SI errors will be taken into account.

A. Cumulative effect of SI errors on the performance of SI memory cells

The isolated influence of main SI errors on the memory cell performance has been analysed in Section III. For our study we are interested not only in the separate effect but also on their cumulative influence on the degradation of SI circuits.

Let us consider the cascaded memory cells shown in Fig.10(a). During clock phase ϕ_1, Cell1 is in hold phase while Cell2 is in sampling phase. The small-signal equivalent circuit for such a configuration is shown in Fig.10(b) [†8]– obtained from models described in Section III. The stationary drain current of the memory transistor in Cell2, $i_{d,n}$, is given by:

$$i_{d,n} = -(1-\varepsilon_g) i_{di,n} \tag{29}$$

The above expression applies only if the memory cell reaches the steady state before the end of the sampling phase. Otherwise, an additional error is generated as a consequence of ε_s. Solving the equivalent circuit of Fig.10(b) for v_{gs} with $v_{gs,n-1} = i^{mem}_{d,n-1}/g_m$ as the initial condition of C_{gs} yields

$$v_{gs,n} = [(1-\varepsilon_s) i_{d,n} + \varepsilon_s i^{mem}_{d,n-1}]/g_m \tag{30}$$

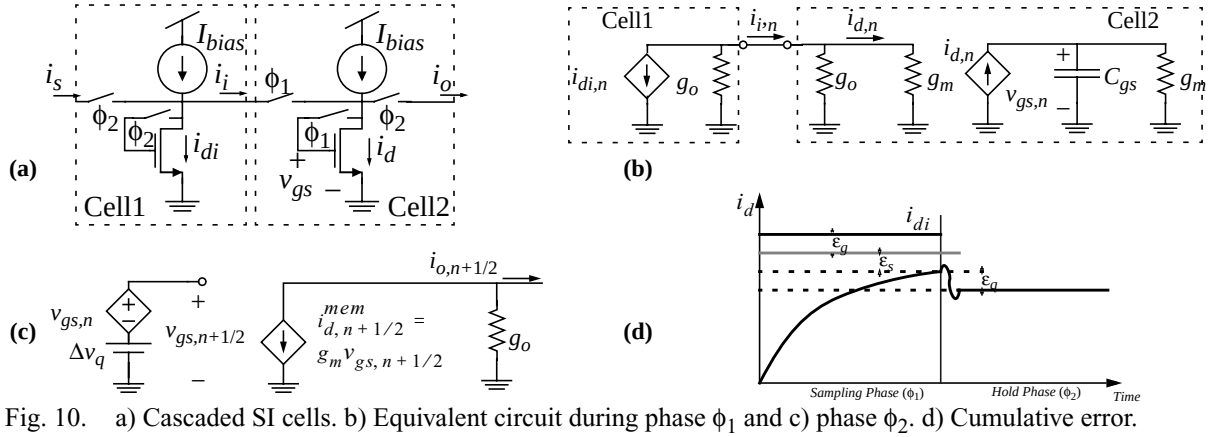

Fig. 10. a) Cascaded SI cells. b) Equivalent circuit during phase ϕ_1 and c) phase ϕ_2. d) Cumulative error.

[†8] To simplify the notation, g_m and g_o are used instead of g_{mQ} and g_{oQ} respectively.

where $i_{d,\,n-1}^{mem}$ represents the memorized drain current in the previous sampling phase. When the memory switch of Cell1 opens, the charge injected in C_{gs} introduces an additional error term (Δv_q), so that

$$v_{gs,\,n+1/2} \;=\; v_{gs,\,n} + \Delta v_q \;=\; (1-\varepsilon_q)v_{gs,\,n} \tag{31}$$

Fig.10(c) shows the equivalent circuit for the Cell2 in the hold phase. Considering all errors above, the Z-transform of i_d^{mem} is given by:

$$i_d^{mem}(z) \;=\; \frac{-(1-\varepsilon_g)(1-\varepsilon_q)(1-\varepsilon_s)z^{-1/2}i_{di}(z)}{1-\varepsilon_s(1-\varepsilon_q)z^{-1}} \tag{32}$$

It can be seen from the above equation that the ideal transfer function of the memory cell, $-z^{-1/2}$, is modified by a gain error which is the sum of ε_g, ε_q and ε_s. This is illustrated in Fig.10(d) where the transient evolution of i_d is represented during both clock phases.

B. Effect on LD Integrators and LDI-based Resonators

Let us consider the LDI whose Z-domain block diagram is shown in Fig.11(a) and its SI realization is shown in Fig.11(b). For the analysis that follows it will be assumed that memory cells which form the integrator are subject to three linear errors: ε_g, ε_q and ε_s and the output current mirror will be considered ideal. On clock phase ϕ_1 of period nT_s, the small-signal equivalent circuit is that shown in Fig.11(c). The steady state drain current of M_2, $\hat{i}_{d_{2,\,n}}$ is given

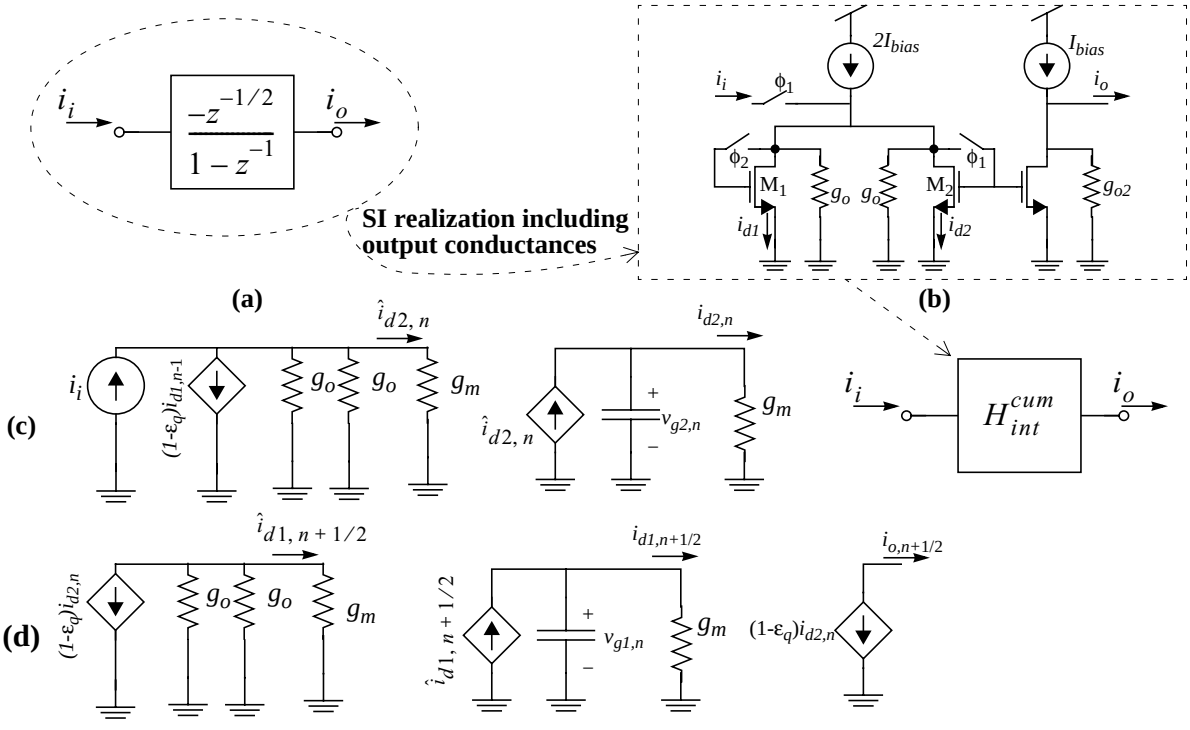

Fig. 11. LD Integrator with cumulative linear errors. a) Z-domain ideal block diagram. b) SI schematic including output conductances. c) Small-signal equivalent circuit on ϕ_1. d) Small-signal equivalent circuit on ϕ_2.

by

$$\hat{i}_{d_{2,n}} \cong (1-\varepsilon_g)[i_{i,n} - (1-\varepsilon_q) i_{d_{1,n-1/2}}] \tag{33}$$

with $\varepsilon_g = 2g_o/g_m$. Due to the incomplete settling,

$$i_{d_{2,n}} = \varepsilon_s i_{d_{2,n-1}} + (1-\varepsilon_s)\hat{i}_{d_{2,n}} \tag{34}$$

On clock phase ϕ_2 of period $(n+1/2)T_s$, the small-signal equivalent circuit for the integrator is shown in Fig.11(d). The drain current of M_1 is given by

$$i_{d_{1,n+1/2}} = \varepsilon_s i_{d_{1,n-1/2}} - (1-\varepsilon_g)(1-\varepsilon_s)(1-\varepsilon_q) i_{d_{2,n}} \tag{35}$$

and the output current will be

$$i_{o,n+1/2} = -(1-\varepsilon_q) i_{d_2,n} \tag{36}$$

From (33)-(36) and after taking the Z-transform we obtain:

$$H_{int}^{cum} \equiv \frac{i_o(z)}{i_i(z)} = \frac{(1-\varepsilon_g)(1-\varepsilon_q)(1-\varepsilon_s)(1-\varepsilon_s z^{-1}) z^{-1/2}}{(1-\varepsilon_g)^2(1-\varepsilon_q)^2(1-\varepsilon_s)^2 z^{-1} - (1-\varepsilon_s z^{-1})^2} \tag{37}$$

The isolated effect of each error on the LDI transfer function – already found in [11]– can be obtained from the above equation by simply nullifying the rest of errors. From (37) it is clear that all error mechanisms contribute as an error gain but the settling error is the only one that changes the poles in a different way as compared to the other errors.

Let us consider now the conceptual SI realization of the LDI-loop resonator block shown in Fig.12. In addition to the memory cell errors (ε_g, ε_q and ε_s), there are some errors due to non-idealities in the connection of the integrators, defined as follows[†9]:

$$\varepsilon_{F,FB} = r_{on} g_{oF,FB}; \varepsilon_{g_{F,FB}} = (g_{oF,FB}/g_m)(1-\varepsilon_{F,FB}) \tag{38}$$

where r_{on} is the steering switch on-resistance and g_{oF}, g_{oFB} are the output conductances of the current mirrors, as stated in Fig.12. Using the equivalent circuit shown in Fig.11 for the inte-

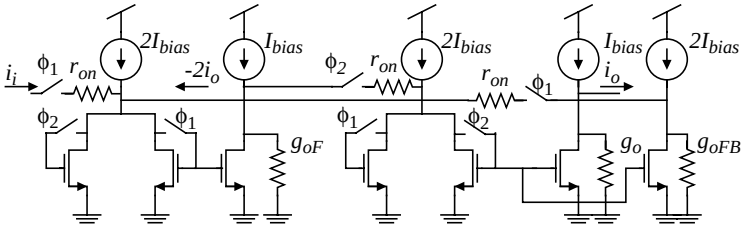

Fig. 12. Schematic of the resonator including SI Errors.

[†9] Mismatch errors also contribute to the scaling stage errors [34]. Therefore, the scaling coefficients of the resonator are modified by the cummulative effect of $\varepsilon_{F,FB}$ and mismatch errors.

grators and following a similar procedure as in the case of LDIs, it can be shown that the transfer function for the non-ideal resonator is:

$$H_{res}^{cum}(z) \cong \frac{(1-\mu_1)z^{-1} + \mu_2 z^{-2}}{1 + \xi_1 z^{-1} + (1-\xi_2)z^{-2}} \tag{39}$$

where

$$\begin{aligned} \mu_1 &= 2\varepsilon_F + 2\varepsilon_s + 2\varepsilon_g + 2\varepsilon_q + \varepsilon_{g_F}; \mu_2 = -2\varepsilon_s \\ \xi_1 &= -(2\varepsilon_F + 2\varepsilon_{FB} + 4\varepsilon_s + \varepsilon_{g_F} + \varepsilon_{g_{FB}}) \\ \xi_2 &= 4\varepsilon_s + 4\varepsilon_g + 4\varepsilon_q + \varepsilon_{g_F} + \varepsilon_{g_{FB}} \end{aligned} \tag{40}$$

C. Non-Ideal Quantization Noise Shaping in SI ΣΔ Modulators

Substituting (37) and (39) in the transfer functions of the integrators and the resonators in Fig.3, the erroneous quantization noise transfer function of the 2nd-LPΣΔM ($N_{TFLP}^{err}(z)$) and the 4th-BPΣΔM ($N_{TFBP}^{err}(z)$) are respectively,

$$\begin{aligned} N_{TFLP}^{err}(z) &\cong \frac{[1 - z^{-1}(1 - 2\varepsilon_g - 2\varepsilon_q) + \varepsilon_s^2 z^{-2}]^2}{[1 + z^{-1}(\varepsilon_g + \varepsilon_q - \varepsilon_s) - \varepsilon_s z^{-2}]^2} \\ N_{TFBP}^{err}(z) &\cong \frac{[1 + \xi_1 z^{-1} + (1-\xi_2)z^{-2}]^2}{1 + 2\xi_1 z^{-1} + [\xi_1^2 - 2(\xi_2 - \mu_1)]z^{-2}} \end{aligned} \tag{41}$$

The zeroes of N_{TFLP}^{err} in the 2nd-LPΣΔM (and of N_{TFBP}^{err} in the 4th-BPΣΔM) are shifted from their nominal positions at dc ($f_s/4$), thus degrading the filtering performed by the integrators (resonators) and making the quantization noise floor to increase in the signal band, and correspondingly, the SNR to decrease.

We can group SI errors in different families attending to the way they degrade the zeroes of $N_{TF}^{err}(z)$, which map into different increases of the in-band quantization noise power P_Q. Note that, in the lowpass case, the only effect of linear SI errors is to increase P_Q. However, in the bandpass case there is a combined effect of increasing P_Q and a shifting of the position of the signal band center frequency, often called *notch* frequency – represented by parameter f_n. As this combined effect is more complex than by simply increasing P_Q, we will discuss in more detail the bandpass case. A similar discussion can be done for 2nd-LPΣΔMs.

Table I shows the non-ideal in-band quantization noise power in 4th-BPΣΔMs for each family of errors – obtained from substituting (41) into (3). This table provides insight on the influence of each error source. Thus, assuming typical variations of the error parameters between 0.1% and 1%, the following conclusions are drawn from (41) and Table I:

- The only effect of errors ε_g and ε_q consists in reducing the Q-factor of the resonator transfer function, thus lowering the bandstop attenuation of the modulator bandpass filtering. For these errors, the deviation in P_Q is dominated by the term $(\varepsilon_{g,q}M)^2$ up to $\varepsilon_{g,q}M \approx 0.6$; beyond this limit the term $(\varepsilon_{g,q}M)^4$ dominates, thus practically destroying all the benefits of the oversampling.
- The errors ε_F and ε_{FB} just change f_n. However, P_Q does not significantly increase. For these errors, the term $(\varepsilon_{F,FB}M)^2$ dominates up to $\varepsilon_{F,FB}M \approx 2.2$.
- The errors ε_s and ε_{gF}, ε_{gFB} degrade the position of f_n and increase P_Q. For ε_s, the term $(\varepsilon_s M)^2$ dominates up to $\varepsilon_s M \approx 0.6$, while for ε_{gF}, $(\varepsilon_{gF}M)^2$ dominates up to $\varepsilon_{gF}M \approx 2.6$.
- For similar values of errors, ε_s produces larger deviations in the noise transfer function than the rest of errors – illustrated in Fig.13(a). This forces using larger oversampling ratios to achieve the ideal SNR level as is shown in Fig.13(b) by plotting DR degraded by the different errors as a function of M.

In addition to the mentioned SI errors, other scaling errors are found at the modulator level. However, they do not influence neither the integrator nor the resonator transfer function, and simply affect the scaling gains in the modulator loop, i.e: A_{INT1}, A_{RES1}, $A_{\text{DAC1,2}}$. As these errors do not shift the zeroes but the poles of $N_{TF}(z)$, their impact on P_Q is negligible for typical values (below 1%).

TABLE I: Non-Ideal P_Q in 4th-BPΣΔMs

SI Error	P_Q
$\varepsilon_{g,q}$	$\frac{\pi^4\Delta^2}{60M^5}\left[1+\frac{160}{3}\left(\frac{\varepsilon_{g,q}M}{\pi}\right)^2+1280\left(\frac{\varepsilon_{g,q}M}{\pi}\right)^4\right]$
ε_s	$\frac{\pi^4\Delta^2}{60M^5}\left[1+\frac{640}{3}\left(\frac{\varepsilon_s M}{\pi}\right)^2+5120\left(\frac{\varepsilon_s M}{\pi}\right)^4\right]$
$\varepsilon_{F,FB}$	$\frac{\pi^4\Delta^2}{60M^5}\left[1+40\left(\frac{\varepsilon_{F,FB}M}{\pi}\right)^2+80\left(\frac{\varepsilon_{F,FB}M}{\pi}\right)^4\right]$
$\varepsilon_{g_{F,FB}}$	$\frac{\pi^4\Delta^2}{60M^5}\left[1+\frac{40}{3}\left(\frac{\varepsilon_{g_{F,FB}}M}{\pi}\right)^2+20\left(\frac{\varepsilon_{g_{F,FB}}M}{\pi}\right)^4\right]$

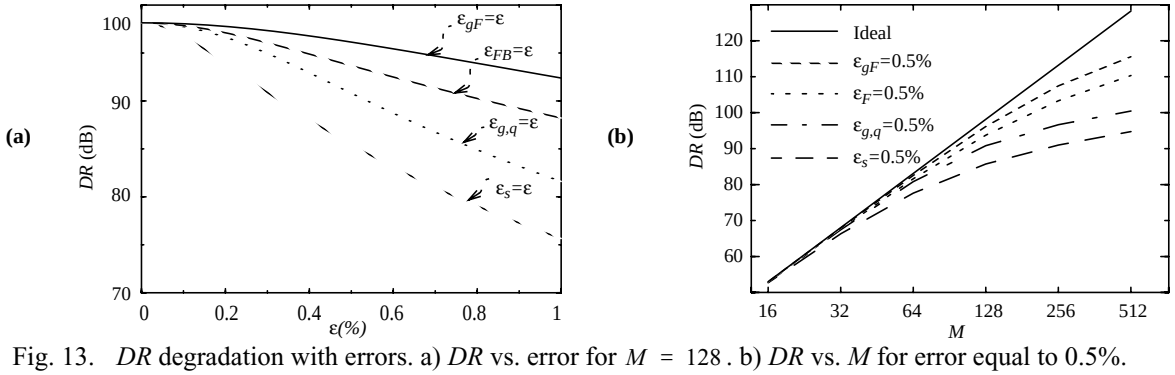

Fig. 13. *DR* degradation with errors. a) *DR* vs. error for $M = 128$. b) *DR* vs. *M* for error equal to 0.5%.

All these results have been validated by simulation using a time-domain SI behavioural simulator described in [35]. As an illustration, Fig.14 shows several simulated modulator output spectra obtained for a 4th-BPΣΔM with a sinewave input signal of amplitude $A_x = \Delta/4$ and centered at $f_s/4$. This figure compares the degradation of N_{TFBP}^{err} in the presence of $\varepsilon_{g,q}$, $\varepsilon_{F,FB}$, ε_s and $\varepsilon_{g_{F,FB}}$, obtained with the theoretical model (solid line) with that obtained through simulation. A good agreement can be observed between both approaches.

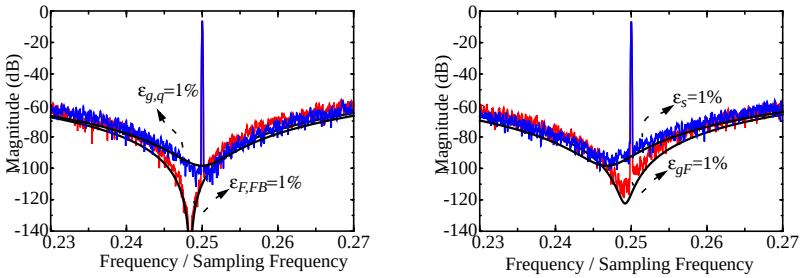

Fig. 14. Influence of Different SI Errors on N_{TFBP}^{err}.

In order to compare the noise-shaping degradation in lowpass and bandpass ΣΔMs we will center on the effect of $\varepsilon_{g,q}$, because these errors only cause an increase of P_Q. Fig.15(a)-(b) show the output spectra of both 2nd-LPΣΔMs and 4th-BPΣΔMs using memory cells with $I_{bias} = 200\mu A$, $g_{mQ} = 400\mu A/V$; $C_g = 2.8pF$ and $f_s = 1MHz$. In this simulation the only non-ideal effect was ε_g. The comparison between both types of ΣΔMs is better illustrated in Fig.15(c) where a half-scale SNR (obtained for a sinewave of amplitude $A_x = \Delta/4$) is plotted as a function of g_{oQ}/g_{mQ} for $M = 128$. It is shown that the effect of ε_g on 4th-BPΣΔMs is two times larger than on 2nd-LPΣΔMs as confirmed by theory.

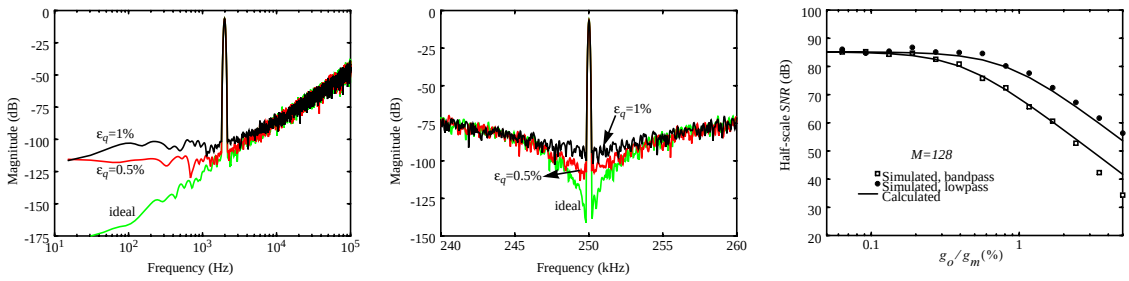

Fig. 15. Comparison of the effect of ε_g on (a) N_{TFLP}^{err} and (b) N_{TFBP}^{err}. (c) Half-scale SNR vs g_o/g_m.

D. Cummulative influence of SI errors on the quantization noise power of SI ΣΔMs

In practical applications, the designer should consider not only the isolate effect but also the cumulative influence of errors on the modulator performance. This will allow us to know the maximum error bound that is allowed for a given resolution. To illustrate this discussion, let us consider the in-band quantization noise power degraded by all errors in 4th-BPΣΔMs[†10] which

can be derived from (3), and (41), giving:

$$P_Q^{err} = \frac{\pi^4\Delta^2}{60M^5}\left[1 + \frac{10}{3}(3\xi_1^2 + \xi_2^2)\left(\frac{M}{\pi}\right)^2 + 5(\xi_1^2 + \xi_2^2)^2\left(\frac{M}{\pi}\right)^4\right] \quad (42)$$

Making all errors equal to an error bound named ε the following expression is obtained:

$$P_Q^{err} \cong \frac{\pi^4\Delta^2}{60M^5}\left[1 + \frac{4960}{3}\varepsilon^2\left(\frac{M}{\pi}\right)^2\right] \quad (43)$$

This equation allows us to express the quantization noise power degradation in terms of ε. Thus, forcing all SI errors in the modulator to be smaller than ε bounds P_Q with (43).

The control of f_n is also critical. We can derive f_n by solving (41) for the frequency of the zeroes. Assuming that $\xi_1, \xi_2 \ll 1$ the error in f_n, denoted as δf_n, is given by:

$$\delta f_n \equiv f_n - \frac{f_s}{4} \cong \xi_1 \frac{M}{\pi}\left(\frac{B_w}{2}\right) \quad (44)$$

From (40) it is seen that $\xi_1 \leq 0$ and therefore $f_n \leq f_s/4$ for all SI BPΣΔMs. On the other hand, considering that the quantization noise power is minimum at f_n, we define a maximum error $|\delta f_{n_{max}}| \leq B_w/2$. From (44) and assuming all errors to be equal to ε, that condition is satisfied if $\varepsilon \leq \pi/(10M)$. For instance, if $M = 128$, yields $\varepsilon \leq 0.25\%$.

V. Harmonic distortion in SI ΣΔ modulators

In the previous study, SI errors have been assumed to be linear. However, practically all SI errors are signal-dependent and hence, introduce HD as demonstrated in Section III. There, the influence of each SI non-linearity on the HD was analysed and closed-form expressions were derived at the memory cell level. Based on that study, closed-form expressions will be derived in this section for the HD coefficients of FD SI integrators, resonators and ΣΔMs.

A. Harmonic distortion due to static non-linear errors

In the analysis that follows, it will be assumed that SI memory cells reach the steady state before the end of the sampling phase and, consequently, ε_s will not be considered[†11]. As shown in Section III, the output current of a memory cell can be generically expressed as:

[†10] We can proceed similarly for 2nd-LPΣΔMs.

[†11] As described in Section III, the output current of a SI memory cell is not only a function of the input current at the sampling instant, but also of the output current at the last sampling instant. This is due to the fact that the value of v_{gs} reached at the end of the sampling phase depends on the initial condition of C_{gs}. In this sense, we will refer to ε_s as a *dynamic* error. Otherwise, the remaining SI errors will be referred to as *static* errors because they only depend on the input signal at the sampling instant.

$$i_{o,n} = I_{off} - (1-\xi_1) i_{i,n-1/2} + i_{th} - \sum_{k=2}^{\infty} \xi_k i_{i,n-1/2}^{k} \tag{45}$$

where I_{off} stands for the offset current at the output, ξ_1 is the linear gain error, i_{th} is the thermal noise contribution and ξ_k represents the k-order non-linear gain error. Note that (45) can be particularized for each SI error (except for ε_s) by simply substituting the corresponding expressions of I_{off} and ξ_k.

Thermal noise will not be considered in the following analysis because it does not contribute to HD. Also, even powers of the input current in (45) can be considered negligible because FD SI cells will be assumed. Taking into account these considerations, (45) simplifies into:

$$i_{o,n} \cong -(1-\xi_1) i_{i,n-1/2} - \xi_3 i_{i,n-1/2}^{3} \tag{46}$$

where it has been assumed that ξ_3 is the dominant non-linear term.

The model in (46) can be used to analyse other SI circuits of higher level in the hierarchy of ΣΔMs. Let us consider the LDI-based SI circuits shown in Fig.16. Fig.16(a) shows a FD SI LDI. In the following, it will be assumed that the operation of memory cells is described by (46). Although these cells are simple, our analysis can be extended to enhanced memory cells – cascode, regulated-cascode or folded regulated-cascode – by conveniently changing the expressions of ξ_1 and ξ_3 in (46).

The operation of the integrator is as follows. After clock phase ϕ_1, which goes on for nT_s, the differential drain current of cell2 is given by:

$$i_{ds_{2,n}} \equiv i_{ds_{2+,n}} - i_{ds_{2-,n}} \cong (1-\xi_1)(i_{i,n} - i_{ds_{1,n-1/2}}) + \xi_3 (i_{i,n} - i_{ds_{1,n-1/2}})^3 \tag{47}$$

where $i_{ds_{1,n}} \equiv (i_{ds_{1+,n}} - i_{ds_{1-,n}})$ represents the differential drain current of cell1.
After clock phase ϕ_2,

$$i_{ds_{1,n+1/2}} \cong (1-\xi_1)(-i_{ds_{2,n}}) + \xi_3 (-i_{ds_{2,n}})^3 \tag{48}$$

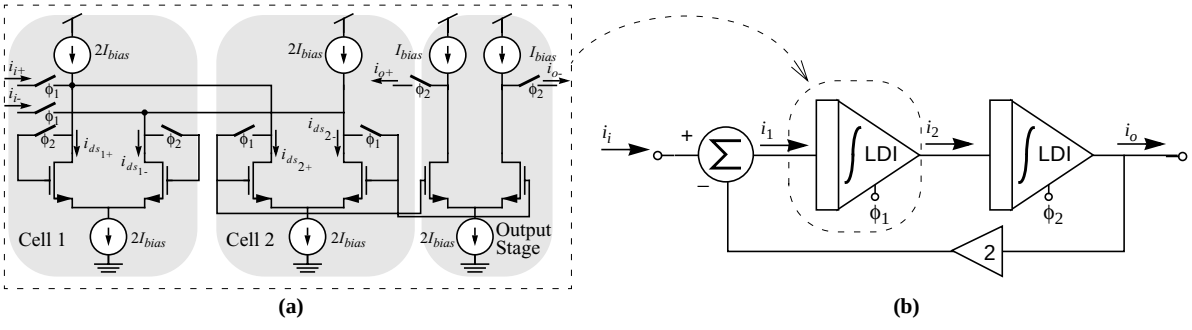

Fig. 16. FD SI LDI-based circuits. a) FD LD Integrator. b) LDI-based resonator.

Assuming that the output stage (represented in Fig.16 as a simple current mirror) is ideal, the output current of the integrator is given by:

$$i_{o,\,n+1/2} = -i_{ds_{2,\,n}} \tag{49}$$

From (47)-(49) it can be derived that the output current of the integrator is

$$i_{o,\,n} \cong (1-\xi_1) i_{x,\,n} + \xi_3 i_{x,\,n}^3 \tag{50}$$

where $i_{x,\,n} = -i_{i,\,n-1/2} + (1-\xi_1) i_{o,\,n-1} + \xi_3 i_{o,\,n-1}^3$.

Assuming that $\xi_1,\ \xi_3 \left| i_{o,\,n} \right|^2 \ll 1$ and performing a Taylor series expansion of (50), obtains:

$$i_{o,\,n} \cong (1-2\xi_1) i_{o,\,n-1} - (1-\xi_1) i_{i,\,n}^* \tag{51}$$

where

$$i_{i,\,n}^* \cong i_{i,\,n-1/2} - \frac{\xi_3}{(1-\xi_1)} (i_{o,\,n-1}^3 + i_{o,\,n}^3) \tag{52}$$

Thus, the analysis of an SI integrator formed by memory cells with *static* non-linear errors can be accomplished considering an integrator formed by memory cells with linear gain errors whose input signal is equal to (52). The equivalent HD at the integrator input can be estimated by analysing the harmonic content of such an expression. For this purpose, let us assume that the input current is a sinewave signal of amplitude I_i and frequency f_i. In this case, i_o will be a periodic signal, with the amplitude of its fundamental harmonic given approximately by:

$$I_o \cong I_i \left| \frac{-(1-\xi_1) z^{-1/2}}{1-(1-2\xi_1) z^{-1}} \right| \Bigg|_{z\,=\,e^{j2\pi f_i T_s}} \tag{53}$$

On the other hand, we will suppose that i_o can be approximated by its first harmonic, so that:

$$i_{o,\,n} \cong I_o \cos(2\pi f_i n T_s) \tag{54}$$

Substituting (53)-(54) in (52) and performing a Fourier series expansion, it can be shown that the amplitude of the third-order harmonic at the integrator input is approximately given by:

$$A_{H,\,3} \cong \frac{\xi_3 I_o^3}{2(1-\xi_1)} \left| \cos(3\pi f_i T_s) \right| \tag{55}$$

The above expression will allow us to calculate HD_3 at the output of a 2nd-LPΣΔM like that shown in Fig.3(a). For this purpose, the following considerations will be taken into account:

- The HD referred to the first integrator input is added directly to the input signal. Thus,

it is not attenuated in the base band. However, the contribution of the second integrator to HD is attenuated by the gain of the first integrator. For this reason, only the first integrator contribution has to be considered for the analysis.

- The HD referred to the modulator input is equal to the HD referred to the modulator output. This is because the gain of $S_{TF}(z)$ is unity.

Assuming that the transfer function of the first integrator in Fig.3 is given by (53), and obviating the quantization noise, it can be shown that for $f_i T_s \ll 1$, the expression for the first integrator output amplitude is:

$$I_o \cong 2(1-4\xi_1)|X(z)| \tag{56}$$

Substituting (56) in (55) and dividing the result by the amplitude of the modulator input, $A_x = |X(z)|$, obtains the expression for HD_3 at the modulator output as follows:

$$HD_3 \cong 4\frac{\xi'_3}{n_b^2}(1-11\xi_1)\left(\frac{A_x}{I_{DAC}}\right)^2\left(1-\frac{3\pi}{2M}\right) \tag{57}$$

where I_{DAC} is the DAC output current, $\xi'_3 \equiv \xi_3 I_{bias}^2$ and $n_b \equiv I_{bias}/I_{DAC}$.

The above expression has been derived for the general case and hence, it can be used to predict HD_3 in SI FD 2nd-LPΣΔMs due to any static error. As an application, let us assume that the integrators in Fig.3(a) are ideal except for ε_q. In such a case, the theoretical prediction of HD_3 is computed by substituting the corresponding expressions of ξ_1 and ξ_3 (see Section III) in (57). Fig.17(a) plots HD_3 vs. C_{sw}/C_{gs} ($C_{sw} \equiv C_{ox}W_{s_{eff}}L_{s_{eff}}$) for different values of $(V_{gs}-V_T)_Q$ and compares the theoretical model with time-domain simulations. Fig.17(b) shows a simulated output spectrum for $(V_{gs}-V_T)_Q = 0.1\text{V}$ and $C_{sw}/C_{gs} = 0.08\,\%$. The theoretical and simulated data, respectively $HD_3 = -86\text{dB}$ and $HD_3 = -85\text{dB}$, agree.

Similarly, the analysis of the HD in 4th-BPΣΔMs like that shown in Fig.3(b) can be accomplished by analysing the harmonic content of the first resonator. This is because the con-

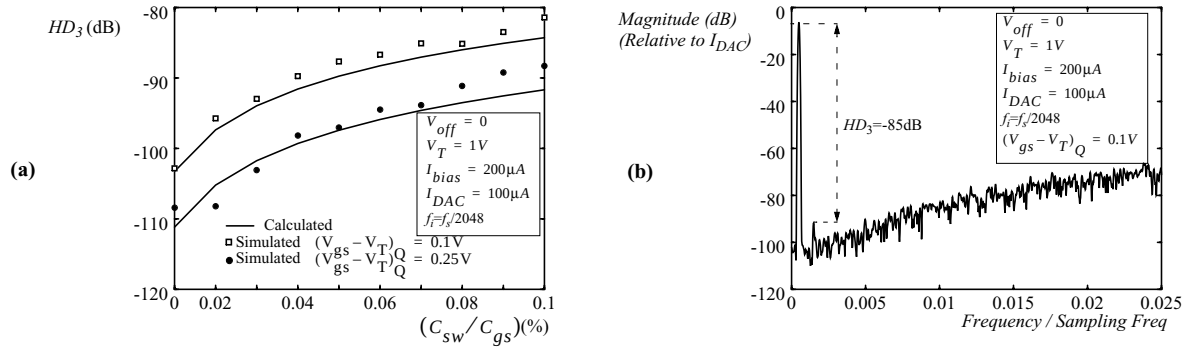

Fig. 17. HD_3 of 2nd-LPΣΔMs due to ε_q. a) HD_3 vs. C_{sw}/C_{gs} for different values of $(V_{gs}-V_T)_Q$. b) Output spectrum corresponding to $(V_{gs}-V_T)_Q = 0.1V$ and $C_{sw}/C_{gs} = 0.08\,\%$ ($I_i = I_{DAC}/2$).

tribution of the second resonator is attenuated by the gain of the first one in the signal band.

Let us consider that the first resonator in Fig.3(b) is realized as shown in Fig.16(b). In the presence of non-linear static errors, the LDIs which form the resonator can be described by (51) and, hence, the difference equations which describe the behaviour of the resonator are:

$$i_{2,n} \cong -(1-\xi_1) i_{1,n-1/2} + (1-2\xi_1) i_{2,n-1} + \xi_3 i_{2,n}^3 + \xi_3 i_{2,n-1}^3 \tag{58}$$

$$i_{o,n} \cong -(1-\xi_1) i_{2,n-1/2} + (1-2\xi_1) i_{o,n-1} + \xi_3 i_{o,n}^3 + \xi_3 i_{o,n-1}^3 \tag{59}$$

where i_1 and i_2 are respectively the input and the output of the first integrator in the loop (see Fig.16(b)) while i_i and i_o are respectively the input and the output of the resonator.
Solving for $i_{2,n}$ in (59), substituting it in (58) and assuming that $\xi_1, \xi_3 |i_{o,n}|^2 \ll 1$, results

$$i_{o,n} \cong (1-2\xi_1) i'_{i,n} - (1-4\xi_1) i_{o,n-2} \tag{60}$$

where

$$i'_{i,n} = i_{i,n-1} + \frac{\xi_3}{1-2\xi_1}[i_{o,n}^3 - i_{o,n-2}^3 + (i_{o,n} - i_{o,n-1})^3 + (i_{o,n-1} - i_{o,n-2})^3] \tag{61}$$

And the amplitude of the third-order harmonic at the resonator input is approximately given by:

$$A_{H,3} \cong \frac{\xi_3 I_o^3}{2(1-2\xi_1)}(1 + 12\pi f_i' T_s) \tag{62}$$

where $I_o \cong I_i \left| [(1-2\xi_1)z^{-1}] / [1 + (1-4\xi_1)z^{-2}] \right|_{z = e^{j2\pi f_i T_s}}$, $f_i' = f_i - f_s/4$ and $f_i' T_s \ll 1$ has been assumed.

Following the same procedure as in the lowpass case, we can obtain HD_3 at the output of 4th-BPΣΔMs. However in bandpass signal processing, the third-order intermodulation distortion, IM_3, is more appropriate for measuring distortion than HD_3. It can be shown that

$$IM_3 = 3HD_3 \cong \frac{12\xi'_3}{n_b^2}\left(\frac{A_x}{I_{DAC}}\right)^2 (1-16\xi_1)(1 + 12\pi f_i' T_s) \tag{63}$$

As an application of the previous analysis, let us assume that the modulator in Fig.3(b) is formed by FD Regulated Folded-Cascode (RFC) memory cells like that shown in Fig.18. In this cell, the current source named I_{br} has to be taken as large as possible in order to obtain an over-damped settling response. However, large values of I_{br} may force some transistors to leave the saturation region, thus causing a non-linear dependence of the input voltage on the input signal which can be modelled as $\xi_1 \cong -2 g_{oQ} r_1$ and $\xi_3 \cong -2 g_{oQ} r_3$, where coefficients r_1 and r_3, which are function of I_{br}, are extracted from dc HSPICE simulations. Fig.19(a) plots IM_3 vs

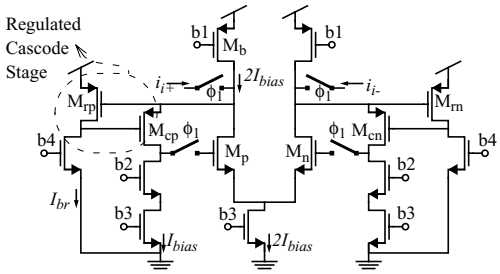

Fig. 18. FD Regulated Folded-Cascode (RFC) memory cell.

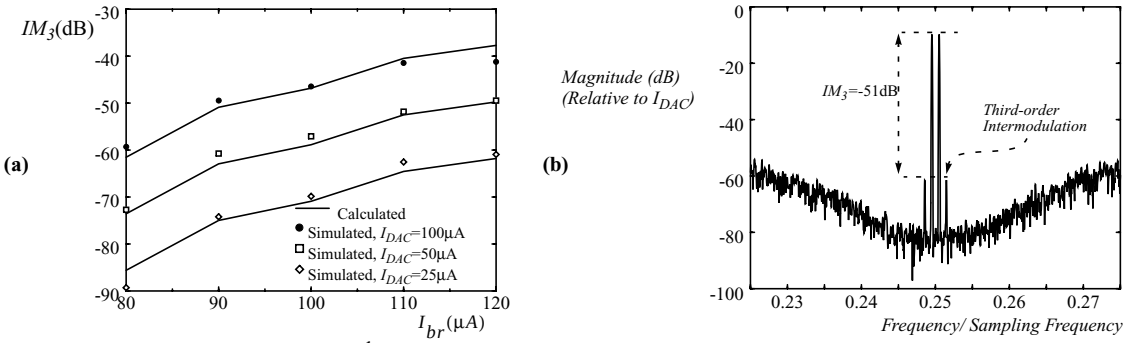

Fig. 19. IM_3 at the output of a 4th order bandpass ΣΔ modulator due to non-linear input impedance of RFC memory cells. a) IM_3 vs. I_{br}. (b) Output spectrum corresponding to $I_{br} = 110\mu A$, and $I_{DAC} = 50\mu A$. (Amplitude of each input tone equal to $(1/2\sqrt{2})I_{DAC}$).

I_{br} for different values of I_{DAC}. Fig.19(b) shows the output spectrum of the modulator for $I_{br} = 110\mu A$ and $I_{DAC} = 50\mu A$. The predicted value for IM_3 is -53dB which agrees with the simulated value (-51dB).[†12]

B. Harmonic distortion due to non-linear settling error

Let us consider that memory cells which form the modulators in Fig. 5 are ideal except for the settling error. Fig.20(a) and (b) illustrate the effect of the non-linear settling on the HD of

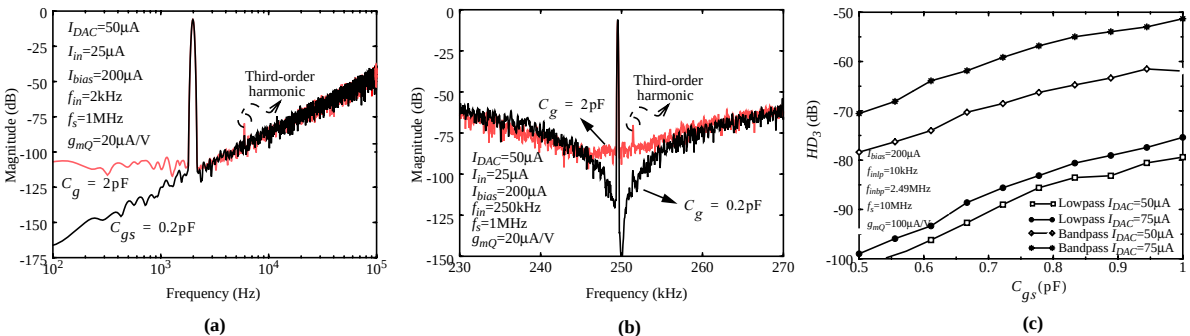

Fig. 20. Effect of non-linear ε_s on SI ΣΔMs. Modulator output spectra for different values of C_{gs}. a) 2nd-LPΣΔM. b) 4th-BPΣΔM. c) HD_3 vs. C_{gs}.

[†12] In the analysis described here, the integrator output stages (see Fig.16(a)) have been considered ideal. In practice, the current mirror used to realize those gain stages have non-linear output conductances and mismatch, which according to Section III, will cause HD. Following a similar methodology to that presented here it can be demonstrated that the IM_3 caused by the current mirror errors can be obtained by replacing the corresponding value of ξ'_3 (see Section III) in (63).

the modulators in Fig.3 by showing some modulator output spectra for different values of C_{gs} and keeping f_s constant. As expected, the in-band quantization noise and HD_3 increase with C_{gs}. However, as shown in Fig.20(c), that effect is considerably larger in 4th-BPΣΔMs. For that reason, and to not be repetitive, in the analysis that follows we will focus in the bandpass case. A similar procedure can be followed for the lowpass case.

Let us assume that memory cells which form the modulator are ideal except for the non-linear settling, and according to Section III, they can be modelled by (21). Let us consider the ideal operation of the integrator shown in Fig.16(a). After clock phase ϕ_1, the differential drain current of cell 2 in Fig.16(a), is:

$$i_{ds_{2,n}} \equiv i_{ds_{2+,n}} - i_{ds_{2-,n}} \cong [1 - \Psi(i_{x,n})]i_{x,n} + i_{ds_{2,n-1}}\Psi(i_{x,n}) \tag{64}$$

where $i_{x,n} = i_{i,n} - i_{ds_{1,n-1/2}}$. After clock phase ϕ_2,

$$i_{ds_{1,n+1/2}} \cong -[1 - \Psi(-i_{ds_{2,n}})]i_{ds_{2,n}} + i_{ds_{1,n-1}}\Psi(-i_{ds_{2,n}}) \tag{65}$$

Assuming that the output stage (represented in Fig.16(a) as a simple current mirror) is ideal, the output current of the integrator is:

$$i_{o,n+1/2} = -i_{ds_{2,n}} \tag{66}$$

Following a similar procedure as in the case of static errors, it can be shown that IM_3 at the modulator output in Fig.3(b) is given by [36]:

$$IM_3 \cong 12\sqrt{2}\varepsilon_{s2}A_x^2(1 + 5\pi f_i'T_s) \cong 4\sqrt{2}\varepsilon_{s2}A_x^2 \tag{67}$$

Note that, due to the oversampling, it is $f_i'T_s \ll 1$, and hence IM_3 practically does not depend on the input frequency as happens at the cell level.

The expression (67) has been validated by time-domain simulation as shown in Fig.21(a) by representing IM_3 vs. ε_s[†13] for different values of I_{DAC} with $A_x = I_{DAC}/2$, $I_{bias} = 200\mu A$, $C_{gs} = 1pF$ and $f_s = 10MHz$. The input signal consisted on two tones of

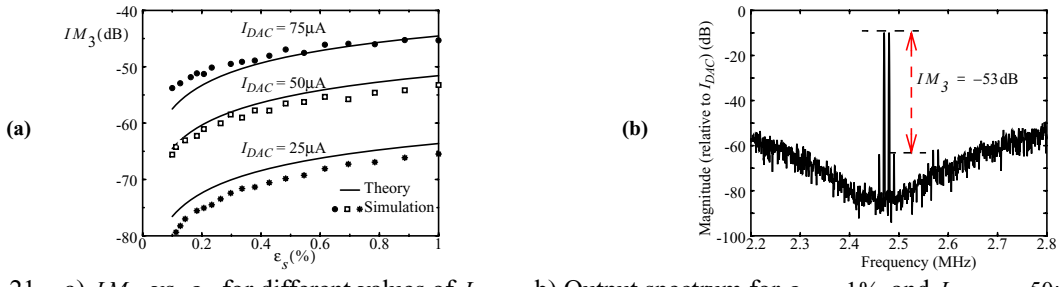

Fig. 21. a) IM_3 vs. ε_s for different values of I_{DAC}. b) Output spectrum for $\varepsilon_s = 1\%$ and $I_{DAC} = 50\mu A$.

[†13] The simulation was carried out by varying g_{mQ} such that $0.1\% < \varepsilon_s < 1\%$.

amplitude $A_x/\sqrt{2}$ and frequencies $f_{i1} \cong 0.247 f_s$ and $f_{i2} = 0.248 f_s$. As an illustration, Fig.21(b) shows the output spectrum corresponding to $\varepsilon_s = 1\%$ and $I_{DAC} = 50\mu A$. Note that, other intermodulation products appears – not critical since they are outside the signal band.

C. Effect of the sampling process at the front-end of bandpass ΣΔ modulators

In Section III it was demonstrated that the non-linear transient of a memory cell with an non-stationary input signal will cause large values of HD even if $\varepsilon_s \ll 1$. In a BPΣΔM, only the memory cell connected to the input node presents that behaviour. As shown in Appendix I, that cell can be modelled as an ideal cell with an input signal having a third-order harmonic of amplitude:

$$A_{H,3} \cong \frac{3\pi f_i \tau}{16(2I_{bias})^2} I_i^3 \tag{68}$$

In order to calculate IM_3 at the modulator output in Fig.3(b), it is necessary to express I_i as a function of A_x. The analysis of the input section of the modulator gives $I_i \cong 2\sqrt{2}A_x$. Substituting this expression in (68), and proceeding as in previous sections, we obtain that

$$IM_3 \cong \frac{9}{8\sqrt{2}n_b^2}\pi f_s \tau \left(\frac{A_x}{I_{DAC}}\right)^2 \tag{69}$$

where $f_i \cong f_s/4$ has been assumed. Fig.22(a) compares (69) with time-domain behaviour al simulation by plotting IM_3 vs. τ for different values of f_s, $n_b = 4$ and $A_x/I_{DAC} = 1/2$. The theoretical model accurately predicts the simulation results except for some cases where a maximum error of 4dB occurs. In these cases a more exact analysis using the exact expressions resulting from the analysis in Appendix I should be used.

To conclude this study, Fig.22(b) compares IM_3 caused by the non-linear settling error and the S/H process for $f_s = 10\text{MHz}$ and $A_x/I_{DAC} = 1/2$. Note that, for $\varepsilon_s > 3\%$, both expressions approximately converge. However, for practical designs, i.e, for $\varepsilon_s < 0.1\%$, IM_3 due to the S/H process dominates, limiting the performance of SI BP-ΣΔMs unless a S/H circuit will be used at the front-end. This will be confirmed by measurements in Section VII.

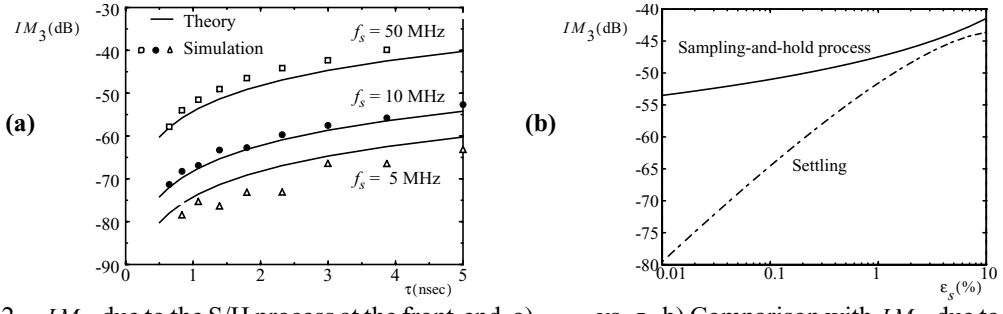

Fig. 22. IM_3 due to the S/H process at the front-end. a) IM_3 vs. τ. b) Comparison with IM_3 due to non-linear ε_s.

VI. Thermal noise in SI ΣΔ Modulators

Thermal noise constitutes the ultimate limiting factor of ΣΔMs [2]. As for the rest of SI errors, only the thermal noise contributions at the modulator input will be important because they are added directly to the input signal, thus appearing without filtering in the output spectrum.

Let us consider the 2nd-LPΣΔM of Fig.3(a). Assuming the noise contribution of DAC1 negligible, the input-equivalent noise PSD is approximately given by:

$$S_{thlp} \cong S_{\text{int1}} \tag{70}$$

where S_{int1} is the input-equivalent noise PSD of the first integrator which, according to [21], is twice the noise PSD of the cell – given by (28).

The analysis of noise contributions in the 4th-BPΣΔM shown in Fig.3(b) shows that, by neglecting the noise contributions of DAC1, the input-equivalent noise PSD is approximately given by:

$$S_{thbp}(f) \cong S_{\text{int1}}(f) + \left|1 - z^{-1}\right|^2\Big|_{z\,=\,e^{-j2\pi f T_s}} S_{\text{int2}}(f) \tag{71}$$

where S_{int2} is the input-equivalent noise PSD of the second integrator. Note that the contribution to the input-equivalent current noise source of the second integrator is twice that of the first integrator because in the signal band, $\left|1 - z^{-1}\right|^2 \cong 2$, and hence:

$$S_{thbp}(f) \cong S_{\text{int1}}(f) + 2S_{\text{int2}}(f) \tag{72}$$

The in-band thermal noise power is calculated by integrating $S_{thlp}(f)$ and $S_{thbp}(f)$, into the signal band,

$$P_{th} = \int_{\text{signal-band}} S_{th}(f)df \tag{73}$$

and in case that the thermal noise dominates the quantization noise, the SNR and the DR for a sinewave input signal of amplitude $A_x = \alpha\Delta/2$ are respectively given by:

$$SNR_{th} = \frac{\alpha^2\Delta^2}{8P_{th}} \qquad DR_{th} = \frac{\Delta^2}{8P_{th}} \tag{74}$$

VII. Experimental Results

To conclude this paper, in this section some measured results are given which demonstrate experimentally the performance degradation of ΣΔMs caused by SI errors. As a case study, measurements were taken from a 0.8μm CMOS SI 4th-BPΣΔM IC realized using FD RFC

memory cells [37]. These measurements are compared with time-domain behavioural simulations and theoretical results, thus validating the study described in this paper.

For practical reasons in the experimental set-up, we only have off-chip control of the bias currents, supply voltages, input signal parameters (amplitude and frequency) and the sampling frequency. Taking into account these limitations, the results here will center on the effect of:

- Static errors, mainly the linear and non-linear part of ε_g, $\varepsilon_{gF,FB}$, and $\varepsilon_{F,FB}$. This will be done by varying the bias current source of the RFC stage, I_{bR} – see Fig.18.
- Dynamic errors, by varying the sampling frequency, f_s.

A. Effect of static errors

As discussed in Section V, both the linear and the non-linear part of the input impedance in the cell of Fig.18 increase with I_{bR}, thus degrading the noise shaping of the modulator and increasing the HD according to Table I and (63), respectively. Fig.23(a) illustrates this by plotting two measured output spectra corresponding to different values of I_{bR}, showing the cumulative effect of errors ε_g, $\varepsilon_{gF,FB}$ and $\varepsilon_{F,FB}$. These effects are predicted by time-domain simulations using the models presented in this paper as Fig.23(b) shows. Note that a similar degradation is obtained by comparing Fig.23(a) and Fig.23(b). However, in the simulations this degradation appears for higher values of I_{bR}, because nominal conditions were used. Fig.23(c) compares two simulated output spectra for $I_{bR} = 40\mu A$ considering both nominal and worst-case speed conditions, showing that the latter are closer to experimental results than the former.

The effect of static errors on IM_3 is illustrated in Fig.24. Fig.24(a) shows the central part of several measured modulator spectra for different values of I_{bR} and an input signal consisting of two $-10dB$ tones at $486kHz$ and $488kHz$ when clocked at $f_s = 2MHz$. These results confirm the degradation of IM_3 with I_{bR} which was analysed in detail in Section V. In that section theoretical analyses were validated by time-domain behavioural simulations using nominal conditions. Those results have been validated by measurements as Fig.24(b) demonstrates by rep-

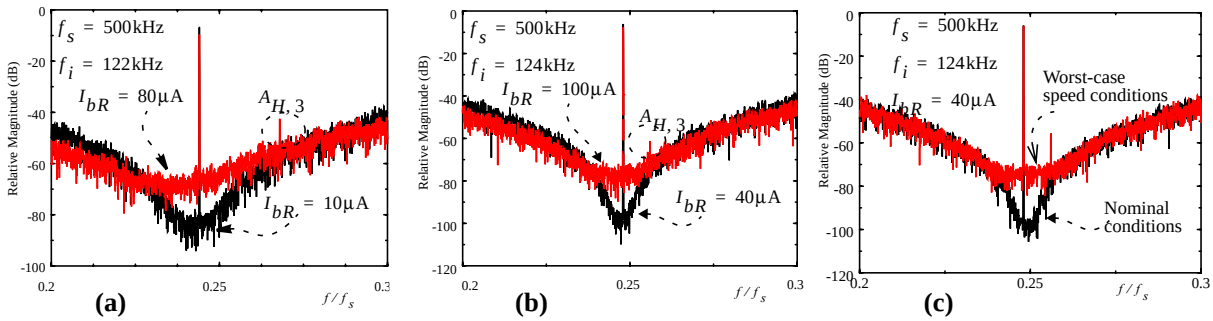

Fig. 23. Performance degradation due to the non-linear static errors. Output spectra for different values of I_{bR}. a) Measured. b) Simulated (nominal cond.). c) Simulated (worst-case speed vs. nominal cond.).

resenting both measured and simulated IM_3 vs. I_{bR}, showing a good agreement.

Other effect of changing I_{br} is to shift f_n. This phenomenon is mainly due to the variation of r_{on} (see Fig.12), thus causing errors $\varepsilon_{gF,FB}$ and $\varepsilon_{F,FB}$ to increase. Fig.25 represents the approximated variation of f_n (see (44)) as a function of I_{bR}, comparing both simulations and measurements.

B. Effect of dynamic errors

Fig.26 shows two measured output spectra corresponding to different values of f_s, and hence, of the settling error, ε_s. As discussed in Section IV, ε_s has two main effects: increasing the in-band quantization noise power and shifting f_n. Both effects are demonstrated in the output spectra shown in Fig.26. Observe that the notch frequency position has been shifted –1.4% from its nominal position as predicted by theory in (44) (data inset Fig.26).

Another important effect of raising f_s is the increase of HD. This phenomenon is caused by two error mechanisms: the non-linear part of ε_s, and the non-linear sampling process. As demonstrated in Section V, for practical values of ε_s, the HD in BPΣΔMs is dominated by the non-linear sampling. Fig.27 confirms this by showing two measured output spectra for $A_x/I_{DAC} = 0.42$ when clocked at $f_s = 2\text{MHz}$ and $f_s = 10\text{MHz}$, obtaining

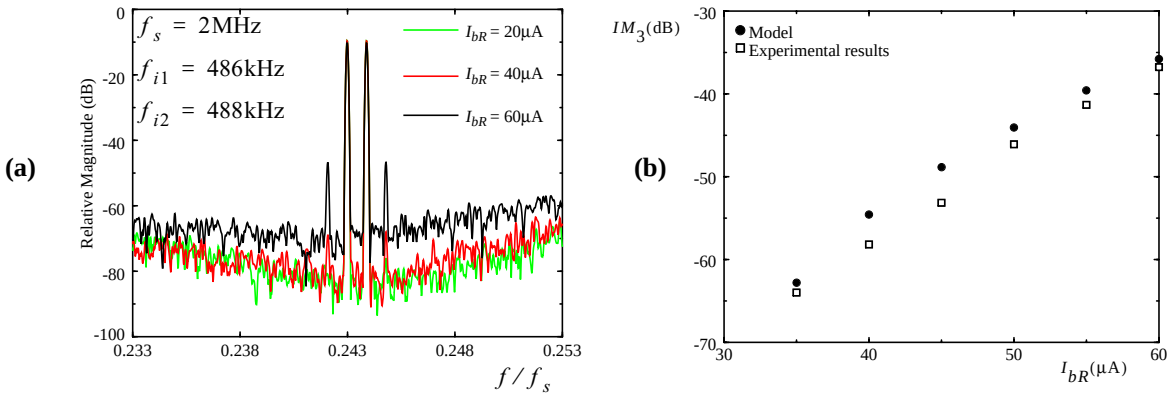

Fig. 24. Intermodulation distortion due to the non-linear input impedance. a) Measured output spectra for different values of I_{bR}. b) IM_3 vs. I_{bR}: Measurements vs. simulations.

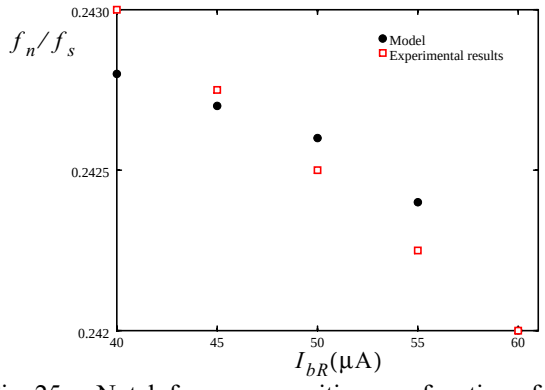

Fig. 25. Notch frequency position as a function of I_{bR}.

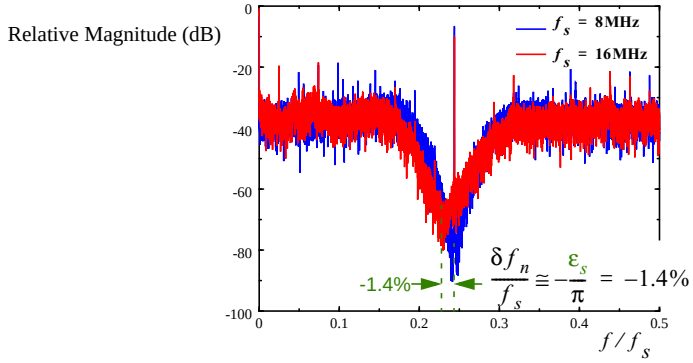

Fig. 26. Experimental noise-shaping degradation with settling.

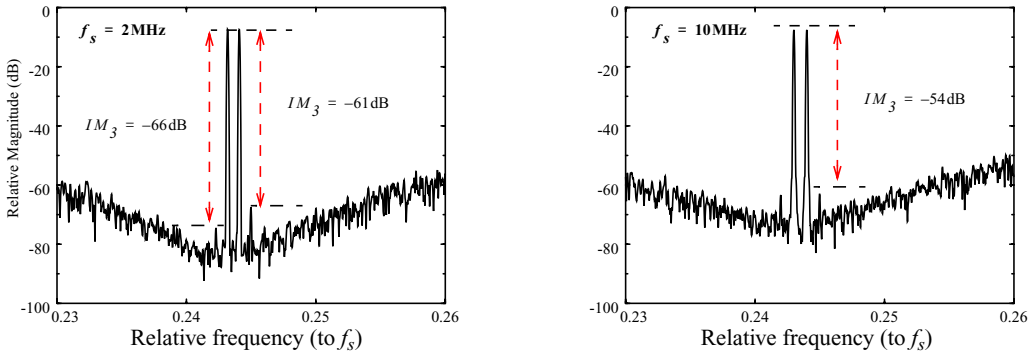

Fig. 27. Measured output spectra for different values of f_s.

$IM_3 = -61\text{dB}$ and -54dB respectively. In this case, $g_{mQ} = 360\mu\text{A/V}$ and $C_{gs} = 2.8\text{pF}$ ($\varepsilon_s = 0.16\%$ at $f_s = 10\text{MHz}$), which according to (69) gives $IM_3 = -64\text{dB}$ and $IM_3 = -55\text{dB}$ respectively.

VIII. Conclusions

A hierarchical systematic analysis of the impact of SI errors on the performance of ΣΔMs has been presented. Precise analytical models have been derived for SI circuits of different hierarchy levels: memory cells, integrators and resonators. Based on the analysis of these blocks, closed-form expressions have been obtained for the noise-shaping degradation and the harmonic distortion of both lowpass and bandpass ΣΔMs. Electrical and time-domain behavioural simulations at the block level and experimental results at the modulator level validate our approach.

Appendix I

Let us consider the simple SI memory cell shown in Fig.4(a). For the analysis that follows, these approximations will be considered:

- The transient response corresponds to a first-order dynamics, dominated by τ.

- The charge injection error and the finite output resistance will be neglected.
- Memory transistor, M, operates in the saturation region and can be modelled by:

$$i_d = \frac{\beta}{2}(v_{gs} - V_T)^2 \tag{75}$$

where $\beta = \mu_o C_{ox} W/L$.

Under the above-mentioned conditions, the cell in Fig.4(a) can be modelled by the equivalent circuit shown in Fig.28(a). Note that, this circuit can be viewed as the cascaded connection of two circuits as illustrated in Fig.28(b): one of them consists of the equivalent circuit of a simple current mirror and the other one is an ideal S/H circuit.

Except for the half clock period delay, the analysis of Fig.28(b) during the sampling phase gives us all information needed to analyse the non-linear transient behaviour of the cell and hence, to get a closed-form expression of the HD. Therefore, in what follows, we will consider for our analysis the circuit in Fig.28(b) during ϕ_1. By applying Kirchoff's current law to node $n1$ (see Fig.28(b)), we obtain:

$$i_i(t) + I_{bias} = i_d(t) + C_{gs}\frac{d}{dt}v_{gs}(t) \tag{76}$$

By making $v_{gs}(t)$ equal to a quiescent voltage, V_{gs}, plus an incremental voltage, $v(t)$, i.e, $v_{gs} = V_{gs} + v(t)$, (76) simplifies into:

$$i_i(t) = g_m v(t) + \frac{\beta}{2}v^2(t) + C_{gs}\frac{d}{dt}v(t) \tag{77}$$

where $g_m = 2I_{bias}/(V_{gs} - V_T)$ and $I_{bias} = \beta(V_{gs} - V_T)^2/2$ has been considered.
The incremental voltage, $v(t)$, can be expressed in its Volterra series as [33]:

$$v(t) = v_1(t) + v_2(t) + v_3(t) + \ldots + v_n(t) \tag{78}$$

where $v_n(t)$ stands for the nth-order term of $v(t)$. Substituting (78) into (77) and keeping only the most significant terms, it can be shown that the differential equations corresponding to the first, second and third-order kernels are, respectively:

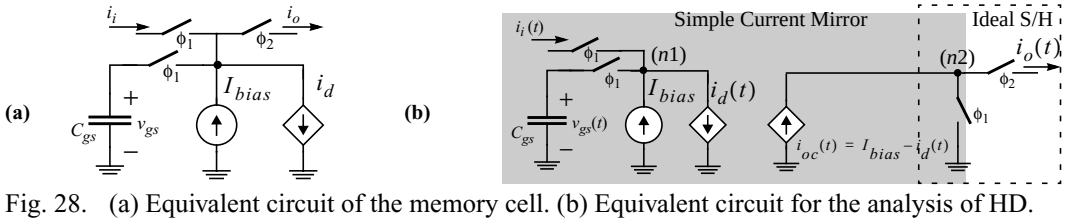

Fig. 28. (a) Equivalent circuit of the memory cell. (b) Equivalent circuit for the analysis of HD.

$$
\begin{aligned}
i_i(t) &= g_m v_1(t) + C_{gs}\frac{d}{dt}v_1(t) \\
0 &= g_m v_2(t) + C_{gs}\frac{d}{dt}v_2(t) + \frac{\beta}{2}v_1^2(t) \\
0 &= g_m v_3(t) + C_{gs}\frac{d}{dt}v_3(t) + \beta v_1(t)v_2(t)
\end{aligned}
\tag{79}
$$

Performing the same analysis for node $n2$ yields:

$$
\begin{aligned}
i_{oc1}(t) &= -g_m v_1(t) \\
i_{oc2}(t) &= -g_m v_2(t) - \frac{\beta}{2}v_1^2(t) \\
i_{oc3}(t) &= -g_m v_3(t) - \beta v_1(t)v_2(t)
\end{aligned}
\tag{80}
$$

where $i_{ocn}(t)$, represents the nth-order term of the Volterra series expansion of $i_{oc}(t)$. Using fasorial analysis and solving for $i_{oc1}(t) = I_{oc1}(j\omega_1 t)$, $i_{oc2}(t) = I_{oc2}(j\omega_1, j\omega_2, t)$ and $i_{oc3}(t) = I_{oc3}(j\omega_1, j\omega_2, j\omega_3, t)$ in the above expressions yields:

$$
H_1(j\omega_1) \equiv \frac{I_{oc1}(j\omega_1 t)}{I_i(j\omega_1 t)} = \frac{-1}{1 + j\phi_1}
\tag{81}
$$

$$
H_2(j\omega_1, j\omega_2) \equiv \frac{I_{oc2}(j\omega_1, j\omega_2, t)}{I_i^2(j\omega_1 t)} = \frac{-j(\phi_1 + \phi_2)}{4I_{bias}(1 + j\phi_1)(1 + j\phi_2)[1 + j(\phi_1 + \phi_2)]}
\tag{82}
$$

$$
\begin{aligned}
H_3(j\omega_1, j\omega_2, j\omega_3) &\equiv \frac{I_{oc3}(j\omega_1, j\omega_2, j\omega_3, t)}{I_i^3(j\omega_1 t)} = \\
&= \frac{j(\phi_1 + \phi_2 + \phi_3)/\left(24I_{bias}^2\right)}{(1 + j\phi_1)(1 + j\phi_2)(1 + j\phi_3)[1 + j(\phi_1 + \phi_2 + \phi_3)]} \cdot \left[\frac{1}{1 + j(\phi_1 + \phi_2)} + \frac{1}{1 + j(\phi_1 + \phi_3)} + \frac{1}{1 + j(\phi_2 + \phi_3)}\right]
\end{aligned}
\tag{83}
$$

.

where $\phi_n \equiv \omega_n \tau$.

In this paper, we are mainly interested in the analysis of FD SI circuits. Thus, even-order harmonic coefficients can be neglected and hence, $\mathrm{THD} \cong HD_3$ is given by [18]:

$$
HD_3(\omega) \equiv \frac{\rho^2}{4}\frac{H_3(j\omega, j\omega, j\omega)}{H_1(j\omega)} = \frac{-3j\omega\tau M_i^2}{32(1 + j\omega\tau)^2(1 + 2j\omega\tau)(1 + 3j\omega\tau)}
\tag{84}
$$

where $M_i = I_i/(2I_{bias})$ for a FD SI memory cell, with I_i being the input signal amplitude. Assuming $\omega_1 \cong \omega_2 \cong \omega_3 \cong \omega$ in (83), and $\omega\tau \ll 1$, HD_3 and IM_3 are given by:

$$HD_3(\omega) \cong \frac{-3}{32} j\omega\tau M_i^2 \qquad IM_3(2\omega_1 \pm \omega_2) \equiv \frac{3\rho^2}{4} \frac{H_3(j\omega_1, j\omega_1, \pm j\omega_2)}{H_1(j\omega_a)} \approx \frac{-9}{32} j\omega\tau M_i^2 \qquad (85)$$

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