Compact Low-Power Calibration Mini-DACs for Neural Arrays With Programmable Weights

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***Abstract*—This paper considers the viability of compact low-resolution low-power mini digital-to-analog converters (mini-DACs) for use in large arrays of neural type cells, where programmable weights are required. Transistors are biased in weak inversion in order to yield small currents and low power consumptions, a necessity when building large size arrays. One important drawback of weak inversion operation is poor matching between transistors. The resulting effective precision of a fabricated array of 50 DACs turned out to be 47% (1.1 bits), due to transistor mismatch. However, it is possible to combine them two by two in order to build calibrated DACs, thus compensating for inter-DAC mismatch. It is shown experimentally that the precision can be improved easily by a factor of 10 (4.8% or 4.4 bits), which makes these DACs viable for low-resolution applications such as massive arrays of neural processing circuits. A design methodology is provided, and illustrated through examples, to obtain calibrated mini-DACs of a given target precision. As an example application, we show simulation results of using this technique to calibrate an array of digitally controlled integrate-and-fire neurons.**

***Index Terms*—Analog design, calibration, current splitters, digital-to-analog converters, fuzzy circuits, neural networks, subthreshold, weak inversion.**

I. Introduction

HARDWARE very large-scale integration (VLSI) implementations of neural and fuzzy systems usually have an array type structure: the same cell is repeated in a large two dimensional array for massive parallel processing, and some additional circuitry is available at the periphery for additional processing and/or out-of- chip communications. For optimum area efficiency it is desired to simplify the cell as much as possible at the expense of complicating the periphery. However, many times one would like to improve the precision in the cells even if this requires some extra cell area. One simple way to provide such precision would be using some very compact and low power mini digital-to-analog converters (mini-DACs). In this paper, we describe a way to exploit this alternative. We propose a mini-DAC scheme that not only provides a way to improve system precision through calibration, but also allows to have a precise programmable weight value at each cell. This is a many times required feature in massive arrays neural-type processing systems. The mini-DACs described in this paper are based on the linear MOS transistor current splitting technique [1] with some extra calibration circuitry to compensate for inter-DAC mismatch.

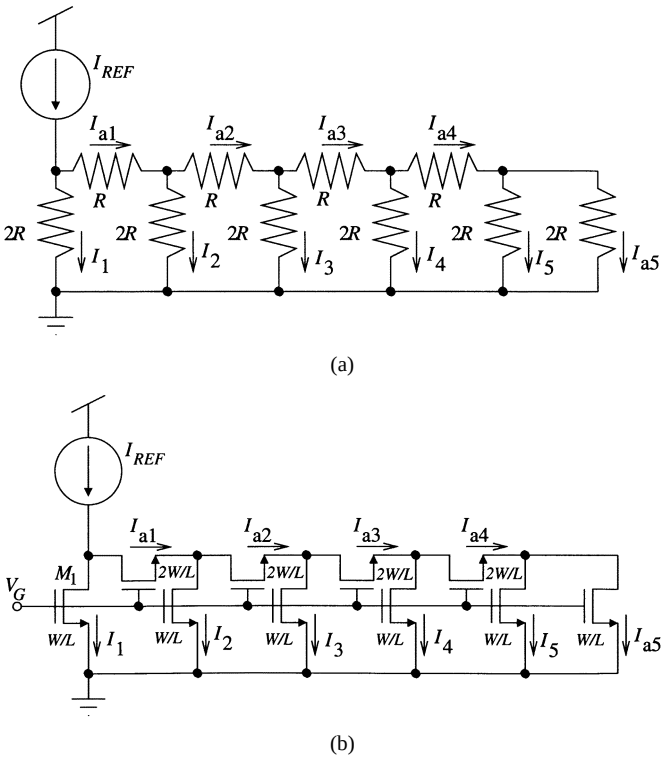

Fig. 1. Current splitter using (a) a resistor ladder or (b) an NMOS ladder.

This mini-DAC-based calibration technique differs substantially from floating gate tunneling techniques [2], [3]. These require the use of a high voltage node, which imposes very conservative layout rules [4], thus sacrificing compactness. As a comparison, the cells developed by Hasler *et al.* [3] consume an area comparable to the mini-DACs in this paper (after normalizing with respect to minimum feature sizes), although achieving better precision. Reliability is also an important issue in analog tunneling techniques (at least for standard CMOS), which is why those techniques are only used by a few very expert groups world-wide.

The paper is structured as follows. Section II describes the conventional MOS ladder structure and it is found that it suffers from huge inter-DAC mismatch, although each individual DAC behaves reasonably well. Section III proposes an alternative bias arrangement that improves precision by a factor of ten, although the circuit is not practical. In Section IV, practical implementations, based on calibration, that yield similar

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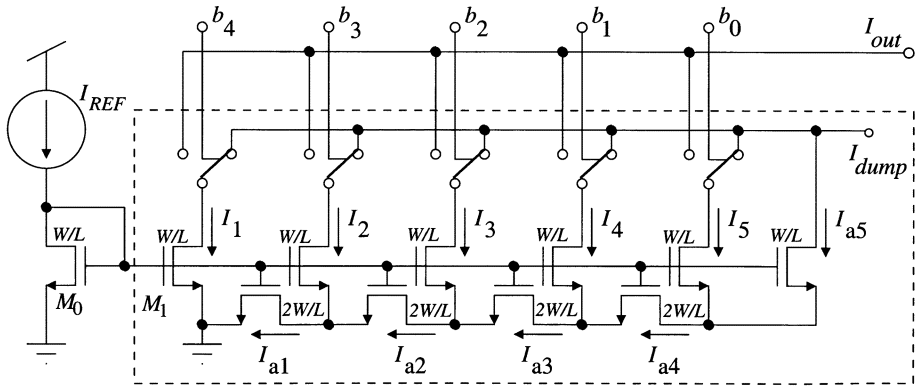

Fig. 2. Current splitting principle used in such a way that output transistors operate as current sources.

improvement factors are shown and verified. Section V establishes a parallel behavior between MOS ladders and resistor ladders, resulting in some interesting conclusions. Section VI discusses about achievable precision and layout compactness, and gives design examples for different precisions. Finally, Section VII describes an application example where an array of integrate-and-fire neurons is calibrated.

II. Voltage Biased Current DAC

In 1992, Bult and Geelen introduced a significant contribution in current mode MOS circuit design [1]. They discovered an inherently linear technique for splitting currents in a similar way that do the traditional resistor ladders. Consider, for example, the resistor ladder in Fig. 1(a). By doing parallel-series groupings of resistors it is easy to see that the reference current $I_{\rm REF}$ sees two $2R$ resistors in parallel, so that $I_1 = I_{a1} = I_{\rm REF}/2$. The same happens for current I_{a1}, so that $I_2 = I_{a2} = I_{a1}/2 = I_{\rm REF}/4$. Similarly, $I_3 = I_{\rm REF}/8$, $I_4 = I_{\rm REF}/16$, $I_5 = I_{\rm REF}/32$. Consequently, the resistor ladder in Fig. 1(a) provides five binary weighted currents $I_i = I_{\rm REF}/2^i$.

Fig. 1(b) shows the original current splitter proposed by Bult and Geelen using MOS transistors. The currents are split in the same way as by the resistor ladder: $I_i = I_{\rm REF}/2^i$. Bult and Geelen showed that the currents are split in the same way independently of the bias conditions of the transistors. Transistors can be in weak or strong inversion, in saturation or ohmic region (obviously, they cannot be off), and the splitting principle still works the same way. Intuitively, one can understand the circuit in Fig. 1(b) by noting that two $2W/L$ transistors in series are equivalent to one W/L transistor. Also, two W/L transistors in parallel are equivalent to one $2W/L$ transistor, and they would split the current equally (independently of bias conditions). Bult and Geelen used the binary weighted current splitter of Fig. 1(b) to build a DAC [1]. In order to select the currents and combine them, it was necessary to provide a virtual ground node for the transistors with grounded sources, which implies the use of some high gain amplifier that consumes an important power and area. Consequently, this approach would not be very efficient for large arrays.

Enz and Vittoz proposed an alternative way of using the current splitting technique which yields more efficient DACs [5]. This alternative is shown in Fig. 2. In this circuit, if the drains are connected to sufficiently high voltage nodes, the output currents are $I_i = I_{\rm REF}/2^{i-1}$. The drain voltages are not critical as long as they exceed a certain minimum so that the output transistors work as current sources, i.e., they are biased in saturation.

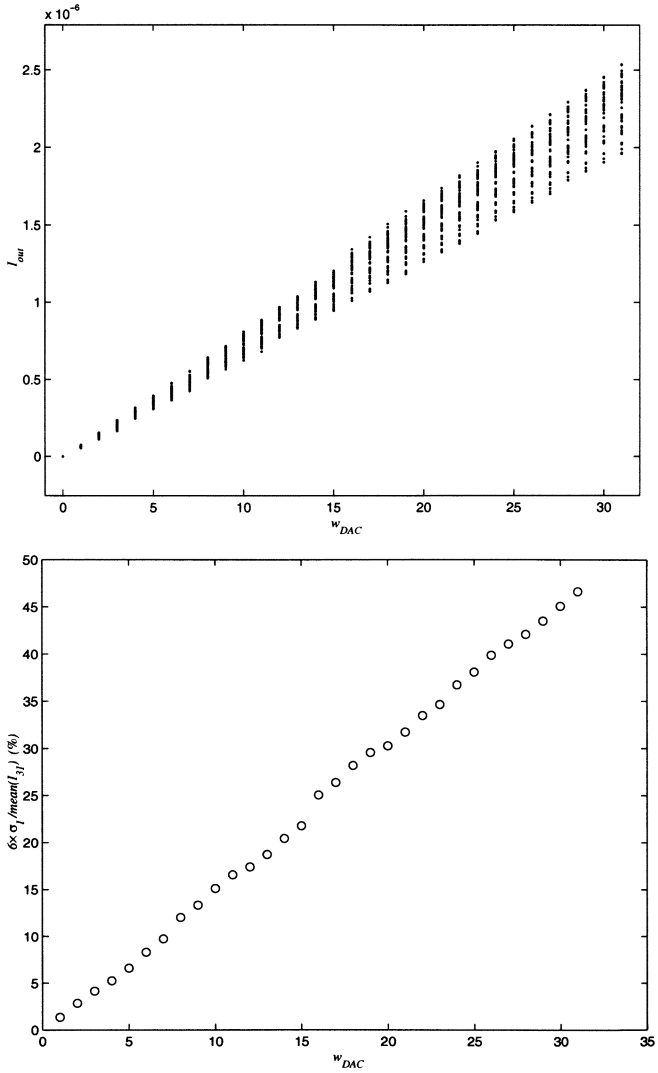

Fig. 3. (Top) Measured output currents for the 50 fabricated DACs. (Bottom) Corresponding standard deviations.

We have fabricated a linear array of 50 DACs, like the 5-bit one in Fig. 2, with $W = L = 5\ \mu$m. It was fabricated in the

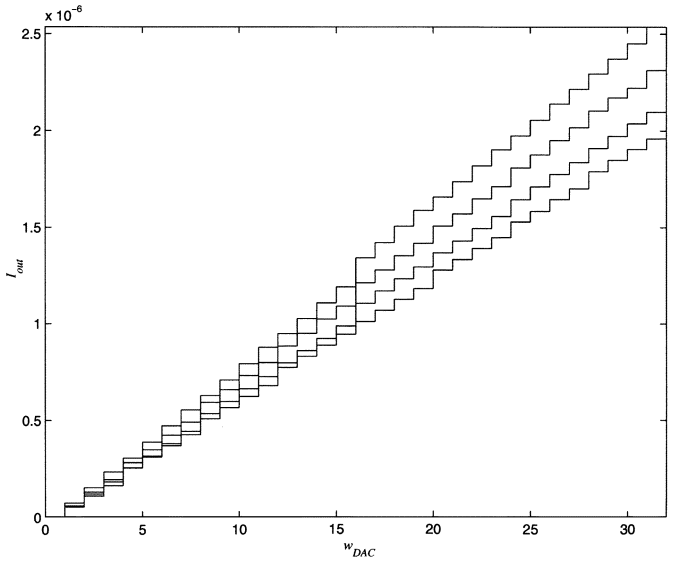

Fig. 4. Measured DAC staircases for a few DAC samples.

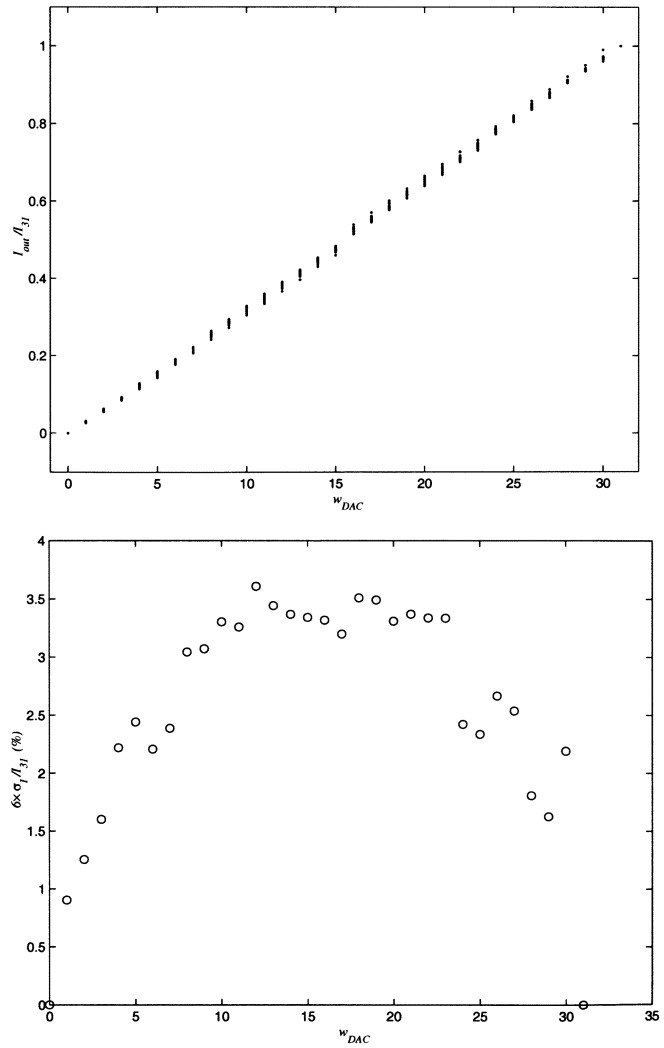

Fig. 5. (Top) DACs output currents normalized to their maximum value ($w_{\rm DAC} = 31$). (Bottom) Standard deviation of the DAC normalized output currents.

AMS 0.35-μm CMOS process. All transistors of the 50 DACs have the gate voltage connected together and to the gate of transistor M_o, which is biased by the reference current $I_{\rm REF}$. We call this type of arrangement *voltage biased DAC*, because the gate voltage is fixed and equal for all DACs. The DAC 5-bit digital control word $w_{\rm DAC} = \{b_4 b_3 b_2 b_1 b_0\}$ can be changed from $w_{\rm DAC} = 0$ to $w_{\rm DAC} = 31$. For each DAC we measured the output current $I_{\rm out}$ while sweeping $w_{\rm DAC}$ from 0 to 31. Fig. 3 (top) shows the measured currents superimposed for all 50 DACs. As can be seen, there is an important mismatch between the different DACs. Specifically, for the maximum current ($w_{\rm DAC} = 31$) the standard deviation is $\sigma_I = 7.77\%$, which means that 99.7% of the samples are within an interval of $6\sigma_I = 47\%$ (assuming a normal distribution). Fig. 3 (bottom) shows the corresponding inter-DAC error

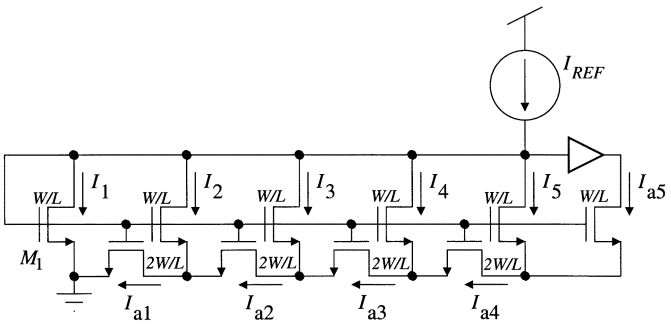

Fig. 6. Current biased DAC.

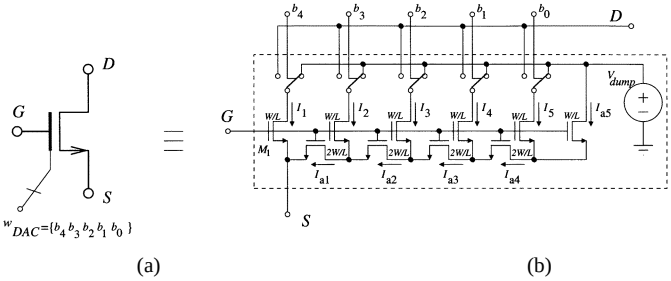

Fig. 7. Digitally controlled MOS (digi-MOS). (a) Symbol. (b) Circuit schematic.

$$\frac{6\sigma(I_{\rm out}(w_{\rm DAC}))}{\overline{I_{\rm out}}(w_{\rm DAC}=31)} \tag{1}$$

in percent. To express this precision in bits, just note that

$$\frac{1}{2^b} = \frac{\Delta I}{I_{\max}} = \frac{6\sigma_I}{I_{\max}} \quad \Leftrightarrow \quad b = -\frac{\ln\left(\frac{6\sigma_I}{I_{\max}}\right)}{\ln 2} \tag{2}$$

where b is the equivalent number of bits. A variation interval of $6\sigma_I = 47\%$ corresponds to a precision of $b = 1.1$ bits. Obviously, this circuit cannot be used as a 5-bit DAC but rather as a 1-bit DAC. The reason for this misbehavior is the mismatch of the MOS transistors, which produces very high inter-DAC mismatch. In what follows we will present different alternatives for lowering this inter-DAC mismatch. These techniques can be used to calibrate arrays of DACs within a single chip, or even among different chips.

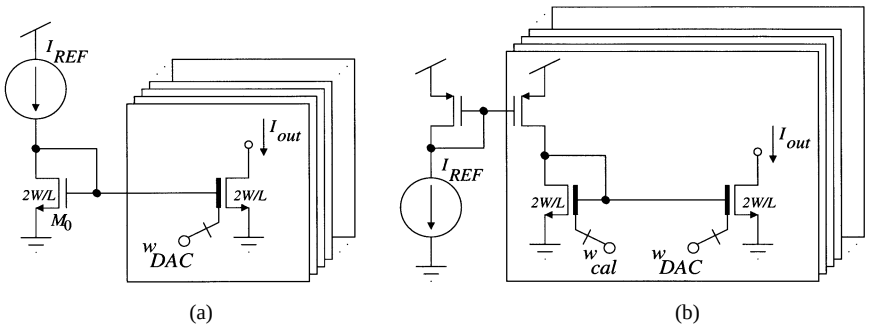

Fig. 8. (a) Array of uncalibrated DACs of Fig. 2. (b) Calibrated version.

III. Current Biased DAC

Although the measurements in Fig. 3 reveal a very high inter-DAC mismatch, it is interesting to note that for each DAC we obtain a well-behaved stair-case. This is, for each DAC the stairs progress monotonically increasing, without showing eventual down steps, as is shown in Fig. 4 for a few samples. This phenomenon can be further visualized by plotting the data in Fig. 3, but where each DAC is normalized to its maximum value. This is shown in Fig. 5 (top). Here we can see that the maximum error is produced in the central part of the range. Fig. 5 (bottom) shows the deviation $6\sigma(w_{\rm DAC})$ in percent as a function of the DAC digital control word $w_{\rm DAC}$. The maximum is obtained in the center for $w_{\rm DAC} = 12$ with $6\sigma_I(12) = 3.6\%$. This corresponds to a precision in bits of $b = 4.8$ bits.

As we can see, by normalizing the output current of the DACs with respect to their individual total current we can improve the mismatch from $6\sigma_I = 47\%$ (1.1 bits) to $6\sigma_I = 3.6\%$ (4.8 bits). One way of achieving in practice such normalization would be by forcing their total currents to be constant, as is shown in the circuit of Fig. 6. In this circuit the gate voltages of the MOS transistors in each DAC is self-adjusted to set the maximum current constant and equal to the reference current $I_{\rm REF}$. We call this bias arrangement the *current biased DAC*.

IV. Calibrated DAC

The problem with the circuit in Fig. 6 is that all currents I_i need to be added permanently and be forced to add $I_{\rm REF}$. Consequently, we cannot select/deselect any of them arbitrarily to form any combination of them, i.e., to form a DAC. One way to overcome this problem and to force the sum of all currents I_i to be constant is through calibration.

Consider the part of the circuit in Fig. 2 comprised by broken lines. Note that this circuit behaves equivalently to a MOS transistor of size $2W/L$ whose source is connected to ground and whose Drain to node $I_{\rm out}$, but from which we are taking just a fraction of its drain current. This fraction is controlled digitally by control word $w_{\rm DAC} = \{b_4 b_3 b_2 b_1 b_0\}$. Let us use the symbol in Fig. 7(a) to represent this circuit, shown in Fig. 7(b), and let us call it the *digitally controlled MOS* or *digi- MOS*. Using this symbol convention, the circuit in Fig. 2 can be redrawn as shown in Fig. 8(a), where we represent an array of DACs (instead of just one as in Fig. 2). This circuit (a voltage biased DAC array) presented an important mismatch behavior. In order to force the output current $I_{\rm out}$ to be constant for $w_{\rm DAC} = 31$ (the maximum value), we can use the circuit in Fig. 8(b) where global transistor M_0 has been substituted by many *digi-MOS*, one for each cell. For this circuit $w_{\rm cal}$ is used to set (calibrate) $I_{\rm out}$, while $w_{\rm DAC} = 31$ is maximum. Decreasing $w_{\rm cal}$ increases the gain of the mirror. Consequently, all values $I_{\rm out}$ of the DACs need to be set to the original uncalibrated maximum value. The final error at $I_{\rm out}$ will be of the order of the least significant bit of the DAC (in this case $I_{\rm REF}/32$). We used this approach with our linear array of 50 DACs (or *digi-MOS*), by grouping them two by two, and using the first one for calibration through w_{cal}. This way, we end up with 25 calibrated DACs. Fig. 9 (top) shows the output currents of these 25 calibrated DACs as a function of the digital control word $w_{\rm DAC}$. Fig. 9 (bottom) shows the precision obtained with this approach. As can be seen, a maximum error of $6\sigma_I = 7.0\%$ is obtained for $w_{\rm DAC} = 30$, which is equivalent to $b = 3.8$ bits.

At this point it is interesting to have a look at the resulting 25 calibration words $w_{\rm cal}$. It turns out that the required calibration words range from a maximum of $w_{\rm cal} = 31$ (no calibration) to a minimum of $w_{\rm cal} = 24$. Consequently, the two most significant bits are not being used in the calibrations (for this particular mismatch distribution). Note that the available precision without calibration was 1.1 bit. Consequently, it is reasonable to expect that at least the most significant calibration bit might not be required. On the other hand, it would be nice to take advantage of this unused bit to further improve the calibration: note that we have been able to calibrate to 3.8 bits instead of the ideal 4.8 limit observed in Section III. The circuit in Fig. 10 intends to pursue this objective. Here, the maximum correction is $I_{\rm REF}/2$ instead of $I_{\rm REF}$, but in steps of $I_{\rm REF}/64$ instead of $I_{\rm REF}/32$. Fig. 11 shows the results for this calibration strategy. Fig. 11 (top) shows the absolute output currents in terms of the digital control word $w_{\rm DAC}$ for all 25 calibrated DACs, while Fig. 11 (bottom) shows the resulting standard deviations in percent. The maximum standard deviation is $6\sigma_I = 4.8\%$ obtained for $w_{\rm DAC} = 20$, which is equivalent to $b = 4.4$ bits. In this situation the calibration words range from a minimum of $w_{\rm cal} = 0$ (no calibration) to a maximum of $w_{\rm cal} = 18$, hence using all five control bits (for this particular mismatch distribution).

V. Comparison With Resistor Ladders

Although resistor ladders and MOS ladders are not exactly the same, their behavior in current splitting is identical [1]. Regarding their behavior with respect to mismatch, they are qualitatively and quantitatively very similar. The linear nature of the resistors allows us, on the other hand, to study its mismatch

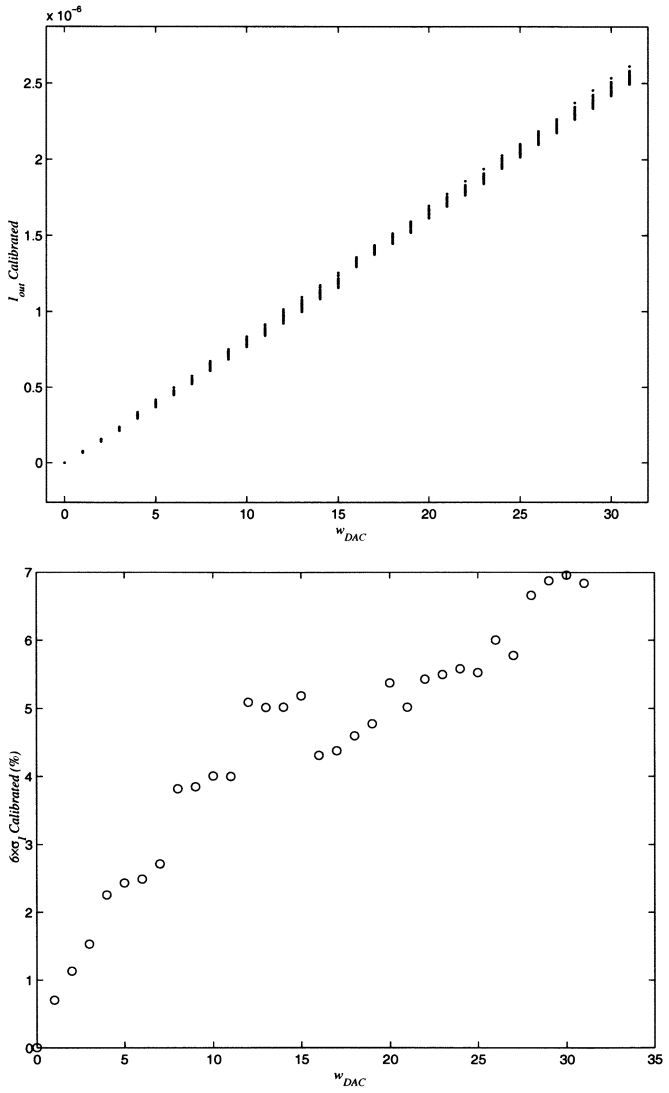

Fig. 9. Measured results for the calibrated DAC. (top) Output current versus digital control word w_{cal} and (bottom) resulting standard deviations.

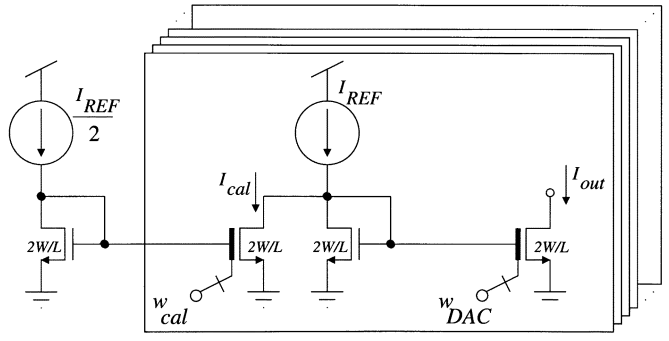

Fig. 10. Alternative calibration arrangement for improved precision.

behavior using relatively simple mathematical models. In order to compare our MOS measurements to eventual resistor ladder numerical (MATLAB) simulations, we need to characterize the standard deviation of our individual MOS devices. In our MOS ladder measurements, we have access only to the output currents I_i [see Figs. 1(b) and 2 or Fig. 6]. Note that the mismatch of these currents is a function of the mismatch

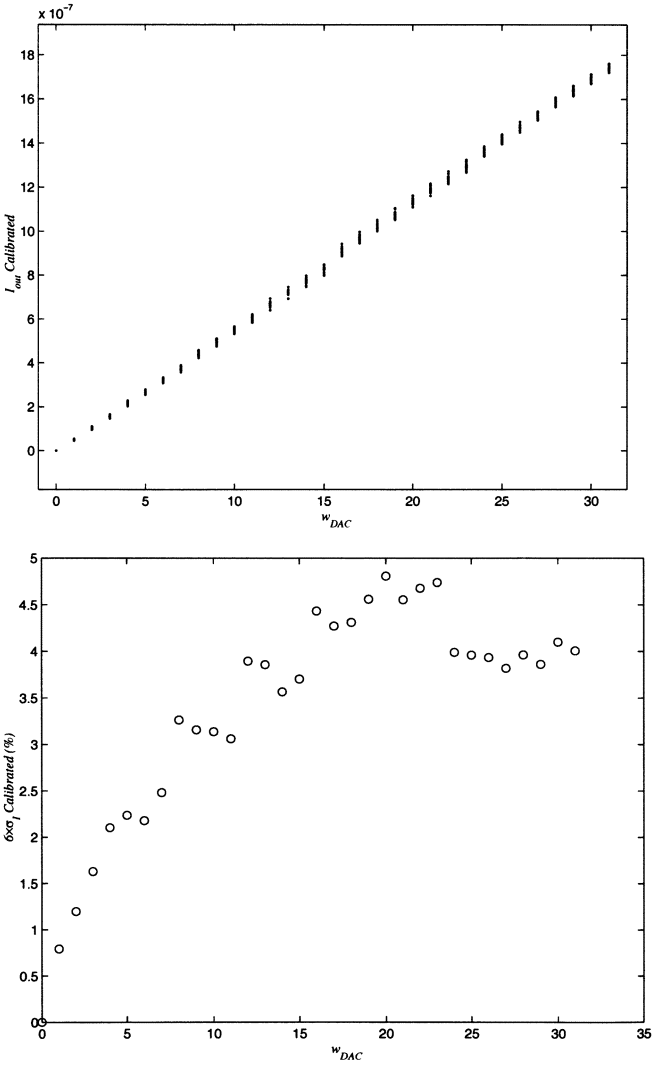

Fig. 11. Measurement results for the calibration arrangement of Fig. 10. (Top) Output current versus digital control word w_{DAC}. (Bottom) Resulting standard deviations.

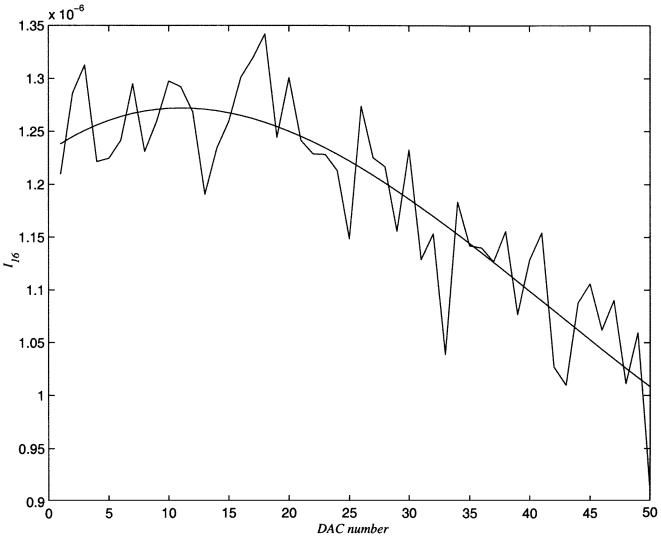

Fig. 12. Measured current at transistor M_1 for the 50 DACs over a distance of 2.6 mm.

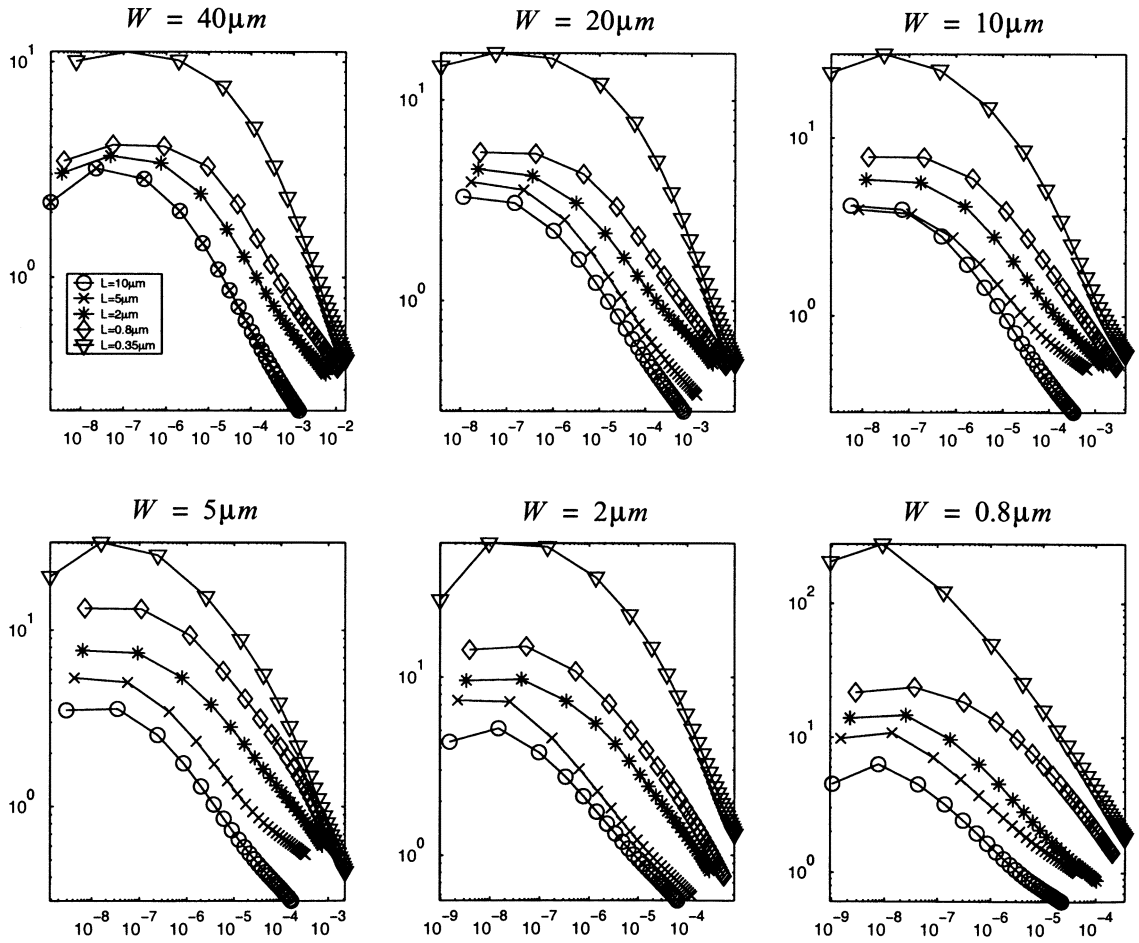

Fig. 13. Current mismatch measurements (in percent) for arrays of transistors of 30 different sizes, as a function of their nominal operation currents. These measurements correspond to a different 0.35-μm CMOS process.

of all MOS transistors in the circuit, except for current I_1 and transistor M_1 in the voltage biased configuration. For this configuration the mismatch at I_1 depends only on the mismatch of transistor M_1 of size W/L. Consequently, the standard deviation measured for the I_1 currents $\sigma(I_1)$ is equal to the standard deviation of the drain- to-source current of one W/L transistor $\sigma(I_{\mathrm{W/L}})$. By looking at the output current for $w_{\mathrm{DAC}} = 16$ we are observing the current I_1 produced by transistors M_1 only. Fig. 12 shows this current for all 50 fabricated DACs as a function of DAC position. The overall standard deviation for this current is equal to $\sigma_{16} = 8.13\%$. The 50 DACs are arranged in a linear array of total length equal to 2.6 mm. As can be seen in Fig. 12, there is a gradient component plus a random component. Fitting the measured data to a third-order polynomial yields the continuous curve shown in Fig. 12. Subtracting this curve from the measured data results in the pure random component. The standard deviation for this pure random component is $\sigma(I_1) = 3.8\%$. Let us assume that this mismatch is approximately the same for all transistors in the ladder, independently of their operating currents. This assumption is approximately true, if all transistors operate within subthreshold [6], [7]. Fig. 13 shows measured standard deviations $\sigma(I_{\mathrm{W/L}})$ of the drain-to-source currents for arrays of NMOS transistors of 30 different sizes: $W = \{40, 20, 10, 5, 2, 0.8\}$ μm, $L = \{10, 5, 2, 0.8, 0.35\}$ μm, by extending a systematic procedure published elsewhere [8] to subthreshold region. These measurements correspond to a different 0.35-μm CMOS process than the one used for the fabricated mini-DACs. Horizontal axes are nominal currents and vertical axes are standard deviations at the drain-to-source currents $\sigma(I_{\mathrm{W/L}})$ in percent. For high currents, the transistors operate in strong inversion and $\sigma(I_{\mathrm{W/L}})$ reaches minimum values. For lower currents $\sigma(I_{\mathrm{W/L}})$ tend to stay at maximum current independent values. By looking at the subframe $W = 5$ μm and curve $L = 5$ μm (crosses) for nominal current 1 μA, the measured current mismatch standard deviation was actually very close to 3.8% (the gradient-less mismatch observed for the data in Fig. 12).

Let us now use this value as the standard deviation contributed by each resistor R of the current biased resistor ladder shown in Fig. 14.[1] Resistors of value $2R$ are implemented with two R resistors in series. Fig. 15 (top) shows the MATLAB simulated currents obtained statistically for all digital combinations of currents $\{I_1, I_2, I_3, I_4, I_5\}$ in terms of the digital control word w_{DAC}. Fig. 15 (bottom) shows the corresponding

[1]For MOS ladders, since the current decreases for each branch, transistor mismatch increases slightly, as can be seen in Fig. 13. However, for weak inversion the mismatch tends to stabilize as current decreases. For example, for $W = L = 5$ μm, σ changes from about 3% for 1 μA to about 5% for 1 nA (three decades). Consequently, it is reasonable to assume σ approximately constant for all branches because the maximum current ratio is 16.

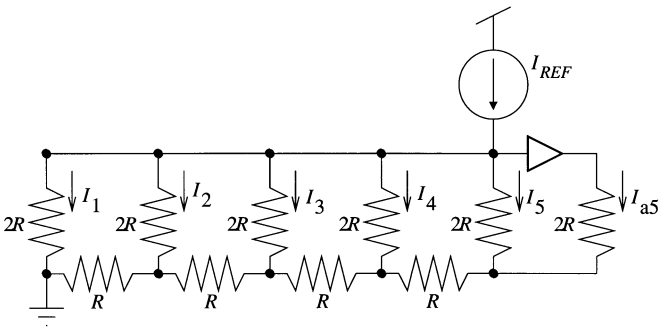

Fig. 14. Current biased resistor ladder.

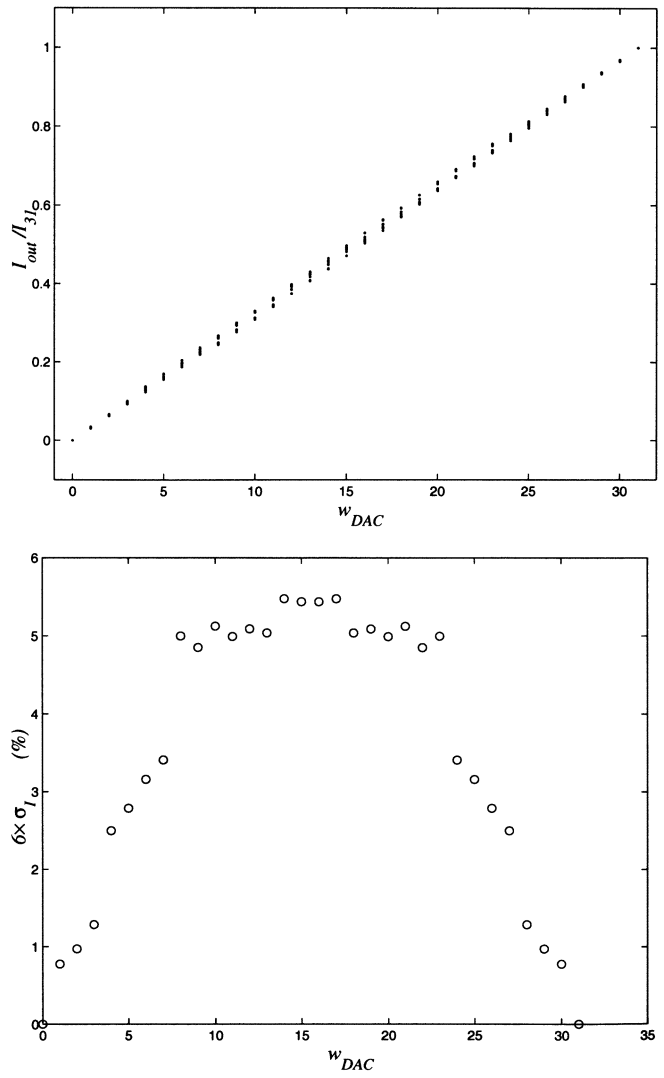

Fig. 15. Current biased resistor DAC numerical MATLAB results. (top) Output currents. (bottom) Resulting standard deviations.

standard deviation $6\sigma_I$ in percent. Comparing Fig. 15 for resistors with Fig. 5 for MOS transistors, we can see that both ladder structures provide similar DAC precision. Consequently, we have reasons to believe that the mismatch behavior of resistor ladders and MOS ladders might be similar.

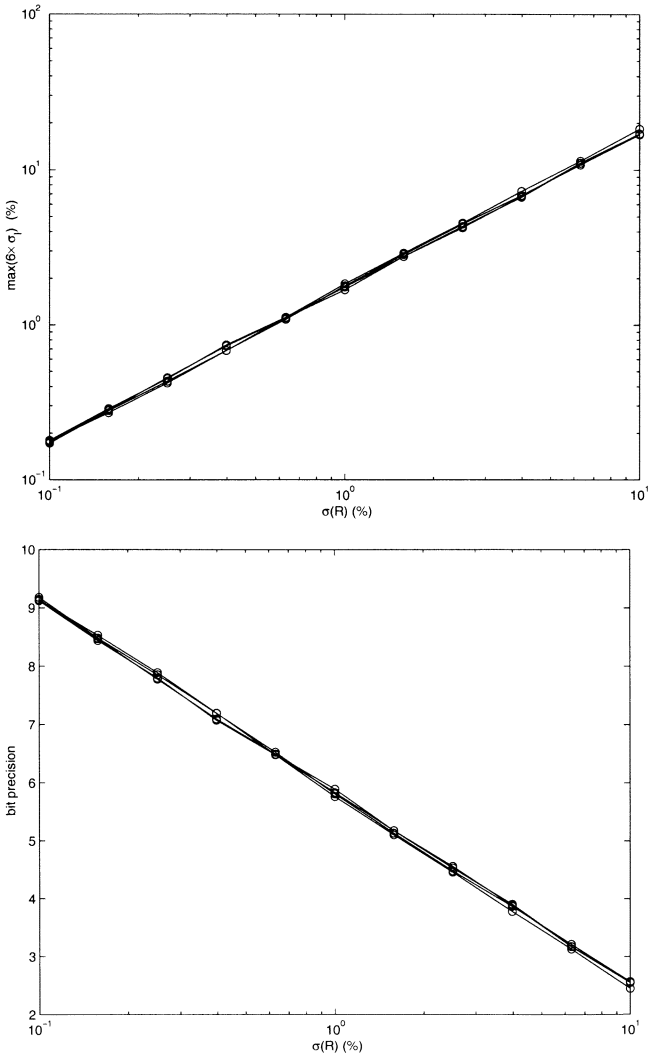

Fig. 16. Current biased resistor DAC effective precisions as function of resistor mismatch $\sigma(R)$ and DAC resolution, expressed (top) as $\max(6\sigma(I_{\rm out}))$ and (bottom) as effective bits.

Taking advantage of this conjecture, let us now study, for the resistor current biased DAC structure of Fig. 14, how the DAC precision

$$6\sigma(I_{\rm out}) = \max_{w_{\rm DAC}}\{6\sigma_I(w_{\rm DAC})\} \tag{3}$$

depends on the standard deviation $\sigma(R)$ of the individual resistors. The results of this study are shown in Fig. 16 (top), where $\sigma(R)$ has been swept from 0.1% to 10%. Each line corresponds to a different DAC resolution (i.e, the number of output branches), which has been changed from three to nine bits. As can be seen, the following relationship:

$$6\sigma(I_{\rm out}) \approx 2\sigma(R) \tag{4}$$

is satisfied approximately for the whole range, independently of DAC resolution. Consequently, we can state that "*for a current biased resistor DAC the worst-case output current standard*

deviation $\sigma(I_{\rm out})$ is approximately 1/3 *that of its individual resistor components $\sigma(R)$.*" Using (2), we can express the DAC precision in bits as well

$$b = -\frac{\ln 6\sigma(I_{\rm out})}{\ln 2} = -\frac{\ln 2\sigma(R)}{\ln 2} \tag{5}$$

which is shown in Fig. 16 (bottom). Since we have reasons to believe there is a similar mismatch behavior between resistor ladders and MOS ladders, Fig. 16 might be extensible to MOS current biased DACs as well.

VI. Achievable Precision and Layout for MOS Low-Power Mini-DACs

Fig. 16 and (5) provide hints on how the effective precision of current biased DACs depend on the mismatch of their individual components. On the other hand, Fig. 13 showed the mismatch of individual MOS devices $\sigma(I_{W/L})$ as functions of current operating level and transistor sizes. Combining both Figs. 13 and 16, one can select the optimum transistor size W/L for a given DAC precision to achieve. For example, Fig. 13 reveals that for $W = L = 5\ \mu$m and currents between 1 μA and $1/16\ \mu\text{A} = 62.5$ nA the current mismatch standard deviation $\sigma(I_{W/L})$ is between 2.5% and 5%. Using this in Fig. 16 (bottom) yields an effective DAC precision around 4 bits, as we obtained experimentally in Sections III and IV. If we would need a 6-bit DAC, Fig. 16 (bottom) reveals that we need components with a mismatch of about $\sigma = 0.9\%$. From Fig. 13 we can see that the transistor size achieving $\sigma = 0.9\%$ with minimum current is $W = 5\ \mu$m, $L = 10\ \mu$m at 6 μA. If on the other hand we need an 8-bit DAC, then according to Fig. 16 (bottom) we require components with a mismatch of about 0.22%. Then looking at Fig. 13 we can see that for transistors of size $W = 40\ \mu$m and $L = 10\ \mu$m operating at or above 1 mA we would be able to obtain an 8-bit DAC.

In the ladder structures seen so far, one can see that the mismatch of the output currents I_i depends on the mismatch of all devices in the structure, except for current I_1 and the transistors in the first branch of the ladder. Consequently, there will be an important correlation in the resulting mismatches. This might be one of the reasons why the standard deviation of the ladder structure improves a factor of three that of the individual devices. If this is the case, building the ladder structure as shown in Fig. 17 would improve the overall precision, since now all output currents will be correlated. In order to verify this postulate we have used our 5-bit DACs data to emulate 4-bit calibrated DACs. One of them using currents $\{I_1, I_2, I_3, I_4\}$ as outputs, and the other using currents $\{I_2, I_3, I_4, I_5\}$ as outputs. It is found that there is a slight improvement in precision (from 5.2% to 4.8%), but not very significant: about a 10% of improvement only.

The layout for these DACs can be made very compact. As an illustrative example, Fig. 18 shows the layout for a MOS ladder structure corresponding to 5-bit resolution, including the selection switches. The unit transistor size is $W = L = 3\ \mu$m, and the resulting total area is 22 μm$\times$ 18 μm. This layout corresponds to the design rules for the AMS 0.35-μm 3-metal, double poly design rules. One calibrated DAC would use two of these structures, as was shown in Fig. 8(b) or Fig. 10.

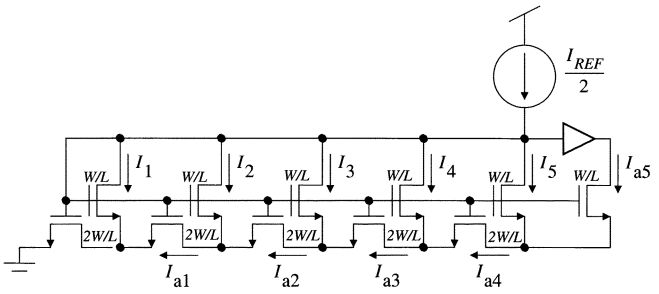

Fig. 17. Alternative ladder arrangement to make the mismatch of all the output currents to be intercorrelated.

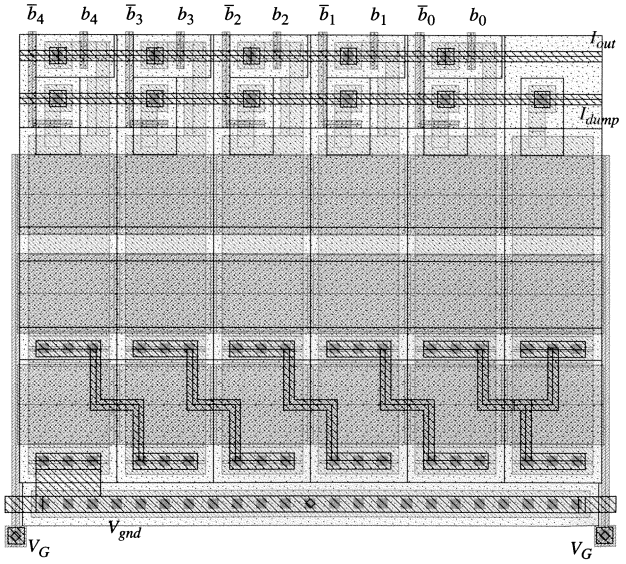

Fig. 18. Example layout of a 5-bit NMOS mini-DAC ladder structure for $W = L = 3\ \mu$m. Size is 22 μm$\times$ 18μm.

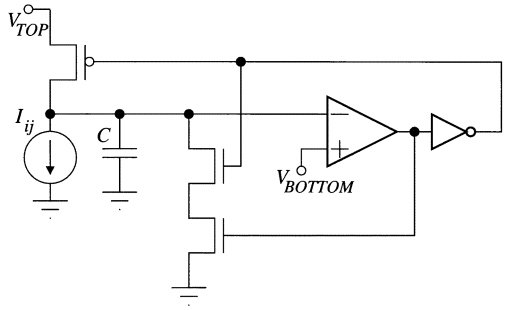

Fig. 19. Circuit schematic of current-driven I&F neuron.

VII. Example Application to Neural Systems

The calibrated mini-DACs described so far have potential application in many low-moderate precision massive array VLSI structures, such as neural and fuzzy systems. In our particular case, we intend to exploit them in arrays of integrate-and-fire (I&F) neurons [9]. Fig. 19 shows the circuit of an I&F neuron that transforms input current I_{ij} into an output frequency f_{ij}. Current I_{ij} could be produced by photo detectors [10] or analog current-mode signal processing circuits [11]. The dependence between I_{ij} and f_{ij} is fairly linear, although the slope suffers from important mismatch between neurons and also between different chips. Using the mismatch characterization results

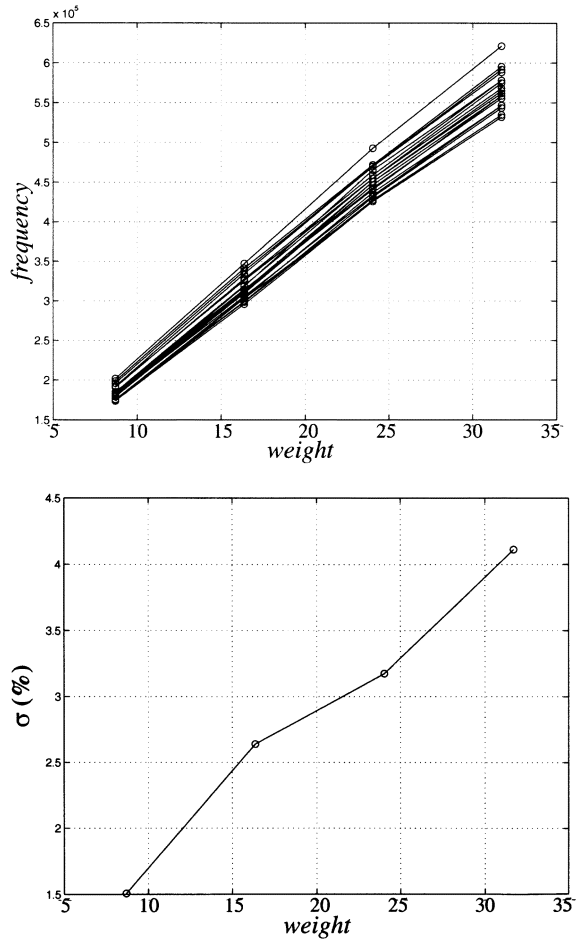

Fig. 20. Monte Carlo simulation results for an array of I&F neurons. (Top) Neurons frequency versus weight for uncalibrated neurons. (Bottom) Corresponding standard deviation in percent.

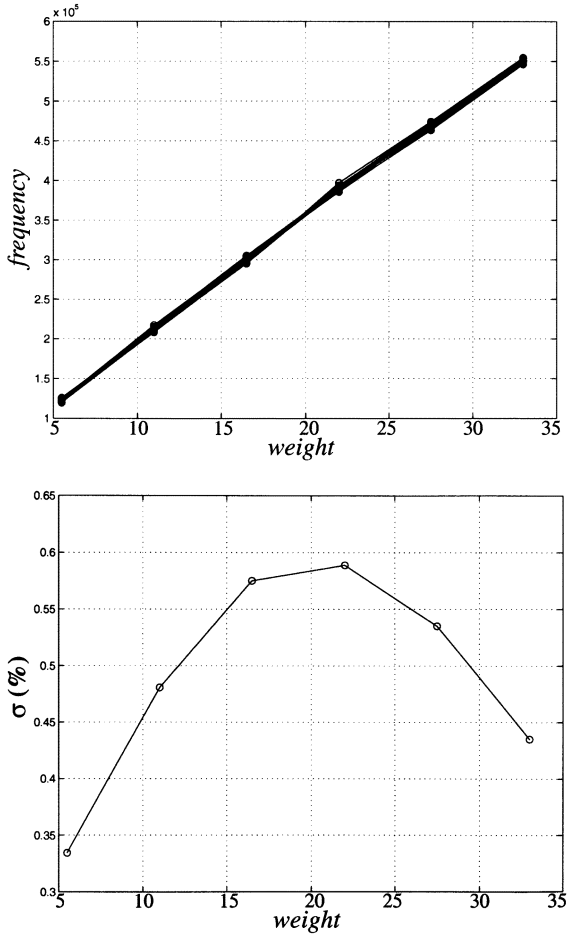

Fig. 21. Monte Carlo simulation results for an array of I&F neurons. (Top) Neurons frequency versus weight for calibrated neurons. (Bottom) Corresponding standard deviation in percent.

shown in Fig. 13 we have performed Monte Carlo simulations to estimate the variations in the slopes f_{ij}/I_{ij}. These results are shown in Fig. 20 (top). Current I_{ij} is set to be proportional to a $\text{weight} = w_{\text{DAC}}$, such that $I_{ij} = \text{weight}_{ij} \times I_{\text{ref}}$. Fig. 20 (bottom) shows the corresponding standard deviation in percent. The maximum value is $\sigma = 4.11\%$, which corresponds to a precision of 2.02 bits. By introducing a mini-DAC calibration scheme, the I_{ij} versus f_{ij} curves change to those shown in Fig. 21 (top), with the mismatch standard deviation depicted in Fig. 21 (bottom). The maximum value is $\sigma = 0.59\%$, or equivalently, 4.82 bits.

VIII. Conclusion

In this paper, we have studied, and validated with experimental results, the possibility of exploiting small size low-power low-resolution DACs for VLSI neural massive arrays. The MOS structure studied is a ladder structure, which scales linearly with the number of resolution bits. Because of low-power requirements, transistors are biased in weak inversion, which yields important mismatch behavior. A calibration scheme is proposed and verified experimentally for compensating mismatch and improve precision by a factor of ten. The MOS ladder structure has been compared against the conventional resistor ladder structure, and it is found that the mismatch behavior is very similar. It is found that the standard deviation of the ladder structure is about one third of that of the single devices used. It is shown how to use the provided experimental data to design calibration mini-DACs for a target precision. As an application, the use of mini-DACs to calibrate an array of I&F neurons is described.

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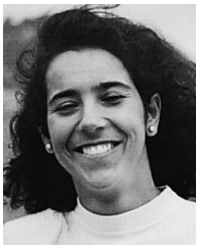

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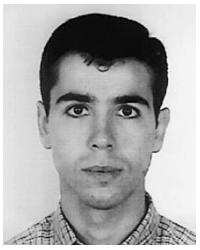

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