A 515 nW, 0-18 dB Programmable Gain Analog-to-Digital Converter for In-Channel Neural Recording Interfaces

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***Abstract*—This paper presents a low-area low-power SC-based Programmable-Gain Analog-to-Digital Converter (PG-ADC) suitable for in-channel neural recording applications. The PG-ADC uses a novel implementation of the binary search algorithm that is complemented with adaptive biasing techniques for power saving. It has been fabricated in a standard CMOS 130 nm technology and only occupies 0.0326 mm^2. The PG-ADC has been optimized to operate under two different sampling modes, 27 kS/s and 90 kS/s. The former is tailored for raw data conversion of neural activity, whereas the latter is used for the on-the-fly feature extraction of neural spikes. Experimental results show that, under a voltage supply of 1.2 V, the PG-ADC obtains an ENOB of 7.56 bit (8-bit output) for both sampling modes, regardless of the gain setting. The amplification gain can be programmed from 0 to 18 dB. The power consumption of the PG-ADC at 90 kS/s is 1.52 μW with a FoM of 89.49 fJ/conv, whereas at 27 kS/s it consumes 515 nW and obtains a FoM of 98.31 fJ/conv.**

***Index terms*—Biomedical, PGA, ADC, low-power, low-voltage, binary search algorithm, successive approximation, SC circuits, mismatch.**

I. Introduction

During the last years there has been a growing interest in the design of neural recording interfaces with wireless transmission capabilities for the untethered measurement of brain activity. These systems are expected to play a significant role both in clinical procedures, e.g., providing new therapies for patients with neurological diseases, and neuroscience applications such as brain-machine interfaces [1]–[10]. These neural interfaces typically consists of a Multi-Electrode-Array (MEA) for capturing the neural activity, followed by a bank of low-noise amplifiers (LNAs), band-pass filters, and programmable gain amplifiers (PGAs) for signal conditioning. Usually, a set of data converters follows in order to digitize the acquired data. Once in digital domain, neural signals are further processed for bandwidth reduction, digital encoding and data transmission purposes [6], [8], [9], [11]–[16]. The trend today is to embed all these electronics in a single System-on-Chip (SoC). However, this poses significant design challenges in terms of power consumption (the overall dissipation should not exceed a few mWs to avoid damages in the brain tissue) and area occupation (the pitch of neural recording MEAs is typically 200-400μm width).

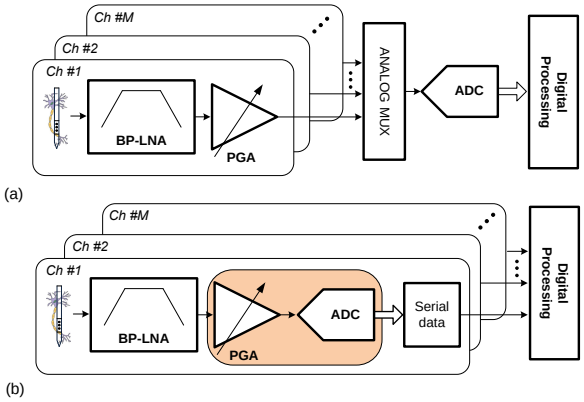

Figure 1. Partitioning of multichannel neural recording interfaces: (a) by time-multiplexing an ADC between M channels and, (b) by embedding an ADC per channel and serially transferring the digital information to a digital processor.

One key issue in the implementation of neural recording SoCs is the *physical system partitioning*. To simplify connectivity and ease system integration, neural interfaces should be aligned to the MEA reticule. This leads to the definition of as many recording channels as microelectrodes in the MEA. Many solutions move part of the front-end electronics, typically the data converter, out of the channel to the periphery of the recording area [1], [2], [17]. This is illustrated in Fig. 1(a) in which an analogue-to-digital converter (ADC), running *M* times faster than for a single channel, is shared among *M* recording sites. This approach relaxes the in-channel integration density, but exhibits important shortcomings. First, stronger demands are placed on the driving capabilities of the blocks preceding the ADC [PGAs in Fig. 1(a)], not only because of the reduced sampling time [18], but also because routing parasitics notably increase the load capacitance of these blocks. It means that even assuming that the power consumption of the multiplexed ADC scales linearly with the sampling frequency for a given resolution, the overall system dissipation increases. Second, as analog signals may eventually cross the complete recording array, they are prone to become contaminated by crosstalk and noise. And, finally, the solution of Fig. 1(a) is not easily scalable: a new multiplexed channel requires the redesign of the ADC and the adjustment of the in-channel output stages, as the driving conditions change.

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Clearly, an architecture like the one shown in Fig. 1(b), in which the complete front-end electronics, included a dedicated ADC, is embedded in every recording channel, avoids the above shortcomings. However, this approach calls for novel design strategies to comply with the severe area constraints of a full in-channel integration.

This paper aims to contribute to this topic and proposes a block reuse approach to afford the extra hardware. Namely, this paper presents a novel combination of PGA and ADC [shaded area in Fig. 1(b)], which avoids the use of the large capacitive DACs typically found in the SAR ADC architectures employed in neural recording interfaces [19]–[27]. Indeed, the proposed block offers much lower input capacitance than SAR structures, thus relaxing the driving requirements of the preceding circuits. In the proposed combined structure, the ADC reuses the Operational Transconductance Amplifier (OTA) of the PGA and requires only two capacitors and a simple switch arrangement to perform the conversion. This is accomplished by successively adding or subtracting binary-scaled versions of the converter voltage reference to the input sample previously acquired during the PGA operation, and keeping track of the sign of the newly generated voltages. Since the voltage excursions shrink as the conversion progresses, the current demand of the OTA relaxes and, hence, adaptive biasing techniques can be used for power saving. By using this approach, an overall reduction of about 55% has been obtained with respect to using a single bias setting.

A prototype of this proposal was designed and fabricated using a standard 130nm CMOS technology within a neural spike recording channel. The gain of the PGA section was adjustable between 0 and 18dB in eight discrete steps. The ADC had 8-bit of resolution and two selectable sampling frequency modes, 27 kS/s and 90 kS/s. The lower data rate is used for raw data conversion of neural activity, whereas the higher one is used for the on-the-fly feature extraction of neural spikes based on Piece-Wise Linear (PWL) approximations. Full details of the feature extraction approach are given in [28]. Experimental results confirmed that the PG-ADC only consumes 1.52 μW for the highest sampling mode, with a FoM of 89.49fJ/conv.

The paper is structured as follows. Section II describes the proposed block, hereafter denoted as PG-ADC, and presents a detailed analysis of the impact of non-idealities on circuit performance from which design criteria for sizing are extracted. Section III presents the implementation of the different building blocks of the PG-ADC with emphasis on the applied adaptive biasing strategy. Section IV shows the experimental results measured from the silicon prototype. Conclusions are compiled in section V.

II. Programmable-Gain ADC Architecture

Fig. 2(a) shows the schematic of the proposed PG-ADC. It comprises a fully-differential OTA, a comparator and some digital circuitry for timing, control and output generation. The circuit implements two basic operations: signal acquisition and amplification, on the one hand, and data conversion, on the other. As illustrated in the timing diagram of Fig. 2(b), both operations are enabled from a single master clock signal with

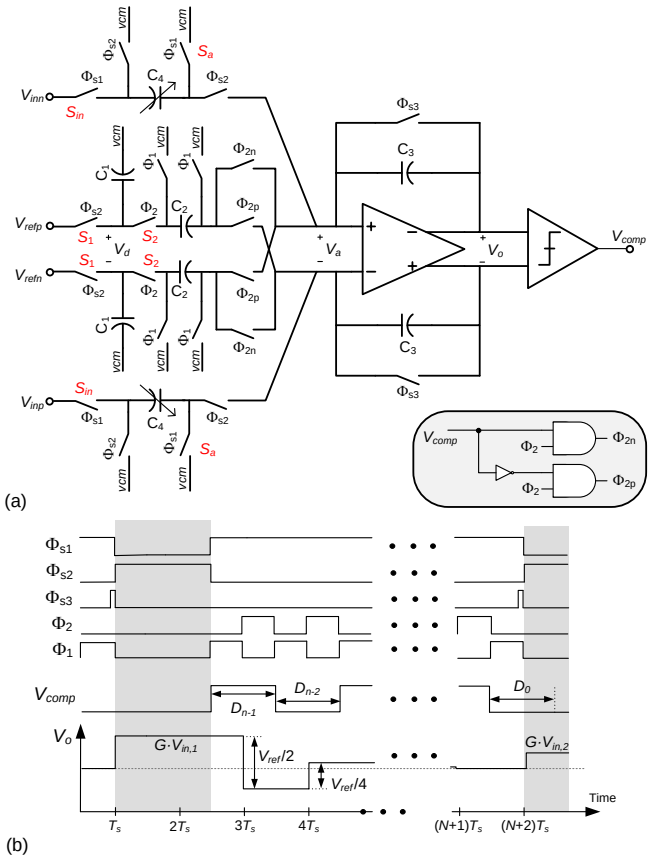

Figure 2. SC-based ADC implementation: (a) Schematic and (b) timing diagram (shaded intervals indicate the charge transfers from the sampling capacitor to the integration capacitor).

frequency f_s and period T_s. The parameters and variables used along this paper are summarized in Table I for easy reading.

During the acquisition and amplification operation, controlled by the clock phases Φ_{s1}, Φ_{s2} and Φ_{s3}, the differential input signal V_{in} is sampled, amplified by the capacitance ratio G^A, and transferred to the integration capacitors C_3 at the feedback loop of the OTA. Simultaneously, the reference voltage $V_{ref} = V_{refp} - V_{refn}$ of the ADC is stored in the capacitors C_1. The amplification gain G^A can be adjusted by implementing C_4 as a programmable capacitor array. The phase Φ_{s1}, which controls the load of the input signal in C4, is active during most of the conversion, except for the initial phase in which Φ_{s2} becomes active, when the input charge is transferred to C3. This long sampling phase aims to relax the dynamic requirements of the preceding block (PGA in case of the solution shown in Fig. 1(b)), in order to reduce their power consumption. Prior to the transfer of the input charge, which lasts for 3/2 master clock periods, the integration capacitor is reset by a short pulse Φ_{s3}.

During the data conversion operation, controlled by the clock phases Φ_1 and Φ_2, the differential signal stored in C_3 is converted to digital domain by a binary search algorithm. This is implemented by successively adding or subtracting binary-scaled versions of voltage V_{ref} to the integration capacitors until the differential voltage stored in C_3 becomes lower than $V_{ref}/2^{n-2}$, where n is the output resolution of the converter.

Table I
RELEVANT PARAMETERS OF THE SC-BASED PG-ADC OPERATION

Parameter	Amplification operation	Conversion operation
Input capacitance	$C_{in}^A = C_4$	$C_{in}^C = C_1 \cdot C_2/(C_1 + C_2)$
Gain of the amplification stage	$G^A = C_4/C_3$	$G^C = C_2/C_3$
Clock cycles involved in the integration	$m^A = 3/2$	$m^C = 1/2$
Feedback factor[a]	$\beta \equiv 1/b = C_3/(C_3 + C_{in} + C_p)$	
Equivalent output capacitance	$C_{eq} = C_p + C_{in} + kC_L$	
Initial voltage jump gain	$\xi = (1 + C_L/C_3)\, C_{in}/C_{eq}$	
Gain-bandwidth product of the OTA	$GB = g_m/C_{eq}$	
Slew-rate of the OTA	$SR = kI_o/C_{eq}$	
Voltage limit of the OTA linear regime	$V_L = I_o/(\xi g_m)$	

[a]For the sake of simplifying notation, parameters with common definitions for the amplification and conversion operations will not distinguished unless it is strictly needed in the analysis of the PG-ADC. In such a case, a superindex A for the amplification and C for the conversion operation will be used.

Accordingly, the conversion operation takes $n - 1/2$ master clock periods for completion (half period overlaps with the charge transfer of a new sampled input signal as shown in Fig. 2(b)). Hence, the total duration employed for amplification and data conversion is $N = n + 1$ clock periods.

The scaled voltages $V_{ref}/2^j$, $j = 1, ...n-1$, are obtained by charge distribution between the capacitors, C_1 and C_2. During phase Φ_1, capacitors C_2 are discharged while capacitors C_1 retain their voltages. At the following phase Φ_2, capacitors C_1 and C_2 in the same branch are serially connected. Hence, by making capacitors C_1 and C_2 nominally identical, the differential voltage across capacitors C_2 is half the voltage previously held in capacitors C_1.

Voltage addition or subtraction is easily implemented by means of the four cross-coupled switches controlled by the signals Φ_{2p} and Φ_{2n}. These signals, aligned with the clock phase Φ_2, are generated according to the sign of the differential voltage across capacitors C_3 in the previous Φ_1 phase. As shown in Fig. 2, this sign is determined by a comparator, latched in phase Φ_1, which retains its output during a full master clock cycle. If the result of the comparison is positive (negative), a differential voltage $G^C V_{ref}/2^j$, $j = 1, ...n - 1$, is subtracted (added) from (to) the voltage stored in capacitors C_3. Note that the amplification gain G^C has to be one in order to implement the binary search algorithm of the conversion operation. Signals Φ_{2p} and Φ_{2n} are derived from the output of the comparator by using the simple logic circuit shown in the inset of Fig. 2(a). The logic outputs generated by the comparator along the conversion stage, from the most significant bit (MSB), d_{n-1}, to the least significant bit (LSB), d_0, constitute the digital representation of the amplified differential input signal, $G^A V_{in}$. This representation, denoted as $\mathbf{D} = [d_{n-1}, ..., d_0]$, is sequentially stored in a successive approximation register for output generation [not shown in the schematic of Fig. 2(a)].

Circuit imperfections make the proposed PG-ADC to deviate from the ideal performance and induce noise, non-linearity, and settling errors. The following subsections address the analysis of these non-idealities in order to extract design considerations for properly sizing the circuit.

A. *Linearity performance*

The residual differential output voltage of the integrator V_o, appearing in the decision level for the LSB, takes ideally the form,

$$V_o = G^A U_{in}^A + G^C \sum_{j=1}^{n-1} U_{in,j}^C \tag{1}$$

where $U_{in}^A = V_{in}$ and $U_{in,j}^C = (-1)^{d_{n-j}} V_{ref}/2^j$. In the above expression, the first term represents the integrated voltage at the beginning of the conversion operation, and the second term results from the application of the binary search algorithm.

Assuming quasi-static operation and that the comparator in Fig. 2(a) presents a resolution better than half LSB, four major mechanisms make V_o deviate from the ideal behavior in 1, thus leading to non-linearity errors. They are: capacitor mismatch, parasitics at the voltage division node [labeled V_d in Fig. 2(a)], finite gain of the OTA, and charge injection from the switches, including clock feedthrough effects. Other mechanisms for non-linearity, such as the voltage dependence of the capacitances or the on-resistance of the switches, are assumed to be non-dominant. To this end, it is assumed that the switches S_{in} connected to the input nodes are bootstrapped so as to reduce the generation of harmonic components during sampling [29]. The remaining switches, whose non-linear on-resistances are less critical for distortion, are implemented with charge-balanced CMOS transmission gates, seeking to reduce charge injection errors.

Regarding the statistical deviations of the capacitor values, let us assume capacitances C_i, $i = 1, 2, 3$, are affected by mismatch deviations so that they can be expressed as $C_i = C_u(1+\delta_i)$, where C_u represents the nominal capacitance value and δ_i is a random variable with variance $E[\delta_i^2] = \sigma_u^2$. In addition, let us assume that the converter remains monotonic in spite of the perturbations induced by capacitor mismatch. In this case, assuming that $|\delta_i| \ll 1$, it can be shown that the integral non-linearity (*INL*) is bounded by (additional information about this derivation is given in the Appendix),

$$INL_{mis} \approx \sum_{j=1}^{n-1} \left(\frac{\Delta_{div} \cdot j}{2} + \Delta_{int} \right) U_{in,j}^{C} \quad (2)$$

where $\Delta_{int} = \delta_2 - \delta_3$ and $\Delta_{div} = \delta_1 - \delta_2$. The *INL* reaches a maximum for $\mathbf{D} = [1, ...1]$ given by,

$$\begin{aligned} INL_{mis,max}(LSB) &\approx \frac{1}{2} \left[(2^n - n - 1)\, \Delta_{div} + (2^n - 2)\, \Delta_{int} \right] \\ &\approx 2^{n-1} (\Delta_{div} + \Delta_{int}) \end{aligned} \quad (3)$$

with a variance $\sigma_{INL}^2 \approx 2^{2n-1} \cdot \sigma_u^2$, where the approximations hold for large n. Similarly, the differential non-linearity (*DNL*) up to the decision level for the LSB can be found to exhibit a maximum at the MSB transition given by,

$$\begin{aligned} DNL_{mis,max}(LSB) &\approx 2\Delta_{int} + \left(2^{n-1} - n - 1 \right) \Delta_{div} \\ &\approx 2^{n-1} \Delta_{div} \end{aligned} \quad (4)$$

with a variance $\sigma_{DNL}^2 \approx 2^{2n-1} \cdot \sigma_u^2$ for large n.

Regarding the impact of parasitics at the division node V_d, we must distinguish between the parasitic during the resetting phase Φ_1, denoted as C_{pr}, and the parasitic during the voltage division phase Φ_2, denoted as C_{pd}. These parasitics perturb the charge distribution between the set of capacitors C_1 and C_2 in such a way that the scaling factor becomes $(C_1 + C_{pr})/(C_1 + C_2 + C_{pd})$. Assuming minimal length connections in the layout, parasitics C_{pr} and C_{pd} are dominated by the top plate capacitances to ground of capacitors C_1 and C_2 and the junction capacitances of the CMOS switches. It can be observed that C_{pd} essentially doubles the value of C_{pr} and, hence, systematic errors are avoided during voltage division. Any potential deviation δ_p, defined by the expression $C_{pd} = 2C_{pr}(1 + \delta_p)$, has a similar impact on linearity to parameter δ_1. Accordingly, it will be assumed that equations 3 and 4 hold with δ_1 modified as $\delta_1 - \delta_p(C_{pr}/C_u)$.

For the evaluation of the impact on the linearity performance of the finite gain of the OTA, A_0, a similar procedure can be followed. Again, assuming that the PG-ADC remains monotonic, it can be found after some algebra that the *INL* considering this error mechanism alone is given by,

$$\begin{aligned} INL_{\mu} &\approx \frac{G^C}{1 + b^C \mu} \cdot \sum_{j=1}^{n-1} [(1 - G^C \mu)^{n-j-1} - (1 + k^C \mu)] \cdot U_{in,j}^{C} \\ &\approx \frac{1}{1 + b^C \mu} \cdot \sum_{j=1}^{n-1} [-(n - j - 1 + b^C)\mu] \cdot U_{in,j}^{C} \end{aligned} \quad (5)$$

where $\mu = 1/A_0$, and C_p is the parasitic capacitance at the input of the OTA. The rest of variables are defined in Table I. Like in the previous case, the *INL* is maximum for $\mathbf{D} = [1, ...1]$ and the *DNL* is maximum at the MSB transition, from where the following expressions can be derived,

$$INL_{\mu,max}(LSB) \approx \frac{2^{n-1}(n + b^C - 3)\mu}{1 + b^C \mu} \quad (6)$$

$$DNL_{\mu,max}(LSB) \approx \frac{2^n \mu}{(1 + b^C \mu)} \quad (7)$$

Let us finally consider the non-linearity induced by the charge injection of the switches. As demonstrated in [30], the non-linearity generated by the switches in the amplification branches can be made negligible by employing clock phases with delayed falling edges, namely, by making switches S_a turn off slightly before switches S_{in} [see Fig. 2(a)]. Besides, the fully differential operation guarantees that the four cross-coupled switches controlled by the signals Φ_{2p} and Φ_{2n} and the reset phase of C_2 do not contribute to distortion. Assuming that switches S_1 and S_2 are equally sized, the charge injected by S_1 into capacitors C_1 at the end of the amplification operation is approximately counterbalanced by the charge removed from these capacitors when switches S_2 turned on at the beginning of the conversion operation. Hence, switches S_1 do not contribute distortion. For similar reasons, the charge packets that are retrieved from or delivered to the capacitors C_1 when switches S_2 turn on or off, respectively, balance each other because voltage V_d holds for a full clock cycle and, hence, they do not affect the linearity performance of the PG-ADC. On the contrary, the charge $Q_{s2,j}$, $j = 1, ...n-1$, collected at the integration capacitor C_3 when switches S_2 turn off are not canceled out and depend on the voltage at node V_d, thus being a potential source of distortion. Indeed, it can be easily demonstrated that the *INL* induced by that uncompensated charge takes the form

$$INL_{inj} = \sum_{j=1}^{n-1} (-1)^{d_{n-j}} \frac{Q_{s2,j}}{C_u} \quad (8)$$

where, $Q_{s2,j}$, can be approximated as $Q_{s2,j} = C_{inj} \cdot V_{ref}/2^{j+1}$ and C_{inj} is a fitting capacitance that is obtained from simulation. From the above expression and using a similar procedure, the maximum *INL* and *DNL* induced by charge injection effects can be calculated as

$$INL_{inj,max} \approx \frac{2^{n-2} C_{inj}}{C_u} \quad (9)$$

$$DNL_{inj,max} \approx \frac{C_{inj}}{C_u} \quad (10)$$

The above analysis reveals that the linearity of the PG-ADC relies on the capacitance C_u of capacitors C_i, $i = 1, 2, 3$, and on the finite gain of the OTA. Hence, the different expressions of INL_{max} and DNL_{max} obtained above for the conversion process can be used to extract minimum values for both design parameters. Assuming that the resolution of the comparator is better than half LSB, the assumed monotonicity of the PG-ADC can be guaranteed as long as $|INL_{max}| < 1\,\text{LSB}$ and $|DNL_{max}| < 2\,\text{LSB}$ [31], which was checked by analytical simulations. Additionally, fulfilling this condition validates the monotonicity assumption taken at the beginning of the analytical analysis.

According to these constraints and taking into account (3-4) and (9-10), Fig. 3(a) plots the minimum C_u value imposed by mismatch and charge injection effects. In this plot, capacitors C_i are implemented as MiM structures with a capacitance per unit area of $2.5\,\text{fF}/\mu\text{m}^2$ and a variance of $\sigma_u^2 = 2.5{\cdot}10^{-5}/A_{C_u}$, where A_{C_u} is the capacitor surface (both data extracted from a 130nm CMOS process). The mismatch

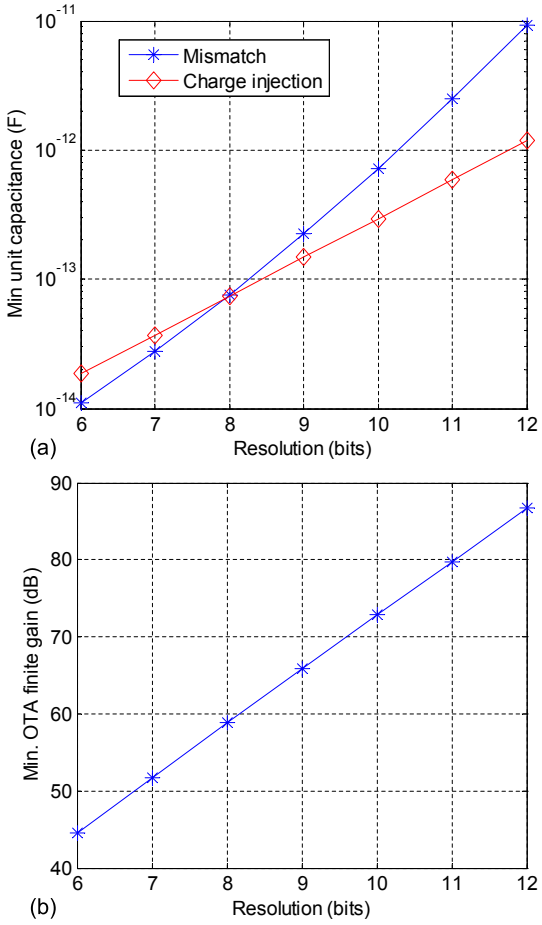

Figure 3. Minimum values of (a) the unit capacitance and (b) the finite gain of the OTA to guarantee the monotonicity of the PG-ADC in terms of the required resolution.

of the parasitics at the division node V_d is as large as 25% of the total parasitic capacitance ($\delta_p = 1/4$). The contribution to C_{pr} due to the junction capacitances takes a worst-case peak value of 0.7 fF and those contributions originated by the top plate capacitances and the routing parasitics are extracted from layout. Finally, C_{inj} amounts 1.15 fF, maximum value obtained from simulations. Fig. 3(a) shows that, for resolutions below 8-bits, charge injection effects dominates over capacitor mismatch. For higher resolutions, the C_u values is bounded by mismatch considerations.

Fig. 3(b) shows the minimum OTA finite gain value that satisfies the linearity conditions for different resolutions. The unit capacitance C_u included in the term b^C of (6) is obtained from the analysis of Fig. 3(a), while the parasitic capacitance C_p is calculated from simulations. As expected, the OTA gain requirement increases with the target resolution.

B. Settling behavior

In (1) it has been assumed that no charge transfer errors occur. In practice, dynamic limitations induce settling deviations in the transfer characteristic of the PG-ADC, which can be modeled by including correction factors in the integrator gain during the amplification and conversion operations, so that $G = G_{ideal} \cdot (1 - \varepsilon_{set})$ [32].

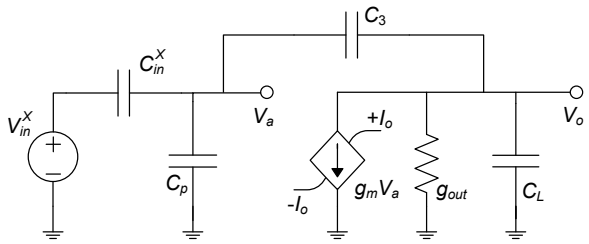

Figure 4. Equivalent circuit model of the PG-ADC during signal integration valid for both the amplification and conversion operations.

In order to estimate ε_{set}, let us assume that the settling behavior of the PG-ADC is dominated by the integration phase (clock phase Φ_{s2} during the amplification cycle or clock phase Φ_2 during the conversion cycle). Accordingly, the simplified equivalent circuit model in Fig. 4, valid both for the amplification and conversion operations, will be considered for analysis. Further, let us assume that the OTA has a single-pole dynamics with a maximum output current I_o, gain-bandwidth product GB and slew-rate during integration SR (see Table I for definitions). In this case, discarding the situation in which the integrator transient response is fully determined by the slew-rate of the amplifier, the value of ε_{set} at the end of the integration phase can be approximated as :

$$\varepsilon_{set} = g(U_{in}) \cdot b \cdot \xi \cdot \exp\left[-m \cdot GB \cdot T_s\right] \tag{11}$$

where m is defined in Table I, ξ is related to the initial voltage jump at the input node of the amplifier at the beginning of the integration phase, $V_{a,ini} = -\xi \cdot U_{in}$; and $g(U_{in})$ is a nonlinear function of the input signal U_{in} given by,

$$g(U_{in}) = \begin{cases} 1 & , |U_{in}| \leq V_L \\ \frac{V_L}{|U_{in}|} \exp\left[-1 + \frac{|U_{in}|}{V_L}\right] & , |U_{in}| > V_L \end{cases} \tag{12}$$

where V_L is defined in Table I. This expression shows that for $|U_{in}| \leq V_L$ (linear regime), the gain of the integrator does not depend on U_{in} and ε_{set} can be interpreted as an extra noise source at the integrator output. Otherwise, when $|U_{in}|$ is larger than V_L (partial-slew regime), there exists a dependency of the gain of the integrator on its input, which leads to non-linear gain and, hence, distortion.

In order not to degrade the converter accuracy, the settling error ε_{set} must be kept lower than 2^{-n} at every clock period. This constraint can be used to estimate the speed requirements of the amplifier in terms of the model capacitances and, eventually, the peak input voltage amplitude$|U_{in,pk}|$ that can be handled by the PG-ADC. During the amplification cycle, the peak amplitude should not exceed the full scale range of the converter, $[-V_{ref}, V_{ref}]$ and, hence, $|U^A_{in,pk}| = V_{ref}/G^A$. During the conversion cycle, U^C_{in} takes on binary-scaled voltages $V_{ref}/2^j$, $j = 1, ...n-1$.

Fig. 5 plots the minimum gain-bandwidth product of the OTA versus resolution, assuming that the PG-ADC operates in the amplification phase with a gain $G^A = 1$ and a maximum input voltage $|U^A_{in,pk}| = V_{ref}$. For each target resolution, the value unit capacitance C_u has been obtained from the analysis of Fig. 3(a). A master clock frequency of 800 kHz is

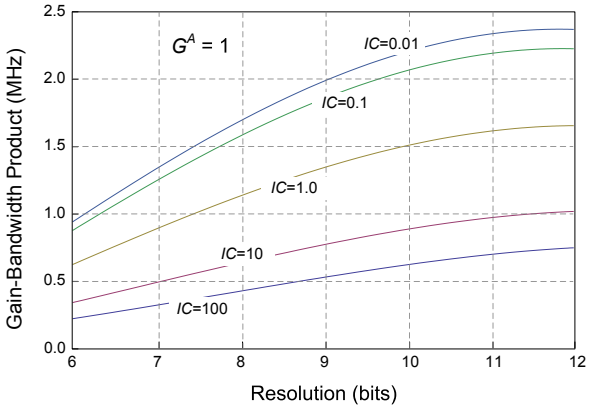

Figure 5. Minimum OTA GB in terms of the required resolution.

assumed. The gain-bandwidth product (GB) has been plotted for different values of the inversion coefficient IC, which is defined by the expression [33]

$$\frac{g_m}{I_o} = \frac{1}{n \cdot V_{th}} \cdot \frac{2}{1+\sqrt{1+4 \cdot IC}} \tag{13}$$

where n is the slope factor of the MOS transistor and V_{th} is the thermal voltage. As expected, the required GB increases with the resolution and it is higher for amplifiers operating in weak inversion ($IC < 0.1$). This is because as IC decreases the voltage limit V_L for linear regime turns smaller, the nonlinear term $g(U_{in})$ increases and GB must be made larger to keep ε_{set} low enough for the target resolution.

C. Noise analysis

Assuming the different noises sources during the amplification and conversion operations are not correlated, the equivalent input-referred power noise of the PG-ADC can be calculated by means of the following expression:

$$P_{in,eq} = P^A_{in,eq} + \left(\frac{C^C_{in}}{C^A_{in}}\right)^2 P^C_{in,eq} \tag{14}$$

where both C^C_{in} and C^A_{in} are defined in Table I and correspond to the input capacitance C^X_{in} shown in Fig. 4. $P^A_{in,eq}$ is the input-referred power noise during the amplification operation and $P^C_{in,eq}$ is the total noise power referred to the input of the conversion branch. The main contributions to $P^A_{in,eq}$ are the thermal noise generated by the switches, given by $P^A_{in,R_{on}} \approx 4kT/C_4$, where k is the Boltzmann constant (the factor 4 is due to the two sampling switches and the fully differential operation); and the noise from the OTA, whose input-referred power is approximately given by $P^A_{in,ota} \approx S^{th}_{ota} \cdot GB^A/2$, where $S^{th}_{ota} = 8kT(1+\eta_{t,ota})/(3g_m)$ is the spectral noise density of the OTA [1] [34]. Hence, the value of $P^A_{in,eq}$ can be approximated as:

$$P^A_{in,eq} \approx 4kT\left(\frac{1}{C_4} + \frac{1+\eta_{t,ota}}{3C^A_{eq}}\right) \tag{15}$$

[1]The $1/f$ noise can be neglected as the minimum GB^X is at least two order of magnitude higher than the $1/f$ corner frequency $f_{cr,1/f}$

where $\eta_{t,ota}$ denotes the noise excess factor of the OTA. Similarly, the noise power integrated at the reference capacitors C_1 at the beginning of the conversion operation can be calculated as:

$$P_{C_1} \approx \frac{2kT}{C_1} \cdot \left(1 + \frac{2(1+\eta_{t,ref})}{3}\right) \tag{16}$$

where it has been considered that the reference voltage V_{ref} is affected by the output noise power $P_{ref} = 8kT(1+\eta_{t,ref})/(3C_1)$ of a driving buffer with a bandwidth similar to that of the OTA in Fig. 2. Parameter $\eta_{t,ref}$ represents the noise excess factor of the corresponding amplifier.

In order to calculate the total input-referred noise of the conversion operation $P^C_{in,eq}$, it must be taken into account that the different noise contributions scale along the successive conversion steps. Further, taking into account that the contributions due to P_{C_1} are correlated, it can be found that,

$$\begin{aligned} P^C_{in,eq} &= \left[\sum_{i=1}^{n-1}\left(\frac{1}{2^{2(i-1)}}\right)\right](P^C_{in,R_{on}} + P^C_{in,ota}) + \left[\sum_{i=1}^{n-1}\left(\frac{1}{2^i}\right)\right]^2 P_{C_1} \\ &\approx \frac{4}{3}(P^C_{in,R_{on}} + P^C_{in,ota}) + P_{C_1} \end{aligned} \tag{17}$$

where $P^C_{in,ota} \approx S^{th}_{ota} \cdot GB^C/2$ is the input-referred noise power of the OTA and $P^C_{in,R_{on}} \approx 2 \cdot (9/4) \cdot kT/C_2$ is the thermal noise generated by the switches during the conversion operation. Replacing (15-17) into (14), the equivalent input-referred power noise of the PG-ADC can be approximated as:

$$\begin{aligned} P_{in,eq} = 4\frac{kT}{C_4}\left(1 + \frac{7+\eta_{t,ref}}{12 \cdot G^A}\right) + \\ + \frac{4}{3}kT\,(1+\eta_{t,ota})\left[\frac{1}{C^A_{eq}} + \left(\frac{1}{G^A}\right)^2 \frac{1}{3 \cdot C^C_{eq}}\right] \end{aligned} \tag{18}$$

which is dominated by the noise power generated during the amplification operation, particularly for low gain values. This is illustrated in Fig. 6 which shows the minimum C_u value required to keep the input-referred noise of the PG-ADC below the quantization noise of the converter in terms of the desired resolution for a reference voltage $V_{ref} = 0.6$V. As can be seen, regardless of the target resolution, the largest C_u capacitance is imposed by the amplification gain $G^A = 1$. It is also worth mentioning that for the parameters used in relation to Fig. 3(a) and Fig. 6, mismatch effects impose stronger demands than noise on the sizing of the unitary capacitance.

III. Adaptively Biased Active Blocks

The settling analysis of Sec. II-B reveals that the current demand of the OTA varies depending on the amplification gain and the peak input voltage amplitude $|U_{in,pk}|$. This is illustrated in Fig. 7 which shows the minimum I_o required for an 8-bit resolution PG-ADC in terms of the unitary capacitance, assuming a sampling frequency of 800 kHz, as required for the 90kS/s case, and different gain settings, $G^A = 1, 2, \ldots, 8$. The curves have been obtained for maximum input voltages $|U^A_{in,pk}|$ and an inversion coefficient $IC = 0.01$, thus, assuming that the input devices of the OTA operate in weak inversion. As expected, the current demand increases with G^A

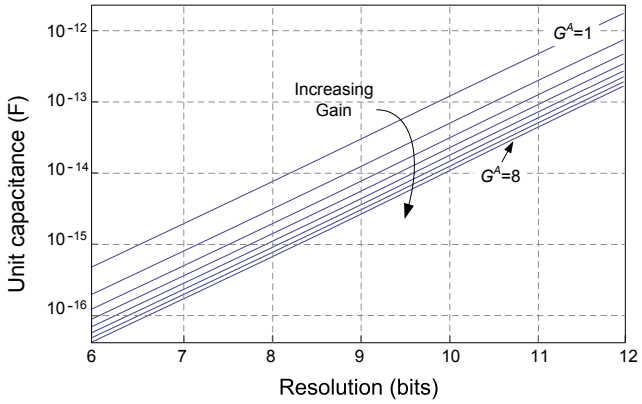

Figure 6. Minimum value the unit capacitance imposed by noise considerations in terms of the desired PG-ADC resolution.

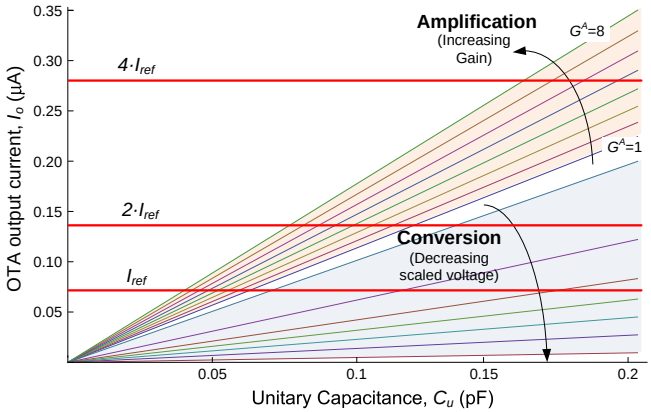

Figure 7. Minimum OTA output current versus unitary capacitance for an 8-bit resolution PG-ADC.

because of the higher equivalent load capacitance. Fig. 7 also shows the minimum I_o requirements during the conversion operation. It is observed that the current demand decreases as the conversion progresses. This is because the peak input voltage value $|U^C_{in,pk}|$ decreases along the conversion, the term $g(U_{in})$ gets lower and the current I_o can be made smaller for the same settling error ε_{set}. It is also worth noting that as long as $G^A \geq 1$, as requested in the intended application, $V^A_L < V^C_L$ and $b^A \cdot \xi^A \geq b^C \cdot \xi^C$ (see Table I) and, hence, the current demand is always higher during the amplification operation than during conversion. This justifies the chosen clock phasing of Fig. 2(b), where the amplification phase consumes three clock semi-periods.

Fig. 7 sets the basis for an adaptive biasing strategy in which the power consumption of the OTA is adjusted depending on the gain setting and the conversion step. However, doing so for every curve in Fig. 7 would complicate the biasing circuitry of the OTA. It follows that there exists a trade-off between circuit complexity and power consumption. In practice, a few current settings suffice to achieve a substantial power reduction.

In our design, which uses a nominal unit capacitance of 100 fF, only three settings are used as shown with horizontal lines in Fig. 7. For the amplification operation, a biasing current $4 \cdot I_{ref}$ is used regardless of the gain setting. This value provides a safety margin to compensate the PVT variations and

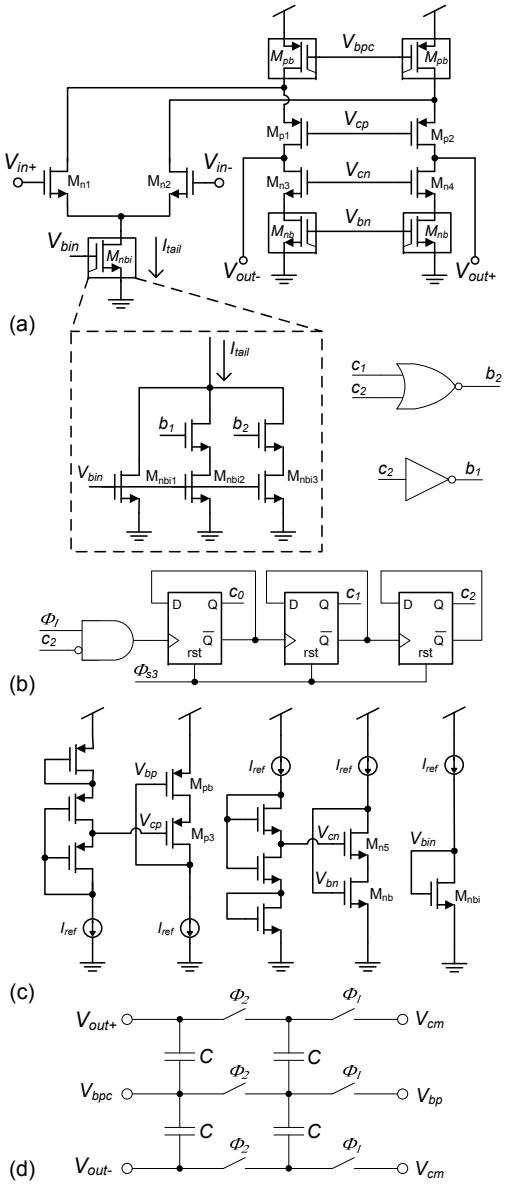

Figure 8. Folded cascode operational amplifier with adaptive biasing: (a) schematic, (b) adaptive biasing, (c) reference voltages generation, (d) CMFB circuit

other non-idealities, such as the matching errors of the bias transistors that could deviate the real settling behavior from the analytical study. A current $2 \cdot I_{ref}$ is used for the two firsts steps of the conversion process, whereas I_{ref} is used for the remaining steps. Taking into account the durations of the different stages, an overall reduction of about 55% is obtained as compared to using a single bias setting.

The I_{ref} value has to be selected based on the target conversion speed of the PG-ADC with enough margin so as to comply with PVT variations. Two output rates of 27 and 90 kS/s are herein considered and, accordingly, I_{ref} amounts to 22 and 70 nA, respectively.

Fig. 8(a) shows the schematic of the adaptively biased OTA used in the proposed implementation of the PG-ADC. It is a standard folded-cascode structure with input transistors

Table II
DIMENSIONS OF THE OTA TRANSISTORS

M_{n1}, M_{n2}		40/1μm	
M_{nbi}, M_{nb}, M_{nb1}, M_{nb2}	1/10μm	M_{pb}	1/5μm
M_{nbi1}, M_{nbi2}, M_{nb3}	2/10μm	M_{pb1}, M_{pb2}	2/5μm
M_{nbi3}	4/10μm	M_{pb3}	4/5μm
M_{n3}, M_{n4}, M_{n5}	1/1μm	M_{p1}, M_{p2}, M_{p3}	2/1μm

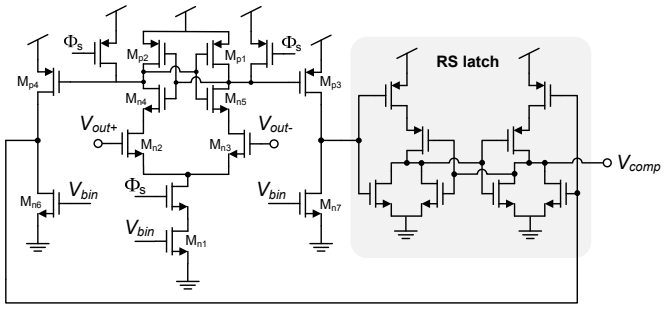

Figure 9. Current controlled dynamic latch comparator

operating in weak inversion. This topology allows to obtain the 60 dB DC-gain needed for the intented 8-bit ENOB (see Fig. 3(b)) and, at the same time, provides a high output voltage swing. The implemented adaptive biasing scheme uses digitally-controlled current sources, represented by transistors inside square boxes in Fig. 8(a). The schematic of one of these current sources, together with the digital block for controlling the supplied current, are shown in Fig. 8(b). Reference voltages for the biasing and cascode transistors are generated by means of the circuit shown in Fig. 8(c). Fig. 8(d) shows the SC-based Common-Mode Feedback (CMFB) circuit used to adjust the bias voltage of the output pMOS transistors M_{pb}. The dimensions of the transistors are summarized in Table II.

The schematic of the comparator is shown in Fig. 9. It is a current-controlled dynamic latch scheme which feeds an RS latch to store the result of the comparison. The gate voltage V_{bin} of transistors M_{n1}, M_{n6} and M_{n7} is provided by the circuit of Fig. 8(b) and, hence, the current consumption of the comparator also depends on the selected sampling frequency. At 90 kS/s, the circuit consumes about 220 nW. Montecarlo analysis under PVT (process, voltage and temperature) variations show that the offset of the comparator is below 1 mV, four times lower than the LSB.

IV. EXPERIMENTAL RESULTS

The complete PG-ADC, embedded in a $400\mu\text{m} \times 400\mu\text{m}$ neural recording channel, has been fabricated in a 130 nm standard CMOS technology (6M2P). Fig. 10 shows a microphotograph of the neural channel, together with the layout of the PG-ADC which occupies $0.0326\,\text{mm}^2$,i.e., about a 20% of the recording channel. The nominal voltage supply of the circuit is 1.2 V.

The PG-ADC offers a programmable amplification range of 0-18dB by digitally scaling the input capacitance C_4 from C_u to $8 \cdot C_u$, where C_u is the nominal capacitance value of capacitors C_i, $i = 1, 2, 3$. Fig. 11 shows the transient response

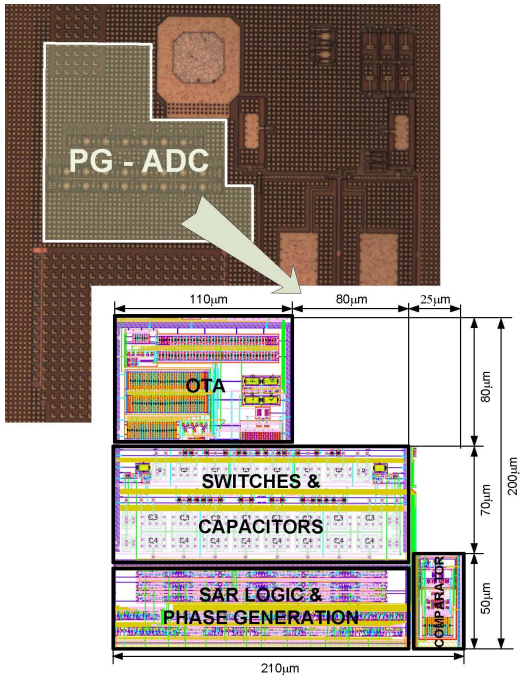

Figure 10. Layout of the SC-based ADC embedded in the microphotography of the neural channel

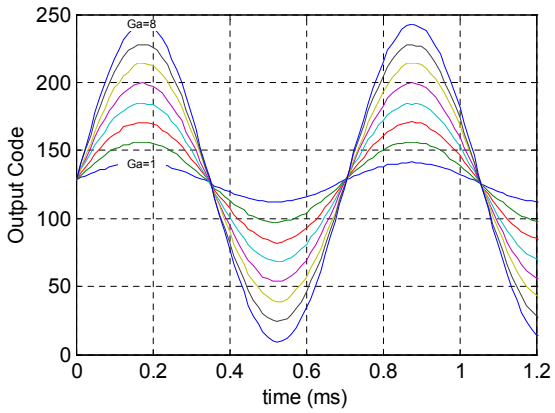

Figure 11. Temporal response of the PGA-ADC for different gain configurations

of the circuit for a $150\,\text{mV}_{\text{pp}}$, 1.4 kHz tone applied to the input of the PG-ADC under all possible gain configurations. As Fig. 12 demonstrates, the ENOB keeps constant under the different gain modes.

Fig. 13 shows the spectrum of the PG-ADC for the two targeted output rates of 27 and 90 kS/s. In both cases, input tones at low frequency (labelled with crosses) and close to the Nyquist frequency (labelled with dots) were applied. It is observed that the Signal-to-Noise and Distortion Ratio (SNDR) is above 47.0 dB and, accordingly, the Equivalent Number of Bits (ENOB) of the PG-ADC is above 7.5 bit for both sampling rates within their respective Nyquist bands. More specifically, within the bandwidth of neural activity from 0.01 Hz to about 5 kHz, it is observed that the ENOB is higher than 7.56 bit for a sampling rate of 90 kS/s and higher than 7.60 bit for a sampling rate of 27 kS/s. These results essentially

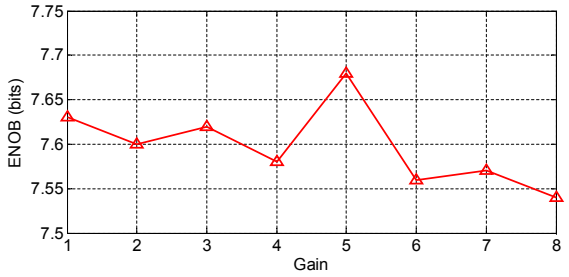

Figure 12. ENOB of the PGA-ADC for different gain configurations

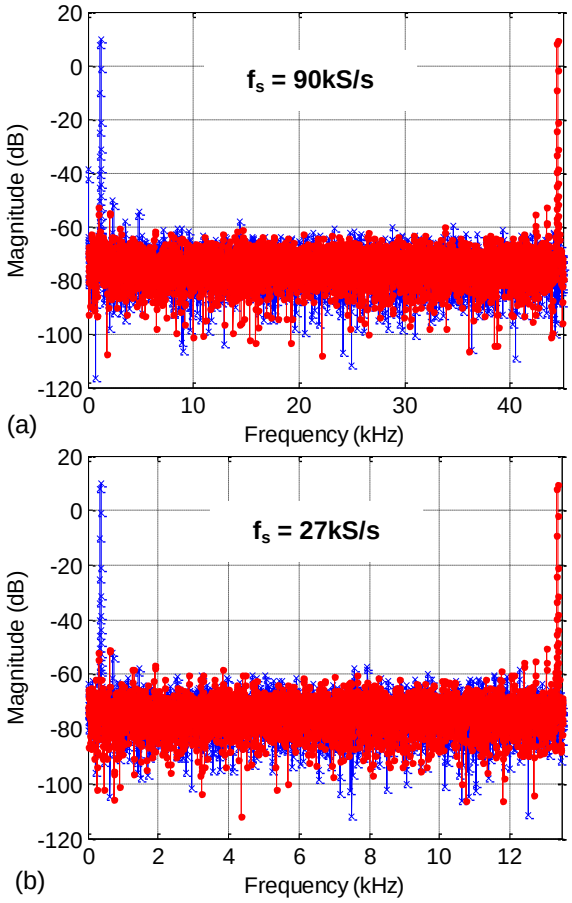

Figure 13. FFT response of the PG-ADC output under two sampling frequency modes: (a) 90kS/s, (b) 27kS/s

hold for the other available amplification gain settings for which even a slight improvement on SNDR is observed. Fig. 13 also shows that the Spuriuos-Free Dynamic Range (SFDR) of the PG-ADC is above 62.5 dB for all the sampling rate configurations.

Linearity was checked with static measurements depicted in Fig. 14, which confirm the predictions from the analysis performed in Section II-A. As expected, the DNL plot exhibits larger peaks in the transition of the MSB (code 128) and the second MSB (codes 64 and 192). The INL is bounded between ± 0.5 LSB, while the DNL varies from a minimum of -0.25 LSB to a maximum of 0.48 LSB.

Fig. 15 shows the ENOB versus input frequency for different supply voltages ranging from 1 V to 1.4 V. Measurements were done for different tones up to the Nyquist frequency using an output rate of 90 kS/s. Similar results were also obtained at 27 kS/s. Observe that the resolution keeps essentially unaltered regardless of the input frequency and the voltage supply deviation.

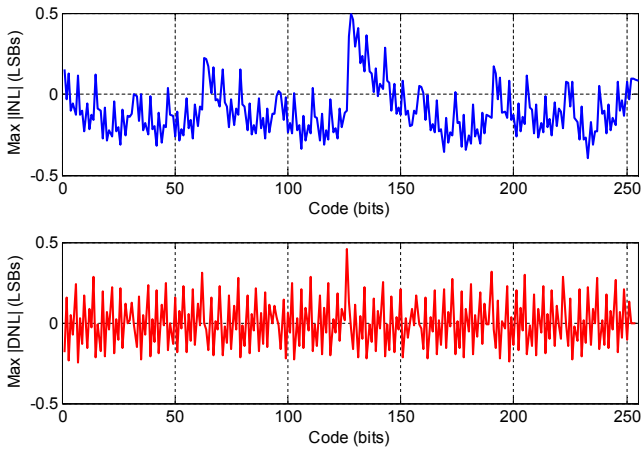

Figure 14. INL and DNL measurements of the PG-ADC

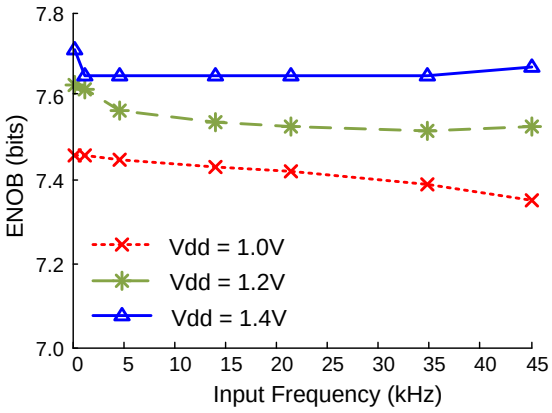

Figure 15. ENOB of the PG-ADC versus input frequency for different voltage supplies.

The functionality of the PG-ADC has been verified with pre-recorded neural activity from the primary motor cortex of a macaque monkey. Recordings were performed using the Cerebus adquisition system by Blackrock Microsystems [35]. Waveforms were loaded onto an arbitrary waveform generator to reproduce the original signal as shown in Fig. 16(a). The synthesized signal was then directly applied to the integrated LNA, which form, together with the presented PG-ADC, the front-end of the recording channel shown in Fig. 10. The full front-end offers a nominal gain of 47-65 dB and an input referred noise of $3\mu V_{rms}$. The driving voltage of the PG-ADC can be externally monitorized by means of a differential low input capacitance buffer included on-chip for testing purposes. Fig. 16(b) shows an oscilloscope capture of this driving voltage when a spike is taking place. It is worth observing the capacitive load imposed by the PG-ADC (set to the maximum gain $G^A = 8$ in this experiment) and

Table III
PG-ADC PERFORMANCE

Process	Standard CMOS 130nm	
Area	0.0326 mm^2	
Voltage Supply	1.2-V	
Input Gain	1-8 (steps of 1)	
Input Range	1.2-V differential	
INL	-0.4 - 0.5 LSB	
DNL	-0.25 - 0.48 LSB	
Sampling frequency	90 kS/s	27 kS/s
SNDR	47.27 dB	47.51 dB
SFDR	62.50 dB	62.53 dB
ENOB	7.56-bits	7.60-bits
Power Consumption	1.52 μW	515 nW
- Comparator	220 nW	85 nW
- OTA + CMFB	605 nW	205 nW
- Biasing	350 nW	110 nW
- Digital	345 nW	115 nW
FoM	89.49 fJ/conv	98.31 fJ/conv

the buffers (nominally 100 fF differential) have a negligible impact on the response of the LNA which closely follows, after amplification, the synthesized signal. This can be explained, on the one hand, by the low input capacitance of the PG-ADC (800 fF maximum) and the long sampling period employed in the proposed PG-ADC which lasts the complete conversion operation [see Fig. 2(b)]. The bottom traces of Fig. 16(c) show the codes (marked with crosses) generated by the PG-ADC at the two output rates of 27 and 90 kS/s, within a time window of 1.25 ms corresponding to the spike captured in Fig. 16(b).

Table III summarizes the PG-ADC performance for the two targeted throughput rates. The average power consumption of the circuit is $1.52\mu W$ and $515nW$ for the 90kS/s and 27kS/s modes, respectively. The employed Figure of Merit (FoM) is the commonly used for medium-resolution ADCs [36],

$$FoM = \frac{Power}{2^{ENOB} \cdot f_S} \tag{19}$$

however, it should be emphasized that our proposal includes PGA functionality, which is not embedded in all ADCs.

Table IV compares this work with other neural sensor interfaces in the literature. Most of these works are multichannel systems, which share the ADC among different channels. In these cases, both sampling frequency and power consumption have been downscaled by the number of the ADC inputs. It is remarkable that the reported work, which embeds both PGA and ADC functionalities, exhibits the best FoM and lowest area occupation. Moreover, the power consumed by the proposed system is independent from the selected gain mode, while in other works, like [10], the difference between the different modes is huge.

V. CONCLUSIONS

A low-power ADC with embedded PGA functionalities, suitable for in-channel neural recording interfaces, has been fabricated in a $0.13\,\mu$m standard CMOS technology. It is based on a binary search algorithm and combines SC techniques and adpative biasing strategies for power saving. The system can be configured at two sampling frequency modes, 27kS/s and 90kS/s. The power dissipation of the PG-ADC from a 1.2 V voltage suply is 515nW and 1.52μW, respectively. The ENOB is above 7.56-bits within the bandwidth of neural activity, from 0.01 Hz to about 5 kHz, regardless of the gain setting and the sampling rate. Due to the low area occupation and low power dissipation performance, this solution is very suitable for area restricted systems, such as multiarray neural recording systems with shrink pitch sizes. Further, the PG-ADC structure can be easily reconfigured for different digital output lengths and/or sampling rates upon an adequate timing control.

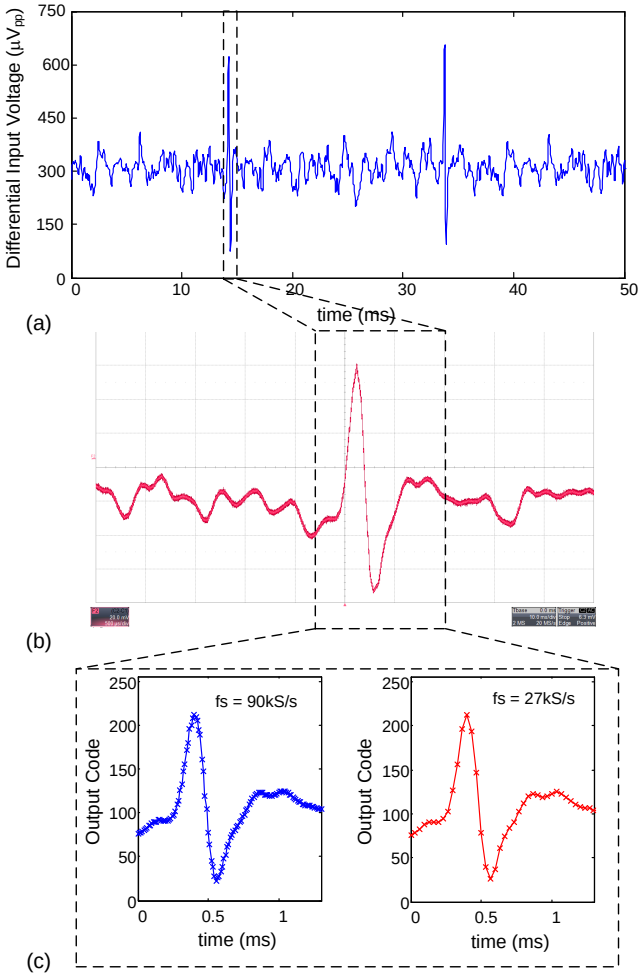

Figure 16. (a) Neural signal at the input of the LNA, (b) Oscilloscope's capture of the LNA output, (c) Output of the PG-ADC at different sampling frequencies

APPENDIX

This appendix section clarifies the derivation of the expressions for the INL errors showed in the text. Let us focus on the INL expression of (2). Neglecting the error induced by the mismatch during the sampling period, which can be considered as a gain error, we can write the output voltage at the end of the conversion from (1) as follows,

Table IV
STATE-OF-THE-ART COMPARISON

	[1]	[2]	[3]	[5]	[10]	[18]	**This work**	
Supply Voltage (V)	0.9	0.5	1 .8	2	1	1	1.2	
CMOS Process (μm)	0.25	0.13	0.18	0.5	0.25	0.35	0.13	
Area (mm^2)	0.1426**	0.086**	0.02**	0.5**	0.065	0.5	0.0326	
Sampling rate per channel (kS/s)	20.2*	30*	31.3*	2*	31.25	1	90	27
ENOB (bits) @ Nyquist Input	7	7.32	7.65	10.6	7.2	10.2	7.56	7.60
Power Consumption (μW)	1.148	0.63	3.08	2.71	0.14 - 2.87	0.38	1.52	0.515
- ADC (per channel)	0.66*	0.2*	0.483*	2.2*	0.087	0.23		
- PGA (per channel)	0.488	0.43	2.6	0.512	0.05 - 2	0.15		
FoM (fJ/conv)	444.68	131.43	491.18	873.66	30.5 - 624.6	323.06	85.85	94.96

*: The ADC is shared by many channels. Both the power consumption and the sampling rate are divided by the number of channels.
**: The reported area doesn't include the PGA.

$$V_o = \sum_{j=1}^{n-1} \left(\frac{C_1}{C_1 + C_2} \right)^j \cdot \frac{C_2}{C_3} \cdot (-1)^{d_{n-j}} \cdot V_{ref} \qquad (20)$$

Considering the effect of mismatch deviations in the unit capacitances defined in the text, we can re-write this expression as

$$V_o^{mis} = V_{ref} \cdot \left(\frac{1+\delta_2}{1+\delta_3} \right) \cdot \sum_{j=1}^{n-1} \left(\frac{1+\delta_1}{2+\delta_1+\delta_2} \right)^j (-1)^{d_{n-j}} \qquad (21)$$

In this case, assuming that $|\delta_i| \ll 1$, we can approximate the former expression by the following:

$$V_o^{mis} \approx \sum_{j=1}^{n-1} U_{in,j}^C \cdot \left(1 + \frac{\Delta_{div} \cdot j}{2} + \Delta_{int} \right) \qquad (22)$$

where Δ_{div} and Δ_{int} take the values defined in the text. The integral non-linearity (*INL*) of the conversion up to the decision level for the LSB can be calculated the by subtracting (22) to (20), which leads to the expression (2).

The same procedure can be employed to derive the expressions (5) and (8), but taking into account the effect of the finite gain and the charge injection, respectively, in the output voltage at the end of the conversion as is done in [34].

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