Effects of capacitors non-idealities in un-even split-capacitor array SAR ADCs

Rafaella Fiorelli, Óscar Guerra, Rocío Del Río and Ángel Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla)
Av. Américo Vespucio s/n, 41092, Seville, Spain.
e-mail: {fiorelli, guerra,rocio,angel}@imse-cnm.csic.es

***Abstract*—This paper studies the effects of capacitors non-idealities in the performance of un-even split-capacitor SAR ADCs. Also, election of the m and l bits of MSB and LSB capacitors banks, respectively, is studied to reduce SAR errors.To exemplify and quantify the non-idealities, MOM capacitors are used. In particular, MOM layout parasitics and effective capacitor's value is obtained with an electrical extraction tool using a flattened view of the MOM. Effects of capacitors layout placement in the SAR and their surroundings in the effective capacitance value are quantified. A quantitative study of a 10-bit un-even split-capacitor SAR is done for different combinations of m and l bits. Finally, a qualitative set of guidelines to choose the distribution of these bits is listed.**

***Index Terms*—Split-capacitor SAR, ADC, SAR, MOM capacitors, layout effects, non-idealities, mismatch, parasitics.**

I. Introduction

Nowadays, an increasing interest in using SARs analog-to-digital converters (ADCs) is gathering strength due to their low power consumption compared to others ADCs architectures [1]–[3]. In particular, the split-capacitor SAR is widely used as it considerably reduces silicon area when compared with conventional binary-weighted SARs. An N-bits split-capacitor DAC of these SARs is presented in Fig.1. It is composed by two banks of m and l capacitors, corresponding to the MSB and LSB SAR bits, and where $N = m + l$. Despite m and l are generally considered as equal [2], in this study m and l can pick arbitrary values. Those SARs are here called un-even split-capacitor SARs.

In this paper, the effects of variations in the ideal values of capacitors' DAC and their parasitics in the performance of a split-array SAR without calibration, are evaluated for different m and l combinations of values, expanding the study done in [4]. The DAC parasitics capacitances are grouped in $C_{eq,MSB}$ and $C_{eq,LSB}$, as seen in Fig.1. Parasitic capacitance between V_{DAC} and V_1 is considered to be included in C_s. If a calibration scheme is implemented, as the one of [4], these parasitics have to be considered separately, and well as to asses the calibration when m and l are unequal.

A un-even split SAR of $N = 10$ bits is considered in this study. To quantify the SAR errors, the DAC is implemented with metal-oxide-metal (MOM) capacitors, as only MoMs were available in the digital CMOS 65-nm 7-metal process (MiMs were unavailable). Despite the impact of parasitic capacitances and random mismatch in even split-capacitor arrays designed with MIMs capacitors has already been studied in [2], [4]–[6], among others, the MOMs capacitors mismatches and parasitics due to layout surroundings have not been reported as well as the effects in un-even SARs, up to the authors' knowledge.

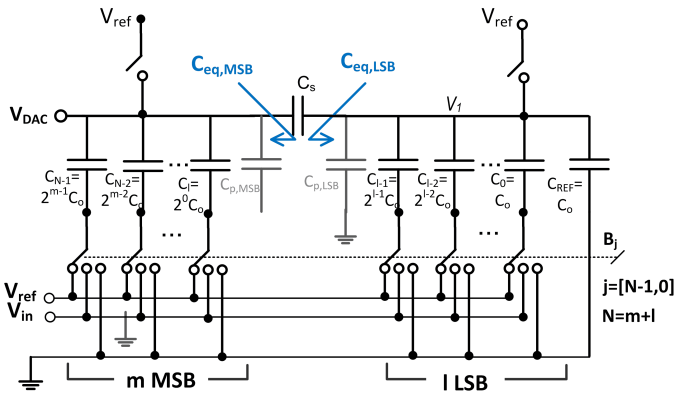

Figure 1. Scheme of an un-even split-capacitor DAC with the inclusion of parasitic capacitances.

In the proposed example, it will be seen that errors due to parasitics capactances in the DAC are worse than errors due to deviations in the DAC's capacitors ideal values.

This paper is organized as follows. Section II presents the MOMs model obtained from layout extraction for different surrounding. In Section III, the effects of MOMs layout placement in split-capacitor array DACs are discussed and a case study is presented in Sect. IV; finalizing with the conclusions.

II. MOM capacitor model extracted from layout

MOM capacitors are formed by interdigitized fingers of several vias-interconnected metals of the CMOS process back-end. Its physical principle is the lateral coupling between these fingers (MOMs are included in the lateral-flux capacitors categorization [7]). The increment in the capacitance density (capacitance per silicon unit area) is done by increasing the number of metal layers. Lateral flux capacitors are more affected by the surrounding metal structures than vertical flux ones (e.g. metal-insulator-metal MIM capacitors) because the metal densities change, modifying these surroundings the lateral electric field.

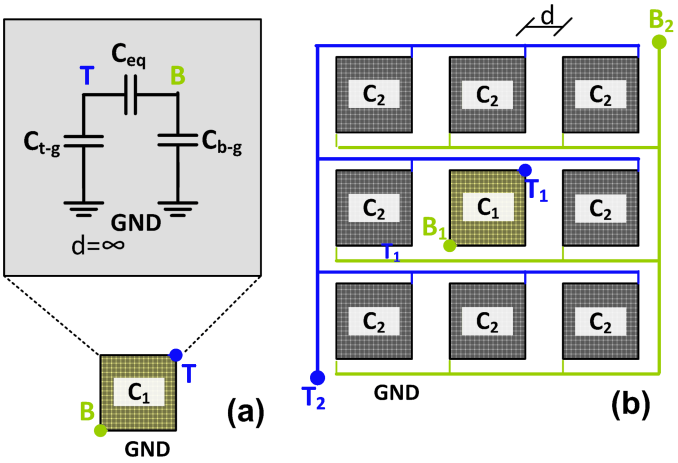

Figure 2. (a) Extracted model of MOM capacitor. Layout of MOM capacitor C_1 (a) without any surroundings, and (b) with eight capacitors C_2, physically identical to C_1.

When, in particular, MOMs are part of a split-capacitor DAC, their surroundings slightly differ depending on their position in the layout, e.g. capacitors' values near the DAC's borders differ from the ones positioned far from them. Hence, despite these deviations are small respect to the ideal value of an isolated capacitor, they lead to error in the SAR conversion. Moreover, coupling between silicon substrate and MOMs terminals increase parasitics, where these parasitics are also affected to variations in MOMs surroundings.

The MOM cell has three terminals: top T and bottom B terminals, formed by Metal1-to-Metal5 inter-digitized fingers, and a poly plate terminal used for shielding the electrical field. In this study, bottom and poly plate terminals are short-circuited (this is not critical as the MOMs bottom terminal is connected to the SAR switches and these parasitics do not modify the SAR behavior). To extract the layout model of the MOM, the following is done: 1) the layout of the chosen MOM capacitor cell, provided by the technology, is flattened; and 2) the extracted model of this layout is found. This extracted model, depicted in Fig. 2(a), considers: (i) the capacitance C_{eq} between T and B terminals, and (ii) the parasitic capacitances C_{t-g} and C_{b-g} between T/B and the substrate GND, respectively. In this paper, the corresponding metal and contact resistances of the MOM are disregarded, without loss of validity in the presented study. The tool used to extract the model of the flattened MoMs is the parasitic extraction tool of Synopsys [1].

To see the behavior of the extracted MOM capacitor model under different surroundings, the following example is presented. Firstly, the layout of an isolated MOM capacitor cell, C_1, as in Fig. 2(a) -with a theoretical value supplied by the foundry of 502.1 fF- is flattened and its model is extracted as explained above. The capacitor sizing, $15\mu m \times 16.5\mu m$, has been considered sufficiently large to reduce effects of random

[1]Flatten MOMs is only used for this study; in a real design, calibration and/or a better modeling tools as Momentum should be used

Table I
EXTRACTION RESULTS OF FLATTENED CAPACITANCES.

	C_{eq} (fF)	C_{t-g} (fF)
$d = \infty \rightarrow$ Isolated C_1		
C_1	525.241	1.059
$d = 5\mu m$		
C_1	514.163	1.375
C_2'	524.934	2.173
$d = 2.5\mu m$		
C_1	510.438	1.563
C_2'	524.579	1.819

mismatch respect to errors due to layout placement. Next, the same MOM capacitor is surrounded by eight identical MOM capacitors C_2, physically identical to C_1, and spaced a distance d, as depicted in Fig. 2(b). All C_2 are interconnected, being the equivalent capacitance C_2', which is ideally equal to C_1. Three possible configurations are studied, $d = \{2.5, 5, \infty\}$ μm; the values of C_{eq} and C_{t-g} are listed in Table I. Capacitance C_{b-g} is not presented as it does not affect the SAR performance.

A change in C_{eq} and C_{t-g} is appreciated when the surroundings of C_1 and C_2 are modified. A reduction in C_{eq} is visible as the distance d is smaller. For C_1, its parasitic C_{t-g} rises respect to that of the isolated capacitor. To compute the C_{eq} and C_{t-g} of C_2', the mean value of the eight C_2 is computed. When C_2 capacitors move closer to each other, the corresponding C_{eq} decreases, but less than the one of C_1. Also, the values of C_{t-g} of C_1 and C_2 become similar when d is smaller. These observations helps to conclude that location and surroundings of MOMs in an array of capacitors affect their effective values. Next sections quantify this fact, studying how these differences affect the behavior of the split-capacitor array SAR.

III. EFFECTS OF MOMS LAYOUT SURROUNDINGS IN SPLIT-ARRAY SAR

The variations of MOM equivalent capacitance and its parasitics values seen in previous section affect the un-even split-capacitor SAR behavior. To quantify these effects, the expression of the DAC voltage -that goes to the comparator- V_{DAC}, of Fig. 1 as function of the DAC capacitances is presented below. For an N split-capacitor DAC, with an arbitrary distribution of m MSBs and l LSBs of Fig. 1, capacitors C_j with $j \in [0, N-1]$ are, ideally,

$$C_j = \begin{cases} 2^j C_o, & \text{for } 0 \leq j < l-1 \text{ (LSBs).} \\ 2^{j-l} C_o, & \text{for } l \leq j \leq N-1 \text{ (MSBs).} \end{cases} \quad (1)$$

with C_o the ideal unitary capacitor. Also, the ideal reference capacitor connected to GND and split capacitor are, respectively, $C_{REF} = C_o$ and $C_s = C_o 2^l/(2^l - 1)$ [5]. However, when real models are utilized, C_j differs from (1) and the ideal rate between them is lost. Additionally, the total parasitic capacitances of MSB and LSB blocks, $C_{p,MSB}$ and $C_{p,LSB}$,

are

$$C_{p,MSB} = \sum_{l}^{N-1} C_{t-g,j} + C_{t-g,s} \quad (2)$$

$$C_{p,LSB} = \sum_{0}^{l-1} C_{t-g,j} + C_{t-g,REF} + C_{t-g,s} \quad (3)$$

where the split capacitor C_s is formed by a pair of capacitors that share their bottom plates to provide similar parasitics, $C_{t-g,s}$, to the MSB and LSB capacitors blocks. As shown in Table I, $C_{t-g,j}$ values are not proportional to C_j, so the effects of $C_{p,MSB}$ and $C_{p,LSB}$ would be dissimilar for different distribution of m and l bits.

For the architecture of Fig. 1 and being $C_{eqMSB} = \sum_{j=l}^{N-1} C_j + C_{p,MSB}$ and $C_{eqLSB} = \sum_{j=0}^{l-1} C_j + C_{REF} + C_{p,LSB}$, the general expression of V_{DAC} at the end of the conversion is

$$V_{DAC} = V_{DAC}^{MSB} + V_{DAC}^{LSB} \quad (4)$$

where

$$V_{DAC}^{MSB} = V_{ref} \frac{\sum_{j=l}^{N-1} C_j B_j}{C_{eqMSB} + C_{s,eqLSB}}$$

$$V_{DAC}^{LSB} = V_{ref} \frac{C_s}{C_s + C_{eqMSB}} \frac{\sum_{j=0}^{l-1} C_j B_j}{C_{eqLSB} + C_{s,eqMSB}} \quad (5)$$

with V_{ref} the DAC reference voltage, $B_j \in [0,1]$ is the j-th bit of the DAC and,

$$C_{s,eqLSB} = C_s C_{eqLSB} / (C_s + C_{eqLSB}) \quad (6)$$

$$C_{s,eqMSB} = C_s C_{eqMSB} / (C_s + C_{eqMSB}) \quad (7)$$

Next, a qualitative study with real MOMs capacitors' values are developed to highlight the effects of $C_{p,MSB}$ and $C_{p,LSB}$ as well as C_j values' spread.

IV. Case Study

To validate the assumptions made above, layouts of a 10-bit un-even split-capacitor DAC have been designed as the one shown in Fig. 3. Dummy capacitors are added around the external border of the array to reduce layout mismatches. Three combinations of m and l are implemented:$m \times l = [4 \times 6, 5 \times 5, 6 \times 4]$. With the same basic layout the three corresponding layouts are obtained by changing the connections between the MOMs. Split capacitor C_s is formed by four capacitors connected in series-parallel to reduce the mismatch effect; all sharing their bottom plates.

A Matlab routine that implements the algorithm of the SAR with $m \times l$ split-capacitor DAC is done. It incorporates (4) to (7) as well as the extracted DAC model for the three layouts.

This routine makes posible to consider separately the non-idealities of capacitors, and parasitics capacitances. Firstly, only the errors due to variations in the values of C_j are studied. In the layouts, the MOMs associated to the most significant bits of the MSB and LSB blocks of the DAC are put

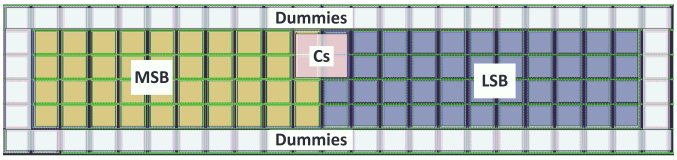

Figure 3. Scheme of MOMs split-capacitors array example.

at the edge of the layout to increase the non-idealities. These capacitors suffer from higher layout mismatch if compared with others, despite having used dummies, as seen in Table II. The resulting SAR Total Error [8] is plotted in Fig. 4(a). Ideally, if C_j are equal to that of (1), and as no random mismatch effects are considered, the error should be below 1 LSB. However, due to capacitors non-idealities equation (1) is not true, reaching errors to 3 LSB for $m \times l = 6 \times 4$, which clearly points out the effects of these non-idealities.

Secondly, only errors due to parasitic capacitances are considered, hence C_j are ideal. From (4) to (7) it can be deduced that the different configurations of m and l bits affect in a different way the SAR errors. To compute $C_{p,MSB}$ and $C_{p,LSB}$, lets consider that ideally $C_{t-g,j}$ is proportional to the parasitic $C_{o,t-g}$ of the unitary capacitor C_o that forms the capacitor C_j. Hence $C_{p,MSB(LSB)} \cong C_{o,t-g} 2^{m(l)}$. However, $C_{o,t-g}$ changes depending on the location in the layout of the corresponding unitary C_o capacitor, and, hence the extracted parasitics are not proportional to the number of unitary capacitors, as confirmed by the results shown in Table III. Therefore, the Total Error due to $C_{p,MSB}$ and $C_{p,LSB}$ differently affects the SAR depending on the election of m and l, as depicted in Fig. 4(b).

From Fig. 4 it can be inferred that errors due to C_j imbal-

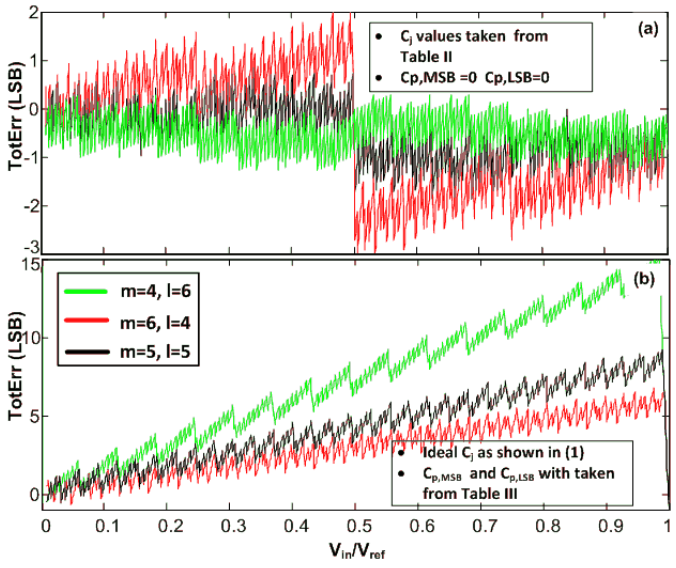

Figure 4. Total Error of a split-capacitor SAR with different $m \times l$ configuration considering only (a) parasitic capacitances with real C_j of (1) and (b) ideal C_j with real $C_{p,MSB} = C_{p,LSB} = 0$.

Table II
EXTRACTED C_j FOR DIFFERENT $m \times l$ CONFIGURATIONS.

	5×5	6×4	4×6
C_9 (pF)	4.0604	8.1777	2.0260
C_8 (pF)	2.0254	4.0642	1.0142
C_7 (pF)	1.0142	2.0274	0.5067
C_6 (pF)	0.5067	1.0141	0.2537
C_5 (pF)	0.2537	0.5072	8.1763
C_4 (pF)	4.0729	0.2538	4.0732
C_3 (pF)	2.0263	2.0263	2.0269
C_2 (pF)	1.0118	1.0119	1.0124
C_1 (pF)	0.5066	0.5066	0.5066
C_0 (pF)	0.2529	0.2529	0.2530
C_{REF} (pF)	2.5312	0.2531	0.2531
C_s (pF)	2.5577	0.2558	0.2578

ances are less significant than parasitic capacitances variations. Also, a trade-off between m and l election is appreciated for this implementation: when $m > l$ the errors due to $C_{p,MSB}$ and $C_{p,LSB}$ are reduced, however, C_j layout mismatches made errors increase, and vice versa.

Finally, the combination of both effects are presented in Fig. 5. From observations of Figs 4 and 5, it is clear that the election of m and l should be made careful not to deteriorate the SAR performance. Hence, from the results shown in those figures, it seems that it is a good election to choose $m \geq l$ to reduce errors.

This study points out the strong layout-dependant performance of the SAR when MOMs are used. An improvement is possible if MOM size is reduced as the distance d between capacitors can be made higher, for the same DAC area. However, doing so, a trade-off arises since the inherent random MOM mismatch also increases (the mismatch model is provided by the foundry). As an example, and for the MOM cell used here, when only random mismatches are considered, the Total Error is below ± 0.25 LSB; if the MOM value is reduced by half, its Total Error increases to around ± 0.5 LSB. Another option is to put the MOMs most significant bits of the MSB and LSB blocks as far as possible from the edge of the array to reduce the equivalent capacitance difference with the rest of the MOMs bits, improving the overall errors.

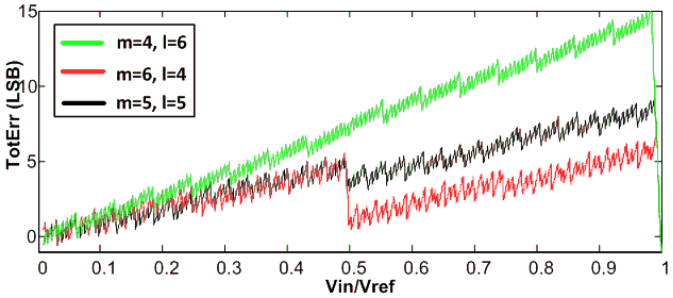

Figure 5. Total Error of a real 10-bits split-capacitor DAC. Black lines limit the zone of ± 0.5 LSB.

Table III
EXTRACTED $C_{p,MSB}$ AND $C_{p,LSB}$ FOR DIFFERENT $m \times l$ CONFIGURATIONS.

	5×5	6×4	4×6
$C_{p,MSB}$ (fF)	72.691	105.958	59.783
$C_{p,LSB}$ (fF)	83.300	70.974	107.155

V. CONCLUSIONS

In this paper, a quantitative analysis of the errors of a un-even split-capacitor array SAR is presented. Particularly, a quantitative study that leads to guidelines in the election of MSB and LSB numbers of capacitors, m and l, is presented. Finally, it is shown that total error increases much more with parasitics than with impairments between each array's capacitor, in a split -capacitor array SAR, no matter the election of m and l values.

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