Resonation-based Cascade ΣΔ Modulators for High-Linearity Broadband A/D Conversion

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Abstract – **This paper presents two new architectures of cascade ΣΔ modulators that, based on the use of resonation, allow to increase the effective resolution compared to previously reported topologies whereas keeping relaxed output swing and high robustness to non-linearities of the amplifiers. In addition, the use of loop filters based on Forward-Euler integrators, instead of Backward-Euler integrators as proposed in earlier approaches, simplifies the switched-capacitor implementation and makes the proposed architectures very suited for the implementation of highly-linear broadband A/D conversion[†].**

I. INTRODUCTION

The increasing demand for high data-rate A/D converters for the next generation of telecom systems implemented in nanometer CMOS technologies is motivating the exploration of new topologies of wideband ΣΔ Modulators (ΣΔMs) [1]-[7]. Among others, the use of resonation [5] and/or unity Signal Transfer Function (STF) [2][3] are demonstrating to be good candidates for low-voltage implementation. On the one hand, loop-filter resonators allow to increase the effective resolution as compared with integrator-based noise-shaping filtering. On the other hand, by making STF unity, the integrators ideally process quantization error only, thus relaxing their requirements of amplifier gain non-linearity and output swing.

The above mentioned strategies can be combined with cascade topologies in order to increase the order of the modulator whereas keeping stability and low oversampling ratio [1][7]. However, the implementation of in-loop resonators requires using Backward-Euler (BE) or non-delayed integrators which makes their Switched-Capacitor (SC) implementation more difficult.

This paper presents two novel topologies of cascade ΣΔMs intended for high-speed and low-voltage applications. Both modulators combine resonation techniques and unity STF. One of them is based on local resonation whereas the other one employs global resonation. In both cases, Forward-Euler (FE) instead

of BE integrators are used, thus circumventing the implementation problems presented in the former architectures based on cascaded resonators.

The paper is organized as follows. Section II provides a background on previously reported low-voltage broadband cascade ΣΔM architectures, based on the use of unity STF and resonation. Section III describes the ΣΔ topologies proposed in this paper. Finally, behavioral simulations are shown in Section IV that demonstrate the benefits of the proposed architectures in terms of effective resolution and robustness to opamp non-linearities and relaxed output swing.

II. BACKGROUND ON BROADBAND CASCADE ΣΔMs

As discussed previously, most promising ΣΔM architectures for low-voltage broadband applications combine cascade topologies with unity STF and resonation. These architectures are briefly described in this section.

A. Unity STF cascade ΣΔM topologies

Fig.1 shows a second-order single-loop that makes use of Analog FeedForward (AFF) paths to implement a unity STF [2][3]. Using a linear model for the internal *B*-bit quantizer, the Z-transform of the modulator output, $Y(z)$, is given by:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \qquad (1)$$

where $X(z)$ and $E(z)$ are the Z-transform of the input and quantization error, respectively; and $STF(z)$ and $NTF(z)$ are the Signal- and Noise- Transfer Functions, respectively given by:

$$STF(z) = 1$$
$$NTF(z) = (1 - z^{-1})^2 \qquad (2)$$

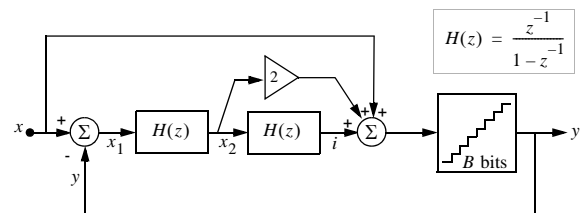One of the most remarkable advantages of the modulator in Fig.1 is that, at least ideally, there is no

Fig. 1: Second-order single-loop ΣΔM with unity STF [2].

input signal trace processed by the integrators. This is easy to demonstrate by obtaining the Z-transform of the integrators inputs, $X_1(z)$ and $X_2(z)$, given by

$$X_1(z) = -(1 - z^{-1})^2 \cdot E(z)$$
$$X_2(z) = z^{-1} \cdot (1 - z^{-1})^2 \cdot E(z) \qquad (3)$$

Therefore, the combination of feedforward paths −giving rise to unity STF−, together with multibit internal quantizers, make the architecture in Fig.1 very suited for low output swing requirements, reduced sensitivity to amplifier non-linearities and high overload levels.

The principles underlying in Fig.1 can be extended to cascade ΣΔMs [3][4]. This is illustrated in the modulator shown in Fig.2, proposed in [4]. This modulator, which from now on will be referred to as AFF-AFF, has the additional advantage of using only one inter-stage path, with the subsequent circuit simplification and increment of robustness with respect to circuit non-idealities.

B. Resonation-based cascade ΣΔM topologies

An efficient way to increase the resolution without penalizing the number of integrators consists of including resonators inside the modulator loop filter. Thus, the so-called *local resonation* technique has been used in ΣΔMs considering either single-loop [5] or cascades [1]. In both cases, this technique allows to shift the zeroes of NTF from DC, thus allowing to distribute them in an optimum way such that the in-band noise can be minimized [6].

In the case of cascade architectures, only the last stage normally uses resonation in order to reduce the digital cancellation logic. As an illustration, Fig.3 shows a cascade with local resonation in the last stage. This topology, originally presented in [1], takes advantage of both the unity STF of the first stage and the feedforward path at the last one, thus obtaining relaxed output swing requirements.

Recently, a new kind of resonation strategy, named *global resonation,* has been applied to cascade ΣΔMs [7]. This new approach, illustrated in Fig.4 for a fourth-order cascade architecture, is obtained by feeding back the error component from the last stage to the previous one. Note that, this topology achieves resonation thanks to a global path that feeds back a scaling version of the last stage quantization error at the input of the first stage quantizer.

In both cases, either using local or global resonation, the $NTF(z)$ is:

$$NTF(z) = \frac{-(1 - z^{-1})^2 \cdot [1 - (2 - K) \cdot z^{-1} + z^{-2}]}{d} \qquad (4)$$

where d stands for the inter-stage gain. Note that the zeroes of $NTF(z)$ are a function of K, which can be
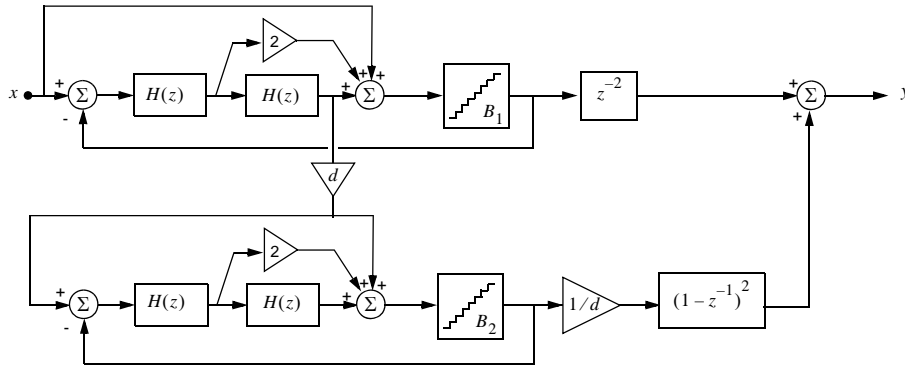

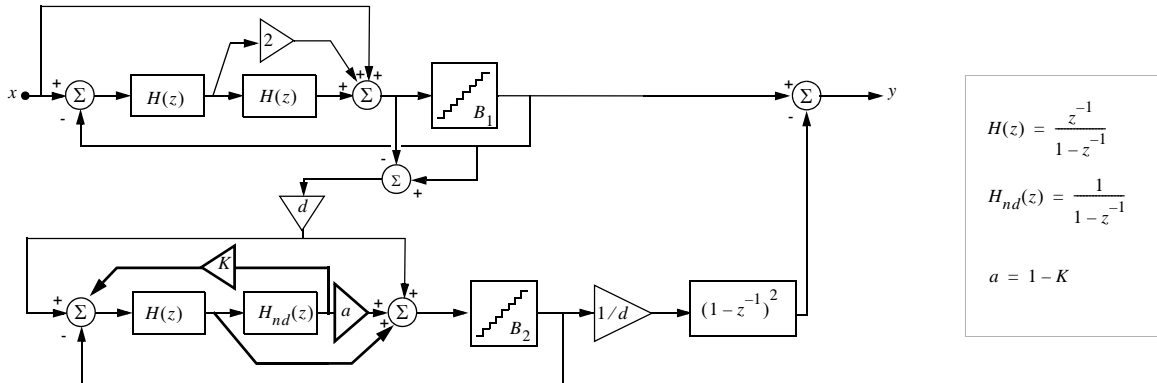**Fig. 2:** Fourth-order Cascade AFF-AFF ΣΔM architecture with unity STF [4].

Fig. 3: Fourth-order Cascade ΣΔM architecture with local resonation and unity STF [1].

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optimally chosen to maximize the Sig-nal-to-(Noise+Distortion) Ratio (*SNDR*). Indeed, practical cases may lead to a resolution increase of up to 10dB [7]. As an illustration, Fig.5(a) shows the optimal distribution of the $NTF(z)$ zeros in the unity-circle for an oversampling ratio of 4, 8 and 16. The effect on the noise-shaping is depicted in Fig.5(b) by representing $NTF(z)$ for the different cases.

Another conclusion that is derived from (4) is that increasing d (to reduce the quantization noise) yields a reduction of the feedback coefficient, a, (see Fig.4). In practice, this results in a smaller capacitor ratio, which makes the electrical implementation more difficult and prone to circuit non-idealities.

III. PROPOSED CASCADE ΣΔM ARCHITECTURES

Previously reported resonation-based ΣΔMs like those shown in Fig.3 and Fig.4 require using BE or non-delayed integrators, $[H_{nd}(z) = 1/(1 - z^{-1})]$, which makes the electrical implementation using SC circuits more difficult and prone to circuit-level errors. Instead of that, the proposed architectures make use of both local and global resonation strategies and include FE-Integrator based loop-filters, that are more suited

for implementing high-linearity low-voltage A/D converters than previous reported topologies.

A. *Proposed cascade ΣΔM with local resonation*

Fig.6 shows the proposed fourth-order ΣΔM architecture. This topology is a cascade architecture implementing local resonation with only delayed or FE integrators. The price to pay is that additional analog coefficients and a feedback path are needed. Note that this modulator is based on the one depicted in Fig.3 with two modifications. The first one is the use of a second-order single-loop FE-Integrator based resonator topology, proposed in [5], as the last stage of the resulting cascade. The second one is that only one branch − instead of two ones as in Fig. 3 − are needed to feed the first-stage quantization error to the input of the second stage.

B. *Proposed cascade ΣΔM with global resonation*

Fig.7 shows the second proposed topology, that makes use of unity STF at every stage whereas resonates through a feedback path from the last stage to the previous one, i.e. using global resonation. However, contrary to the cascade AFF-AFF ΣΔM, the modulator in Fig.7 feeds necessarily the last stage input through

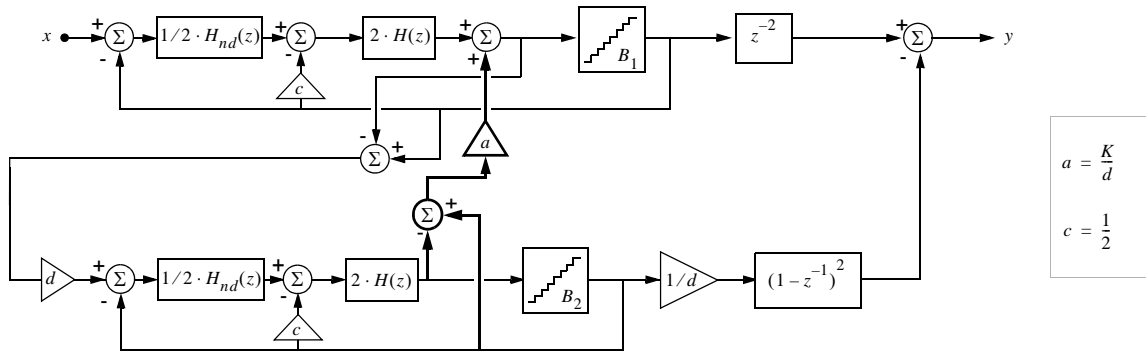**Fig. 4:** Fourth-order Cascade ΣΔM with Global Resonator [7].

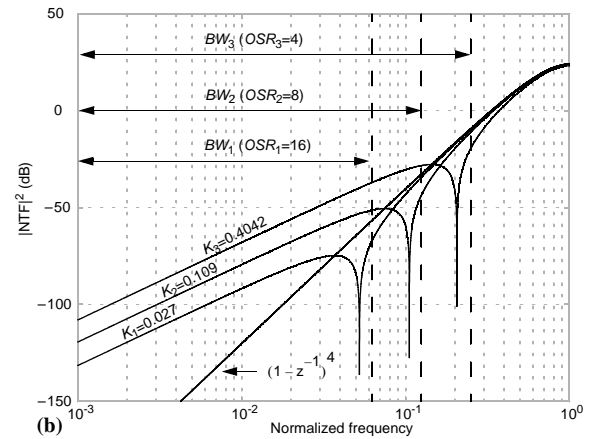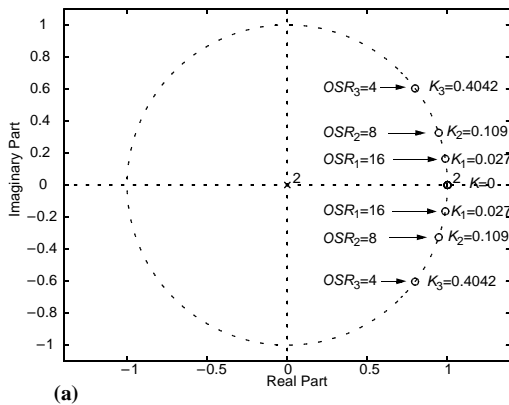**Fig. 5:** Optimum distribution of NTF zeroes in resonation-based ΣΔMs with different oversampling ratios.
(a) Zero location in the unity-circle. (b) NTF vs. frequency.

two branches. However, since FE integrators are used, an additional analog delay – that can be implemented by proper clock-phase scheme [8] – is required. Nevertheless, in order to overcome the implementation of the extra analog delay, there is a more efficient mode to realize the global resonation with unity STFs stages. Indeed, analysing the linearized Z-transform of Fig.7, it can be shown that the input and the output of the second-integrator in the last-stage are respectively given by:

$$X_4(z) = -z^{-1} \cdot (1 - z^{-1}) \cdot E_2(z)$$

$$I_2(z) = -z^{-2} \cdot E_2(z) \tag{5}$$

Note from (5) that the delayed quantization error of the last stage can be directly obtained as

$$X_4(z) + I_2(z) = -z^{-1} \cdot E_2(z) \tag{6}$$

This modification has been incorporated in Fig.7, resulting in the architecture depicted in Fig.8. Notice that the addition $X_4(z) + I_2(z)$ is already done at the
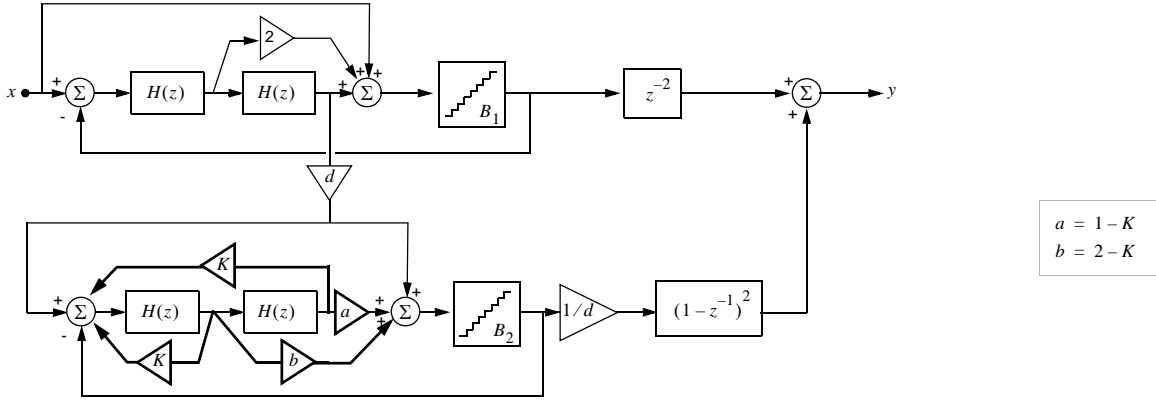

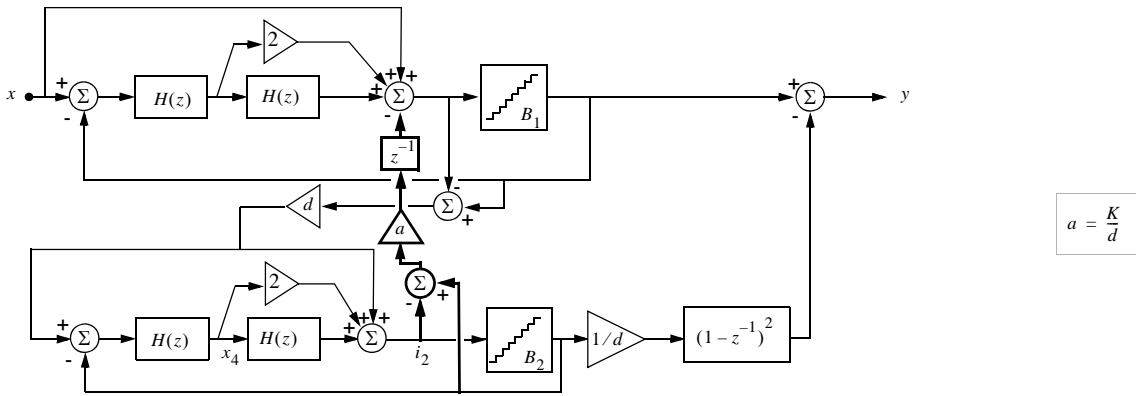**Fig. 6:** Proposed (I) Cascade ΣΔM with Local Resonator.

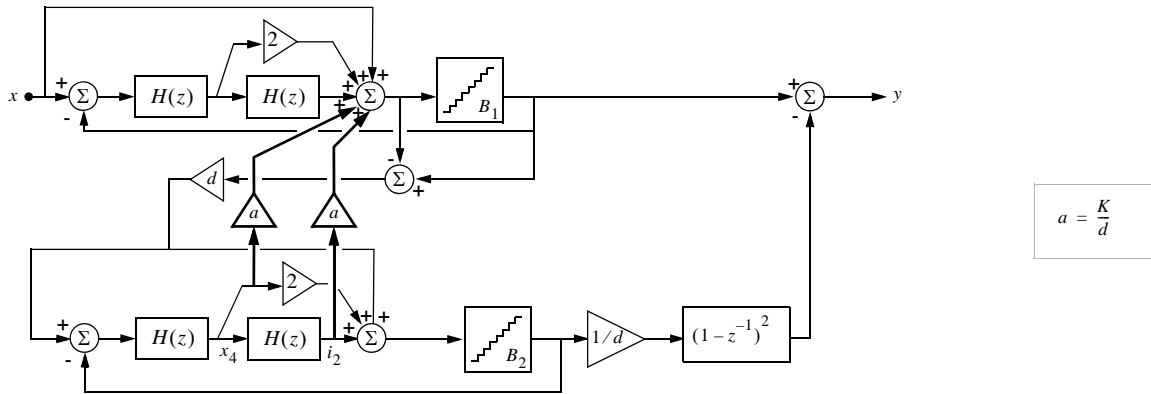**Fig. 7:** A first approach to the Proposed Cascade with Global Resonation Topology.

Fig. 8: Proposed (II) Cascade with Global Resonation Topology.

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input of the first-stage quantizer. Therefore –contrary to the modulator in Fig.4 – there is no need of an extra addition. Note that, in addition to avoiding the use of an extra delay, the ΣΔM in Fig.8 requires only one analog coefficient (K) to make the resonation, instead of three coefficients [K, $(1-K)$ and $(2-K)$] as in Fig.6, which simplifies the electrical implementation and reduces the sensitivity to circuit non-idealities.

IV. SIMULATION RESULTS

In order to compare the performance of the proposed ΣΔM architectures (Fig.6 and Fig.8), several behavioral simulations has been done using SIM-SIDES, a Simulink-based time-domain simulator for ΣΔ modulators [9]. All topologies operate with an oversampling ratio of 16, 4-bit internal quantizers, an inter-stage gain (d) of 1 and a 1-V reference voltage.

As an illustration, Fig.9 shows the effect of resonation on the output spectrum of the proposed topologies. Note that the resulting spectrum is the same for both architectures.

The optimal feedback coefficient that causes the resonation in the topology depicted in Fig.8 is $K = 0.027$, resulting in a shift of two zeroes of the *NTF* from 0 to $0.9865 \pm j \cdot 0.1638$. Note that, thanks to this optimum distribution of the *NTF* zeroes, the in-band noise has already been minimized. This is better illustrated in Fig.10 where the *SNDR* is represented versus the input amplitude. In this example the resolution of the proposed architectures is slightly 10dB larger than the one obtained by the cascade AFF-AFF in Fig.2 within the whole input range. This increase of the *SNDR* is due to the use of resonation.

Another advantage of the proposed architectures comes from the use of unity STFs yielding to the subsequent reduction of the amplifiers' output swing. This is illustrated in Fig.11 and Fig.12 by plotting the histograms of the integrator outputs in the architectures proposed in this work and those previously reported. In addition, a classical cascade 2-2 architecture is also
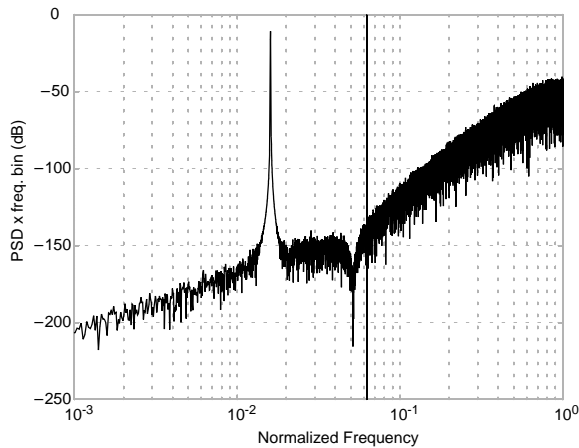
included in the comparison for completeness. Note that, the integrator output swings of the proposed modulators are similar to those in the modulator of Fig.2. However, they are smaller than the ones in the modulator of Fig.4. This is translated in a better linearity of the proposed architectures as compared to the one in Fig.4.
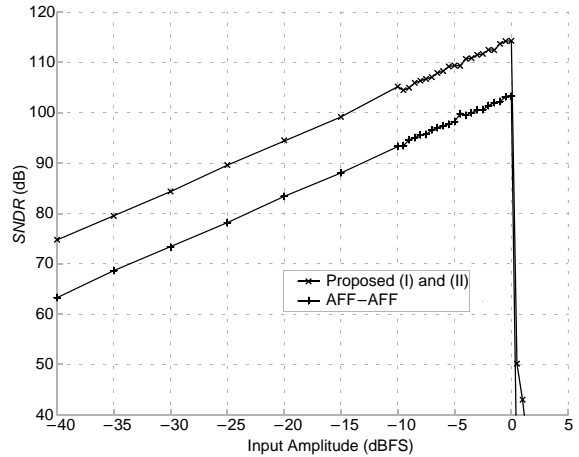

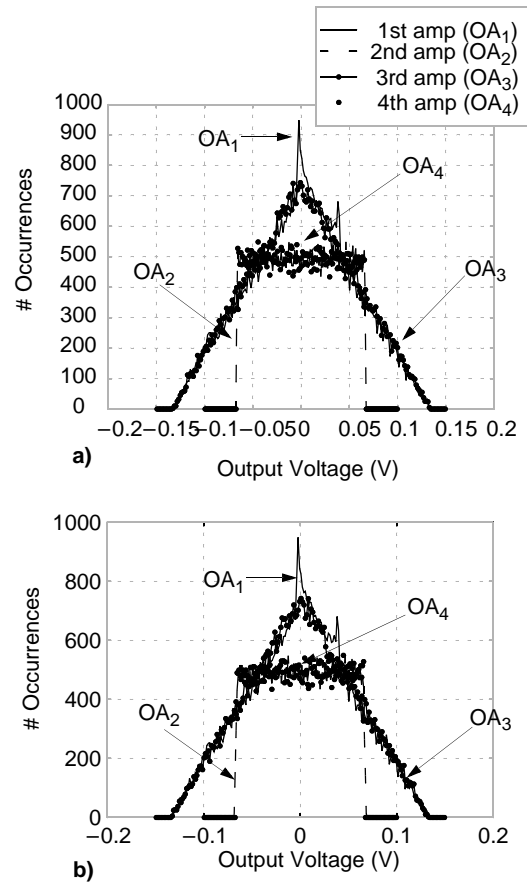**Fig. 10:** *SNDR* versus input amplitude.

a)

b)

Fig. 11: Output swing requirements for the proposed topologies: a) Proposed (I) and b) Proposed (II).

Fig. 9: Modulator spectrum with resonation.

The latter is illustrated in Fig.13 by plotting the effect of opamp gain non-linearity on the *SNDR*. In this simulation, a finite gain of 55dB is considered for all the amplifiers, while the gain second-order non-linearity for the first stage amplifiers is varied. The results of the previous simulations are summarized in Table 1, which shows the non-linearity that causes the *SNDR* to fall 3dB. Note that the robustness of the proposed
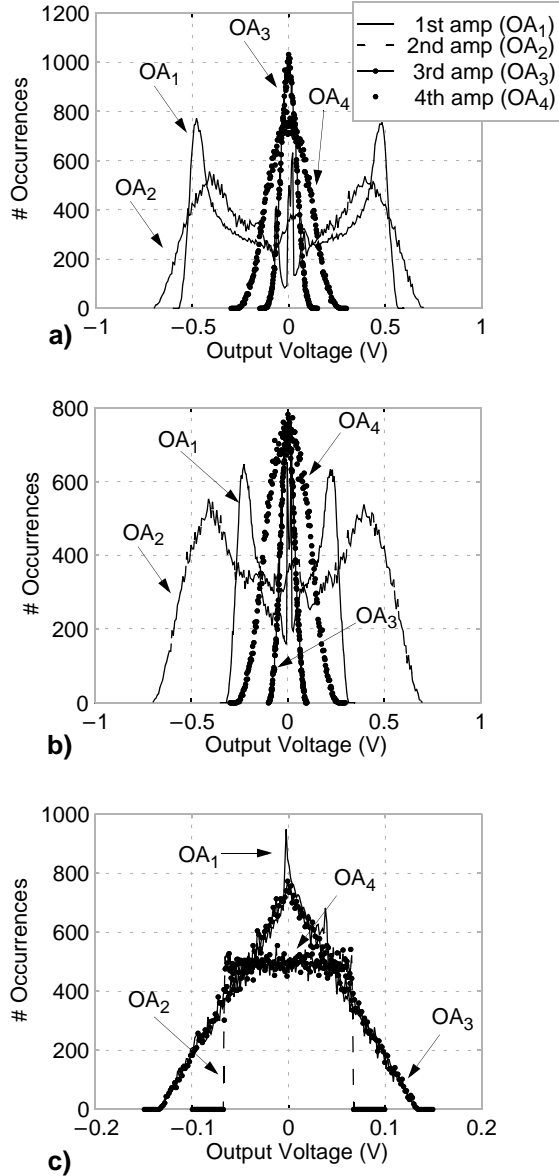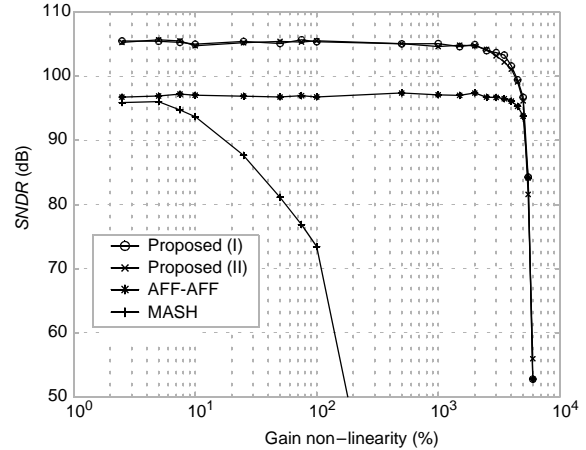

Fig. 13: Non-linearities effect on the *SDNR*.

architectures to non-linearities is similar (strictly speaking it is slightly smaller for this example) than the cascade AFF-AFF (Fig.2). However, the proposed ΣΔMs present an increased effective resolution by the action of resonation. On the other hand, compared with classical cascade (MASH) architectures, the presented ΣΔMs have better linearity performance.

CONCLUSIONS

Two novel topologies of cascade ΣΔMs have been presented. They combine resonation-based loop-filter with unity STF to achieve high-linearity whereas increasing resolution and robustness with respect to non-linearities as compared to previous approaches. These characteristics make the proposed modulators very appropriate for the implementation of low-voltage wideband A/D conversion.

Fig. 12: Output swing requirements for the amplifiers of: a) Classical MASH architecture, b) Global Resonation structure in Fig.4 and c) AFF-AFF in Fig.2.

TABLE 1. Summary of non-linearity effects

Topology	Maximum non-linear gain
Proposed (I)	4000%
Proposed (II)	3500%
AFF-AFF	5000%
Classical MASH	10%

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