A Test-rig to Evaluate a Dual-3-Phase Induction Motor Drive

Bojoi R[1], Tenconi A[1], Profumo F[1], Gallardo S[2], Barrero F[2] y Toral S[2]

[1] Dipt. di Ingegneria Elettrica Industriale, Politecnico di Torino, Turin, Italy
Corso Duca degli Abruzzi, 24, 10129, Turín. Italia
Tel.:+39 011.564.7105, fax:+39 011.564.7199 , e-mail: bojoi@polito.it, tenconi@polito.it, profumo@polito.it

[2] Electronic Engineering Department. University of Seville. Seville. Spain
Avda. Camino de los Descubrimientos, s/n. 41092. Seville, Spain
Tel.:+34 954 48 73 68, fax:+34 954 48 73 73, e-mail: sgallardo@gte.esi.us.es, fbarrero@gte.esi.us.es, toral@gte.esi.us.es

1. Abstract

The potential advantages of multi-phase solutions over the conventional 3-phase ones have been widely described in the literature. However, their feasibilities and performances have been poorly described and proven. The main goal of this paper is the design and implementation of a test rig to evaluate some control policies for a double-3-phase induction motor drive, a multiphase drive with interest in Electric Vehicle (EV) applications.

Keywords:

Test-rig implementation, multi-phase induction motor drives, EV applications.

2. Introduction

Multi-phase motor drives have been studied from more than thirty years, but starting from the last two years, the interest has grown so that some international power electronic conferences have hosted sessions on the multi-phase motor drives [1]. Multiphase motor drives have been proposed for different applications where some specific advantages (lower torque pulsations, less DC link current harmonics, higher overall system reliability, etc) can be better exploited justifying the higher complexity in contrast to the three-phase solution [2]. Some of the most suitable applications are the high current ones (ship propulsion, aircraft applications, locomotive traction, electrical vehicles), where the main advantage of multi-phase drives is the splitting of the controlled power (current) on more inverter legs, reducing the single switch current stress compared to the three-phase converters. Since the power switches rated current is reduced proportionally with the phase number, the increased number of power switches does not represent an additional cost; on the contrary, in some cases the cost is reduced by the "non-linearity" of the component prices. However, the system cost (and complexity) is penalized by the increased number of the current sensors, gate drive circuits, additional circuitry power supply, etc.

Among the different multi-phase induction drives solutions, the dual-3-phase induction machine having two stator winding sets spatially shifted by 30 electrical degrees with separated neutral has important advantages [3-4]:

1. The current stress of each semiconductor power device is reduced by one half compared with the same power 3-phase machine counterpart.
2. The dual-3-phase solution can benefit of the wide availability of components dedicated to 3-phase systems.
3. These electrical machines are convenient in high power and/or high current applications, such as ship propulsion, aerospace applications, and electric/hybrid vehicles (EV). In applications like EV, often the low available DC-link voltage imposes high phase current for a 3-phase machine. In this case, the dual-3-phase induction machine is an interesting alternative to the conventional 3-phase counterpart.

Due to the insufficient available technical literature concerning controlled dual-3-phase induction motor drives, this paper is going to cover the prototype realization and experimental validation of a test-rig for this kind of multi-phase drives.

3. Experimental Rig

A diagram of the complete system is shown in Fig. 1. The system is divided in four different blocks:

The analogical board. The functionality of the analogical board is to serve as interface beetwen the power electronic and the control electronic of the system, all the information that comes from the analog signals are inputs of the analogical board, all the measures, currents, temperatures, etc., are previously analogically-processed to generate the appropriate signals to the control board.

The control board, it implements all the system control intelligence, is based on a digital signal processor (DSP) and a field programmable gate array (FPGA) working in a parallel configuration and the same clock timing. The communication between the DSP and the FPGA is implemented via a dual port ram implemented over the FPGA.

The power inteface and drives, a conventional power converter controlled via digital control board signals. Fault signals that comes from the power interface have been also designed to protect the system integrity.

Dual-three phase motor, the 10 kW induction machine has two sets of stator three-phase windings spatially shifted by 30 electrical degrees.

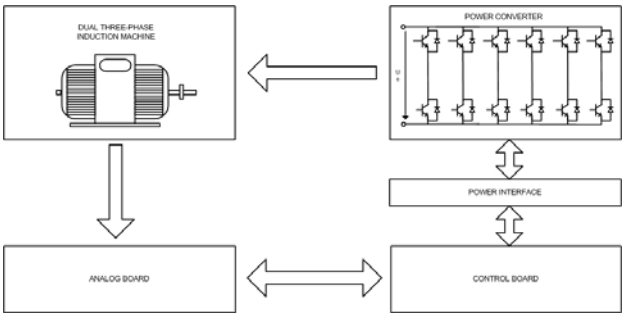

Fig. 1. Schematic of the dual three phase motor test rig

4. Hardware description

As we mentioned, the test rig is divided in four different blocks. We will focus on this article in the description of the analog and digital board.

4.1. Control Board Description

The designed control board is based on a digital signal processor and a field programmable gata array. They both manage all the system, control the power converter drives operation, analize the input signals, process the errors, etc. The DSP that is used is a TMS320LF2407 [5] of Texas Instruments®

The TMS320LF240x devices are part of the TMS320C2000™ platform of fixed-point DSPs. The 240x devices offer enhanced architectural design, low-cost, low-power, and high-performance processing capabilities. The 240x offers increased processing performance (30 MIPS) and a higher level of peripheral integration.

The high-performance, 10-bit analog-to-digital converter (ADC) has a minimum conversion time of 500 ns and offers up to 16 channels of analog input. The autosequencing capability of the ADC allows a maximum of 16 conversions to take place in a single conversion session without any CPU overhead.

A serial communications interface (SCI) is integrated on all devices to provide asynchronous communication to other devices in the system. For systems requiring additional communication interfaces, the 2407 and 2406 offer a 16-bit synchronous serial peripheral interface (SPI). The 2407 and 2406 also offer a controller area network (CAN) communications module that meets 2.0B specifications. To maximize device flexibility, functional pins are also configurable as general-purpose inputs/outputs (GPIOs).

To streamline development time, JTAG-compliant scan-based emulation has been integrated into all devices. This provides non-intrusive real-time capabilities required to debug digital control systems. A complete suite of code-generation tools from C compilers to the industry-standard Code Composer Studio™ debugger supports this family. Numerous third-party developers not only offer device-level development tools, but also system-level design and development support.

In other hand we employ a FPGA, in particular, the EPF10K100E device [6].

The Altera® FLEX 10K® embedded programmable logic family delivers the flexibility of traditional programmable logic together with the efficiency and density of embedded gate arrays.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster, ByteBlasterMV, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation. FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

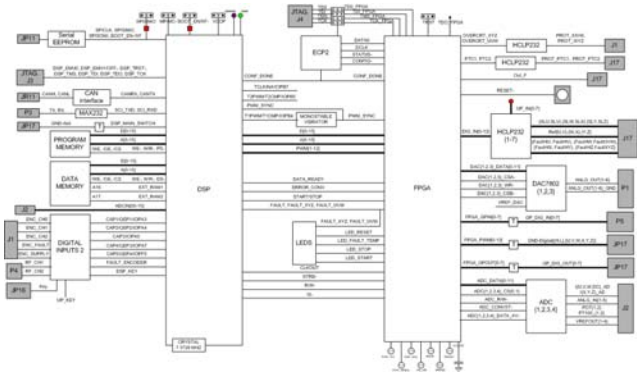

Fig. 2. Control board schematic

As we can see in Fig. 2, control board incorporates multiple elements to enable a complete functionality.

The system core is based on the digital signal processor (DSP) and the FPGA, the copressor of the board. Both implement all the control and intelligence of the system. To implement this control politicy is necessary to download a executable program over the DSP and the FPGA. The DSP download process can be made in different ways. In one hand, we have a serial EEPROM memory to enable a serial bootloader operation over the DSP internal memory. A executable program must be downloaded over the serial EEPROM previously, employing a EEPROM programming device. The EEPROM of the designed board is a M95640. These electrically erasable programmable memory is accessed by a high speed SPI-compatible bus. The memory array is organised as 8192 x 8 bit. The device is accessed by a simple serial interface that is SPI-compatible. In other hand, a JTAG-in-system-programming (ISP) is possible, thanks to the JTAG connector that we can find in the control board, allowing boundary-scan and programming. This is speciallity useful in the developing stage of the system to debug the program to be executed over the DSP. A external program memory is implemented to download the program to be executed. To load temporal data and variables, a external data memory is employed, as we can see in figure 2. The external memory that is used in the proposed design is the IDT71V416, a high-speed Static Ram organized as 256Kx16 bits.

The FPGA programmation process take place using the JTAG interface. FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream, in our system, a ECP2 device is employed. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster TM, ByteBlasterMV TM, or MasterBlaster download cables.

EPC2 device has reprogrammable Flash configuration memory 5.0-V and 3.3-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. With SRAM-based devices, configuration data must be reloaded each time the system initializes, or when new configuration data is needed. Altera configuration devices store configuration data for SRAM-based APEX II, APEX 20K, Mercury, ACEX, and FLEX devices.

A set of jumpers enables the configuration of the DSP and the FPGA to be used in the corresponding working frame.

The parallel process between the DSP and the FPGA take place thanks to different communication lines implied in this process. To interchange information between the DSP and the FPGA a internal dual port RAM has been implemented inside the FPGA, the data bus and the address bus of the DSP are used. Some control lines as IS, R/W, STRB, etc, are also employed to control the communications. The PWM control implemented over the DSP logic is also carried to the FPGA device employing a PWM bus. Lines employed to determine the efectiveness state of the FPGA are also used, as the CONF_DONE signal, that informs to the DSP about the end of the FPGA configuration process. Other important signals in the system are CLKOUT and PWM_SYNC, that synchronizes the inter-communication process between both, the DSP and the FPGA devices.

To interface with the control board we can find different elements. In one hand, we can mention a group of elements that enables external communication with the DSP, as a display controller HD44780U, for example. The HD44780U dot-matrix liquid crystal display controller can be configured to drive a dot-matrix liquid crystal display under the control of a microprocessor. In other way, a group of elements and connectors are used to interface the control board and the analogical board that acquires all the external signals of the system.

Some interfaces have been designed to enable an external interface of the system with a control console or/and monitor. Thanks to the internal pheripherals that we can find in the TMS320LF2407, a control area network communcation (CAN) and an asynchronous serial communication can be developed. A display console has been implemented employing the FGPA and the HD44780U LCD controller. The internal architecture incorporates a protocol to interface with a display of the system status. To start/stop the system a external console of two buttoms has been used, these buttoms are connected to the control board via the FPGA device, that controls the execution process. An internal state machine determines the system behaviour.

The interface between the control board and the analogical board take place employing two connectors. One of them is employed to interface the encoder signals and the current protection signals and the other one is employed to interface all the analog inputs of the system, measured currents and temperatures mainly. The encoder signals previously adapted by the analogical board are optocoupled, employing a HCLP-0630 high-speed optocoupler, and wired directly to the DSP inputs. The DSP will manage these signals. In other way, the current protection signals are inputs of the FPGA, previously optocoupled and its internal logical will manage these events as we will see. The analog inputs are carried to analog to digital converters, employing the TH1206 components, a CMOS, low power, 12 bits, 6 MSS analog to digital converter with a multistage pipelined architecture.

To determine the best behaviour of the system two different A/Ds have been employed, the internal A/D of the DSP and external A/Ds manage by the FPGA device.

The control board also interfaces with the power board, this is, with the power converter switches, to control the the PWM strategy. The PWM algorithm is implemented by the DSP that proporcionates to the FPGA, via PWM bus, the values in each moment and the FPGA wires

these signals to the power board, to control the power converter.

To recognize the status of the system a group of LEDs are present in control board. These LEDs help to determine the system status and error signals that disable the control of the converter.

To reset the control board, a reset buttom can be employed, the reset signal is managed by the FPGA .

Other general purpose elements are present in the system, as general purpose digital inputs and a external digital to analog converter.

4.2. Analog Board Description

The analog board functionality is to interface the measurements from the power converter signals, the encoder, the temperatures,…, and proporcionate to the control board the adecuate input signals to manage the system. Different functional blocks can be described in this board, as we can see in the following figure:

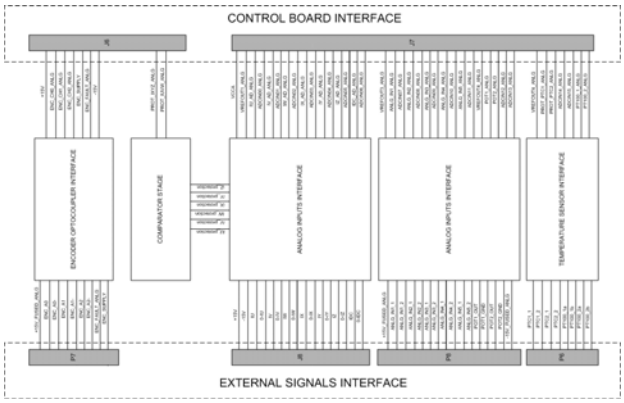

Fig. 3. Analog board schematic

Five different functional blocks can be mentioned:

Temperature sensors interface. Four temperature sensors are used, two PT100 (platinum thermistor) and two PTC thermistors (Positive Temperature Coefficient). A adaptation of the temperature measured by the PT100 sensors is realized. The output signal of the PTC interface are two digital overcurrent flags to protect the system integrity.

Currents inteface. To measure the currents six LA 200-P current transducers have been employed. A conventional interface take place to enable the adecuate levels and amplitudes of the signals. Some overcurrent protection signals are generated and wired to a comparator stage to determine a overcurrent condition.

Comparator stage. It compares the current with two predefined values, OVERCURRENT+ and OVERCURRENT-. If the amplitude of the overcurrent is enough, a overcurrent signal is generated. Two different signals are generated to diference between the two separated wires of the stator motor.

General purpose, analog inputs interface. A general purpose analog inputs interface is implemented in prevision of future ampliation of the system.

Encoder stage. The encoder signals are interface to the control board, as is shown in figure 3.

5. Software description

The DSP will control the power converter, this is, the dual three phase motor. All the algorithms implemented to control the system are, at this moment, implemented over the digital signal processor. The FPGA works as a coprocessor that helps the DSP to manage some of the external events and the external elements, i.e., the analog to digital converters.

However, the system configuration, where a parallel process is posible, enables the posibility to implemented a section of the control process in the FPGA, employing, for example, look-up-tables, improving the system control strategies and posibilities.

5.1. DSP Software description

The software implemented in the DSP is nowadays being developed, it is employed to implement the different strategies to control the dual three phase machine. A internal state machine has been developed. A general flowchart can be shown:

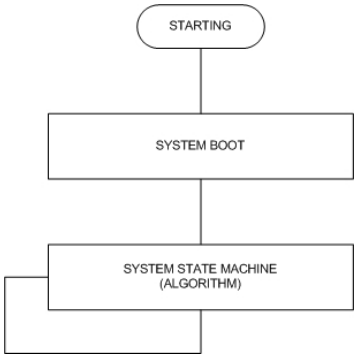

Fig. 4. DSP operation flowchart

5.2. FPGA Software description

The software implemented in the FPGA has been organized in different functional blocks. The different functional blocks, have been designed employing the Max Plus II® enviroment of Altera®. The FPGA manages the main of the external signals that are inputs and outputs of the system and acts as coprocessor of the DSP, that implements the control strategies mainly. The FPGA has been structured in well-functional-separated blocks, each one implements an operation and they are internal communicated to determine when and how to start to work, as we can see in the following figure:

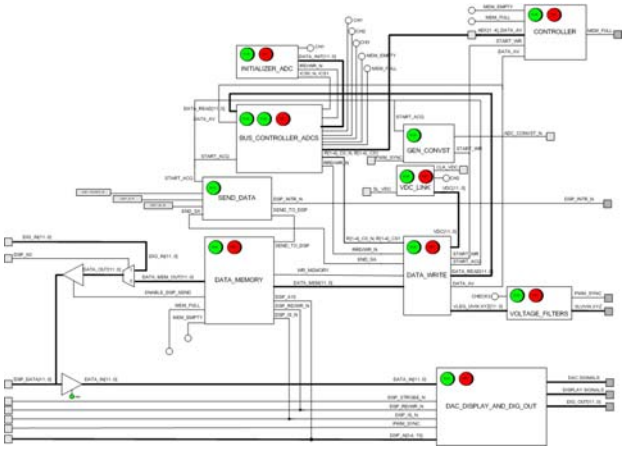

Fig. 5. FPGA functional blocks schematic

The FPGA operation start with the start/stop signals. The FPGA operation is as follows: First at all, after a reset the FPGA initiates the external analog to digital converters and configures its registers. After the boot process, the A/D conversion process of the analog inputs start to work periodically. Other inputs signals are also processed employing other blocks, as the voltage of the DC link or the voltage of the phase-branches. All the measured inputs are stored in an internal memory that enables to be readed by the DSP. The memory to load these measures has been, at first, implemented as a convectional FIFO memory, however, after to test the system, and to improve the time necessary to read the data from the FPGA by the DSP, a dual port RAM memory has been designed, improving the transfer time. Other functional block is the the managing of the digital to analog converters, the display signals (employing a LCD), and the digital outputs, employing other block. The PWM ad error signals are managed to enabled or disabled the modulation process if a non adecuate state has been reached. Finally, a block implements some external signals to switch on/off the LEDs to have a visual inspection of the system status.

4. Conclusions

An important operative result is the availability of a flexible and fast development tool to test future improvements, such as sensor number reduction, sensor less applications, EV applications, and advanced control implementation for this kind of motor drives.

A DSP-based advanced controller for a double-3-phase induction motor drive has been designed. The potential advantages of multi-phase solutions over the conventional 3-phase ones (the reduction of the single static switches current stress, which decreases proportionally with the phase number; the reduction of torque pulsation; the reduction of rotor harmonic losses; the reduction of the harmonic content of the DC-link current; and the improvements of the overall system reliability) have been tested.

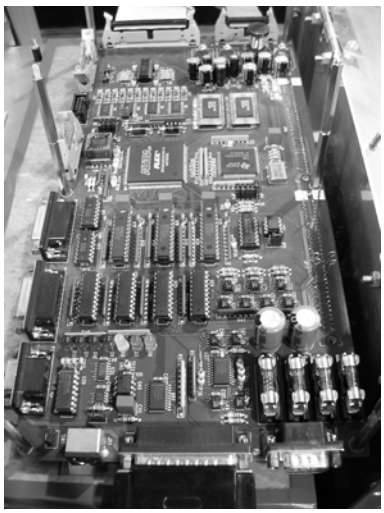

Fig. 6. Photography of the control board based on the TMS320LF2407 DSP

References

[1] E. Levi, “Editorial - Special Issue on Multi-Phase Motor Drives”, EPE Journal, Vol. 14, No. 3, June-July-August 2004, pp. 4.

[2] G. K. Singh, “Multi-Phase Induction Machine Drive Research – a Survey”, Electric Power Systems Res., Vol. 62, 2002, pp.139-147.

[3] R.Bojoi, F.Farina, M.Lazzari, F.Profumo, A.Tenconi, "Analysis of the Asymmetrical Operation of Dual three-Phase Induction Machines”, Conf.Rec.IEEE-IEMDC’03, Madison (USA), June 2003, pp.429-435.

[4] R.Bojoi, F.Profumo, A.Tenconi, "Digital Synchronous Frame Current Regulation for Dual Three-Phase Induction Motor Drives", Conf.Rec.IEEE-PESC’03, Acapulco (Mexico), June 2003, 1475-1480.

[5] “TMS320LF2407, TMS320LF2406, TMS320LF-2402 DSP Controllers”. SPRS094I-April 1999, revised September 2003.

[6] “FLEX 10K. Embedded Programmable Logic Device Family”. January 2003, ver. 4.2, datasheet.