A SELF-CHECKING CURRENT-MODE ANALOGUE MEMORY

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ABSTRACT

A long-term analogue memory based on continuous-time, current-mode algorithmic A/D-D/A converters is presented. It achieves an efficient performance in terms of speed, resolution, power, and area, while incorporating self-checking capability. Its operation is described and illustrated with experimental results of a CMOS-2.4μm prototype with 7-bit resolution.

INTRODUCTION

Long-term storage of analogue data is one of the main challenges faced by VLSI implementations of adaptive signal processing systems and neural or fuzzy networks [1]. Among the solutions reported in the literature, floating gate memories share the drawbacks of requiring high voltages and long time to write the data [2]. Another approach is to make use of a quantizer (basically a combination of A/D and D/A converters) that stores the discrete level closest to the analogue input data [1, 3, 4, 5]. Instead of voltage-mode data converters [1], current-mode techniques seem more suitable as resolution (number of quantized levels) increases or the voltage supply decreases. Continuous-time flash-type, switched-current single-slope and successive-approximation current-mode converters have been respectively employed in [3-5].

The current-mode memory that we propose, based on continuous-time algorithmic converters, achieves an efficient trade-off between write/read speed and power consumption, and between silicon area occupation and resolution. Besides, it offers the novelty of self-checking behaviour which permits on-line error detection.

CIRCUIT DESCRIPTION

As a consequence of having selected a continuous-time algorithmic conversion technique, the proposed memory has a modular structure consisting of a cascade of identical or alternating (odd/even) cells, each of one associated with a quantization bit. Hence, the silicon area of the proposed memory (which is proportional to the number, N, of quantization bits) can be considerably smaller than the area of the memory presented in [3] (which is proportional to the number, 2^N, of discrete levels stored).

The schematic of a bit cell is shown in Fig. 1a. During the load or write process (W is "1" and R is "0"), the bit cells implement the A/D conversion method illustrated in Fig. 1b, thus obtaining the binary representation, $\{b_i\}$, of the analog input data. The input current to each cell, I_i, is compared with the reference current, $I_{FS}/2^i$, where I_{FS} is the full-

scale current admitted by the memory. A high operation speed is achieved by using the current comparator proposed in [6-7] and by including the transistor M_a, because they both avoid large voltage swings at nodes *x* and *y*, respectively. The current comparator is also exploited to perform the subtraction operation between I_i and $I_{FS}/2^i$, when b_i is "1". The high errors usually caused by subtraction operations are reduced with this solution since the voltage swing at node *x* is low. The different quantization bits, b_i, of the A/D conversion are obtained in an asynchronous way. As a consequence, our design requires a simpler control circuitry (with 2 control signals, W and R) than the memories reported in [4-5] that require 8 and 2+N signals, respectively.

The cascade of N cells to form an N-bit resolution memory is shown within the dashed box of Fig. 2. Once the write process is finished, W is "0" and the bits are stored in the digital latches. Read process is implemented by exploiting the D/A converter that is included within the A/D one. This operation is synchronized by signal R, thus reducing glitches. The restored current is $I_{out} = b_1 \cdot I_{FS}/2 + ... + b_N \cdot I_{FS}/2^N = Q(I_{in})$, where I_{in} is the input current to store and Q(.) is a quantization operator. The inherent quantization error of I_{out} is $\pm I_{FS}/2^{N+1} = I_{LSB}/2$, where I_{LSB} is the current corresponding to the least significant bit. Offset, gain, and linearity errors of the A/D and D/A parts contribute to increase the global error, $I_{out} - I_{in}$, of the memory.

SELF-CHECKING

An interesting feature of the proposed structure is that it can be easily extended to incorporate self-checking capability. In a fault-free memory device:

$$\left| I_{out} + I_{LSB}/2 - I_{in} \right| \leq K \cdot I_{LSB} \qquad (1)$$

where the value of the constant K (always superior to 1/2 due to the quantization error) depends on the accuracy required by the application.

Having designed the memory for a particular K, the above condition is checked by adding the circuitry shown at the middle of Fig. 2. It includes a current-mode absolute value operator, a current mirror that scales I_{LSB}, and a current comparator. The test is performed at the beginning of the read process, so that the input data must be hold while W or T are "1". The pass/fail signal obtained on line identifies if the restored current, I_{out}, is right or wrong according to (1). Duplicating the extra circuitry we can guarantee that the whole system is self checking.

EXPERIMENTAL RESULTS

A memory device with 7-bit data converters has been integrated in a 2.4μm CMOS process. Its die photograph is shown in Fig. 3. This prototype includes a shift-register with master-slave latches to also allow serial load of digital data and it replicates the reference current in each bit cell ($I_{FS}/2^i$) so that the data can be read while a write process is performed. Its active area is 1118μm x 216μm (0.241mm^2). Fig. 4 illustrates the 128 levels in which an input current, I_i, can be stored. This result corresponds to an I_{FS} equal to 12μA, an output voltage of 1.4V and a supply voltage of 3.3V. The circuit can operate at low voltage because it employs simple current mirrors. The error in the restored data (I_o-I_i), shown at the bottom of Fig. 4, is ± 1.40% with an offset of 0.07% of the full-scale current. In this fault-free prototype, the value of K in equation (1) is 2. The load process is performed in 1.43μs and the power consumption is 845μW at the full-scale current.

CONCLUSIONS

A modular current-mode memory with a compact circuit design has been proposed. Its features of high speed, low power consumption, small area, and self checking make it very suitable for VLSI implementation of adaptive signal processing systems and neural/fuzzy networks. Experimental results from a CMOS-2.4μm prototype with 7-bit resolution gives a figure 'speed/power' above 80Msamples/100mW•sec at a 3.3V power supply.

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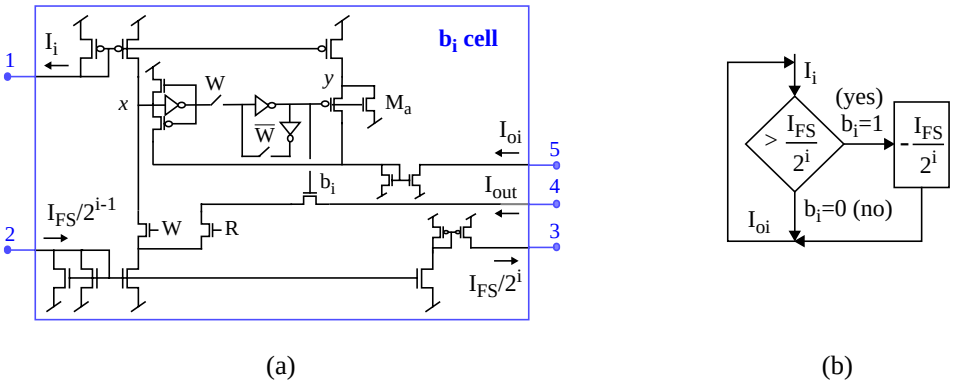

Figure 1: (a) Bit-cell schematic of the proposed memory circuit.

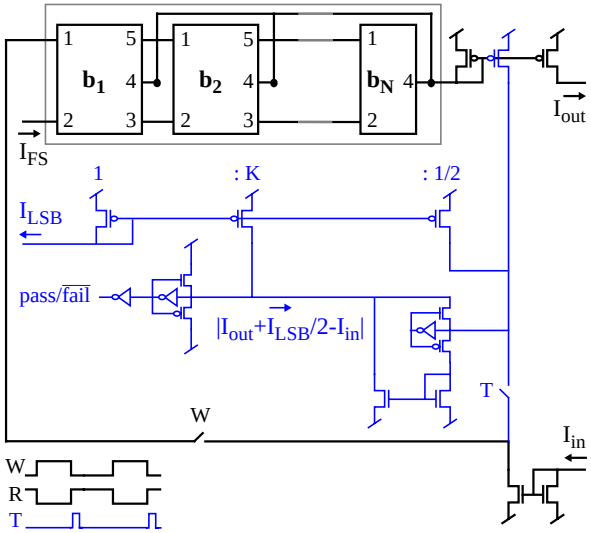

Figure 2: N-bit memory with self-checking capability.

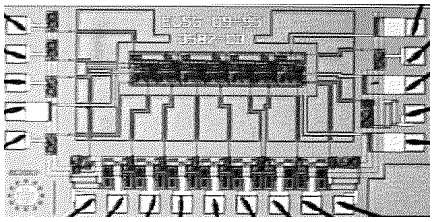

Figure 3: Die photograph of a 7-bit prototype.

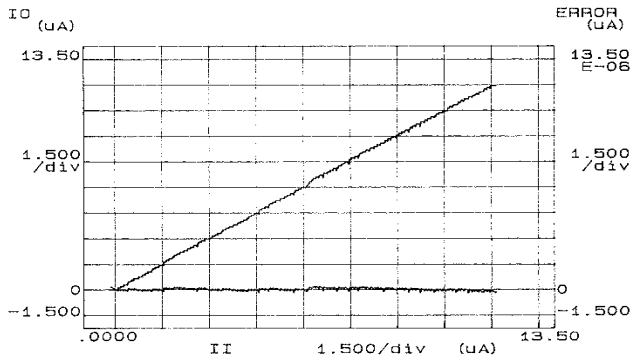

Figure 4: Experimental result of the prototype storing the input current into 128 levels.