Integrated Circuit Implementation of Fuzzy Controllers

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Abstract

This paper presents mixed-signal current-mode CMOS circuits to implement programmable fuzzy controllers that perform the singleton or zero-order Sugeno's method. Design equations to characterize these circuits are provided to explain the precision and speed that they offer. This analysis is illustrated with the experimental results of prototypes integrated in standard CMOS technologies. These tests show that an equivalent precision of 6 bits is achieved. The connection of these blocks according to a proposed architecture allows fuzzy chips with low silicon area whose inference speed is in the range of 2 Mega FLIPS (fuzzy logic inferences per second).

I.- Introduction.

The use of fuzzy systems is widespread, mainly in the control field. Most fuzzy microcontrollers presently used in industrial applications are digital implementations. However, fuzzy logic is intrinsically more like the multivalued and continuous analog world than the digital one. In addition, fuzzy systems process this continuous information in a massively parallel way. Regarding these features, analog implementations may offer a better 'silicon area / inference speed' ratio.

Adapting fuzzy concepts to meet microelectronics constraints, in terms of both architecture and circuitry, has been a major issue in this field. In particular, the selection of the inference method greatly determines the resulting hardware. Among the various inference methods reported in the literature, the singleton or zero-order Sugeno's method is very adequate for hardware implementations as well as to ensure efficient control [1]. A singleton fuzzy controller chip is adapted to solve a control problem by defining its rule base, that is, the parameters describing each antecedent's membership function and the parameter representing the singleton consequent. In the case of analog fuzzy chips, these parameters can be fixed prior to chip fabrication [2,3] or afterwards through programming [4-6].

This paper presents mixed-signal IC techniques to implement programmable singleton fuzzy controllers. Current-mode analog circuits are used to provide a high functional efficiency in the realization of the basic operations required (addition/subtraction, bounded difference, and division). Mixed-signal circuits, namely current-mode D/A converters (DAC), are used to implement the scaling operation and to offer the advantages of the digital world, such as ease of programming and capability of long-term storage for the controller parameters. Section II identifies the functional blocks required. The CMOS circuits to implement these blocks are presented in Section III. Their static and dynamic behavior are analyzed and illustrated with experimental results of prototypes integrated in standard CMOS technologies. These circuits constitute a set of analog building blocks (input-output compatible) that facilitates the design of programmable fuzzy chips according to the architecture discussed in Section IV.

II.- Functional blocks.

The knowledge base of a singleton fuzzy controller consists of IF-THEN rules that relate fuzzy antecedents with crisp or singleton consequents. In the case of single-output controllers, these rules assume the form:

Rule i: IF x_1 is A_1^i and ... and x_u is A_u^i THEN y is c_i

where x_j (j=1,..., u) are controller input signals, y is the output, A_j^i are linguistic values defined by fuzzy sets on the input universe of discourse, and c_i are crisp values.

The global output is obtained from an average in which each consequent value, c_i, is weighted by the activation degree, h_i, of its corresponding rule:

$$\text{output} = \frac{\Sigma_i h_i \cdot c_i}{\Sigma_i h_i} \qquad (1)$$

The following functional blocks are necessary for hardware implementation of this algorithm:

(a) Membership function circuits (MFCs) whose transfer characteristics represent the antecedents' membership functions. They provide the degree of matching between the controller input signals and the antecedents of the rules.

(b) Minimum/maximum circuits (MIN/MAX) that connect the antecedents of a rule to compute its activation degree.

(c) Consequent scaler circuits (CONSs) that weight the singleton consequent with the activation degree.

(d) A divider (DIV) to obtain the overall output.

The use of current-mode techniques allows saving adder circuits to calculate the values of the numerator and denominator in Equation (1). They are obtained simply by leading the currents representing h_i and $h_i c_i$ to a common low-impedance node.

III.- CMOS implementation of functional blocks.

Membership Function Circuits: Figure 1a illustrates the schematic of an MFC which allows implementing triangular and trapezoidal membership functions (Figure 1b). These are defined by the parameters I_{aux} (central point of the fuzzy label), I_{sat} (saturation of the trapezoidal function), and m (the slope of the membership function), according to the expression:

$$MFC(I_{in}) = I_{ref} \; \Theta \; m(\; | \; I_{in} - I_{aux} \; | \; \Theta \; I_{sat} \;) \tag{2}$$

where I_{ref} is the maximum degree of pertenence and Θ is a rectification or bounded difference operator, defined as:

$$a \; \Theta \; b = \begin{cases} a - b & \text{if } a > b \\ 0 & \text{otherwise} \end{cases}$$

Digital programmability is added in a rather straightforward manner via current-mode DACs that are based on current mirrors. Two of them fix the values of I_{aux} and I_{sat}, while another performs as a programmable multiplier to implement the scaling by m. The diode-connected input transistor of this DAC also implements the bounded difference with I_{sat}.

The combination of T_1, T_2, and the PMOS current mirror (proposed in [7]) is the simplest solution we have found to implement the absolute value operation in Equation (2). It avoids replication of I_{in} or I_{aux}, thus saving area and power consumption. What may cause systematic errors in the generation of I_{in} and I_{aux} are the large voltage swings at the input node (source of transistors T_1 and T_2): if T_1 and T_2 are biased with the same gate-voltage, as in [7], the voltage swing is at least $V_{Tn} + |V_{Tp}|$, being V_T the transistor threshold voltage. Voltage swing can be reduced if their gates are biased by voltages whose difference is approximately equal to $V_{Tn} + |V_{Tp}|$ so that both transistors are at the edge of conduction [8]. Another solution is to include negative feedback, for instance via a simple inverter as depicted in Figure 1a [9].

Low voltage swings at nodes also allow high frequency behavior since the time delay to charge or discharge the parasitic capacitances is decreased. The transient response of the circuit is closely related with the transient response of the current mirrors which process the signals. Since the time constant of a current mirror is g_{mi}/C_{gs} [10] (g_{mi} is the transconductance of the input transistor and C_{gs} is the gate-to-source capacitance), the smaller the input current to the mirror (I_{aux} - I_{in} or $| I_{in} - I_{aux} | \Theta I_{sat}$), the longer the transient response.

A prototype of this MFC has been integrated in a 1.5-µm CMOS technology, occupying an active area of 0.07 mm^2 (Figure 2). It is programmed by an 8-bit word (4 bits to fix I_{aux} and 2 bits for I_{sat} and m). Experimental results obtained by programming the slope value are shown in Figure 3a. Figure 3b shows the test results from fixing a value of I_{sat} and m, and varying the digital code for I_{aux}. The response time of this MFC, to within 1% of the full scale output current and for input current steps greater than 0.5µA, has been estimated as less than 250ns. To provide this MFC with voltage input, the differential version of the voltage-to-current converter proposed in [11] has been employed.

Connective circuits: Figure 4a shows the schematic of a multi-input MAX circuit [12]. It is used to implement a connective MIN between the rules antecedents, according to De Morgan's law:

$$\text{Min} (I_1, ..., I_n) = \overline{\text{Max}} (\bar{I}_1, ..., \bar{I}_n) = I_{ref} - \text{Max} (I_{ref} - I_1, ..., I_{ref} - I_n) \tag{3}$$

Therefore, in a fuzzy chip the bounded difference with I_{ref} (see Equation (2)) is not performed within each MFC, but after antecedent connection.

Transistors T_i, acting as voltage followers, compete to fix the voltage at their source node to the value needed by its corresponding M_i to operate in saturation conducting the input current I_i. This follows the idea proposed by Lazzaro et al. [13] to implement a WTA circuit and in [14] to realize a MAX circuit. The circuit in Figure 4a exploits another potential of transistors T_i, which is that the winner T_i, acting in a common-gate configuration, transfers the winner or maximum current from a low-impedance to a high-impedance node, thus avoiding loading errors at the output node, with no need of additional cascode or regulated output stages as used in [14].

The algorithm implemented by this circuit to calculate the maximum input current is:

$$I_o = A \, \Sigma_i \, (I_i \ominus I_o) \tag{4}$$

This can be seen if the circuit is considered as the connection of improved Wilson current mirrors that share their output diode-connected transistor. According to the improved Wilson-mirror's schematic shown in Figure 4b, a small signal analysis leads to:

$$i_o = g_{mT} r_{dsM} \left(i_{in} - \frac{g_{mM}}{g_{mM'}} i_o \right) \tag{5}$$

where transistor output conductances, $(r_{ds})^{-1}$, have been neglected with respect to transistor transconductances, g_m.

Comparing (4) and (5), the gain value A, which governs the resolution of the circuit, is then equal to $g_{mT} r_{dsM}$. Improved Wilson current mirrors are connected instead of Wilson mirrors because the latter suffer from DC matching errors due to their asymmetrical biasing [15].

If there is only a maximum input current, only one T_i is conducting, so that the circuit operates like an improved Wilson mirror. Therefore, the output impedance is given by [15]:

$$r_o \cong g_{mM} \cdot r_{dsM} \cdot r_{dsT} \cdot \frac{g_{mT}}{g_{mM'}} \tag{6}$$

When there are *p* maximum input currents, the output impedance is increased approximately by a factor $p^{1/2}$ because *p* transistors T_i are now conducting a current I_{max}/p. The precision of the circuit is slightly reduced in this situation due to the appearance of DC matching errors, however

their contribution, which can be approximated as:

$$\frac{I_{out}}{I_{in}} - 1 \cong -\lambda(V_{GSM'} - V_T)\left(\frac{1}{\sqrt{p}} - 1\right) \tag{7}$$

remains smaller than that of a Wilson mirror, given by [15]:

$$\frac{I_{out}}{I_{in}} - 1 \cong -\lambda V_{GSM'} \tag{8}$$

As to dynamic behavior, the transient response of this circuit (similar to that of an improved Wilson mirror) presents an overshoot with an underdamping coefficient related to g_m/C, where C is the total capacitance at the gate of transistors M_i. The typical trade-off 'speed/precision' of many analog circuits also appears in this case: precision (associated with $g_{mT}r_{dsM}$) is proportional to $1/I^{1/2}$ (transistors operating in saturation), while speed is proportional to $I^{1/2}$.

A 3-input MAX prototype has been integrated in a 2.4-μm CMOS technology (Figure 5). Figure 6a shows its static behavior, obtained by varying two of the input currents while the third current is fixed to zero. Absolute error of less than 1.16% of a full scale current of 30μA is achieved, which means an equivalent precision of 6 bits[1]. Another prototype was integrated with V-to-I and I-to-V converters at the input and output, respectively, thus performing as a voltage-mode MIN operator [16]. As shown in Figure 6b, transient responses of 160ns were measured.

Consequent circuits: According to the Singleton Method, the activation degree of each rule must be scaled by its corresponding consequent. The circuits to implement this scaling are current-mode DAC where the consequent value, c_i, is fixed by digital programming, like the block to generate m in the MFCs. Since these circuits are based on current mirrors, they display no offset, that is, the output current is zero if the input is zero. This is a very good feature because the influence of offset errors in the fuzzy controller output may be a source of troubles.

Divider: The numerator and denominator of Equation (1) are represented by currents. However, a voltage-mode controller output is preferable to enable simple interface with conventional control circuitry. For this reason, the transresistance amplifier in Figure 7 has been selected. It converts the difference of input currents into voltage through a voltage-controlled resistance made of four matched transistors biased in triode region. Its transfer characteristics are:

$$V_o = V_1 - V_2 = \frac{I_a - I_b}{\beta(V_a - V_b)} \tag{9}$$

where β is the transconductance of MOS transistors.

The four-transistor cell has been widely used in the literature [17-19]. It cancels the nonlinearities of MOS transistors and the dependence on the transistor threshold voltage, which only influences the output dynamic range, given by:

$$\max(V_1, V_2) \leq \min(V_a - V_T, V_b - V_T) \tag{10}$$

Mobility reduction is the dominant second-order effect in the transistors of the resistance. It causes both harmonic distortion and increased transresistance. Other second-order effects are the

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1. Equivalent_bits $\leq \log_2$ (full_scale_value / absolute_error).

amplifier nonidealities, such as input voltage offset, V_{os}, and finite gain, A. Including these effects in Equation (9) and retaining only the first-order terms of θ (the mobility degradation parameter), it follows that:

$$V_o = \frac{A}{A + \frac{1}{f}} \cdot \left\{ \frac{I_a - I_b}{\beta(V_a - V_b)} \cdot \left[1 + \theta\left(V_a + V_b - v - 2V_T - \frac{V_1 + V_2}{2}\right) \right] + \frac{V_{os} - \frac{V_2}{A}}{f} \right\} \quad (11)$$

where v is the voltage at the input of the amplifier and 1/f is the closed-loop voltage gain, given by $(V_a + V_b - 2v - 2V_T)/(V_a - V_b)$.

Regarding frequency behavior, the divider circuit dynamics are governed by the amplifier, since the four-transistor cell is self-compensated to MOS parasitics [17-18]. Considering a dominant-pole model for the amplifier, that is A=GB/s, where GB stands for the gain-bandwidth product, the dominant pole of this divider is:

$$s_p = -GB \cdot \frac{V_a - V_b}{V_a + V_b - 2v - 2V_T} = -GB \cdot f \quad (12)$$

so V_a must be greater than V_b to achieve stability.

The circuit in Figure 7 has been used by some authors to implement a voltage-input voltage-output divider [18-19]. Since the aim of this application is a current-input voltage-output divider, an I-to-V converter is added so that $V_a - V_b$ is obtained from a difference of currents, $I_c - I_d$. The CMOS structure in Figure 8 has been used, obtaining:

$$V_o = \frac{\beta'(v_2 - v_1)}{\beta} \cdot \frac{I_a - I_b}{I_c - I_d} = k_d \cdot \frac{I_{num}}{I_{den}} \quad (13)$$

where β' is the equivalent transconductance of the CMOS pair [20].

A prototype of this current-input voltage-output divider has been integrated in a 2.4-μm CMOS technology, with a two-stage single-ended Miller opamp. The total active area is 0.0497mm^2. It is shown in the microphotograph of Figure 9. Figure 10a shows the experimental V_o-I_{den} curves obtained with I_{num} as a parameter. The two-quadrant behavior results from the bipolar nature of I_{num} that ranges from -20μA to 20μA. Figure 10b shows experimental V_o-I_a curves, where I_b is fixed to 10μA and I_{den} ranges from 10μA to 60μA. The nonlinearity of these curves is less than 1% for an output voltage range of 2v with a 5-v power supply. Figure 11 shows the absolute error resulting from the difference between experimental and theoretical values, the latter being calculated with k_d adjusted to experimental results. This infers that for a full scale output of 2 volts, 4 decades for I_{num} (from -20μA to 20μA), and 3 decades for I_{den} (from 20μA to 50μA), an equivalent precision of 6 bits is achieved. Within this range of operation, the step response to changes in I_{num} and I_{den} (with a 5-pF load at the output node) is less than 200ns.

IV.- Fuzzy controller design.

The previously described circuits are input-output compatible blocks that can be connected following a selected architecture. The number of bits to program the MFCs' and CONSs' parameters must be known to choose the corresponding DACs. Precision and speed requirements of the

MFCs and MAX circuits must be considered to choose the geometries of their constituent transistors. The divider circuit requires more careful design. Equations (9) to (13) relate the different variables of the design space: ranges of V_o, I_{num}, and V_a-V_b (related in turn to the range of I_{den} and transresistance of the I-V converter), and values of β, V_2 (a bias voltage), A, GB, and V_{os}. An important issue in this design is the selection of an adequate opamp.

Many analog implementations associate MFCs and CONSs to each rule [3, 4, 14], with the drawback of possibly repeating blocks in different rules. Another solution is that all the rules share the MFCs, which is preferable when the number of rules is large compared to the number of antecedents' fuzzy sets. Figure 12 illustrates the resulting matrix-like architecture of a two-input fuzzy controller that implements the complete fuzzy rule set. This figure shows the MFCs completely connected by MIN/MAX circuits and the digital bus to easily program the antecedent parameters. Regarding the output space, sharing CONSs is also advantageous when the number of rules is large compared with the number of singleton values. In this case, the switches in the lower part of Figure 12 are programmed to conduct the values h_i (represented by currents) to the input of their associated CONS.

Following this architecture, a two-input one-output rule chip has been integrated in a 2.4-μm CMOS technology (Figure 13). Its analog core, which occupies 0.90 x 1.05 mm^2, contains six MFCs and three CONSs to generate the fuzzy labels that cover the discourse universe of input and output variables, and nine MAX circuits to implement the complete rule set (nine rules). Digital words to program antecedent and consequent parameters have 8 and 4 bits respectively, while the rule set is fixed to the typical arrangement depicted in Figure 14. The output signals provided by this rule chip (the numerator and denominator currents of Equation (1)) have a transient response to a step input voltage of less than 300ns, as shown in Figure 15 (a low resistive load was connected at the output). To illustrate the behavior of a whole controller, the rule chip was combined with the divider chip of Figure 9 and the parameters that define the antecedents and consequents were changed to obtain different control surfaces. Figure 16 illustrates several ways of covering the input variables with three fuzzy labels and Figure 17 shows measured control surfaces that basically depend on how these labels overlap each other. If the divider is included in the same chip, simulations predict a computation time for the controller of about 500ns.

V.-   Conclusions.

The behavior of current-mode circuits to implement singleton fuzzy controllers has been analyzed and confirmed with the experimental results of prototypes integrated in different CMOS technologies. The combination of these blocks following an efficient architecture results in small-area and low-power singleton fuzzy controllers with an equivalent precision of 6 bits and inference speed in the range of 2 MFLIPS. The internal processing is carried out in current-mode but input and output signals are represented by voltages to ease communication with conventional circuitry. The use of mixed-signal techniques allows flexible controllers that can be adapted to solve different control tasks via a digital programming interface. Measurements from the combination of a rule chip with a divider chip illustrate this issue.

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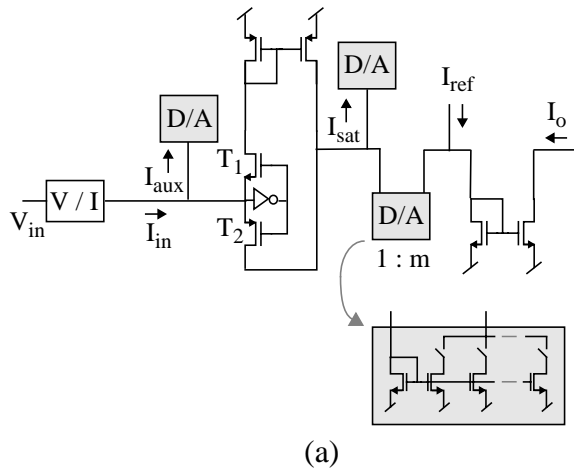
(a)
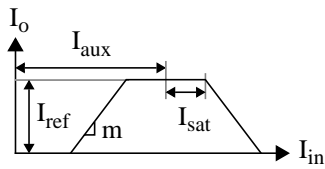
(b)

Fig 1: (a) Schematic of a programmable MFC. (b) Parameters to define a generic trapezoid.
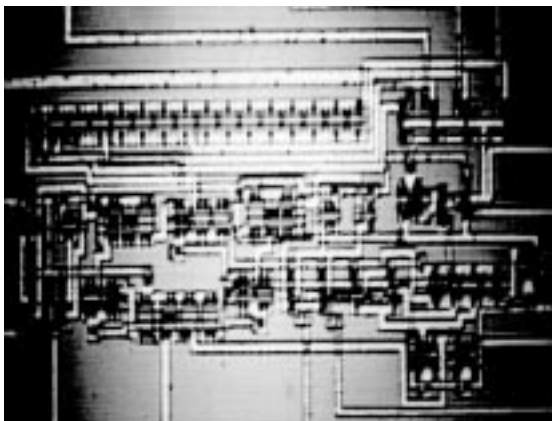
Fig 2: Die photograph of an 8-bit program-mable MFC.

****** GRAPHICS PLOT ******

I_o (µA) CURSOR (3.638pA, 14.98µA)
MARKER (6.000µA, 17.45pA)

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-2.50E+00	-401E-03	6.0E-06	15.0E-06
LINE2				

(a)

****** GRAPHICS PLOT ******
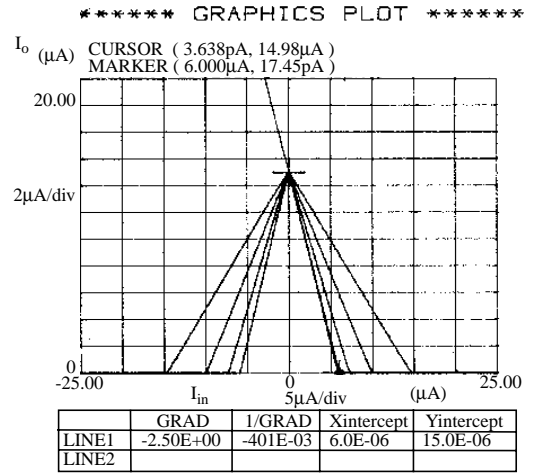
I_o (µA)
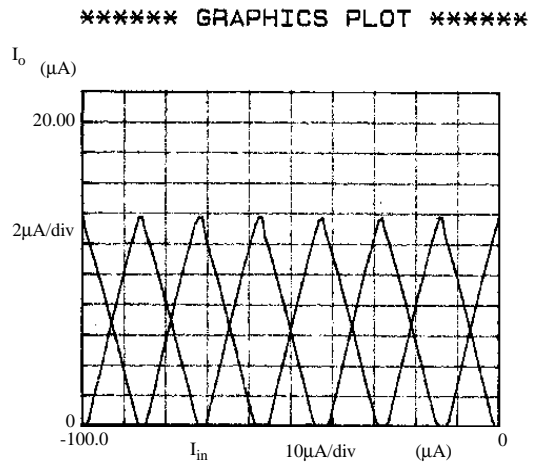
(b)

Fig 3: Experimental results of the MFC prototype: (a) When varying the 2-bit word that programs the slope. (b) When varying the 4-bit word that programs the central point, I_{aux}.
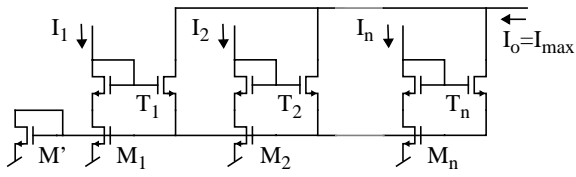
(a)
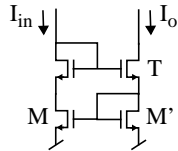
(b)

Fig 4: (a) Schematic of a multi-input MAX circuit. (b) Schematic of an improved Wilson current mirror.
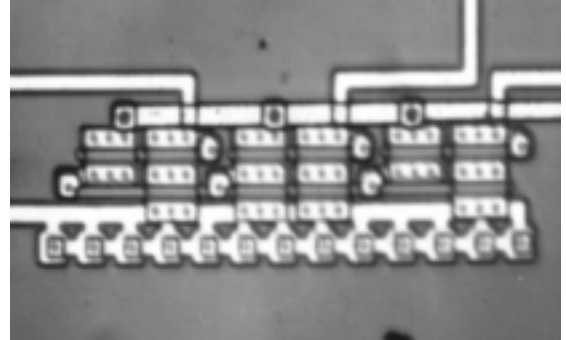
Fig 5: Die photograph of a 3-input MAX circuit.
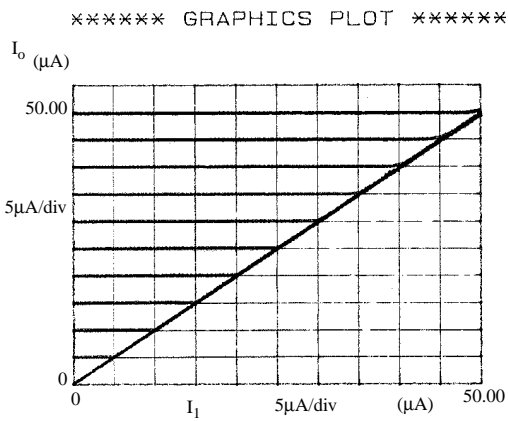
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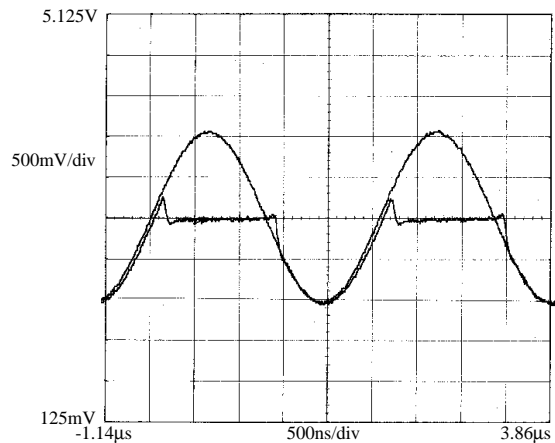
(b)

Fig 6: Experimental results of the MAX/MIN prototypes: (a) MAX static behavior. (b) MIN dynamic behavior.

13
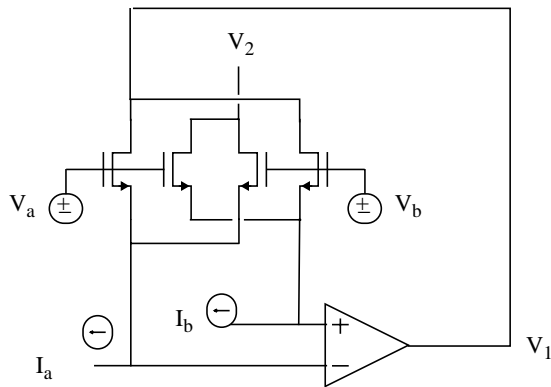
Fig 7: Schematic of a transresistance amplifier.
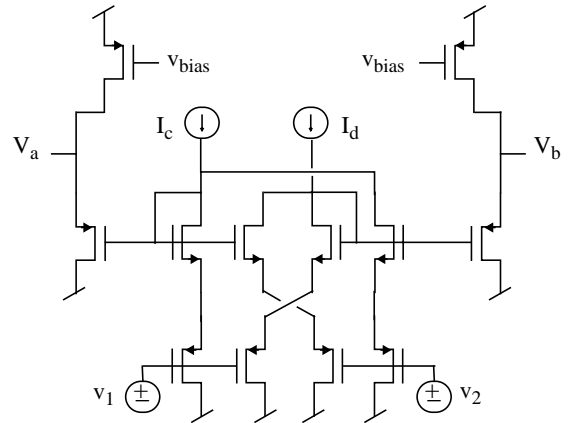
Fig 8: Schematic of the I-to-V converter used.
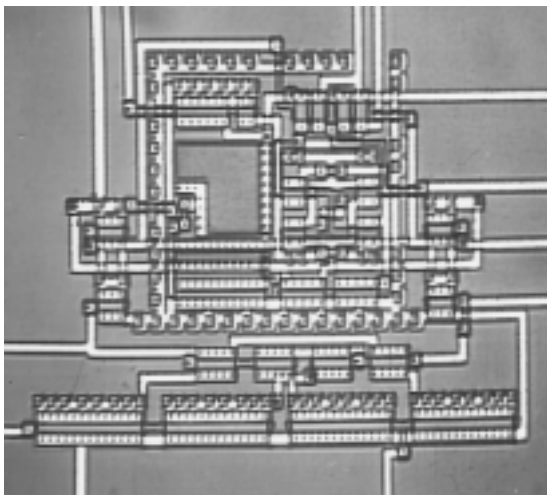
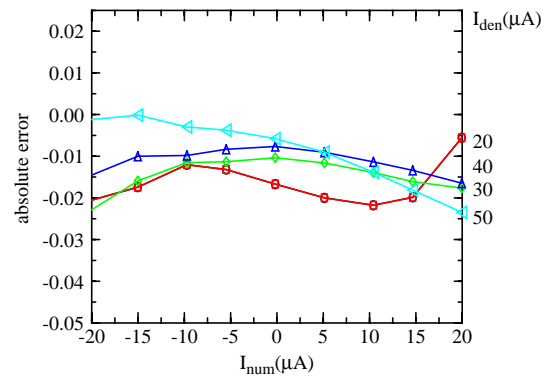Fig 9: Microphotograph of a current-input voltage-output divider.

Fig 11: Absolute error in the divider prototype.

14

(a)   (b)
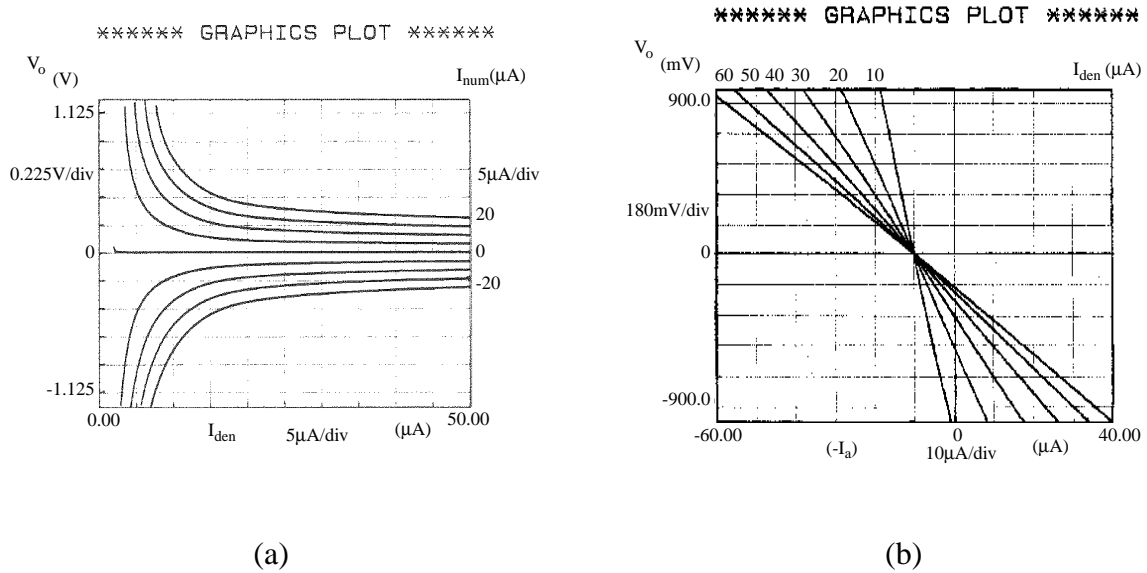
Fig 10: Experimental results of the divider: (a) V_o-I_{den} curves with I_{num} as a parameter. (b) V_o-I_a curves with I_{den} as a parameter.
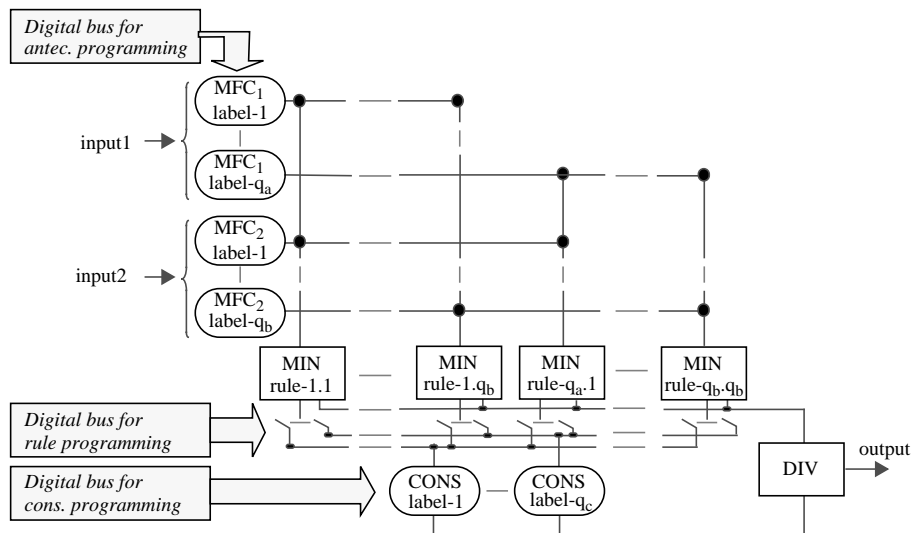

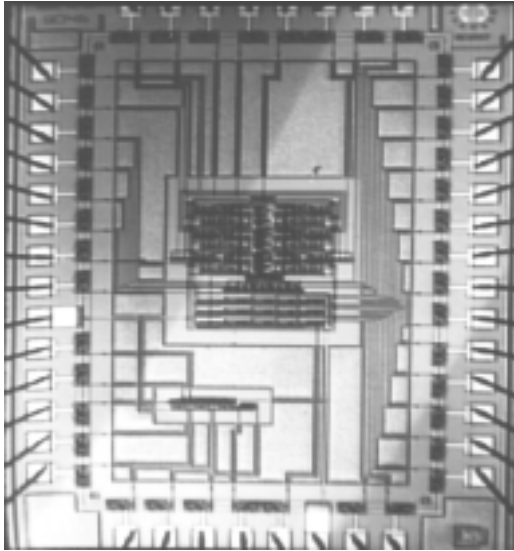Fig. 12: Matrix-like architecture with rule and membership functions programmability.

Fig 13: Microphotograph of the rule chip.

y \ x	N	Z	P
N	P	P	Z
Z	P	Z	N
P	Z	N	N

Fig 14: Rule set implemented in the rule chip. P, Z, and N represent programmable fuzzy or singleton labels.
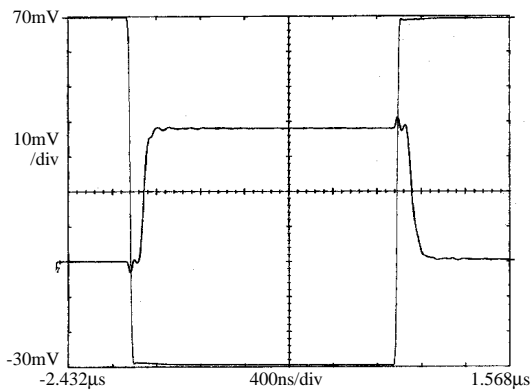

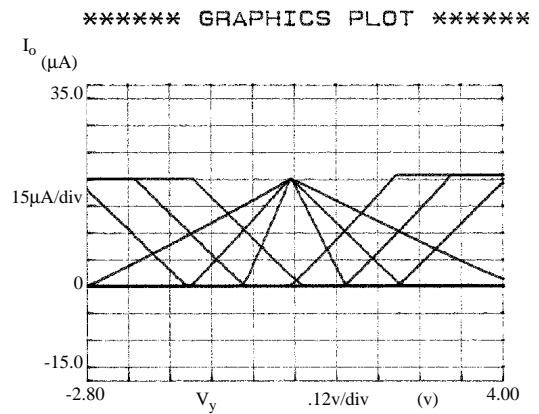Fig 15: Pulse response of the rule chip.

Fig 16: Experimental results showing the programmability of the input fuzzy labels.
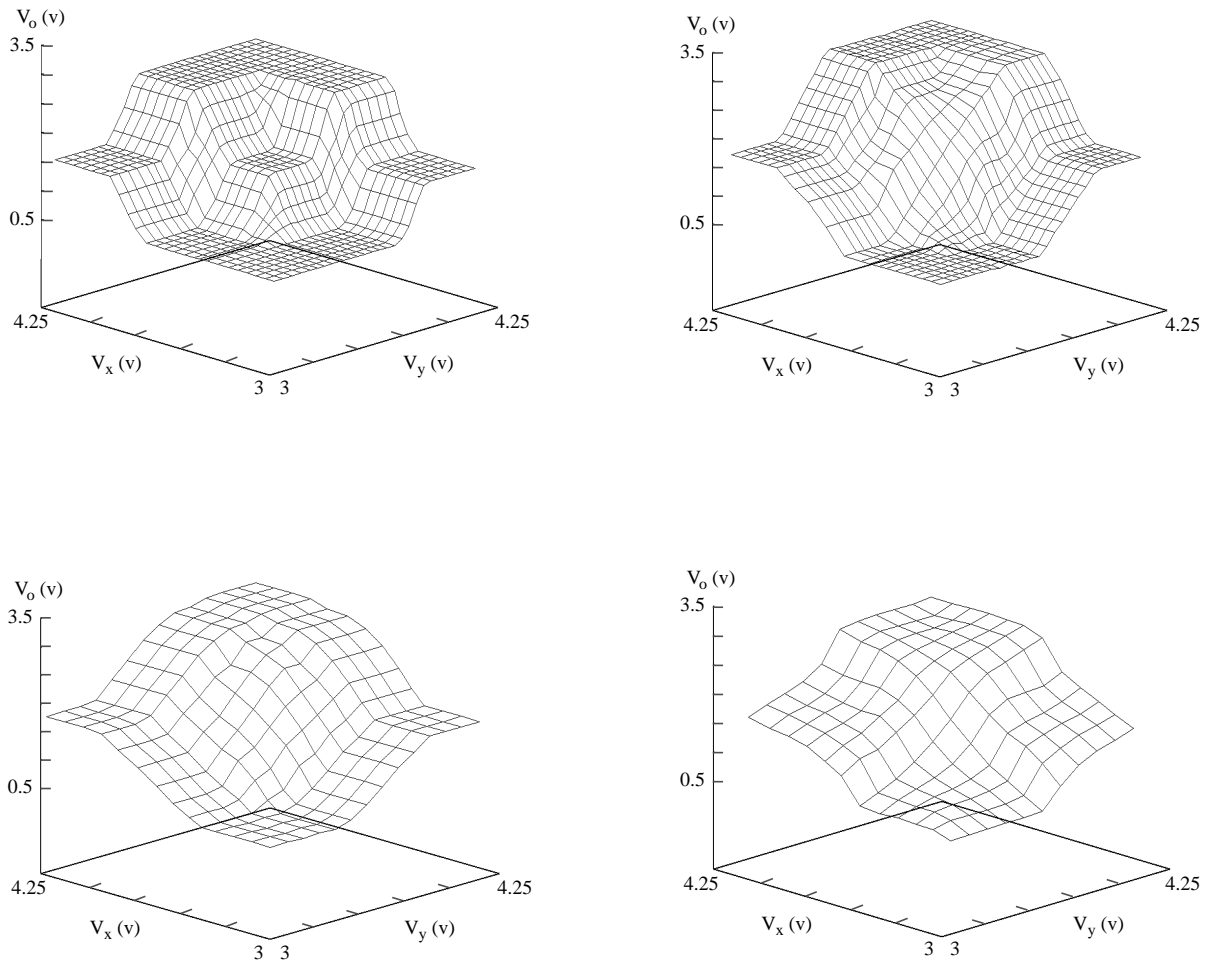
Fig 17: Experimental control surfaces corresponding to different sets of programmable parameters.