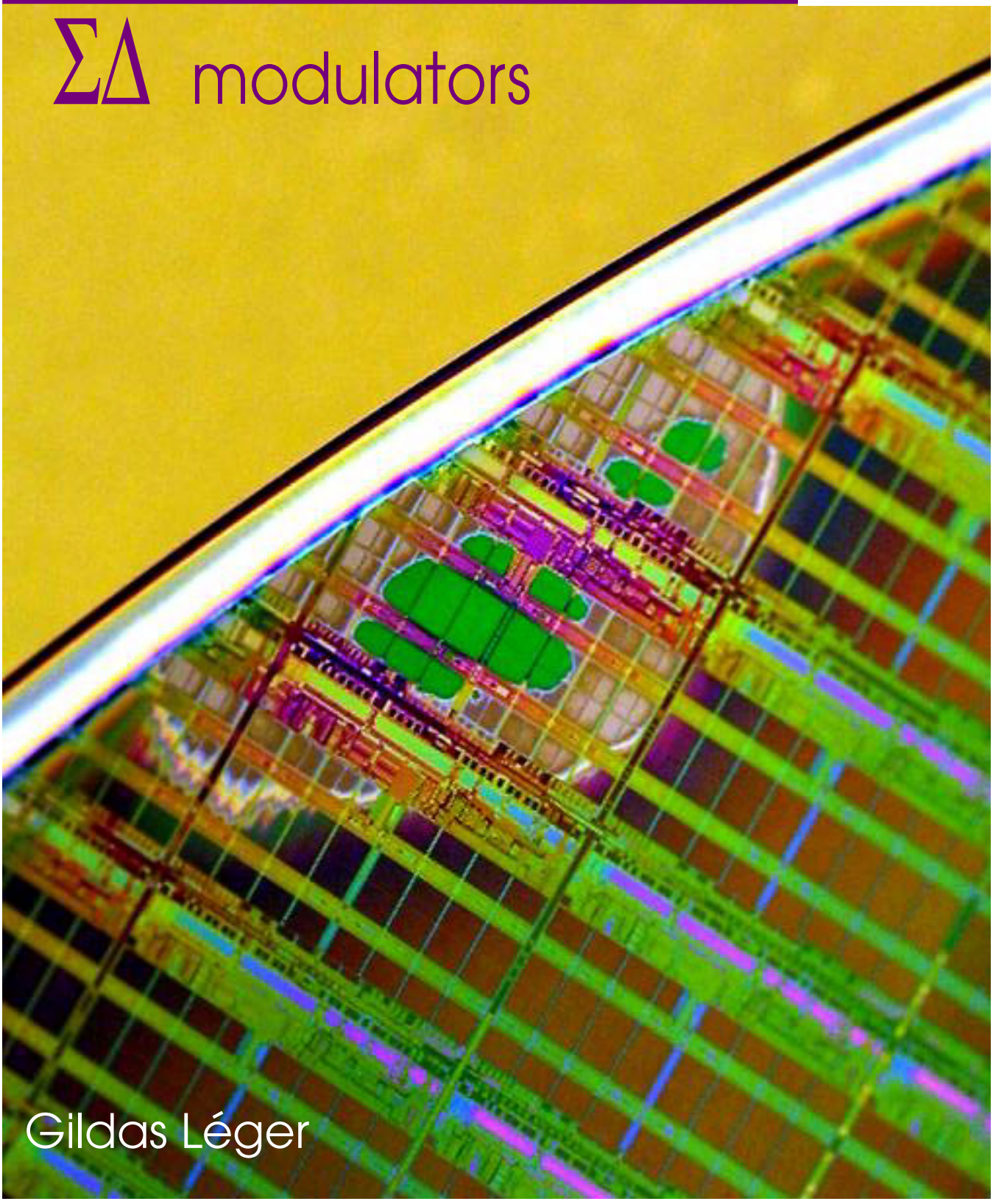
Digital Tests for $\Sigma\Delta$ modulators



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Tests digitales para moduladores Sigma-Delta

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Digital tests for ΣΔ modulators

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A ma famille, tout simplement

Susana

María

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“Le moyen d’ennuyer est de vouloir tout dire”

Voltaire

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Introduction

GENERAL THOUGHTS ON TEST

Today, we, in the first world, are surrounded by an incredible number of integrated circuits. They fulfil many different tasks and there is no industrial sector that can remain free of electronics. As an example, we could cite a well-known sports brand that has introduced a running shoe with a microprocessor that calculates the exact amount shock absorption that the runner needs.

This tremendous development relies on a law that everybody among the electronics players have struggled to maintain: Moore's Law [1]. However, the cost that has to be paid to follow this geometric evolution is increasing at a rate that is not sustainable. That is in part due to the fact that integrated circuits have to be sold at a reasonable price point. And consequently, their production costs have to remain bounded. Nevertheless, the ever increasing complexity of ICs has brought a component of the production costs to a bottleneck. This cost component is circuit test.

I • 1 TWO TEST PHILOSOPHIES

The tremendous expansion of electronics is undoubtedly a fruit of our consumption society where the principal goal of industries is to compete to offer more for less money. In other words: the customer rules. This is also true in the field of IC test, which is somewhat driven by end-user considerations. When you buy something, you want some guarantee that the product will fulfil your need. Translated to the IC test world, the customer has chosen a given IC on the basis of a datasheet and he wants the specifications to be guaranteed. That is what sets the basis of functional testing: what you sell is what you test. At first sight it seems logical to think that the best way to guarantee the specifications is by measuring them.

Nevertheless, we should take into account that the only physical reality is the chip. This small piece of silicon has been crafted according to a given layout and its functionality is guaranteed within the normal variations of the fabrication process. A defect is whatever makes the physical chip go out of the box of the normal process variation. Such a defect can cause a permanent failure in the circuit (like an open or a short), be totally harmless (like a dot of extra metal in a clear part of the layout), or even express itself during the useful life of the circuit (like an oxide pinhole causing an oxide breakdown). From this last consideration the concept of defect-oriented testing has been born. The goal of such testing is to ensure that the IC is defect-free. Provided that a defect-free chip is within the normal process variations, the design specifications are guaranteed by-design. The main drawback of this philosophy is that it is very difficult to ensure that a circuit is defect-free. Actually, it is almost impossible to search for and detect any possible physical defect. Hence, what is actually detected by defect-oriented tests are not the physical defects present on the chip but their local expression at circuit level: in other words the faults that they cause. Historically, test has been considered mainly as a manufacturing issue. In this context, particle contamination during the fabrication process is the main source of defect. The interaction of these particles at the different process steps usually leads to spots of additional or missing material. At circuit level, these spots are likely to cause either opens or shorts. As a results, the spot defects that can have an impact on circuit functionality are those that modify the topology of the circuit either by shorting two node or by opening a conductive path.

Technological progress cannot be stopped and circuits are nowadays fabricated at the 65nm node. For such a deep-submicron process, considering only contamination-related spot defects and shorts or opens is not sufficient anymore, even for digital circuits. Nevertheless, the quasi-monopoly of spot defects for manufacturing concerns has led to two important consequences: i) the defect-oriented tests are often called structural tests has they target defects that are supposed to alter the circuit topology, ii) opens or shorts have been gathered into stuck-at (one or zero) and stuck-open faults models that aim to represent their effects on digital gates. Ideally, defect-oriented test should be associated to a level of confidence, a defect-coverage that would give a measure of how many defects a given test can detect. However, such a metric is not possible to extract so simpler one is used: the fault-coverage. For digital circuits, as the considered faults are often limited to stuck-at and stuck-open, fault coverage can be evaluated.

For digital ICs, structural test techniques have been adopted widely by the industry for three main reasons. One of them is that tools are available to evaluate the fault-coverage of the different structural tests. Another powerful reason is that there is just no alternative: the functionality of today complex digital systems is so wide that it is impossible to make an exhaustive validation. It would take too much time to test all the possible combinations and sequences in sequential circuits, and time is a key parameter in a production line. The cost of test is directly proportional to test time and is not mitigated by high volumes as could be the cost of test instrumentation. The last reason is that some generic and reusable structural test techniques exist. Automatic Test Pattern Generators (ATPGs) are able, as the name indicates, to generate automatically a number of input sequences (the test patterns) that maximize the detection of stuck-at faults in a circuit. In order to improve the accessibility and observability of digital circuits, that is inherently limited to the number of pads, the so-called boundary –scan technique has been introduced and formalized in the IEEE 1149.1 test bus [2]. At last, Built-In Self-Test (BIST) techniques are also available that integrate the resources required to test a circuit on the same chip. Ideally, the chip only requires a control signal to start the test and outputs a pass/fail decision.

On the other hand, the analog and mixed-signal realm has not reached the point where functional test is impossible. The reason for this is that the difficulty of analog test is not driven by functional complexity but by performance [3]. While it is possible to manufacture

industrial test equipment of higher performance than the circuit under test, functional test will be the preferred solution for the industry. It was said at the ITC [5] that, for a defect-oriented test to succeed in a production environment, it should:

- Enable testing mixed-signal circuits blocks or ICs in parallel, and provide test time savings greater than the extra silicon cost, or
- Enable use of a lower-cost tester whose capital and/or operating cost savings are greater than the extra silicon cost (if the whole chip can be tested on the tester), or
- Enable testing a performance that is otherwise untestable, and which must be tested.

As was said above, what is sold to the customer is a piece of silicon and a datasheet. What the customer wants is that the datasheet specifications are fulfilled. A conceptual hitch in this thought is that the functional measurements are realized at a given instant while the specifications have to be guaranteed over time. If reliability tests are performed (like burn-in tests), some confidence can be gained that the circuit should work properly during a given period. But this is just a matter of probability and in-field failure can still occur. It seems natural and intuitive to associate a 100% confidence to a functional test, but this is erroneous: A circuit that fulfils all the datasheet specifications may still present a defect.

Although the SIA roadmap has already pointed out that these systems will face serious test problems, industry is still reluctant to adopt defect-oriented test solutions. As was said above, this is because functional testing is still possible in many cases and the customer is more comfortable with that. Despite the intents to extend digital test bus capabilities to analog [6,7], there are still no re-usable analog test techniques whose defect-coverage can be easily evaluated. Actually test quality evaluation is a cornerstone to the move toward defect-oriented test.

I • 2 THE DIFFERENT TEST NEEDS

It is not a trivial task to determine the test needs of ΣΔ converters. Indeed, these circuits appear in a wide variety of applications each of which puts the emphasis on a particular aspect.

The principle of operation of ΣΔ converters consists of trading signal bandwidth for resolution. As a consequence, it was first applied to the low-frequency/high resolution segment

of the ADC market. This segment includes applications like geophysics and seismology measurements, where resolutions as high as 24bits can be found for signals below 2Hz, and also DC instrumentation. Then sigma-delta converters extended to the audio range (up to 44kHz for music CD) and will surely be the preferred solution for the audio DVD standard.

In order to benefit from technology scaling, the industry has been pushing this digital-friendly conversion type. That is why ΣΔ converters can now be found in communication applications like ADSL or ADSL+ and research is even underway to extend ΣΔ modulation capability to radio-frequency front-ends. In addition, simple sigma-delta converters are also being considered as a good candidate for Analogue Response Extractors in Mixed-Signal Design-for-Testability (DfT) schemes [8]. Several DfT schemes have been proposed in the last few years that involved ΣΔ converters [9]. Nevertheless, in [10], Cheng pointed that such embedded DfT modulators should also be tested in order to guarantee the validity of the extraction.

I • 2 . 1 Test across circuit life-cycle

Despite the fact that test needs are application-specific they can still be described similarly across the circuit life cycle [4]. This life cycle is depicted in Figure I-1

- Design.

  Though it is far from being a systematic industrial practice, test experts claim that it is of utmost importance to consider Circuit testing in early phases of the design. That does not necessarily mean that special DfT features will be introduced in the design. Rather, because the designer gains a deep knowledge of the circuit during the design phase, he is probably the most skilled to know how the circuit should be tested. Indeed, for validation purposes, he will have to set a simulation test bench up. This information may be of interest for further exploitation. The introduction of DfT in the circuit also represents some extra design effort. Nevertheless, the cost associated with this effort may be reduced via systematic (reusable) approaches.

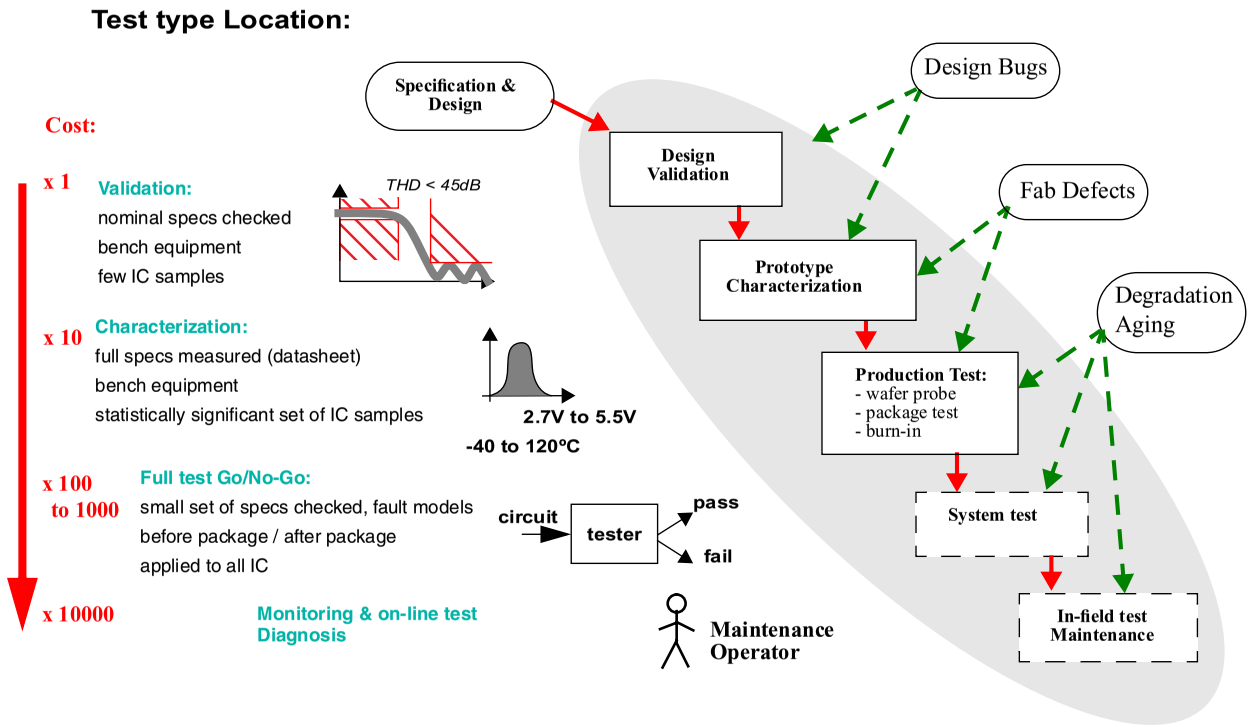


Figure I-1: Test needs across the circuit life

- Prototyping / first silicon validation.

  Once the design has been accepted, a first prototype is fabricated and a small number of samples is submitted to exhaustive characterization. The goal is to validate the design; here, the complexity and test time is not a major concern. The most important thing at this stage is to guarantee that the design fulfils all the specifications for any process within the normal variability. Hence, DfT may not have so much impact at this point. Nevertheless, if DfT enables extra diagnosis capability, it may help debugging the design and proposing new solutions.

- Wafer probe / burn-in

  After the necessary redesign cycles, the circuit is sent to production, and circuit test costs are focused on volume concerns. The first production test is known as wafer-probe. The recently fabricated wafer is introduced in a handler and interfaced to an ATE via a probe card. The circuits on the wafer are contacted, usually using bed of nails fixtures. More concretely, needles contact on the circuit pads. At this stage, it is very important to keep the test time as low as possible, as it will limit the production line throughput. Moreover, wafer-probe intends to detect the major number of defective parts before packaging. Indeed, the packaging operation represents an important cost. Hence, wafer probe allows one to save the money related to the packaging of defective parts. Nevertheless, circuit testing at this stage is quite limited due to the parasitics introduced by the probe. For instance, at-speed testing is difficult to implement, which limits the test coverage. Hence, DfT schemes focus on improving test time or test coverage.

- Package test

  Once the circuits are within the package, their handling is easier and they can also be tested in conditions closer to their final operation. In particular, extra circuitry can easily be included on the test board close to the pins. This test can thus detect the defective parts that were not detected during wafer probe, but also the parts which have been damaged by packaging. Anyway, the concerns are the same as for wafer probe test, in terms of test time and test coverage.

Nevertheless, the type of product will greatly influence the package test. Indeed, a sigma-delta modulator can be integrated as a standalone part and all its inputs and outputs are available. However, the modulator may be integrated together with its corresponding decimation filter, such that the modulator bit stream is not available and the high frequency noise shaping cannot be studied directly. The limitations are even worse for product types that have been gaining much interest in the last few years such as System-on-Chip (SoC) and System-in-Package (SiP). In these cases, a complex system is integrated on a single die for the former and on several dies but in a single package for the latter. In the case of a modulator, it could be integrated, for instance, together with a sensor, a decimation filter, a complex DSP, and some memory. In that case, DfT is mandatory as it becomes very difficult to check exhaustively the functionality of the system (just like for digital systems) and neither the modulator inputs nor outputs are available.

- Burn in

  In order to ensure the quality of the device, a burn-in test is performed. The reliability of a circuit can be compromised by defects that cannot be detected under normal test conditions. For example, a defect could stretch a metal line without causing an open. Nevertheless, electromigration may cause an open at that point during the circuit life. Burn-in test consists of putting the circuit under conditions that tend to accelerate the expression of latent defects. Normally, the circuit is operated at a temperature and polarization above the maximum specified. Normally, reliability defects are associated with an activation energy, and increasing the operating temperature is equivalent to accelerate the aging of the circuit.

- System test

  Finally, when the circuit is introduced into a complex system, the components of the system are likely to be tested. At a minimum, the system functionality is verified, which implicitly comprises the components functionality. Any DfT feature at component level that could ensure proper operation and help diagnosis would be very valuable. Indeed, system assembly may have caused some components to fail. This

is the last test step before the product is shipped to the customer so it is of interest to be able to repair the system by replacing defective components.

- In-field test

  In some cases, where a circuit failure could have disastrous consequences, in-field test could be valuable. Application fields such as automotive, spatial applications, medical instrumentation or oilfield prospecting are possible candidates. In-field testing is usually very difficult to perform, as the required test resources are usually neither available in the field of operation, nor possible to implement within the system. Hence, in a majority of cases, only a clever DfT strategy could enable in-field testing. Notice that two important categories have to be distinguished. The first one gathers the strategies that allow one to test the circuit when it is idle, for example at powering-up. The second one gathers the solutions that enable concurrent testing which consists of performing the test without stopping the circuit's normal operation. These solutions are much more difficult to find and usually much less affordable than the first ones. Indeed, they are likely to imply some kind of redundancy and may have an important impact on area, performance and/or power consumption.

- Maintenance

  Maintenance is a different problem to that of in-field testing. Indeed, test resources are normally available but the key objective is to diagnose which part of the system is failing and not only to detect the failure. For complex systems involving a great number of components and even different technologies (electronics, optics, MEMS, sensors …) this task could become very tricky. Hence, DfT could bring an important added value to system debugging. To an ideal extent, every components could be made self-testable and system diagnosis would only consist of reading the failure flags sent by the components. Maintenance and diagnosis is of utmost importance in automotive applications, as cost is a great concern and total system replacement may not be affordable.

Ideally, for a given application, a test cost function should be built, taking into account all of the aspects described above. For instance, a very stringent test may detect almost all defective parts at the expense of also rejecting some of the good parts. For an application with relatively low volume but with strong quality and reliability requirements, this could be affordable. Indeed, the cost of the consequences of a defective part shipped as a good part may outweight the cost of the test-related yield loss. The latter cost can easily be calculated, but the former cost includes several concepts that are difficult to describe accurately and may be more related to the company business model than to simple production aspects: maintenance cost, replacement cost, and also impact on the company image, relation with the yield learning curve (process quality), etc. It is obviously not the same to manufacture a chip for a communication satellite application as for a low cost toy.

I • 2 . 2 Enhancing testability

Four parameters can be considered as critical across the different test points:

- test time
- test coverage
- cost of external resources
- limited access to circuit nodes (including in some cases the primary input and output)

The International Technology Roadmap for Semiconductors [11] urges that Design-for-Testability (DfT) for Analog and Mixed-Signal circuits be investigated to overcome these shortcomings. Some research areas are sketched:

- Increase accessibility and observability: structured methodology should be provided to input a test stimulus at internal points of the circuit and/or to monitor a given node. The main objective is to circumvent the SoC specific issues, where even the inputs and outputs of a circuit are not directly accessible. But the same structures could be used to access internal circuit nodes and develop new test methodologies with the purpose of improving test time and/or test coverage. The IEEE 1149.4 ana-

log test bus standard goes in this direction, though much work is still necessary to meet the AMS test needs.

- Shift part of the characterization equipment on-chip: this would relax the tester and tester interface requirements, and standard characterization test methodologies could be used. Nevertheless, in many cases it would be too expensive to implement high quality instrumentation on-chip. Thus, clever solutions also have to be found to relax the test signal requirements.
- Develop BIST: Built-In Self-Test methods are also a recommended way to tackle most of the issues specified in the previous paragraph. An ideal BIST method does not require any external resources apart from control signals and power supplies. In other words, test stimulus generation, data acquisition, signature calculation and even test interpretation can be performed on-chip. The most direct benefit of such an approach is the reduced external resource requirements. Actually, ITRS states that circuits with BIST facilities may be tested on specialized DfT testers, that only have to provide clocking, power supply and low (medium)-speed I/O. An additional benefit is the potential reduction in test time. Despite the fact that the circuit test time is determined mainly by the measurements performed, the implementation of BIST methods may enable massively parallel testing, improving the test chain throughput dramatically. Finally, BIST schemes have to be contemplated in early phases of the product design, which enables original test methodologies (functional or structural) which can further reduce test time or improve test coverage.

The ITRS is focused primarily on cost issues related to IC manufacturing, and the issues and sketched solutions concern production tests. Nevertheless, DfT can also be seen as an added value for the end user in the large variety of application where reliability monitoring is of interest.

I • 2 . 3 Two specific topics

The research of alternatives to functional circuit testing has been motivated primarily by the explosion of manufacturing test costs for digital ICs. Indeed, a functional test has to verify exhaustively all the circuit functionality and that takes a long time. As all the fabricated ICs havw to be tested, test time becomes the limiting factor on the production line. As an example, a combinational circuit with N inputs should be tested for 2^N combinations. For a circuit with 100 inputs it would take about $4x10^{12}$ years to perform an exhaustive test at 10 GHz. Needless to say, the case of sequential circuits is even worse. As the cost of testing complex circuits become significant, much research effort has been focused on reducing test time while minimizing test escapes. From a manufacturing viewpoint, test is also necessary to avoid customer returns. Customer returns represent an elevated cost as it usually involves the cost of part replacement, the cost of repair, the cost of the damages the failure may have caused, and also the not-so-direct impact on company image. The earlier a defect can be detected in the circuit fabrication process, the more money is saved. For instance, if a defect is detected at wafer-probe level, the test saves the cost of packaging this defective circuit.Nevertheless, test should not be restricted to the manufacturing concern. There are situations where test suffers other kind of limitations that it would be interesting to address.

I • 2 . 3 . 1 Harsh environment applications

The testability needs for harsh environment circuits are different from production needs: the testability features represent an added value for the application and thus for the end customer, and the defects that are targeted are not (or at least not only) those that appear during manufacturing but those that are due to environmentally-driven failure mechanisms.

The circuit is readily in the hands of the end-customer and the new focus of test is no longer to avoid customer returns but to provide added-value. Money can be saved by minimizing the impact of a defect occurring in the field of operation. Indeed, if a failure is detected early, this enables a quick reaction; fault location, at least at system level, facilitates maintenance and repair.

In harsh environment applications, circuits are generally not accessible and it is thus highly unlikely that an operator can realize any test on the system in its field of operation.

Furthermore, the lack of accessibility and observability of circuit inputs and outputs along with the eventual limitation of communication channels is also a strong drawback to remote testing. In that context, DfT solutions could be of interest, in particular to detect those parametric faults that affect the validity of the system output but cannot be diagnosed externally.

A very appealing DfT solution for these applications is Built-In Self-Test (BIST), which could potentially enable periodic testing of the device in the field. This obviously lacks the possibility of detecting transient events occurring during normal operation from which the circuit recovers but offers the potential of being much more efficient in terms of fault coverage, area, power and robustness than concurrent-test solutions.

For analog circuits, a functional full-BIST would be very valuable as it provides an easy interpretation. Moreover, as functional parameters are estimated, such a BIST scheme could set the pass-fail limit to the absolute minimum requirements of the application. The counterpart is that a functional full-BIST requires the implementation of analog test circuitry to provide (analyze) the input (output) signals, and this analog circuitry has to provide performance that is superior to the device under test. This requirement is likely to cripple reliability as the test circuitry could be as sensitive to defects and drifts as the device under test. The reliability of the BIST circuitry is possibly the major concern of any proposal. Extra-area may not be as important as for production-oriented BIST because yield is not an issue. Depending on the application, large test times may also be affordable. Defect-oriented BIST solutions represent an interesting alternative. However, harsh environments are not production environments and the nature of defects is thus not the same in both. The faults caused by these defects may also be different.

A harsh environment can be defined as an environment with parameters that are far from the norm. Some of these environmental parameters are temperature, pressure, contamination, humidity, radiation, vibration, and electrical overstress. All the matter resides in defining what the norm is for these parameters. In the field of electronics, a comfortable definition of a harsh environment could be any environment for which circuit operation has not been qualified. For instance, several temperature ranges are defined for different applications. In principle, a circuit is certified for one of the ranges seen in Table I.

Table I: IC qualification temperature ranges

Circuit class	Minimum temperature	Maximum temperature
commercial	0ºC	70ºC
industrial	-40ºC	85ºC
extended	-40ºC	125ºC
military	-55ºC	125ºC

In petroleum and geothermal wells, the temperature may reach +200 to +300˚C. This can be considered as an even harsher environment than for circuits specified in the military range. Companies dedicated to well logging are thus often obliged to realize their own qualification process for any component that may be used in such applications. Actually the operation of a circuit in a harsh environment can be compared to the operation of a circuit during a reliability test. Indeed, many of these environmental parameters are used as stress vectors in reliability tests.

Harsh environments are thus more likely to cause failure mechanisms that normally correspond to the circuit end-of-life phase [16,17]. ASICs for harsh environment application should be designed with the highest reliability requirements in mind. DfT in a harsh environment context should focus on in-field test capability and target a variety of defects much broader than production tests [16,17,18]. Spot-like defects like opens or shorts in the different material layers can still appear in the field of operation and those production-test techniques that have been developed to detect them still find an application. A well-known failure mechanism that is related to temperature and aging is electromigration. Electromigration can cause both opens and shorts. Similarly, other mechanisms that can cause opens include mechanical stress due to unmatched dilatation coefficients of the different materials and temperature cycling, corrosion, electrostatic discharges causing local melting ... Shorts can be due to a variety of phenomena. Electromigration has been seen as a possible cause but conducting pipes of dopants difused along crystal defects, cracks or pinholes causing “oxide breakdown” (that can be seen as a short between gate and channel in a transistor) are

also candidates. Serious drawbacks can arise if pinholes only debilitate the oxide, as oxide breakdown could occur during the active life of the circuit. Oxide breakdown can also be induced by the environment through an electrostatic discharge or an electrical overstress.

Spot defects that affect circuit topography are likely to have catastrophic consequences. In many cases, it is not even necessary to carry out simulations to assess the effects of a given defect. For instance, an open in the power supply line of the amplifier will set its output to a high impedance. A short between the inputs of a differential integrator will also be catastrophic. However, a short between the gate of a cascode transistor and a supply line in an amplifier may only produce that transistor to settle in its linear region instead of its saturation region. This could change the amplifier output range and DC gain as well as its dynamic characteristics while preserving its function. In that sense, parametric defects, that inherently cause parametric deviations, may have more pernicious effects than catastrophic spot defects. A circuit that does not work at all is easily detected and some very simple tests (like DC tests for instance) could suffice. Parametric drifts, in turn, are likely to cause performance degradation of the device, bringing it out of specification. In that case, it is much more difficult to assess wether the circuit under test is faulty or not.

Temperature variation in itself causes a variation of silicon properties. For instance, a temperature decrease makes the transistors more conductive and thus increases current flow. This can have both positive and negative effects but necessarily influences the performance of the device. Similarly, transistor threshold voltages vary with temperature, as do leakage currents. If a circuit is operated out of the temperature range for which it is specified, the effects could be dramatic.

Dislocations can affect carrier relaxing time and recombining time and mobility. Ionic and electronic superficial conduction over the LOCOS (Local Oxide) can provoke the appearance of unwanted inversion layers. Small ions (as Na^+, Cl^- and K^+) can diffuse rapidly within Si, modifying the charge density and affecting the threshold voltage of the transistors. Oxide breakdown (due, for instance, to an electrostatic discharge) may be only partial and induce a drain-to-source current lower than that predicted. Interstitial states in the interface of silicon with its oxide can trap electrons and holes, inducing a phenomenon known as slow-trapping that results in an increase of $|V_t|$ for an NMOS transistor and in a decrease for a PMOS one. Moreover, these charges are not fixed, and if a low potential is applied to the

transistor gate they can be liberated. This means that such a parametric deviation could be transient and recover with time. It is obviously a critical test issue that only concurrent testing could solve with certainty. A similar phenomenon is secondary slow trapping. The accumulation of positive charge at the source of NMOS transistors, due to the presence of H^+ ions (as function of the process and humidity) effectively lowers the active channel length and thus increases the threshold voltage.

The effect of radiation on CMOS circuits may also cause parametric defects. The interested reader is referred to NASA documentation [19] for more details on these effects. In a rough summary, the effects can be divided in two parts. The first one is related to ionization. As high energy particles impact the device, pairs of electrons and holes are created in the substrate and in the active zones. The electrons usually have high mobility and are quickly swept by electrical fields. That is not the case for holes that may be trapped in silicon/oxide interface defects, just like for the slow-trapping described before. The variation of the threshold voltage will thus depend on the Total Ionization Dose received by the device. Indeed, the effects of ionization are cumulative though some annealing is also possible. The second part is linked to particles that can produce a high number of electron-hole pairs at a time, such as heavy ions for instance. In that case, a transient parasitic current is created that could impact the circuit functionality at the impact instant. For instance, that current could be sufficient to reset a digital latch. These effects are known as Single-Event Effects and are very difficult to detect due to their transient nature.

This kind of defect will thus cause parametric deviations of the circuit either at global or local level that may vary with time. The stuck-at fault model is totally inappropriate to represent the faults associated with these defects [7]. Hence, harsh-environment applications have testability requirements that are quite different from manufacturing ones.

I • 2 . 3 . 2 System-on-Chip

As outlined above, the main factor that has motivated the move from functional test to structural test for digital circuits is the geometric evolution of their complexity. It has also been stated that analog test difficulty is not driven by function complexity but by performance. This last assumption is only partially true. If analog or simple mixed-signal circuits are manufactured as stand-alone parts, the test complexity is reduced. However, there is a

particular case for which analog test difficulty is also driven by circuit complexity; namely the case of Systems-on-Chip (SoC).

Deep-submicron processes have brought the possibility to implement on a single piece of silicon a complete system with several functional cores. These cores can be micro-controllers, memory banks, DSP units and also sensors, analog signal conditioners and data converters. Many Socs are actually mixed-signal parts. This may not represent at first sight a testability issue as one may argue that the different cores can be tested separately. Nevertheless, such a simple sentence is much easier to pronounce than to bring to reality. One consequence of such an approach is that the SoC test is bounded to the highest test requirements among the different cores. For instance, if all the cores can be tested in parallel (which is not necessarily possible), the slowest test is what will determine the SoC test time. Similarly, if there is a high-speed digital core and a high-resolution Analogue-to-Digital converter an ATE with both capabilities would be required. If the different cores have to be tested separately as if they were stand-alone parts, accessibility and observability problems arise. Fortunately, some solutions exist for digital circuits like boundary-scan or digital BIST, but if an embedded analog circuit has to be tested functionally, analog signals have to be carried in some manner to and from the SoC pads. In demanding application of either high-speed or high-resolution this could be difficult to perform. Furthermore, the circuitry (busses, multiplexers, buffers, filters) added for such purpose should not significantly impact yield. In that sense, standard approaches like the IEEE 1149.6 [6,7] test bus do not seem to help much.

Some techniques have been proposed to re-use part of the resources available on a chip. For instance, it would be possible to use the memory and a DSP unit to perform an FFT on the output of an ADC. However, such a re-use approach does not allow the concurrent test of memory, ADC and DSP nor does it provide a solution to the generation and/or interfacing of the test stimulus. Much of the research done to improve the testability of mixed-signal circuits targets BIST solutions. The concept is quite explicit: the objective is to carry out most of the test on-chip, from test signal generation to data analysis. An ideal or full-BIST would require only a digital start signal and output a digital PASS/FAIL signal. Such testability would be ideal for SoC. Indeed, if each core could feature some kind of BIST, a simple 1149.1 test bus [2] could be used to trigger properly the different tests and to recover their outputs.

In that sense, SoC is a domain where analog test cost is not necessarily dominated by test time. As for harsh environment applications, SoC analog test requires a significant research effort to provide test solutions where the classical (functional) ones are not adapted.

I • 3 THE APPROACH IN THIS THESIS

An optimum test solution would be one that retains the main advantages of both traditional approaches while avoiding their main shortcomings. That is, a test solution that could - directly or indirectly - be interpreted as a measurement of the circuit performance but at the same time could detect the greatest number of defects. This, in turn, should be achieved with limited resources.

Design is what relates the circuit structure to its function as seen in Figure I-2. As such, it should be the bridge between functional and structural test. While going through the design flow, downward in the modelling hierarchy, some macro specifications are set, building blocks and their characteristics are defined, architectures are chosen, transistors are dimensioned and finally laid out to determine the physical actions that will bring the chip to reality.

As we have said before, the manufacturing step is what actually defines what the chip will be. Physical defects can only be properly described at the manufacturing level, taking into account material properties. Albeit, inverting the design flow it could be possible to model the defects or their impact on the chip (the faults) at higher hierarchy levels. The lower the level, the more precise the defect modelling, but the harder its study and its testing. At each hierarchy step towards the higher levels, it is likely that the information on test coverage is less and less confident. In turn, more insight is gained into the functionality of the defective chip. Thus, there may be an optimum at which defect modelling can easily be interpreted in terms of functional impact while maintaining good coverage of the realistic defects.

The approach that we defend in this thesis is probably not the optimum but is driven by the above mentioned considerations. It consists of testing, directly or indirectly, the main specifications of the basic building blocks that form the circuits under test. Taking a look at

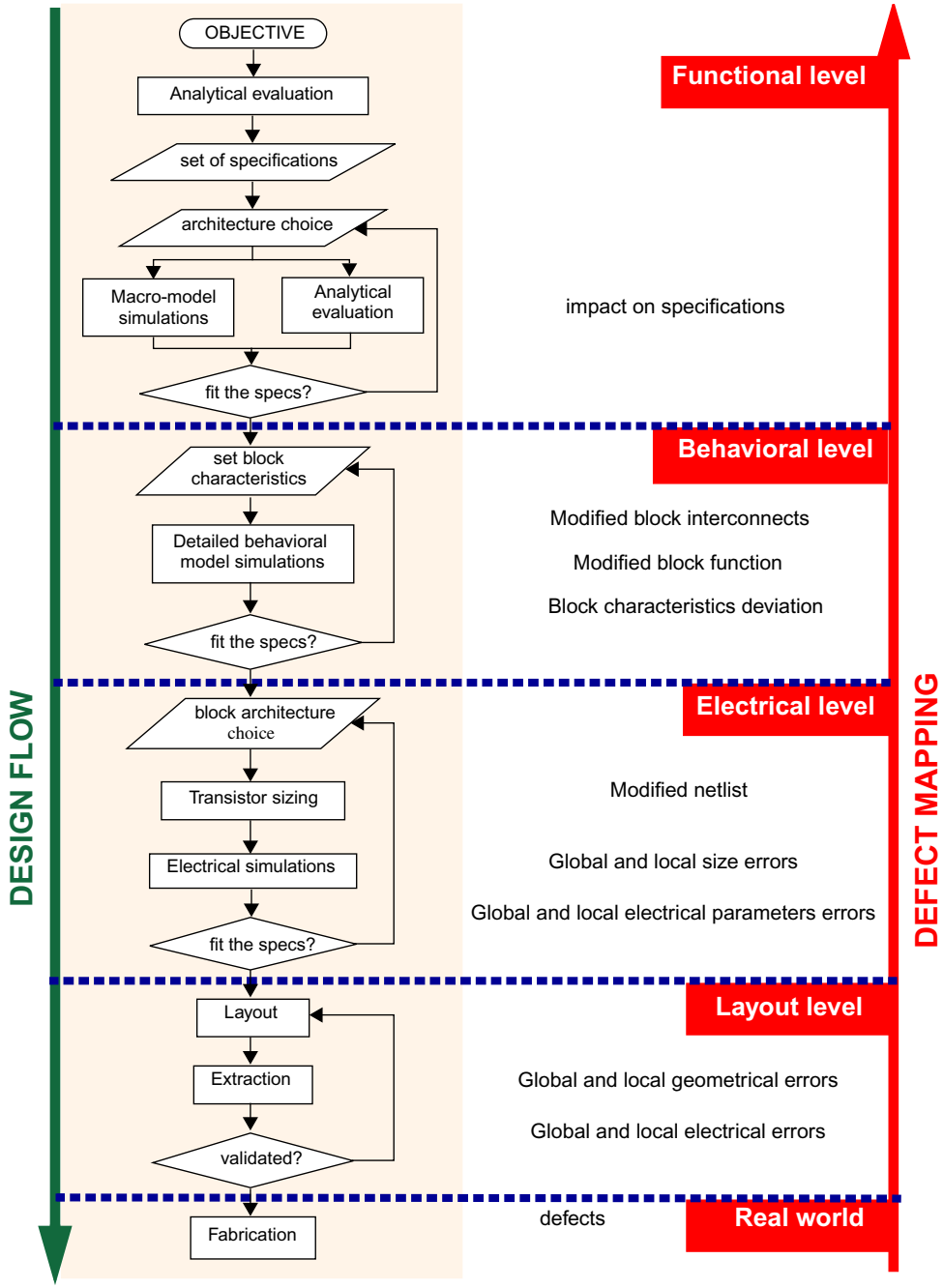


Figure I-2: Relating design-flow and defect mapping

Figure I-2, we perform the test at the behavioural level. It may not be considered as a new concept since testing the building blocks could be seen as part of the “divide and conquer” approach. However, the novelty of our proposal is more in the line of the “design-based testing” concept because the test is closely linked to the design flow and target the design parameters. Actually, this approach is probably the intuitive way of testing complex systems.

The main contribution of this thesis is the full development of a digital design-based test approach for ΣΔ modulators. It intends to determine the characteristics of the main building blocks using only simple digital tests, without breaking the ΣΔ modulation loop.

The direct relation to circuit performance helps to maintain a good level of confidence, even if the circuit specifications are not measured explicitly. And conversely, such a test can detect defects that have brought circuit blocks out of normal process variations but have no direct/strong impact on the top level specifications.

The rest of the thesis is organized as follows.

The first chapter of the thesis will introduce the reader into the field of ΣΔ converters. The principle of operation as well as the main architectures will be described. A section will also be dedicated to behavioural modelling and another to classical characterization methods.

The second chapter deals with the testability solutions that exist in the literature and that could be applied to ΣΔ converters.

The third chapter describes the motivations of the approach defended in this thesis from both a phylosophical and practical point of view.

The fourth and fifth chapters provide a detailed description and analysis of several digital tests for the most important non-idealities of the ΣΔ modulator building blocks.

The sixth chapter introduces important guidelines for the implementation of the test proposal.

The seventh chapter discusses the design of an integrated prototype and presents a number of experimental results that validate the approach.

Finally, the thesis closes with concluding remarks.

1

ΣΔ MODULATORS TEST PARADIGM

The objective of this chapter is to discuss the testability of ΣΔ modulators. In the first section, the operating principles of Analog-to-Digital converters based on ΣΔ modulation are summarized. The most common architectures are described and modulators' behavior is discussed.

These basic considerations should allow the reader to understand the particular test needs of ΣΔ modulators, which will then be discussed. A particular emphasis is put on the techniques used to test A/D converters based on ΣΔ modulation functionally; these characterization techniques are applicable to any class of A/D converters.

1 • 1 A BRIEF SUMMARY OF A/D CONVERTERS BASED ON ΣΔ MODULATION

1 • 1 . 1 The structure and principles of ΣΔ converters

An Analog-to-Digital Converter based on ΣΔ modulation consists ofthree main parts, as seen in Figure 1-1. A simple anti-aliasing filter, a ΣΔ modulator and a digital filter.

The ΣΔ modulator samples the input signal at a high rate (f_s) and digitizes it at a low resolution. Its output is a low-resolution bit-stream at frequency f_s. The digital filter then transforms this low-resolution high-rate bit-stream into a high-resolution low-rate word-stream. Apart from the filtering operation, the digital filter also performs a down-sampling operation. For that reason, it is often called a decimation filter. This singular A/D conversion is based on two main principles: oversampling and noise-shaping.

Oversampling is a concept that can be applied to any A/D converter. Consider an application for which the signal to be converted is limited to the bandwidth [0; f_c]. According to the well-known Shannon's theorem, a finite-bandwidth signal can be fully represented (with no ambiguity) by its sampled version whenever the sampling frequency f_s is higher than double the maximum signal frequency. Otherwise, a phenomenon known as aliasing occurs, and the part of the signal spectrum above half of sampling frequency (the Nyquist frequency) mixes with the reflected spectrum at the sampling frequency. This is illustrated in Figure 1-2.

For the input frequency range defined above, a sampling frequency f_s=2f_c would thus be sufficient. Oversampling simply consists of digitizing the input signal at a rate deliberately higher than is strictly necessary. This offers the possibility to further filter the output and gain some precision. For instance, if a flash converter samples input signal at a frequency

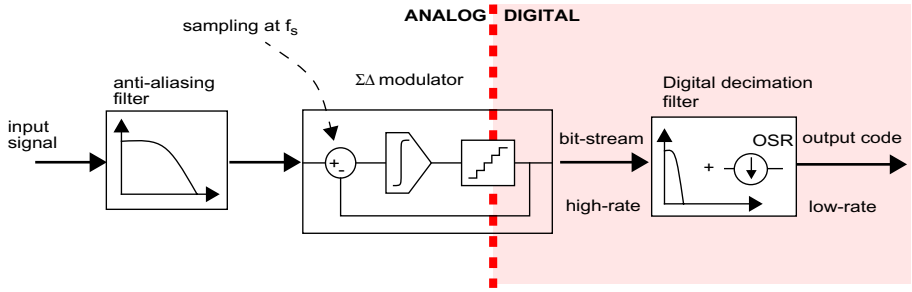


Figure 1-1: The structure of a ΣΔ converter

f_s=4f_c, it is possible to take as the converter output the average of two consecutive codes, providing a filtered output.

The ratio between the sampling frequency and twice the cut-off frequency of the output filter is called Over-Sampling Ratio (OSR).

$$OSR = \frac{f_s}{2f_c} \quad \textbf{(1-1)}$$

Notice that the filter cut-off frequency is what actually limits the input frequency range of the oversampling converter. For a ΣΔ converter, the input frequency range in often referred to as the converter (or modulator) base-band. The down-sampling factor that can be applied by the decimation filter is also equal to the OSR.

In the conversion process from analog to digital, the signal is approximated to digital discrete levels. As any approximation, this can be seen as an error and such error power sets the absolute limit to the converter precision. The error power obviously depends on the converter quantization step Δ. The finer the step, the better the signal approximation and the lower the quantization error power. For any analog input (provided that the converter is not in overrange), the quantization error is always bounded between -Δ/2 and Δ/2. In principle, it is possible to calculate the probability density function of the quantization error in the range [-Δ/2;Δ/2] from the density function of the sampled input signal. Nevertheless if the input signal varies randomly across the quantizer full-scale from sample to sample and the number of quantizer steps is large, it can be shown [20] that the quantization error behaves as a uni-

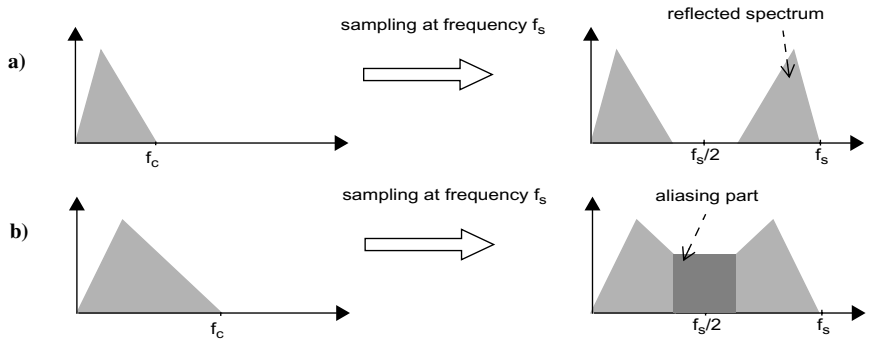


Figure 1-2: Sampling a continuous-time signal
a) with no aliasing, $f_c<f_s/2$
b) with aliasing, $f_c>f_s/2$

form random variable in the range [-Δ/2,Δ/2]. In that case, its power spectral density is constant,

$$S_E(f) = \frac{\sigma^2(er)}{f_s} = \frac{1}{f_s}\int_{-\Delta/2}^{\Delta/2}\frac{er^2}{\Delta}der = \frac{\Delta^2}{12 f_s} \quad \textbf{(1-2)}$$

The quantization error power spreads over the entire Nyquist range (from 0 to $f_s/2$), so by low-pass filtering the converter output, the part of the quantization error above the cut-off frequency is attenuated and the converter precision is improved. As a result, the quantization error (also called the quantization noise) power can be calculated by integrating the power spectral density of Eq (1-2) over the converter baseband.

$$P = \int_{-f_c/2}^{f_c/2} S_E(f)df = \frac{\Delta^2}{12}\times\frac{f_c}{f_s} = \frac{\Delta^2}{12}\times\frac{1}{OSR} \quad \textbf{(1-3)}$$

If the converter output is filtered, the precision improvement associated with that filtering (i.e. due to oversampling) is limited to 10dB per decabe of the OSR.

The heart of ΣΔ converters is the ΣΔ modulator and its objective is to improve the benefits of oversampling by shaping the quantization noise to high frequency. In that way, most of the quantization error can be eliminated and the performance greatly improves. Bringing the concept to an extreme, it is even possible to use a 1-bit quantizer and obtain, by proper quantization noise shaping, high precision converters. The concept and benefits of noise shaping are easily understood. What is less obvious is the manner to achieve it. The next subsection will introduce it through a description of the first order modulator.

1 • 1 . 2 The first order modulator

The noise-shaping capability of ΣΔ modulators is achieved by feeding back the quantization error to the input. Figure 1-3 depicts a first order ΣΔ modulator. It can easily be seen

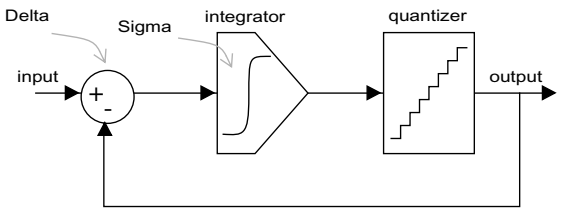


Figure 1-3: First order ΣΔ modulator diagram

from that diagram the reason for the ΣΔ name. Indeed, the quantizer output is subtracted from the input signal to form the modulator quantization error: that is the *delta* operation (Notice that here the modulator quantization error is not the same as the quantizer quantization error). Then, this error signal is integrated which, in a discrete-time basis, is a summing operation: the *sigma* operation.

In many cases, the approximation of the quantization error as a white noise does not hold true. If the ratio between the input signal frequency and the sampling frequency is a rational number, only a finite number of different levels are sampled and that sequence repeats periodically [21]. If the ratio is

$$\frac{f_{in}}{f_s} = \frac{M}{N}, \tag{1-4}$$

where M and N are mutually prime, a number of N different points are sampled, so the quantization error appears as a periodic sequence of fundamental frequency f_s/N.

For low-resolution quantizers there is also a strong correlation between the quantization error and the quantizer input signal. Let us take a brief example, depicted in Figure 1-4: an input sinewave of amplitude 1 is sent to a 1-bit quantizer of full-scale 2. This quantizer is indeed a simple comparator: a logic zero at the comparator approximates the input voltage to a -1 input and a logic one to a 1 input. The comparator performs the *sign* operation. Hence, we can write the quantization error as,

$$er = sign(\sin(x)) - \sin(x) \tag{1-5}$$

Nevertheless, in ΣΔ modulators, the signal manipulation before the quantizer typically provides a quantizer input that is reasonably random or at least de-correlated from the modulator input signal, so that the result of Eq (1-2) gives a good insight into modulator performance.

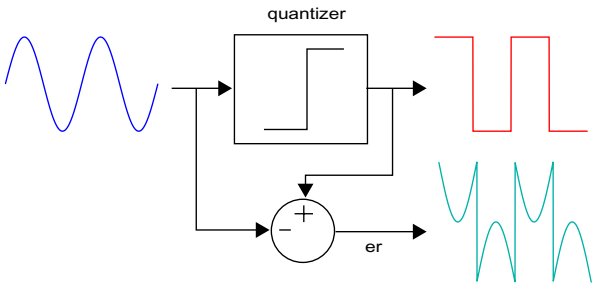


Figure 1-4: 1-bit quantizer error

If we consider the approximation of a uniform random quantization error for the quantizer to be valid, the z-domain description of the modulator can be built as shown in Figure 1-5, where the quantizer is linearized and an additive noise source (E) models the quantization error.

This provides a linear description of the ΣΔ modulator that gives an insight into its operation. The following equation can be written that relates the modulator input X to its output Y

$$Y = E + \frac{z^{-1}}{1 - z^{-1}}[X - Y], \tag{1-6}$$

This reduces to,

$$Y = z^{-1}X + (1 - z^{-1})E, \tag{1-7}$$

Thus, the modulator output is thus equal to the delayed modulator input plus the quantizer error shaped by the function $(1\text{-}z^{-1})$. Considering that

$$z = e^{2i\pi\frac{f}{f_s}}, \tag{1-8}$$

the power spectral density of the modulator quantization noise can easily be calculated,

$$S_Q(f) = S_E(f) \times \left|1 - e^{-2i\pi\frac{f}{f_s}}\right|^2 = S_E(f) \times 4\left[\sin\left(\pi\frac{f}{f_s}\right)\right]^2 \tag{1-9}$$

Assuming a large OSR ($f << f_s$), a first order Taylor series expansion of the sine function can be used to calculate the total quantization noise power in the modulator baseband. Using Eq (1-2), the noise power is,

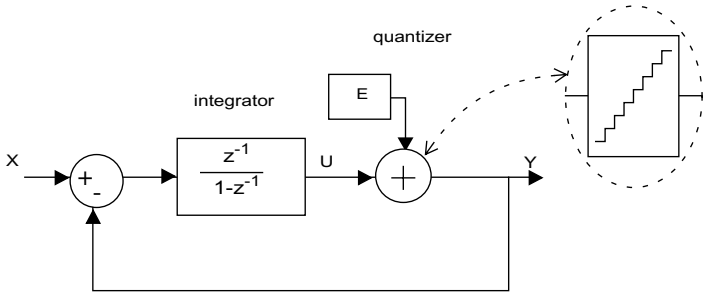


Figure 1-5: First order ΣΔ modulator linearized z-domain model

$$P_Q = \int_{-f_c}^{f_c} S_Q(f)df = \frac{\Delta^2}{12} \times \frac{\pi^2}{3OSR^3} . \quad \textbf{(1-10)}$$

So it is shown that the noise shaping allows for a 9dB noise reduction per octave of OSR, which represents a 6dB/octave improvement with respect to the gain for an unshaped quantization noise. Considering that the converter full-scale is normalized to the range [-1;1], the theoretical maximum effective number of bits (ENOB) of the first order ΣΔ modulator can also be calculated by resolving the following equation, assuming an N bit quantizer,

$$\left(\frac{\Delta_{eq}^2}{12} = \frac{\Delta^2}{12} \times \frac{\pi^2}{3OSR^3}\right) \Leftrightarrow \left(\frac{1}{12}\left(\frac{2}{2^{ENOB}-1}\right)^2 = \frac{1}{12}\left(\frac{2}{2^N-1}\right)^2 \times \frac{\pi^2}{3OSR^3}\right). \quad \textbf{(1-11)}$$

This equation reduces to,

$$ENOB = \frac{\ln\left((2^N-1)\frac{3^{1/2}OSR^{3/2}}{\pi} - 1\right)}{\ln(2)} . \quad \textbf{(1-12)}$$

For instance, a first order modulator with a simple one-bit quantizer could achieve a resolution equivalent to a 9bit converter assuming an OSR of 138.

1 • 1 . 3 Second order modulator

The second order modulator was introduced to improve the noise shaping and consequently to gain more resolution for a given OSR. At first sight, second order modulation could have been obtained by simply adding another integrator in the loop, as seen in Figure 1-6. Nevertheless, it can be easily shown that any perturbation would drive the state variables U_1 and U_2 out of bound.

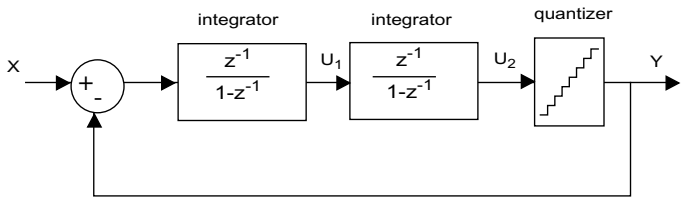


Figure 1-6: Direct unstable implementation of a 2nd order ΣΔ modulator

In order to avoid this issue [22] proposed to add a feedback path at the second integrator input, as shown in Figure 1-7. This stabilizes the modulator and its internal states remain bounded. Actually, it can be shown that second order modulators are unconditionally stables for DC inputs [23, 24] and also for periodic inputs [25]. Due to this extra feedback path, this modulator is sometimes called a double-loop modulator.

Other degrees of freedom in the modulator design can be obtained by adding gain coefficients to the integrator branches. In particular, it is shown in [26] that adding a 0.5 gain to each integrator allows the use of two delaying integrators instead of one, which is very valuable from an implementation viewpoint.

1 • 1 . 4 High-order architecture

In previous subsections, the principles of ΣΔ modulation have been explained and it has been shown how a first order modulator allows one to shape the quantization noise towards higher frequencies. Since the introduction of first and second order modulators, researchers have been working on improving the efficiency of the concept. Indeed, the resolution for a given OSR could be improved by shaping the noise more sharply. Or conversely, for a given resolution, the OSR could be relaxed, allowing the A/D conversion over a broader range of frequency.

This objective can be achieved and has actually been achieved through the generalization of the 1st order ΣΔ modulator to higher orders. Consider the general scheme in Figure 1-8. It represents a modulator diagram such that the integrator is replaced by a general filter whose representation in the z-domain is H(z) and another filter G(z) has been included in the feedback path. The modulator output can be related to the input as,

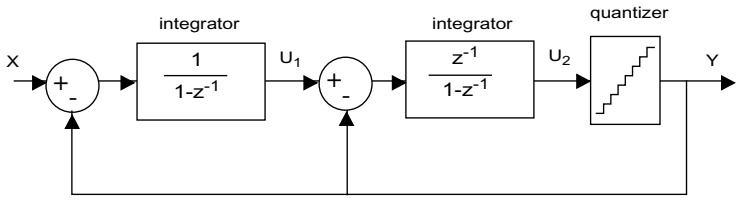


Figure 1-7: Stable double-loop 2nd order ΣΔ modulator

$$Y = STF(z) \times X + NTF(z) \times E$$
$$STF(z) = \frac{H(z)}{1 + G(z)H(z)} \quad . \qquad \textbf{(1-13)}$$
$$NTF(z) = \frac{1}{1 + G(z)H(z)}$$

It appears clearly that, to achieve a better conversion, the Signal Transfer Function (STF(z)) should be an all-pass or a low-pass filter with a cut-off frequency above the desired OSR, and the Noise Transfer Function (NTF(z)) should be a high-pass filter with the deepest rejection band.

1 • 1 . 4 . 1 Single-stage

The design of single-stage high order modulators is not simple. Indeed, the loop filters have to be properly designed such as to provide the desired noise shaping. Typically, a modulator is considered of order L when its NTF is of the form

$$NTF(z) \propto (1 - z^{-1})^{L} . \qquad \textbf{(1-14)}$$

A wide range of different filter implementations could achieve such a result, but much care has to be taken to ensure the stability of the loop [23,25]. Indeed, such modulators are usually stable only in a given signal range. Notice that here, we are using a notion, stability, with two different meanings. The first one is the most usual that requires from a stable device that its internal states are bounded. The second and more practical one requires that the internal states remain bounded within a given range.

A wide number of different ad-hoc architectures have been proposed in the literature for different orders, but it is very difficult to provide a general architecture together with general design guidelines. One of the better known proposal is probably the Lee-Sodini architecture

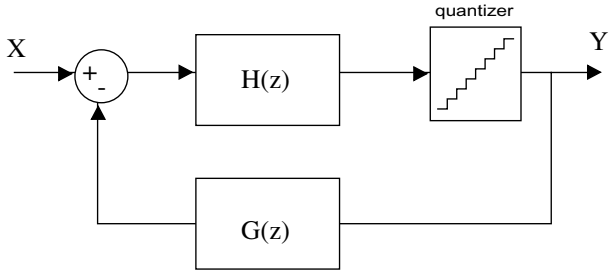


Figure 1-8: Generalized ΣΔ modulator diagram

[27], depicted in Figure 1-9, that contemplates the use of a series of integrators with local feedback and feed-forward paths. In that case, the Signal and Noise Transfer Functions can be written as

$$STF(z) = \frac{\sum_{i=0}^{L} a_i (z-1)^{L-i}}{z\left[(z-1)^L - \sum_{i=1}^{L} b_i (z-1)^{L-i}\right] + \sum_{i=0}^{L} a_i (z-1)^{L-i}}. \qquad \textbf{(1-15)}$$

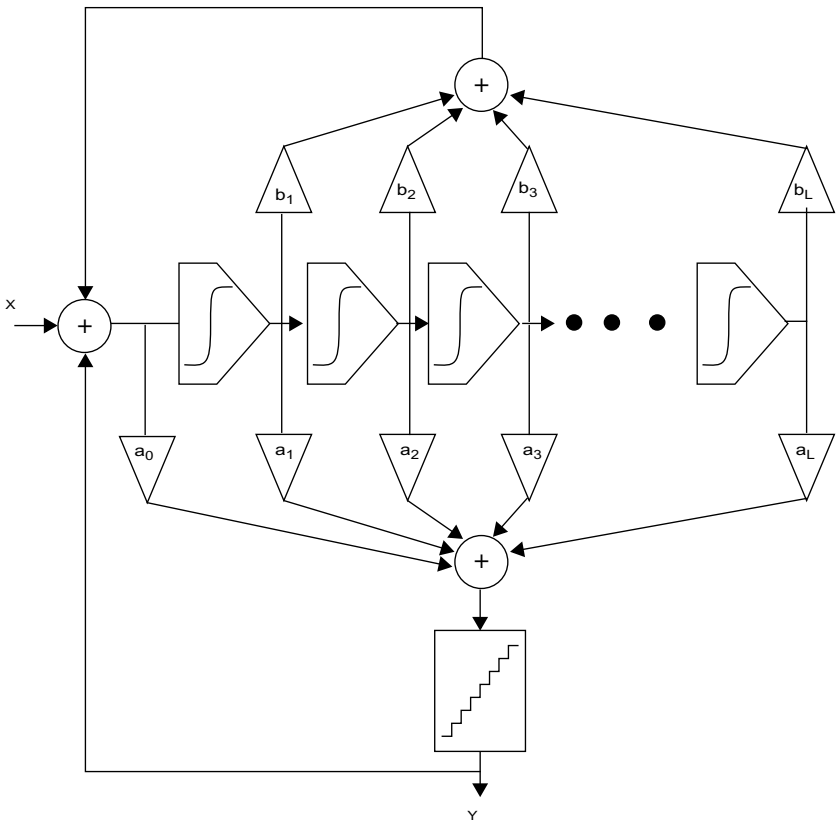


Figure 1-9: General diagram of an L[th] order Lee-Sodini ΣΔ modulator

$$NTF(z) = \frac{(z-1)^L - \sum_{i=1}^{L} b_i (z-1)^{L-i}}{z\left[(z-1)^L - \sum_{i=1}^{L} b_i (z-1)^{L-i}\right] + \sum_{i=0}^{L} a_i (z-1)^{L-i}} \quad \textbf{(1-16)}$$

The choice of the coefficients is a trade-off between filter characteristics (i.e. the modulator noise-shaping performance), stability and complexity. In switched-capacitor implementations, the filter coefficients are defined by capacitor ratio. Successful matching techniques require the use of rational coefficients so as to build all the required capacitors as an array of unit capacitors. If the above mentioned criteria require the use of very small (or conversely very large) coefficients, large capacitors have to be used, which in turn require high current driving capabilities from the amplifiers.

In an attempt to make the design of high-order switched-capacitors single-loop modulators more systematic, a methodology is proposed in [24] to find appropriate coefficients to implement a given noise transfer function in any of the following architectures: Cascade-of-Integrators FeedBack (CIFB), Cascade-of-Integrators Feed-Forward (CIFF), Cascade-of-Resonators FeedBack (CRFB), and Cascade-of-Resonators Feed-Forward (CRFF).

Further scaling of these coefficients can be used to meet output range requirements for each integrator.

1•1.4.2 Cascaded

As explained above, high order modulators are difficult to design as they are prone to instability. To cope with this drawback, [28] proposed to implement high order ΣΔ modulation using a cascade of second and/or first order modulators in a way similar to what is done in pipeline converters. The first stage digitizes the input signal and the successive stages digitize the quantization error of the preceding stage. Figure 1-10 shows a generic cascaded modulator that consists in n stages of order L_i, with i varying from 1 to n. The modulator output is obtained after proper cancellation by the reconstruction filter of all but the last stage quantization errors.

For such a generic cascaded modulator, the following set of equations can be written,

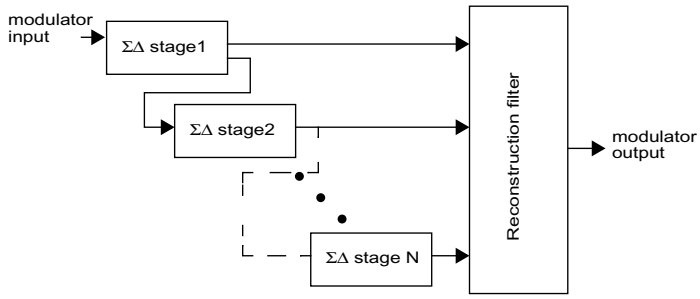


Figure 1-10: Diagram of cascaded ΣΔ modulators

$$Y_1 = z^{-L_1} X + (1 - z^{-1})^{L_1} E_1$$
$$\cdots \qquad \textbf{(1-17)}$$
$$Y_i = -z^{-L_i} E_{i-1} + (1 - z^{-1})^{L_i} E_i$$

where L_i is the order of the stage i modulator.

Hence, the reconstruction of the modulator output has to be

$$Y = \sum_{i=1}^{n} \left(z^{\left(-\sum_{j=i+1}^{n} L_j\right)} (1 - z^{-1})^{\left(-\sum_{k=1}^{i-1} L_k\right)} Y_i \right) \qquad \textbf{(1-18)}$$

such that an equivalent order $L=L_1+...+L_i+...+L_n$ is obtained

$$Y = z^{\left(-\sum_{i=1}^{n} L_i\right)} X + (1 - z^{-1})^{\left(-\sum_{i=1}^{n} L_i\right)} E_n . \qquad \textbf{(1-19)}$$

There exist variations in the implementation of the cascade that depend on the architectural choices for each stage. Moreover, it is also possible to feed to the next stage the quantizer input instead of the quantizer error (the output minus the input). However, this change has to be taken into account in the reconstruction filter.

1 • 1 . 5 ΣΔ modulator analysis and modelling

Since the introduction of ΣΔ modulation, the overwhelming success of the concept applied to A/D conversion has motivated a wide number of studies of ΣΔ modulation behavior.

1 • 1 . 5 . 1 Ideal behavior

Even the simplest ΣΔ architecture - the first-order single-bit modulator - is not easy to study. Several papers deal with peculiarities of its behavior even without considering non-idealities. The quantizer linearization that has been used to derive an analytical transfer function is indeed a coarse approximation that is valid mostly for multi-bit quantizers. For a single-bit-quantizer (even embedded in a loop) it has been seen that the quantizer error is strongly correlated to its input.

In principle, the appropriate mathematical domain to study ΣΔ modulation is that of non-linear dynamics. The starting point of the study are the difference equations that govern the modulator. Considering the 1st order modulator of Figure 1-5, we can write

$$u_{n+1} = u_n + x_n - sign(u_n), \tag{1-20}$$

where u is the integrator output and x the input signal. The modulator output is not explicit in Eq (1-20) and is equal to

$$y_n = sign(u_n). \tag{1-21}$$

Within these seemingly simple equations is contained a complex behavior that can have undesirable effects when considering the ΣΔ modulator as a data converter.

An example of such an odd behavior is that of limit cycles. Let us consider the case when x is a DC input to the modulator that can be expressed as an irreducible fraction of the Full-scale (consider the Full-scale normalized to [-1;1])

$$x = \frac{n}{p}, \tag{1-22}$$

It has been shown that for such an DC level, the modulator output is periodic with period p if both n and p are odd and of period $2p$ if n and p are even [29]. Actually, the exact structure of a limit cycle can be predicted by decomposing the fraction of Eq (1-22) using the Euclid algorithm. For instance a 1/4 input DC level would lead to a repeating sequence of the form 1 1 0 1 0 1 0 1, considering that a digital 1 corresponds to the Full-scale top level

1 and a digital 0 to the Full-scale bottom level -1. The DC value associated with such a sequence is exactly 1/4. It could thus be thought that such an effect is not significant as the output mean value strictly follows the input mean value. Nevertheless, the noise shaping is far from what was predicted by the linear theory in Eq (1-7). Indeed, quantization noise is concentrated in high power tones at $kf_s/8$ (k varying from 1 to 4), f_s being the modulator sampling frequency.

Furthermore, it has also been shown [30], that integrator leakage stabilizes limit cycles for a small range of DC levels around the nominal level expressed in Eq (1-22). This obviously causes non-linearity in the modulator transfer function and is highly undesirable for data converters. For the interested reader, it comes that the transfer function takes the form of the Devil's staircase [31]: a figure well-known by mathematicians and related to Cantor's set. As was said before, the quantization noise of limit cycles concentrates in high power tones that are usually out of the converter base-band. Hence, it may appear that the quantization noise is totally filtered by the decimation filter such that the converter output appears as noise-free. The DC range over which the modulator locks in a limit cycle is thus referred to as a dead-zone.

In another study [32], it has been shown that ΣΔ modulation is a mapping: if a bit-stream is used as an input to a first order modulator, the output follows the input exactly. In that sense there is absolutely no quantization error. This consideration does not concern common-use of ΣΔ modulators but we will see further that it has to be taken into account for our test purpose.

Another important aspect of ΣΔ modulators is stability, which depends mostly on the architecture and can thus be evaluated at difference-equations level. Further refinements may include non-idealities like integrator clipping that will obviously influence the device stability. However, as stated in [23], whenever clipping occurs some state information is lost and it is likely that modulator performance be degraded. A modulator should thus be designed such that clipping is avoided. Analytical studies of ΣΔ modulator non-linear dynamics are not easy to perform, specially for complex modulators. One approach consists of describing the quantizer as an input-dependent gain k element [24]:

$$k = \frac{E[|y|]}{E[y^2]}. \quad \textbf{(1-23)}$$

The term y stands for the quantizer input.

In this way, it is possible to study the locus of the Noise Transfer Function poles as a function of the quantizer gain. If any pole goes outside unit circle the modulator become unstable. Extensive simulations are necessary to evaluate the quantizer effective gain as a function of the modulator input, according to Eq (1-23). Indeed, the quantizer input statistics cannot be evaluated analytically. It is then possible to limit the modulator input-range to the domain that produces stable behavior.

A technique was also proposed in [33] to predict the effective gain of the quantizer. Considering the quantizer as multiple linearized gains for multiple inputs, the modulator can be represented as two interconnected linear systems. The main difference with respect to the describing function is that the distortion components produced by the non-linearity are not neglected but are treated separately from the signal. This method provides results in accordance with simulations but it is very complex to apply. With the computational power available in a current workstation, it is probably easier to simulate the system of difference equations extensively.

1 • 1 . 5 . 2 Introduction of non-idealities

A simple z-domain model can thus be used to gain some insight into the non-linear behavior of complex architectures. Nevertheless, much more work is necessary to evaluate what could be the performance of a real device. The results obtained for the ideal model only set the maximum attainable value. On the other hand, as will be seen in the next section, performance evaluation of ΣΔ modulators usually requires the simulation of a large number of samples. As a result, electrical simulations become prohibitively time-consuming. In a bottom-up approach, macro-models of the modulator building blocks could be built in order to simplify the circuits. By reducing the number of nodes, the simulation would speed-up. However, the drawbacks are two-fold. On one hand the bottom-up approach implies that the modulator architecture is clearly defined and that the macro-models are developed specifically for a given implementation. On the other hand, if the simulator remains electrical, the speed improvement will remain limited. In turn, the main benefit is that, if the macro-models

are implemented accurately, the behavioral model simulation will give results that are very close to a full electrical simulation. As electrical simulations are prohibitive, much work has been done to identify modulators'performance degradation mechanisms and to model them in a high level language (for example Matlab and its Simulink extension, VHDL, VHDL-AMS, VerilogA). Hence, ΣΔ modulators can be quite accurately simulated at the behavioral level using analog macros (integrators, comparators, DACs) that integrate the most important non-idealities.

Behavioral simulations trade accuracy for speed with respect to electrical simulations. But even in the context of behavioral simulation, a large grading of complexity can be found. On one hand, a number of non-idealities can be included or not. In particular, it is well known that the non-idealities that occur inside the modulator loop are spectrally shaped to a greater or lesser extent. For instance, effects that can be referred to the quantizer input will be shaped in the same way as the quantization noise. They are thus very unlikely to produce any significant effect in the base-band. By contrast, the effects that can be referred to the modulator input can be mapped to the input signal and directly affect the resolution. In that sense, many designers opt for introducing non-idealities only in the first integrator [34,35]. This obviously decreases the complexity of the model but sacrifices some subtleties in the modulator behavior.

In simulations, the non-idealities can be modelled with more or less accuracy. Even simple modelling provides significant insight into the impact of those non-idealities on performance. Such modelling can be fruitfully adopted to make architectural level decisions. On the other hand, if the behavioral model has to represent a given implementation in a reliable manner, much more care has to be taken and model complexity increases [38].

This subsection is intended to give an overview of the most common non-idealities that should be considered in ΣΔ modulator behavioral models. As most ΣΔ modulators are implemented in switched-capacitors structures [26,24,38,41], we will focus on the non-idealities that affect the two main building blocks: the integrator and the comparator.

Guidelines are also provided to introduce these non-idealities in event-driven simulators such as Matlab Simulink. The reader interested in a more details on Matlab Simulink implementation is referred to [35, 36,37].

- Noise

  Noise in ΣΔ modulator occurs basically in switched capacitors and in the op-amp. This phenomenon can easily be modelled by a random source. The noise associated with switched capacitors has the well-known white spectral density of kT/C (in V^2/Hz), where k is the Boltzman constant, T the temperature and C the capacitance. Op-amp noise is slightly more complicated to quantify. There is an input-referred white noise that depends roughly on the amplifier transconductance and also a flicker (1/f) noise source should be taken into account.

  White noise sources can be implemented using gaussian random number generators. Flicker noise, in turn, cannot simply be generated with a white random source as it is spectrally shaped. One solution consists of calculating a flicker noise sequence prior to simulation. This can in principle be done by filtering a white noise source. A simple implementation would be to take several white noise sources and sample and hold them at different octaves. The first noise source would be sampled and held for each point of the simulation, the second one each 2 points and so on. The last noise source would be sampled and held twice over the whole simulation. It can be shown that the sum of these noise sources has a power density close to 1/f with a ripple of the order of 1dB.

  The relevance of each noise source greatly depends on its position in the ΣΔ loop. Theoretically, all switched capacitors and op-amp should be provided with their respective noise sources. Nevertheless, it is easy to show that the noise sources that are located inside the loop and cannot be referred directly to the modulator input are attenuated, at least partially, by the NTF. As a result, it is usually sufficiently accurate to introduce noise sources only in the first integrator. This practice, however, is not recommended if the nonlinear dynamics of the modulator are of great concern. Indeed, noise sources located inside the loop may not affect the base-band noise power but may help stabilizing the loop or smoothing some non-linear effects. This positive effect, known as dithering, is sometimes deliberately introduced in the form of a pseudorandom noise source.

- Offset

  In principle, offsets in the integrators and in the comparator do not affect the performance of the ΣΔ modulator in terms of Signal-to-Noise Ratio. However, their introduction in the behavioral model is straightforward and inexpensive in terms of simulation time so there is no reason for not introducing them.

- Capacitor mismatch

  In switched-capacitor integrators, branch coefficients are defined by capacitor ratios. Limitations in the achievable capacitor precision thus cause errors in these coefficients, which set the locations of the poles and zeros of both the Noise and Signal Transfer Functions of ΣΔ modulators. The consequences of a coefficient error may thus range from an increased noise floor to stability issues in high-order modulators that are only conditionally stable. In cascaded modulators, which are usually composed of 1^{st} and 2^{nd} order sections that are unconditionally stable, an error in branch coefficients may lead to incomplete cancellation of the intermediate sections quantization noise. This is due to the fact that the digital reconstruction filter does not match the analog transfer functions that have actually been implemented.

  The modelling of these non-idealities is straightforward as it consists of modifying the gain elements on each branch. It should be noticed, though, that mismatch depends on the particular implementation of an integrator. Let us take a look at the general case of Figure 1-11, that displays a simple model of a two-branch integrator together with a possible switched-capacitor implementation.

  Capacitor C_1 is shared by the two branches of the integrator so as to reduce the number of capacitors. This obviously means that an error in capacitor C_1 affects both branches. The model of such an integrator should be better parametrized as shown in Figure 1-12.

  Brought to an extreme, if two integrator branches share the same coefficient, a single sampling capacitor may be used and branch mismatch would be totally avoided.

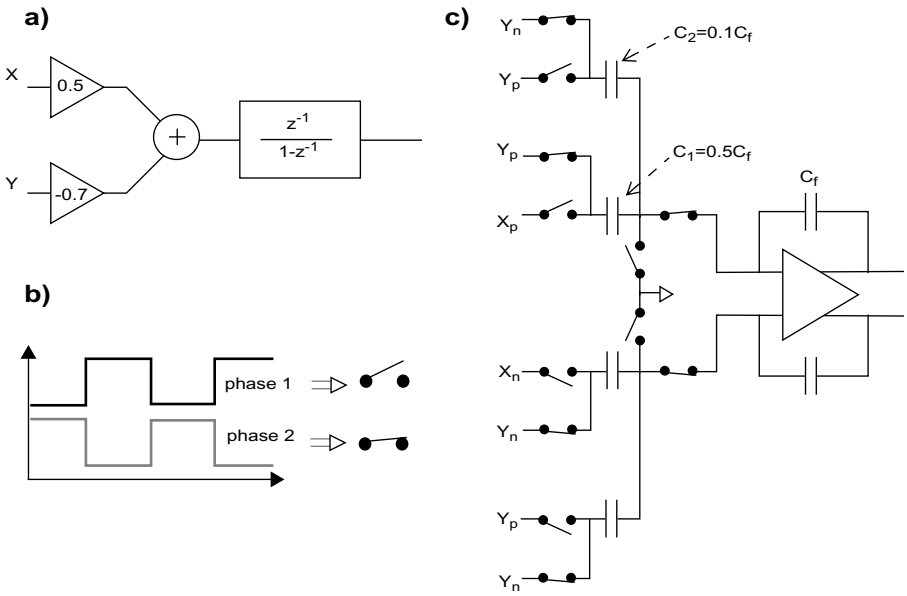


Figure 1-11: a) z-domain model of a two-branch integrator;
b) non-overlapping phases;
c) possible switched-capacitor implementation.

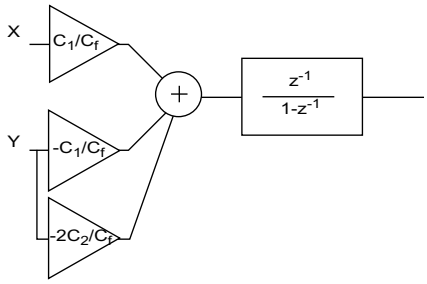


Figure 1-12: Good parametrization of the integrator z-domain model

An error in either the feedback capacitor or in the sampling capacitor would result only in an integrator gain error.

- Capacitor non-linearity

  Another non-ideality that affects the capacitors is their non-linearity: the effective capacitance may depend slightly on the charge stored on the capacitor. This is a concern for the sampling capacitance and for the feedback capacitance in the first

integrator. Indeed, such a non-linearity causes harmonic distortion. Nevertheless, fully-differential implementations greatly mitigate the impact of first order capacitor non-linearity. Anyway, this phenomenon can be relevant if the ΣΔ modulator is implemented in a fully digital process where no dedicated capacitors are available. In such a case, MOS capacitors are to be used, which are prone to exhibit non-linearity. Even if good quality MIM (Metal-Insulator-Metal) capacitors are available, their linearity may be a concern for very high resolution converters.

Non-linearity of sampling capacitors can be approximated by simply adding a polynomial transfer function to each input branch of the integrator. Notice once again that only the first integrator is relevant to the output harmonic distortion.

- Amplifier DC gain

  In the ideal z-domain models presented above, the amplifier is considered to have an infinite DC gain which leads to a lossless integrator. However, real world implementations impose a limit on the DC gain of the amplifier and hence real integrators exhibit a pole error

$$\left(\frac{z^{-1}}{1-z^{-1}}\right) \rightarrow \left(\frac{z^{-1}}{1-pz^{-1}}\right). \qquad \textbf{(1-24)}$$

  The effect of integrator pole error, known as integrator leakage, on ΣΔ modulator performance depends on the chosen architecture. In a single loop modulator of order L, it causes quantization noise shaped at an order L-1 to leak into the base-band. The amount of leakage is directly proportional to the pole error. In cascaded modulators the impact of integrator leakage can be more severe [42]. The quantization noise leaking in section *n* cannot be cancelled by the reconstruction filter. As a result, the shaping of the noise leaking into the base-band is equal to L'-1, L' being the order of the partial cascaded modulator formed by sections 1 to *n*. For instance, if the leakage is produced in the first section and this first section is a 2^{nd} order modulator, the noise leaking into the base-band will be shaped as a first order. This puts higher requirements on the DC gain of the amplifiers in the first section of a cascaded modulator than on those of a single-loop modulator. Furthermore, integrator leakage also influences the non-linear dynamics of ΣΔ modulators [29]. For

instance, it has been shown that it stabilizes limit cycles in 1st order modulators [30].

A pole error can be included in the z-domain transfer function of the integrator in a straightforward manner. This pole error can be linked to the amplifier DC gain through classical circuit analysis. The relationship depends on the actual integrator implementation but it can be said that the pole error is inversely proportional to the amplifier's DC gain.

- Amplifier DC gain non-linearity and saturation

  Amplifier DC gain is usually a small-signal parameter. That is, the DC gain is defined as the slope of the amplifier transfer function for a balanced input. However, the integrator branch coefficients in a ΣΔ modulator are usually scaled to make use of the major part of the amplifier output range. In other words, the amplifier is not used only in a small range around zero. As a result, the amplifier DC gain is input-dependent and this is a cause of distortion. Closely related to the input dependent DC gain is the amplifier saturation. Indeed, saturation can be seen as the level above which the amplifier DC gain is reduced to zero. If the ΣΔ modulator has been designed properly and its coefficients scaled, the amplifiers should not saturate. Otherwise, the integrator output would clip the signal above the amplifier saturation level and this would introduce distortion, particularly if this clipping occurs in the first integrator. Notice, however, that integrator clipping (i.e. amplifier saturation) is also used to put a physical bound to the modulator's internal states. This phenomenon enhances the modulator stability when it is subjected to input transients that are outside its allowed input range.

  In the z-domain model, the amplifier input is not available as the amplifier is embedded in the integrator. However, the amplifier output is the integrator output. Hence the input-dependent DC gain can be mapped to an output-dependent DC gain. One way to model the transfer function of an amplifier is to use the hyperbolic tangent function as,

$$y = sat \times \tanh\left(A_{DC0}\frac{x}{sat}\right) \qquad \textbf{(1-25)}$$

This would represent an amplifier that saturates at output voltages +/- *sat* with a small-signal DC gain of A_{DC0}. In that way, the large signal DC gain can be written

$$A_{DC}(y) = \frac{\partial y}{\partial x} = A_{DC0} \times \left(1 - \left(\frac{y}{sat}\right)^2\right). \quad \textbf{(1-26)}$$

This expression efficiently relates the DC gain to the output voltage. It can be seen that the DC gain non-linearity is intimately related to the amplifier saturation voltage *sat*. In order to model the DC gain non-linearity with one more degree freedom, the actual saturation can be modeled by a saturation block, clipping the integrator output at +/- *sat*. The saturation parameter in Eq (1-26) is then replaced by a coefficient a_{NL} that has to be greater than the actual saturation voltage

$$A_{DC}(y) = A_{DC0} \times \left(1 - \left(\frac{y}{a_{NL}}\right)^2\right). \quad \textbf{(1-27)}$$

It would also be possible to implement a non-symmetrical DC gain by adding a first order term to Eq (1-27), though this is usually unnecessary as most ΣΔ modulators use fully differential structures and are thus inherently symmetrical.

The inclusion of an output-dependent DC gain (i.e. an output-dependent pole error) in the z-domain behavioral model generates an algebraic loop that can only be solved iteratively with respect to a convergence criterion. This may slow down the simulation. The first solution to limit this negative impact is to introduce output-dependent gain only in the first integrator. Indeed, just like with noise, the non-idealities that occur inside the ΣΔ loop are attenuated by the NTF. The second solution consists of arbitrarily fixing the number of iterations, assuming that the approximation is satisfactory. Although this is not a rigorous approach, it is much easier to implement than the resolution of the algebraic loop. Moreover, it can be seen that the convergence is quite fast and acceptable results can be obtained in a small number of iterations.

- Amplifier settling

  The amplifier used in the integrator is expected to settle properly. However, for large integrator input signals, the time given to the amplifier to settle properly may be insufficient, causing a settling error. The impact of the settling error is two-fold. On

the one hand, the part of the settling error that is proportional to the input voltage (this could be the case for a settling error dominated by a poor bandwidth) can be considered as equivalent to an integrator gain error, just like an error in the value of the feedback capacitor. On the other hand, the non-linear part of the settling error causes distortion, just like the non-linear DC gain of the amplifier. Once again, that distortion is relevant mainly if it occurs in the first integrator.

A first order approximation to include incomplete amplifier settling in a behavioral model consists of considering the amplifier as having a single pole (which can be specified as a Gain-Bandwidth product) and a limited output current (i.e. a maximum Slew-Rate). Higher order approximations could eventually contemplate a two-pole approximation but the modelling process would be identical: the integrator output can be calculated as a function of the input through classical circuit analysis. A mathematical closed form expression is obtained that relates the settling error to the integrator input. Such an expression can easily be implemented in the behavioral model.

- Quantizer ADC non-linearity

  The quantizer in ΣΔ modulators consists of an Analog to Digital Converter followed by a Digital-to-Analog Converter. The ADC, for latency requirements, is almost always a FLASH converter, that is, a bank of comparators associated with the appropriate reference voltages. Such an ADC is prone to exhibit non-linearity but this has little impact on the modulator performance, whenever monotonicity is ensured.

- Comparator hysteresis

  Like any non-ideality that can be referred to the comparator input, hysteresis effects are further filtered by the NTF and thus have little impact on the modulator performance. Anyway, they can easily be included in a behavioral model. In Simulink, a relay block can be used.

- Comparator uncertainty zone

  As comparator offset is not usually of great concern, very simple structures are used to maximize speed. One of the most used structures is the dynamic latch comparator. Such a comparator is reset before each new comparison but may partially retain information of the previous comparison. These comparators thus exhibit some metastability around their threshold. Such an uncertainty zone can easily be modelled by the addition of a small noise source at the comparator input.

- DAC non-linearity

  Switched-capacitor DACs consist simply of a bank of properly sized capacitors sampling a reference voltage. Mismatch in capacitor sizes is the main cause of DAC non-linearity. The consequence of such an implementation is that different DACs are implemented at each feedback node, and a different non-linearity has thus to be considered. DAC non linearity can simply be modelled as integrator branch coefficient mismatch. Once again, the non-linearity of the DAC that enters the first integrator is the most relevant to the modulator output distortion.

The non-idealities can be introduced incrementally in the ideal z-domain model to reach the required accuracy. The most intuitive way to design such a incremental model is probably to use Matlab Simulink. The blocks required to build an ideal z-domain model are available in the standard library and most non-idealities require only a small tailoring of library blocks. For instance, comparator hysteresis is introduced straightforwardly using a relay block, while integrator clipping can be modelled using a saturation block. The integrator transfer function can be implemented as a user-defined Matlab expression derived from circuit analysis. In order to implement the amplifier DC gain non-linearity, the DC gain has to be introduced in the integrator transfer function as an additional input. This additional input allows forming an algebraic loop that requires iterative resolution.

Figure 1-13 represents what could be a Simulink model of a two branch integrator. The integrator is implemented with the “fsolve” function but the algebraic loop could be broken as shown in Figure 1-14.

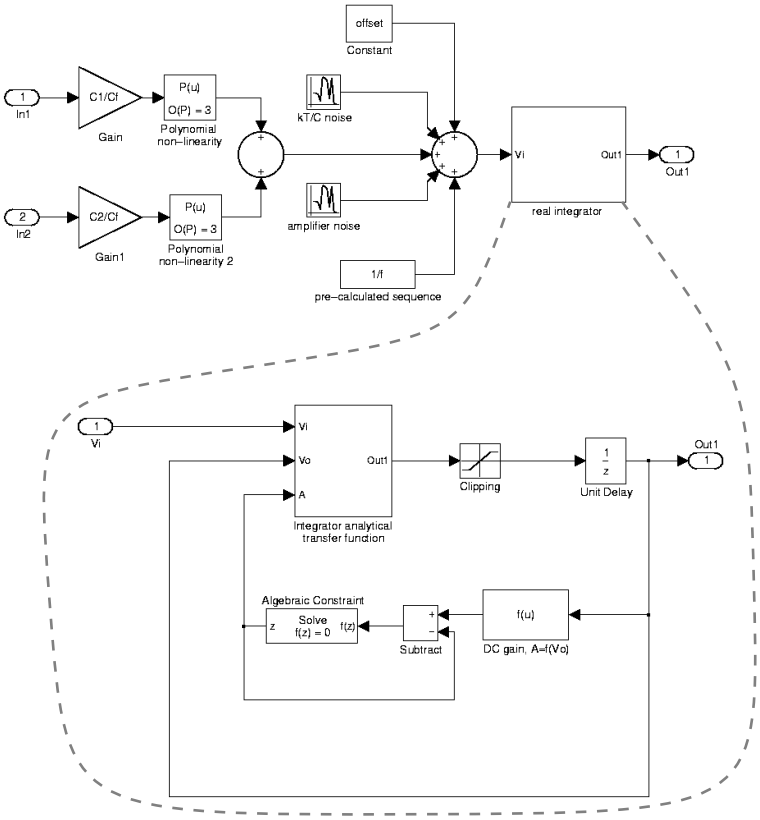


Figure 1-13: Simulink model of a two branch integrator

Figure 1-15 represents the evolution of the maximum Integral Non-Linearity (a definition can be found in next section) for a 2nd order modulator, as a function of the DC gain non-linear parameter a_{NL} of the first integrator (the nominal DC gain was set to 3000). The simulation results are presented for a model resolving the algebraic loop with “fsolve” and for a model breaking the loop in three iterations. It can be seen that the results match quite well.

Such a model can be used to explore the design space and provide much insight into the impact of certain behavioral parameters on performance. Figure 1-16 represents the evolution of the Signal-to-Noise Ratio of a cascaded 2-1 modulator with OSR=100 as function of the DC gain of the first integrator. This figure was built simulating a realistic model of the

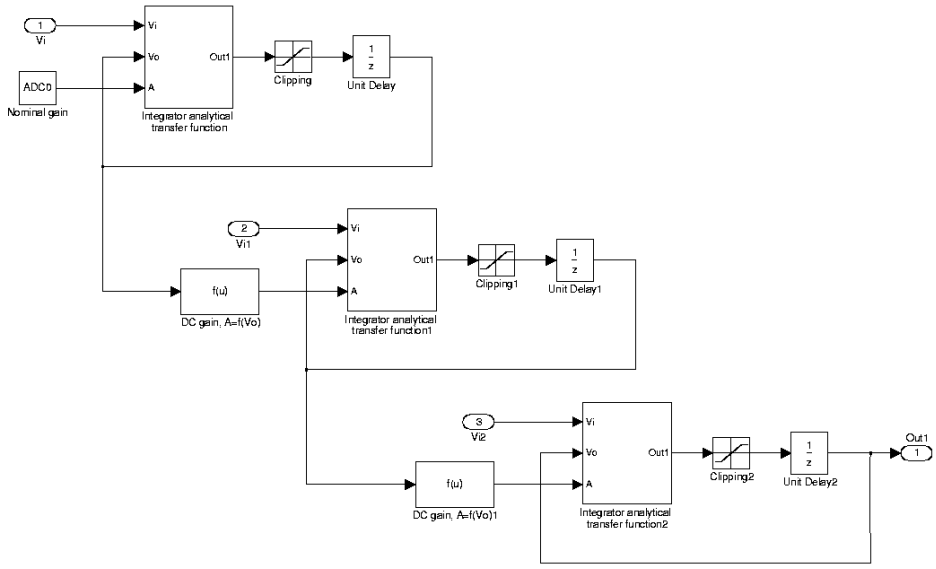


Figure 1-14: Opening the algebraic loop

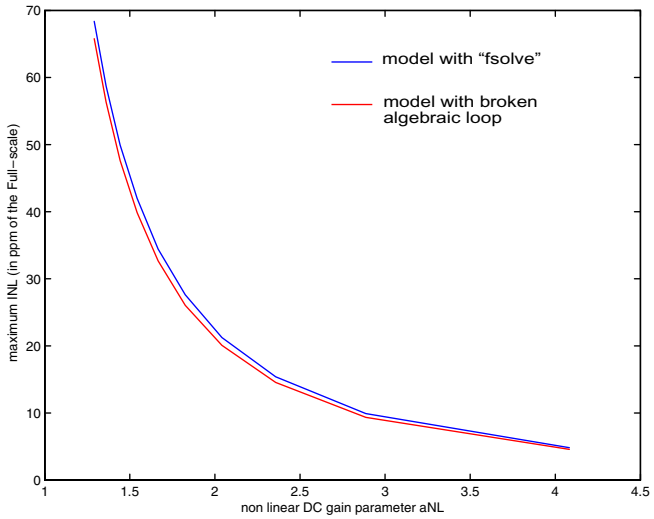


Figure 1-15: Maximum INL of a 2nd order modulator as function of the 1st amplifier DC gain non-linearity

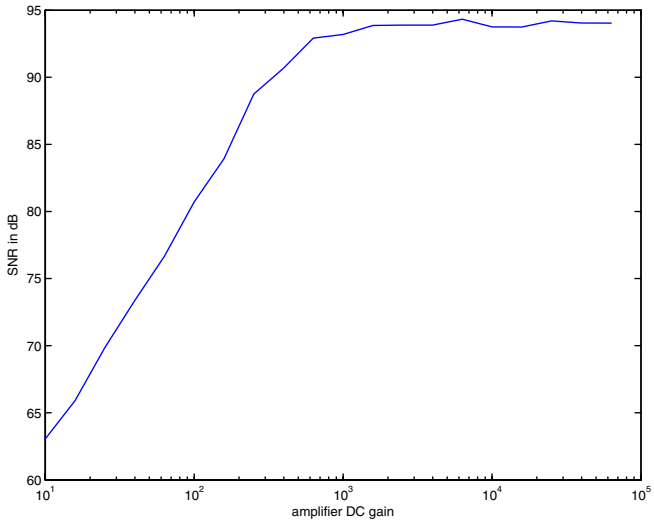


Figure 1-16: SNR of a 2-1 cascaded modulator as function of the 1st amplifier DC gain

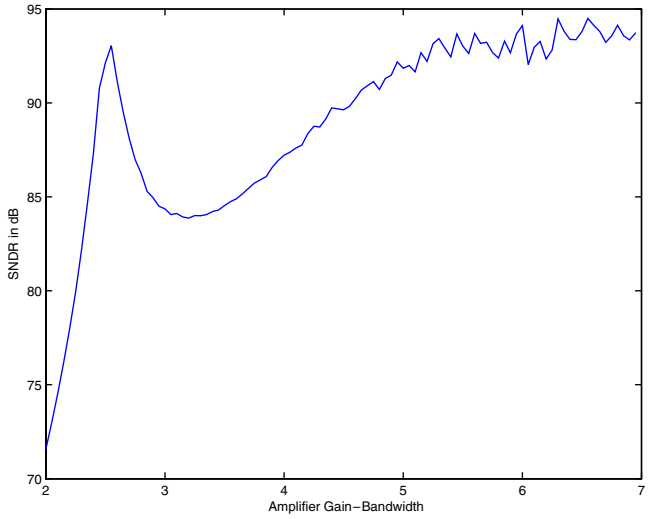


Figure 1-17: Impact of 1st amplifier Gain-Bandwidth product on the SNDR of a 2-1 cascaded ΣΔ modulator

modulator as described above for different value of the DC gain, while maintaining the rest of the parameters to an acceptable value (from a performance viewpoint).

Similarly, Figure 1-17 displays the evolution of the Signal-to-Noise-and-Distortion Ratio as a function of the Gain-Bandwidth product (GBW) of the first amplifier. Notice that a high performance is obtained for any value of the GBW (normalized to the sampling fre-

quency) above 5.5, which corresponds to a proper settling. However, a performance peak singularity can also be observed at a much lower value of GBW=2.7. This is quite counter-intuitive and it means that the settling error at that point is in some manner internally compensated by the modulator non-linear dynamics. Both Figure 1-16 and Figure 1-17 are congruous with analytical studies and the observed trends had already been commented on in the literature [38].

1 • 2 ΣΔ CONVERTERS TESTING

ΣΔ converters have gained in the last decade a large part of the A/D conversion market. Initially, they were limited to low-frequency applications, mainly instrumentation and audio range due to the high oversampling rate that was necessary to achieve good precision. But the introduction of new architectures and technology scaling have opened the doors to communication applications.This trend is ever increasing as there is much interest in these converters that rely on minimal analog circuitry.

In this section, we will briefly review the main characterization techniques for converters. The objective is to introduce concepts that will be used throughout the thesis. Indeed, characterization is none other than an exhaustive version of functional testing, and it is key to understanding the shortcomings and benefits of any DfT approach.

Metrology is a science in constant evolution, and it cannot be said that the characterization of A/D converters is a closed research area. Nevertheless, there has been an effort by the IEEE to provide a framework in this domain, and two consecutive standards can be said to define most of the characterization techniques used in the industry [39]. Then, some other metrics are application specific with dedicated characterization methods [40].

1 • 2 . 1 Performance metrics

An issue that is common to all ΣΔ converters and also to all A/D converters is to define some metrics that allow the evaluation of their performance. These metrics serve to define the specifications and the measurements that have to be performed in functional testing.

They can roughly be divided into two sets: the static parameters and the dynamic ones.

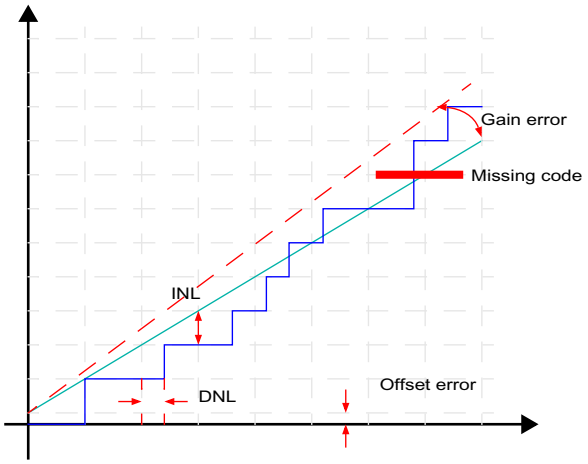


Figure 1-18: A/D converter static metrics

1 • 2 . 1 . 1 Static parameters

These parameters are devoted to the description of the DC transfer function of the converter. An A/D converter translates an analog signal, which is continuous, to a digital representation that is discrete. This operation, known as quantization, can be seen as a rounding function: a real value (continuous) is represented by the closest integer value (discrete). For an ideal converter, the transitions between two discrete levels are evenly spaced across the full-scale range and the transfer function takes the form of a regular staircase. But in real cases, the transitions may be displaced from their ideal location, and the stair widths may thus vary across the full-scale range.

The metrics that define the quality of the transfer function are thus:

- the Integral Non-Linearity (INL), that measures the displacement of the transitions from their ideal location
- the Differential Non-Linearity (DNL), that measures the error committed on the stair width

  Both parameters have to be defined for each possible output code. Typically, only the maximum (worst-case) INL and DNL is specified. Notice also that DNL and

INL are greatly correlated. Indeed, the INL is actually the cumulative sum of the DNL.

- the number of missing codes, as its name indicates, is the number of possible output codes that are not actually reached for any analog input level within the full-scale range.
- monotonicity: an A/D converter should ensure that its transfer function is monotonous. That means that for any pair of input values, the code corresponding to the higher one should be greater than or equal to the code of the lower.
- the gain error
- the offset

1 • 2 . 1 . 2 Dynamic parameters

These parameters are used to describe the non-idealities of a converter for AC input signals and more precisely for sine-wave input signals. There exist an important number of metrics that correspond to specific dynamic tests, but we will only present the most important ones.

- The Signal-to-Noise Ratio: this metric is defined according to

$$SNR = \log\left(\frac{P_{signal}}{P_{noise}}\right), \tag{1-28}$$

where P_{signal} is the input sine-wave power and P_{noise} is the power of the random noise across the converter bandwidth. The noise floor is ultimately limited by the quantization noise, that is, by design. However, other noise sources will add to the quantization noise contribution in such a way that the converter will never reach the ideal value. One unavoidable noise source is thermal noise that is present in every integrated circuit. A white noise floor is represented in Figure 1-19.

- The Total Harmonic Distortion: this metric is defined according to,

$$THD = \log\left(\frac{P_{signal}}{\sum_{i=2}^{\infty} P(A_i)}\right), \tag{1-29}$$

where $P(A_i)$ is the power of the tone whose frequency is i times the input sinewave frequency, that is, the power of the i^{th} harmonic.

- The Signal-to-Noise and Distortion Ratio (SNDR) is similar to the SNR but adds the power of the harmonics to the noise power

$$SNRD = \log\left(\frac{P_{signal}}{P_{noise} + \sum_{i=2}^{\infty} P(A_i)}\right). \quad \textbf{(1-30)}$$

- The Effective Number Of Bits (ENOB) is a transformation of the SNDR. As said above, for an ideal converter, the precision is limited only by the quantization noise, that is, in turn, only defined by the number of quantization steps. The quantization noise power for an ideal converter of n bits (2^n-1 transitions), for an input sine-wave covering the full-scale is

$$P_{noise} = \frac{\Delta^2}{12} = \frac{FS^2}{12 \times 2^{2N}}. \quad \textbf{(1-31)}$$

This is derived by considering that the quantization error for any output code has a uniform distribution over the range [-Δ/2;Δ/2], where $\Delta=FS/2^N$ is the ideal width of the quantization step. This approximation does not hold true for an input sinewave. Nevertheless, if the number of bits is sufficiently high, the sinewave over a given code range ([-Δ/2;Δ/2]) can be approximated as a linear segment and the error in Eq (1-31) is small.

The full-scale sine-wave power is

$$P_{signal} = \frac{FS^2}{8}. \quad \textbf{(1-32)}$$

Therefore, the maximum achievable SNR reduces to

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right) = 10\log\left(\frac{FS^2/8}{FS^2/(12 \times 2^{2N})}\right) \approx 6,02N + 1,76. \quad \textbf{(1-33)}$$

The ENOB is defined by inverting this relation using the SNRD instead of the SNR. In other words, it represents the number of bits that an ideal converter should have in order to exhibit an SNR equal to the measured SNRD, i.e.,

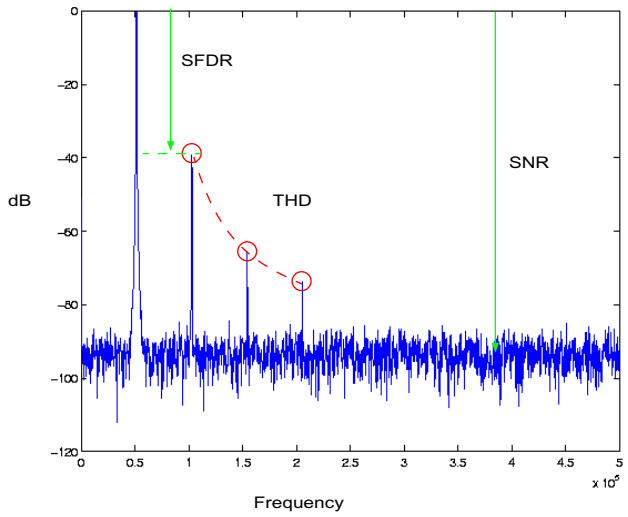


Figure 1-19: A/D converter dynamic metrics

$$ENOB = \frac{SNRD - 1,76}{6,02}. \quad \textbf{(1-34)}$$

- The Spurious-Free Dynamic Range (SFDR): Is defined as the relation between the highest spur (usually an harmonic of the input signal) and a full-scale tone power.

$$SFDR = \log\left(\frac{P_{signal}}{max_i(P(A_i))}\right) \quad \textbf{(1-35)}$$

  Assuming that the spur power is proportional to the input tone power (which is a questionable assumption), it would represent the input signal power limit below which the generated spurious tones would be indistinguishable from the noise floor.

Though static and dynamic set of metrics represent two different approaches and may not account for the same effects, there are some relationships between them. For example, harmonics will appear if the transfer function can be approximated by a polynomial function (of order greater than 1). Hence, there is a relationship between THD and INL, as the latter is sensitive to continuous variations in the transfer function. Similarly, there is a relationship between SNR and DNL, as a random-like variation of quantization steps across the full-scale range will translate into an increase of quantization noise. Despite these consider-

ations, there is no formal equivalence between the two set of metrics. Actually, some non-idealities such as comparator hysteresis are inherently dynamic and could only be detected in a dynamic test. Conversely, missing codes may not have a great impact on dynamic metrics but could be of utmost importance in control applications.

1 • 2 . 2 Determining ΣΔ converters static performance

In most Nyquist-rate ADCs, the conversion is performed on a sample-to-sample basis. The input signal is sampled at a given instant and that sample is in some way compared to a voltage reference. The digital output code determines to what fraction of the full-scale the input sample corresponds. In flash converters, the input sample is compared to a bank of references evenly distributed over the full-scale range. In dual-slope converters, the time necessary to discharge a capacitor previously charged at the value of the input sample is measured by a master clock. There exist a variety of solutions to derive the digital output code, but in all cases a given output code can be associated with a given input sample. For ΣΔ converters, however, that is not the case. Indeed, the output of a ΣΔ converter is provided at a low-rate, but the input is sampled at a high rate. How could be a digital output code associated with a given input sample? This absence of direct correspondence between a given input sample and a given output code is even more significant considering a stand-alone ΣΔ modulator. The adaptive loop of the ΣΔ modulator continuously processes the input signal and the modulator output at a given instant depends not only on the input sample at that instant but also on its internal state. That internal state depends on the whole history of the conversion. Actually, if the same input signal is sent twice to a ΣΔ modulator in identical operating conditions, two different output bit-streams will be obtained. The low-frequency components may be identical and the output of the decimation filter may be identical, but the actual modulator output would be different.

ΣΔ modulation breaks the traditional representation of the A/D conversion as a sample-to-code mapping. This does not mean that the static metrics are useless but that their interpretation has to be done with care. The monotonicity of ΣΔ converters is ensured by design. Indeed, ΣΔ modulators can be seen as control loops: Therefore, if the converters were not monotonous, they could be unstable. The output code of a ΣΔ converter is built by

the decimation filter from the modulator output bit-stream. Provided that the decimation filter is well designed and no rounding operation limits its resolution, there should not be missing codes. DNL does not provide much information but INL could describe general trends in the transfer function such as polynomial approximations. Anyway, measuring the INL for all output codes does not make much sense either. As a result, the standard techniques used to measure the INL and the DNL of ADCs are not adapted to ΣΔ converters. There exist two main techniques to derive static ADC parameters: The servo-loop and the histogram.

1 • 2 . 2 . 1 The Servo Loop

The converter is forced to oscillate around a given code transition as shown in Figure 1-20. If the ADC output is greater than or equal to the reference code, the ADC input is slightly decreased, and conversely, if the ADC output is less than the reference code, the ADC input is slightly increased. Hence, the ADC input oscillates around the transition associated with the reference code. This transition can be further located by measuring the DC component of the oscillating waveform at the ADC input.

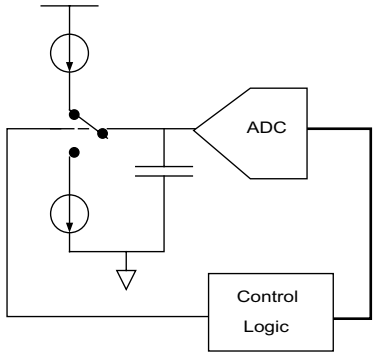


Figure 1-20: Servo-loop diagram

The slope of the ADC input will define the maximum achievable precision, though that random noise has to be taken into account. Noise has a dithering effect, so its impact is not necessarily negative. The IEEE 1241-2000 standard presents a plot of the number of samples needed to be averaged as a function of the required location precision (i.e. the code edge standard deviation), for different values of the ratio of the quantizer step size over rms-noise.

Apart from the previously noted concerns about the concept of code transitions in ΣΔ converters, a drawback of this technique is that the algorithm should take into account the potentially large latency of the decimation filter. It should also be revised to take into account the influence of noise at high resolution. Indeed, a ΣΔ converter with a nominal resolution of 24 bits may have an effective resolution around 20 bits. Trying to locate transitions at 24 bits resolution would imply finding an oscillation buried into a noise that is 16

times larger. Lastly, an exhaustive test of all transitions would require an incredible amount of time: for resolution above 14 bits the number of codes is very large. Furthermore, in order to obtain the static transfer function, the increase and decrease rates of the input voltage should be very slow.

1 • 2 . 2 . 2 Histogram or Code-Density Test

The most used test for determining of static metrics like INL and DNL is without doubt the histogram test or code density test. The principle of operation is the following. The test input stimulus is a known (precisely controlled) signal covering the full-scale and exciting all the possible codes of the ADC. This already implies that care must be taken with coherent sampling. Then, for a given duration of the signal, it is possible to calculate how much time any given code is excited. Let vt_k be the transition to code k. The ADC will output code k wherever the signal is in the range $[vt_k, vt_{k+1}]$. If the slope of the test signal is approximately constant over the range $[vt_k, vt_{k+1}]$, and is equal to s_k, the time spent by the signal on code k is

$$T_k = \frac{vt_{k+1} - vt_k}{s_k} \times N_k , \tag{1-36}$$

where N_k is the number of times that the signal passes in the range $[vt_k, vt_{k+1}]$ during the total duration T of the test. Notice that the slope of the test signal may not be the same each time the signal passes through the range $[vt_k, vt_{k+1}]$. Hence, a more general definition should be used, namely

$$T_k = \sum_{i=1}^{N_k} \frac{vt_{k+1} - vt_k}{s_k^i} = (vt_{k+1} - vt_k) \sum_{i=1}^{N_k} \frac{1}{s_k^i} , \tag{1-37}$$

where s^i_k is the slope of the test signal at its i^{th} passage through the range $[vt_k, vt_{k+1}]$.

The expected number of occurrence of code k during test duration T is simply Tkf_s, where f_s is the AD sampling frequency. The number of occurrence for each code is thus proportional to the corresponding step width, and the DNL and INL can thus be retrieved, whenever the input signal is precisely known. Eq (1-37) is an approximation and is only valid if the slope is almost constant in the range of the quantization step. The real operation that should be done is an inversion of the signal, as can be seen in Figure 1-21, but this operation cannot be performed in the general case for any input signal. Notice that the precision of the DNL measurement will depend on the number of occurrence per code, i.e. on the duration of the test. The higher the number of occurrence, the finer the code width evaluation. Indeed, if only two samples are taken for each code, the DNL precision will be 0.5LSB at best. Noise and jitter effects will further reduce this maximum precision. Hence, the histogram test method requires a large number of samples per code, which can be prohibitive in the case of a high precision converter.

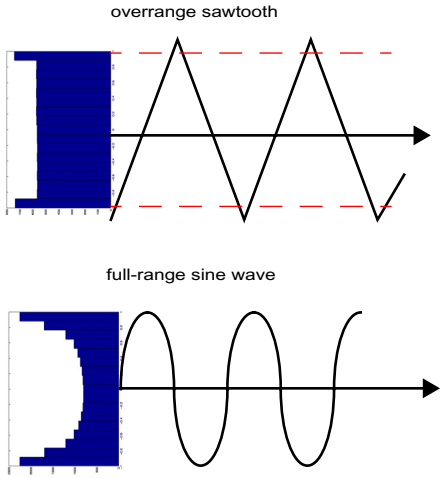


Figure 1-21: Sawtooth and sine-wave density histograms

The histogram test is usually carried out with a linear slow ramp of controlled slope. In that case, N_k is equal to 1 and all the s_k^i are equal to the ramp slope s. Ideally, all the codes are of equal width and thus all the numbers of occurrences should be the same. Any excess or lack in an occurrence number is directly proportional to the code DNL. The input ramp also exhibits a small symmetrical overdrive such that the two extreme codes are excited during more time. This allows one to derive other two static characteristics: gain error and offset.

Another widely used signal is the sine-wave. In that case, the slope varies with the code location, and some calculation has to be done to retrieve the DNL and INL from the deviation of the numbers of code occurrences. Notice that the input sine-waves should also exhibit some controlled overdrive.

On the overdrive part, Eq (1-37) is obviously not valid, but it is easy to calculate the time spent in overdrive, and thus at the extreme codes.

Recently, another stimulus has been proposed as a good candidate for histogram testing: the exponential signal [44]. Indeed, the main shortcoming of almost all characterization techniques is to ensure the specifications of the test signal, that should be superior to that of the converter under test. Ramp linearity or pure sine waves are difficult to ensure up to 24 bits (which is the resolution of an industrial ΣΔ converter). The idea is thus to use an exponential discharge, which can easily be generated by filtering a voltage step with an RC filter, as a test stimulus. Actually, the authors propose to use several exponential waveforms such that the total full-scale is properly covered. They also propose to perform a fitting algorithm to determine the exact value of the exponential discharge time constant.

1 • 2 . 3 Determining ΣΔ converters dynamic performance

ΣΔ modulators raise a number of particular concerns related to their dynamics characteristics. Quantization noise in ΣΔ modulators usually appears as a spectrally shaped random noise but in some conditions spurious tones can appear due to internal coupling with the input signal or even idle tones. Similarly, the quantization noise power in the base-band can vary with the frequency and amplitude of the signal. In order to cope with the little control of the ΣΔ modulators non-linear dynamics, the metrics associated with the dynamic characteristics (THD, SNR, SFDR, etc.) are usually measured and plotted over a broad range of input conditions. As most dynamic characterization techniques rely on asine-wave input, the metrics of interest are measured for several amplitudes and frequencies. A periodic test signal is thus sent to the converter input and a register of N data points is acquired at the converter output. Two main analysis techniques exist.

1 • 2 . 3 . 1 Sine-fit

A sine-fit is used to derive the converter mse (Mean Square Error) including dynamic effects and noise. The test stimulus is a sine-wave and, as its name indicates, the technique consists of fitting the ADC output to a sine-wave. The error between the best-fit sinewave and the ADC output is used to calculate the mse. Two important cases have to be considered.

The first and simplest one is when the input frequency is known precisely. In that case, the problem reduces to a linear-in-the-parameter regression, as only the amplitude, phase and offset of the sine-wave have to be determined. This involves only matrix manipulation and the precision of the mse estimation will basically depend on the number of points used to realize the fitting and on the precision with which the input frequency is known. This latter consideration leads us to the second case, when there is no a-priori knowledge of the input frequency. In that case, several algorithms can be used to determine the best-fit parameters (including frequency), but it is not a linear regression and the convergence rate of the search algorithms is difficult to ensure. Hence, this latter case is more rigorous than the former but requires more processing power and thus more test time.

1 • 2 . 3 . 2 Discrete Fourier Transform (DFT)

The other and almost ubiquitous analysis technique is spectral analysis based on the Discrete Fourier Transform. As it is the technique best suited to analyzing ΣΔ converters, we will describe its application in more detail than the previous techniques.

The Fourier transform of a signal *s(t)* is its exact representation in the frequency domain. Actually, a signal can be represented as the linear combination of a infinite number of base functions such as complex exponential waveforms of the form

$$e^{-i2\pi ft}. \tag{1-38}$$

The Fourier transform of *s(t)* is the set of coefficients of the linear combination, that is, the values of the projection of the signal onto each one of the complex exponential waveforms. The transform is usually represented as a function *S(f)* (or more correctly a distribution) of the frequency *f*, as the coefficients are calculated performing the projection in a generic manner as,

$$S(i2\pi f) = \int_{-\infty}^{\infty} s(t)e^{-i2\pi ft}dt \tag{1-39}$$

The Fourier transform induces no information loss with respect to the signal specified in the time domain. In practice the transform can never be performed exactly on a real signal due to that fact that the signal to be analyzed is only known over a finite number *N* of evenly

distributed points. To tackle this problem a simplified version of the Fourier transform, the Discrete Fourier Transform (DFT), can be calculated as,

$$\tilde{S}(i2\pi f) = \sum_{m=1}^{N} s_d(mT)e^{-i2\pi fmT} \quad \textbf{(1-40)}$$

where T is the sampling period of the N points.

For ΣΔ modulators, which rely on quantization noise-shaping to obtain their high resolution, the DFT is almost unavoidable. However, the DFT should be applied with care because the simplicity of interpreting the results contrasts with the subtlety of the underlying concepts.

The first issue to consider is that performing the DFT over a finite number of points gives an approximation of the Fourier transform of the signal under study. Actually if N points are acquired at a frequency f_{acq} the outcome of the DFT is the Fourier series of the periodic signal of period N/f_{acq} that best approximates the acquired samples. Most of the time, however, the acquired signal has not the required period. It may not even be periodic at all due to noise or spurious components. For that reason spectral leakage occurs. The signal components at frequencies other than the available frequency bins (kxf_{acq}/N, with k varying from 0 to N-1) will leak and spread across adjacent bins, making them unobservable. Actually, the obtained spectrum can be considered as the Fourier transform of an infinite-length version of the analyzed signal multiplied by a rectangular signal with N ones and an infinite number of zeros. That signal is called a rectangular window. The multiplication in the time-domain corresponds to a convolution in the frequency domain. So a spectral line at a given frequency (a Dirac distribution) in the ideal Fourier transform of the signal will appear as a version of the rectangular window spectrum centered at the same frequency. More exactly, what will appear in the FFT output are the samples of the displaced rectangular-window spectrum that corresponds to the available frequency bins. This is illustrated in Figure Figure 1-22.

If the spectral line exactly corresponds to one of the FFT bin it means that it can be represented adequately by a Fourier series of length N. This corresponds to case a) in Figure 1-22. In this case, the rectangular window spectrum is sampled at its maximum, and the rest of the samples correspond exactly to the nulls of the window spectrum. However, if

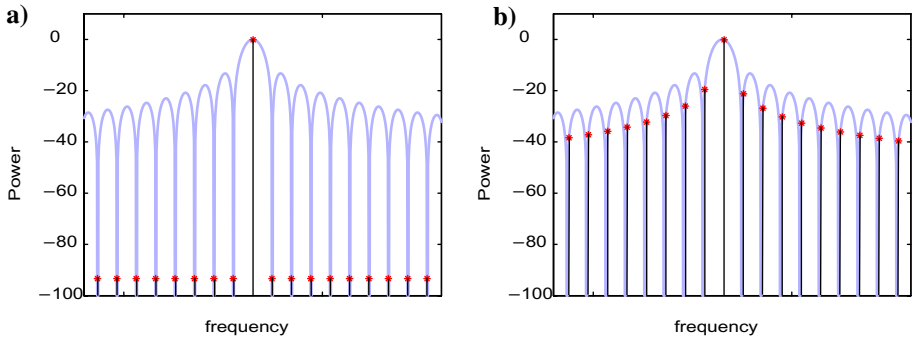


Figure 1-22: Spectrum of a rectangular window. a) for a coherent tone, b) for a non-coherent tone

the spectral line falls between two FFT bins [case b)], the rectangular window spectrum is not sampled at its maximum on the main lobe. Part of the missing signal power leaks into adjacent FFT bins that sample the rectangular window side-lobes.

Coherent sampling is the first technique that is used to limit these undesirable effects. It consists of carefully selecting the test frequencies such that they correspond as closely as possible to FFT bins. In practice, this can be implemented if the test signal generator can be synchronized with the ADC. It can be shown [21] that the test frequencies should be set to a fraction of the acquisition frequency,

$$f_{test} = \frac{J}{N} f_{acq}, \tag{1-41}$$

where N is the number of samples in the acquisition register and J is an integer, prime with N, that represents the number of test signal periods contained in the register. This choice also ensures that all the samples are evenly distributed over the test signal period and that no sample is repeated.

However, it is not always possible to control the test frequencies with sufficient accuracy. Similarly, there may be spurious tones in the converter output spectrum at uncontrolled frequencies. In those cases, a window different from the rectangular one is required. Spectral leakage occurs because the analyzed signal is not periodic with a period N/f_{acq}. The idea behind windowing is to force the acquired signal to respect the periodicity condition. For that to be done, the signal has to be multiplied by a function that continuously tends to zero at its edges. As a result, the power contained in the side-lobes of the window spectrum can

be greatly reduced. The window has to be chosen such that the leakage of all components present in the ADC output signal falls below the noise floor and thus does not corrupt spectrum observation. The counterpart of such an operation is that the tones present in the output spectrum are no more represented by a sharp spectral line at one FFT bin. Indeed, the main lobe of the window is always sampled by a number of adjacent FFT bins that is greater than one. As a result, frequency resolution is lost. There is a trade-off between frequency resolution and side-lobe attenuation. Figure 1-23 represents the spectrum of several windows sampled for a 1024-points FFT. Case a) shows how the window would be sampled for a non-coherent tone that would fall exactly between two FFT bins. Case b) shows a close-up on the main lobes of the window spectra for a coherent tone. Notice that for case b), there is one marker per FFT bin.

In order to limit spectral leakage, the authors in [43] proposed to combine sine-fit and FFT. A sine-fit is performed on the acquired samples in order to evaluate the gain and offset of the modulator. Then, an FFT is performed on the residue of the sine fit. As the high power spectral line has been subtracted from the register, the residue contains mainly noise, spurious components and harmonics. In most cases, these components do not exhibit high power tones. A simple window or even a rectangular window can be used. The spectral leakage of these components should be buried below the noise floor. The overall spectrum (what the authors call pseudo-spectrum) can be reconstituted by manually adding the spectral line corresponding to the input signal. The main drawback of this technique is obviously that it requires the computational effort of both sine-fit and FFT.

The proper application of FFT requires that three parameters be determined: the number of samples in a register, the number of averaged registers and the window to be applied. The window type sounds too qualitative and it is useful to divide it into four parameters: the main lobe width (for instance, 13 FFT bins for the Rife-Vincent window of Figure 1-23), the window energy, the maximum side-lobe power and the asymptotic side-lobe power evolution. Figure 1-24 shows how these parameters relate to the measurement objectives and to the setup constraints through a number of central concepts.

The required frequency resolution is defined by the need for tones discrimination and affected by setup limitations such as the frequency precision of the signal generator. For a

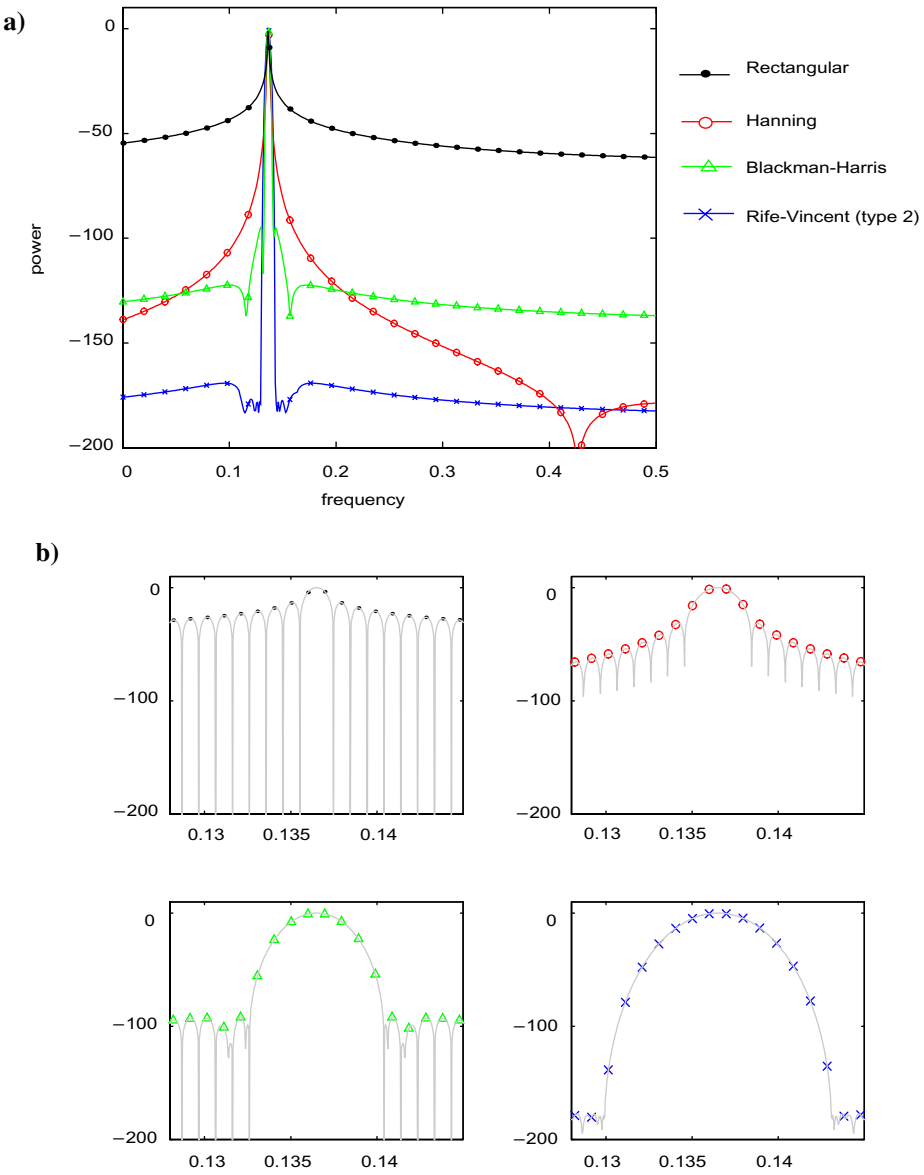


Figure 1-23: a) 1024 points FFT of four windows in the worst case of non-coherent sampling (signal between two FFT bins) b) Main lobes of the window spectra

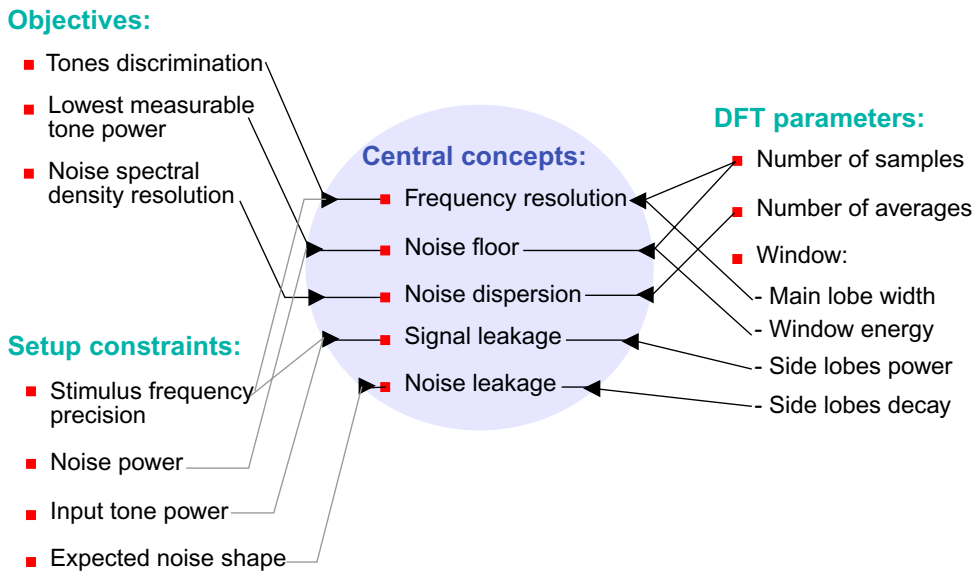


Figure 1-24: Relating FFT parameters to test objectives and setup constraints

given type of test, a number of tones are expected in the output spectrum. For instance, in an intermodulation test, the user has to calculate, as a function of the input tone's frequency, the expected frequency of the intermodulation and distortion tones. Similarly, expected spurious tones such as those at 50Hz (or 60Hz) can be taken into account. All of these components should be correctly discriminated by the FFT in order to perform correct measurements. Frequency resolution is primarily driven by the number of samples in the acquired register but the window type is also of great importance. Indeed, the main lobe width for an efficient window (from a leakage viewpoint) like the Rife-Vincent window shown in Figure 1-23 is as large as 13 FFT bins. This means that the frequency resolution is reduced by a factor 13 with respect to a rectangular window whose main lobe is only 1-bin wide. In many cases though, few tones are expected in the output spectrum and the frequency resolution issue can easily be solved by a judicious choice of the test frequency.

The noise floor is the concept of greatest importance. The power of a random signal spreads over a given frequency range. For white noise, it spreads uniformly from DC to half the acquisition frequency ($f_{acq}/2$). What the FFT measures is actually the amount of noise power in a small bandwidth centered on each FFT bin. Obviously, the more samples are

acquired the smaller the bandwidth is and the smaller the amount of noise that falls in that bandwidth. The expected value for a noise bin is,

$$\overline{\|X_k\|} = \sigma_{noise}\sqrt{\frac{2}{N \times E_{win}}}, \quad \textbf{(1-42)}$$

where σ_{noise} is the standard deviation of the white noise, N the number of samples in the acquisition register and E_{win} the energy of the applied window. Indeed, the window is applied to the whole output data, including the noise and influences the effective noise bandwidth. The energy of the window is calculated simply from the time-domain samples of the window (w_k) according to

$$E_{win} = \frac{N\sum_{k=0}^{N-1} w_k^2}{\left(\sum_{k=0}^{N-1} w_k\right)^2}. \quad \textbf{(1-43)}$$

On the other hand, the noise floor is related to the setup constraints by the actual noise power in the output data, which should be estimated *a-priori*. The noise floor has to be set to a value that enables the observation of the lowest expected tone power. In other words, if a tone of 90dB below full-scale has to be detectable, the number of samples and the window energy have to be chosen such that the noise floor of the resulting FFT falls below 90dB.

The noise dispersion should also be taken into account. It can be shown that the random variable that corresponds to an FFT bin and whose mean value is expressed in Eq (1-42) has a standard deviation of the same order as its mean value []. As a result, in the representation of the spectrum in decibels of the Full-scale, random noise appears as a large band that goes from 12dB above the expected power level down to tens of decibels below. Averaging the magnitude of the FFT bins for K acquisition registers helps to reduce the standard deviation of the noise FFT bins by a factor of $K^{0.5}$. For a significant number of averages, the noise floor tends to a continuous curve, which would be its ideal representation. Actually, the following equation could be used to derive the FFT parameters from the requirement of the lowest detectable tone

$$10\log\left(\frac{1}{2P_{noise}}\right) - 10\log\left(\frac{N \times E_{win}}{2}\right) + 20\log\left(1 + \frac{3}{\sqrt{K}}\right) = P_{spur}, \quad \textbf{(1-44)}$$

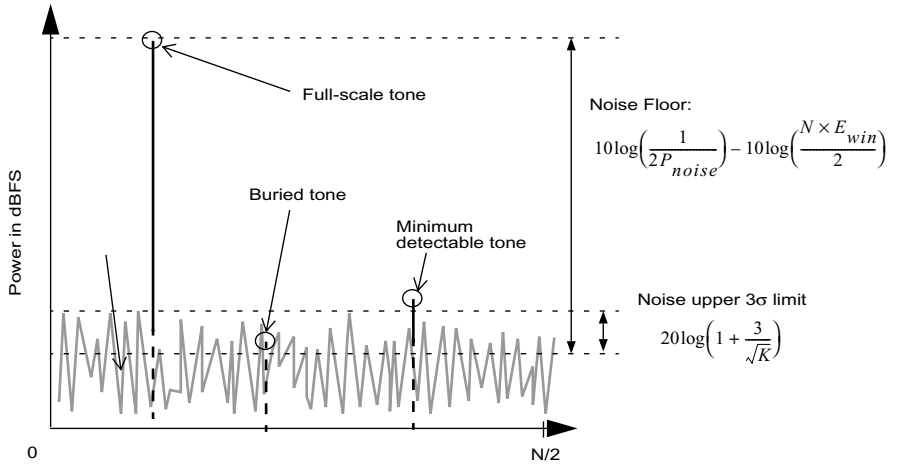


Figure 1-25: FFT noise floor and noise dispersion

where P_{noise} is the expected noise power of the converter, K the number of averaged registers and P_{spur} the power of the minimum spur that has to be detected. Notice that a full-scale tone is taken as the power reference in Eq (1-44). The last logarithmic term in Eq (1-44) stands for the dispersion of the noise floor. Figure 1-25 illustrates the contributions to Eq (1-44).

The dispersion term should be maintained below the variations of the noise spectral density that have to de detected. For instance, if an increase of 6dB of the noise density due to flicker noise has to be detected, the noise dispersion term should be lower than 6dB, which implies averaging K=10 FFT registers. Note that if the actual noise power is higher than expected, the noise floor of the obtained FFT is increased. As a result, the minimum detectable tone is higher. To compensate for this effect, the number of points in the register should be increased to decrease the noise floor. An extra guard-band may be introduced in Eq (1-44) in order to account for an unexpected increase in the noise.

Returning to Figure 1-24, the concept of signal leakage has already been explained. Considering the maximum input tone power and the frequency precision of the signal generator available, the window should be selected such that the side-lobe power falls below the noise floor. Notice that if the frequency precision of the generator is better than half the FFT

bin bandwidth, $f_{acq}/(2N)$, the side-lobe power requirements may be relaxed as the window spectra would not be worst-case sampled. Taking that case to an extreme, if coherent sampling is available in the test setup, no signal leakage occurs.

For ΣΔ converters, however, another leakage concept may have to be taken into account: noise leakage. ΣΔ converter non-idealities are located mainly in the analog part which is the ΣΔ modulator. In that sense, performing the FFT on the modulator bit-stream gives more insight into the operation of the ΣΔ modulator because it is possible to check the correctness of the noise shaping at high frequencies (beyond the cut-off frequency of the decimation filter). If the FFT is performed on the output of the decimation filter, a number of samples N has to be acquired at the filter output frequency (f_{acq}) in a high resolution format (for instance, the filter output of a 24-bit precision filter can be in a 32-bit format). If it is performed on the modulator bit-stream, a number of samples N' has to be acquired at the sampling frequency of the modulator (which is equal to the filter output frequency multiplied by the OSR) in a low-precision format (typically one bit). Taking into account that the same non-idealities have to be detected in the base-band, the same frequency resolution has to be selected in both cases. Hence, the FFT of the modulator output bit-stream requires OSR times more points than the acquisition at the filter output. The acquisition time is thus the same in both cases, and the memory requirements should be of the same order due to the difference in the samples formats. The counterpart of performing the FFT on the modulator bit-stream is that it puts more stress on the choice of the window that has to be applied to the data register. Indeed in most ADCs, the noise spectral distribution is almost flat and its power is far lower than full-scale signal power. As a result, noise leakage has little or no impact on the output spectrum. This reasoning is also valid for a ΣΔ converter if data is acquired at the output of the decimation filter. But if the FFT is performed directly at the modulator output, the spectral density of the modulator quantization noise is not flat at all and the leakage of high frequency noise into the modulator base-band could severely corrupt the FFT analysis. The window has to be chosen not only on the base of the test signal leakage but also on the basis of the spectrally-shaped noise leakage. In other words, the performance of the window depends on the attenuation of the first side-lobes for signal (or tones) leakage, and on the asymptotic attenuation for noise leakage. It can be seen in Figure 1-23 how Blackman-Harris and Rife-Vincent window achieve a low side-lobe power. On the

other hand, Hanning's window induces more signal leakage but the counterpart is that the side-lobe power greatly decreases with frequency. This window outperforms the Blackman-Harris at relatively low frequencies. It may thus be more suitable to avoid high frequency noise of the ΣΔ modulator output bit-stream leaking into the base-band. This may be particularly true if a combination of a sine-fit and an FFT is performed, as the fundamental component that is most likely to exhibit visible leakage is removed. In that case, noise leakage becomes the dominant component, unless there are high power spurious tones. In order to choose the window properly, it could be useful to simulate white noise filtered by the theoretical Noise-Transfer Function of the modulator and perform an FFT with the candidate windows. That allows one to check if the shape of the noise-floor in the base-band is higher than expected.

The main conclusion that arises from this description of characterization techniques is that whatever the employed method, a test stimulus has to be provided with more accuracy than the converter to be tested. Achieving a suitable signal source may be a challenging task, be it from a precision or speed point of view. Moreover, if all the possible codes have to be tested, the amount of data acquired increases dramatically with the converter precision, at a rate $Nf \times 2^N$, where Nf is the number of bits of the converter output word and N its specified precision. ΣΔ converters for geophysical measurements can be found with a precision as high as 24 bits, and an output word written in a 32-bit format (that includes some validity flags). The exhaustive characterization of such a converter would thus require the acquisition of at least 64Mb of data.

2

ADC TESTABILITY SOLUTIONS

Analogue-to-Digital Converters are basic electronic blocks that can be found everywhere. Indeed, since the introduction of digital processing, they have to be used as an interface to our inherently analogue world. Moreover, as have been said earlier, ΣΔ modulators have been widely used in the industry for almost two decades. Hence, the concern for the testability of ADCs and in particular for ΣΔ converters is increasing but not new. As a matter of fact, a large number of DfT solutions can be found in the literature and the goal of this chapter is to review and classify the most important proposals.

We will try to go from the most general to the most specific. Therefore, we first address some schemes that tackle problems that are common to Mixed Signal Systems. Next, we review the DfT proposals that have been designed to test Analogue-to-Digital Converters as a Black-Box; these schemes also apply to the particular case of ΣΔ converters. Finally, we will deal with some proposals that are specifically dedicated to ΣΔ converters.

At the end of this chapter, we summarize the different contributions in tabular form, presenting their benefits and shortcomings from a sigma-delta point of view.

2 • 1 General Mixed-Signal DfT

One of the major objective of Design-for-Test for Mixed-Signal circuits is to enhance accessibility and observability. Accessibility is the ability to apply a test stimulus at a given node of the circuit under test. This is of great importance in the case of SoCs, as the components primary inputs may not be accessible, which impede even functional testing. Observability is the ability to read the value of an internal node voltage or branch current. Both aspects should be contemplated with care to provide solutions that do not affect circuit performance.

Accessibility and observability have been quoted as a critical concern for quite a long time. That is the reason why the IEEE has extended the digital test bus standard 1149.1 to mixed-signal systems. This extended test bus is named 1149.4 or more simple “dot 4”. Its basic scheme is represented in Figure 2-1. Basically, the proposal consists of designing Analog Boundary Modules so as to provide an analog Boundary Scan. In that sense, the voltage at any node connected to an ABM can be shifted off-chip through the Analog Test Access Port. The main objective of the IEEE 1149.4 test bus was initially to test chip interconnects, which are known to be a critical reliability issue. Nevertheless, some room had been managed to enable core testing, as testified by several works [1].

A straightforward approach to enhance accessibility is to use multiplexers to select between the normal operation input and a test stimulus. That is more or less the technique that is used in the IEEE 1149.4 test bus to disconnect the ABMs from the core circuit or from the pads. The problem associated with such an approach is that it introduces an extra switch in the signal path, and the impact of this switch on performance has to be taken into account. This puts more stress on the design margins and should thus be avoided. Similarly, sensing an analog signal that is not the normal circuit output usually requires the use of a buffer to adapt to a test pin load. The parasitics introduced by this buffer also have to be

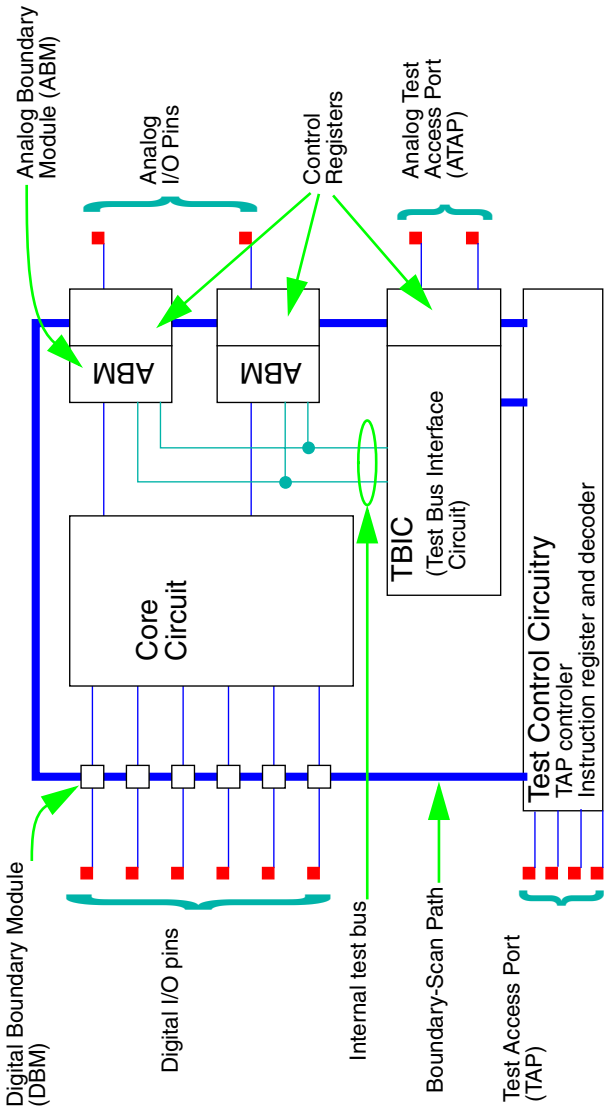


Figure 2-1: IEEE 1149.4 test bus generic scheme

taken into account. In order to cope with these issues, a solution was proposed some years ago that is called swopamp, for switched-operational amplifier. Many mixed-signal circuits and systems are based on the switched-capacitor technique. This implies that operational amplifiers are used to build filters, integrators and most functional macros. The swopamp solution consists of modifying the operational amplifier such that it is transformed during

test mode into a buffer of a test input. Such a modification can be carried out in several ways, but the key point is that it does not modify the signal path and thus has no impact on the circuit performance. The only costs associated with that solution is the area overhead and test control. Such an approach has been successfully used in a Dual Tone Multi Frequency receiver with innovative test features [46]. In that work, swopamps are used to isolate biquad filter sections from the preceding sections and to carry the test output signal to the normal output pad by reconfiguring the following stages into buffers.

2 • 2 GENERIC ADC TEST

In the field of DfT, much effort has been done to develop generic and thus reusable solutions for important macros like Phase-Locked Loops, Opamps and also Analogue-to-Digital Converters. Due to the great number of possible ADC architectures, generic ADC DfT solutions are normally derived from functional testing. Indeed the only thing that all the possible ADCs share is the way they are specified, as has been described in Chapter 1. Hence, a solution to perform an histogram test on-chip would in principle allow one to determine the Integral Non-Linearity and Differential Non-Linearity for a pipeline converter as well as a FLASH or ΣΔ converter.

Actually, most of the proposals are aimed at developing BIST schemes, as they provide the most added value. Nevertheless they seldom contemplate at the same time the two main aspects of functional BIST: on-chip test stimulus generation and on-chip test evaluation.

2 • 2 . 1 On-chip test stimulus generation

The generation of analogue signals is not a domain reserved to DfT and BIST schemes and it even constitutes a whole chapter of electronics theory. In particular, many techniques are dedicated to the elaboration of oscillators (like Colpitts or Wien-bridge oscillator). Nevertheless, a test stimulus generator should also be testable, or at least sufficiently robust to be sure that it is the circuit under test that is failing and not the test stimulus generator. Moreover, it should also be simple so as to keep its impact on chip area low. This put severe con-

straints upon the suitable candidates and that is why we review only those generators specifically dedicated to DfT.

2 • 2 . 1 . 1 Sine-wave generation

Two of the principal test stimuli for converter characterization are single and multi tone sine-wave signals. It has been seen in Section 1 • 2 . 3 that sine waves are often required to determine their dynamic characteristics. Nevertheless, the generation of sine wave signals is not an easy task. The most important advance in the field of sine-wave generation for DfT has been carried out by the team led by Gordon Roberts [47,48,49]. Their proposals can be split into two basic schemes. The first one consists of building a sigma-delta digital oscillator, by embedding a ΣΔ attenuator in a digital resonator, as seen in Figure 2-2 [47]. The selection of the attenuation coefficient (K_i) defines the oscillation frequency. The digital ΣΔ output bit stream encodes a very precise sine-wave tone (defined by the design of the digital oscillator). Then, an analogue filter has to be used to attenuate the significant amount of quantization noise. This scheme has the advantage of being mostly digital and is thus very robust and testable. However, the scheme is primarily intended for low-speed converters (and in particular ΣΔ modulators) as the maximum test tone frequency is limited by the ΣΔ oscillator quantization noise. Notice that in the case of ΣΔ modulator test, the analogue filter associated with the stimulus generator is greatly relaxed, as only the noise within the decimation filter bandwidth is of real importance. Hence, this scheme keeps the area impact low. The principal limitation of this proposal is that it can only produce single-tone waves.

In [50], Lin and Liu modify the technique so as to generate multi-tone waveforms. The core of their idea is to use Time Division Multiplexing to accommodate the additional tones. In order to maintain the same efficiency as the original scheme, the master frequency has to be raised by a factor M (M being the number of tones). Similarly, the order of the digital ΣΔ modulator that can be seen in the loop in Figure 2-2 also has to be multiplied by a factor M. Actually, each delay element in the original modulator has to be replaced by M delay elements. This scheme is thus practical only for a reduced number of tones. The authors also propose a particular 4th order leapfrog architecture for the digital ΣΔ modulator, arguing that it requires simple loop coefficients, which is key for a successful VLSI implementation. With that architecture, the authors show that the output signal for a two-tone waveform

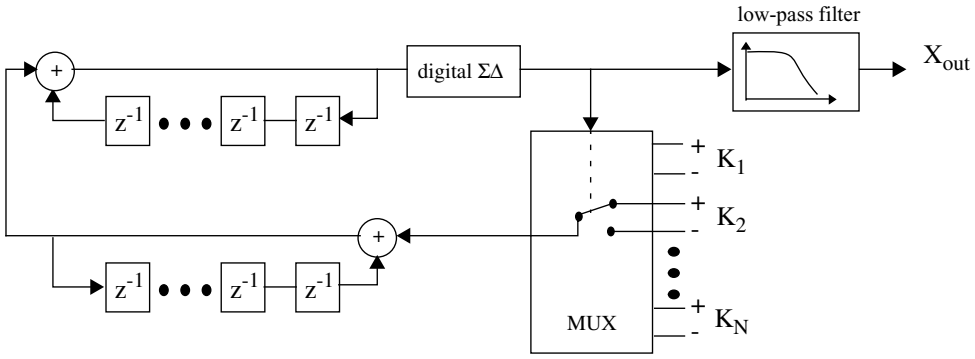


Figure 2-2: A ΣΔ oscillator with programmable frequency

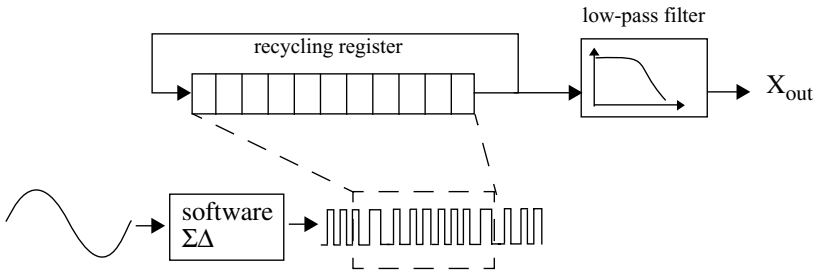


Figure 2-3: A ΣΔ programmable periodic wave

exhibits an SNR greater than 90dB with high level MATLAB simulations. Notice that for a two-tone waveform, the modulator order has been raised from 4 to 8.

The other solution proposed by the same team consists of recording in a recycling register [48,49] (i.e. a 1 bit shift register whose output is fed back to the input) a portion of a ΣΔ encoded signal. The advantage with respect to the previous proposal is the flexibility of the encoded signal, as the only a-priori restriction is that the wanted signal be periodic with a maximum period equal to the length of the register. On the other hand, the drawbacks concern the trade-off between precision and extra area. Indeed, the wider the register, the more precise the encoded signal and the larger the required silicon area. Nevertheless, if the generator had to be implemented in a chip with a testable digital part, they also proposed to reuse the boundary-scan register for the generator shift register. This would provide a potentially

large register with low overhead. Alternatively, a RAM available on-chip could also be reused. Notice that it is important to optimize the recorded bit stream to obtain the best results. The bit-stream recorded in the shift register is a portion of the output bit stream from a software ΣΔ modulator encoding the wanted test stimulus. Optimization consists of choosing the best performing bit stream portion over the total bit stream and in slightly varying the software ΣΔ modulator input signal parameters to get the best results in terms of resolution. Indeed, the SFDR results of a modulator can vary greatly with the input signal amplitude. These proposals are quite mature, and alternative generation methods for the bit stream have been shown to improve the obtained signal precision.

In [51] the authors take the idea of Gordon Roberts'team and build a fourth order ΣΔ oscillator in an FPGA to demonstrate the validity of the approach. Their oscillator was designed to avoid the need for multipliers and required around 6000 gates. They achieved more than 110 dB dynamic range for a tone at 4 kHz (the modulator master clock was set to 2.5 Mhz).

In turn, [52] presents a prototype of a signal generator that uses the idea of the recycling register. The authors propose to optimize the performance of the generator (in terms of frequency resolution as well as SFDR and THD) by selecting the proper register length for each desired signal. The prototype thus implements a programmable-length shift register (between 100 and 200 bits). Single tones between 10Hz and 1MHz can be obtained with a SFDR taht is always greater than 42dB, which is quite interesting considering the relatively small size of the register.

2 • 2 . 1 . 2 Ramp generation

The second most used test stimulus is without doubt the ramp signal. As seen in Section 1 • 2 . 2, a very linear ramp is of interest to determine the INL and DNL using a histogram (or code-density) test. In [53], the authors reuse the proposal of Roberts that has been described in previous paragraphs. Indeed, storing of a ΣΔ bit-stream in a recycling register is not restricted to sine-wave signals. Actually, any periodic signal could, in theory, be encoded in that way. That is the case of a triangular wave. A triangular wave is not exactly a ramp signal. Nevertheless, the advantage of the digitally generated signal is that it allows precise coherent sampling, as the operating frequency of the shift register can be set in an exact rela-

tion to the converter sampling frequency. Hence, the use of under-sampling may enable one to build an equivalent slow ramp. It also allows one to select either the increasing or decreasing part of the triangular wave. Anyway, notice that the triangular wave is suitable for histogram test, as the monotonicity of the test stimulus is not mandatory. Indeed, the code density associated with a triangular wave is the same as that of a slow ramp.

The generation of a ramp stimulus in an analog fashion may also be suitable for BIST applications. Indeed, a slow ramp can easily be generated with a current source loaded by a capacitor. This can simply be implemented in a CMOS technology. Nevertheless, this implementation has to be done carefully in order to avoid some shortcomings and reach an acceptable precision. In [54], the authors state that a linearity of 15 bits could be reached in CMOS (taking into account the linearity of the current source and the capacitor), which would allow the characterization of 12bit converters. However, the linearity of the generated ramp is not the only important parameter. Indeed, if the generator is targeted at histogram testing, the expected number of occurrence of each code during an evaluation period has to be precisely controlled. In other word, the ramp slope should be fixed by design. This is very difficult to achieve in CMOS where the matching of components is good but the absolute value is not so precise. A variation of 20% in the absolute value of the integrating capacitor would cause a 20% variation in the slope, which would be unacceptable. Hence, the authors propose a simple adaptive algorithm to correct the slope of the ramp, which operates on the integrating current. Given the ideal (wanted) slope and a reference voltage, the integration time necessary to reach this reference voltage after initialization can be calculated. If the actual slope is greater than desired, the reference voltage will be reached earlier and the integrating current is reduced. Conversely, the integrating current is increased if the reference voltage is reached too late. The ramp slope can be adjusted to 0.4% of the desired slope in less than 10 cycles.

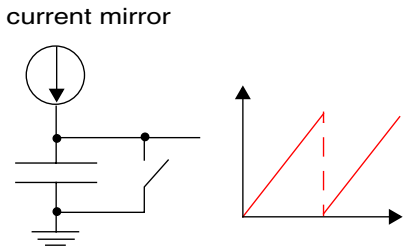


Figure 2-4: Generic scheme of a ramp generator

In [55], two architectures are discussed. The first one concerns the generation of a slow ramp and is very similar to that proposed in [54] (without calibration), but the authors point out that the current is sent to the integrating capacitor and also to the input of the converter under test. Hence, it may be necessary to introduce a buffer, which in turn requires more power and limits the achievable linearity and/or output range. The second proposed architecture tackles the issue of generating a “high-speed” triangular waveform. It is actually a relaxation oscillator (with two current sources to charge or discharge a capacitor). Notice that the authors propose to use a capacitor amplifier to reduce the required area. Both architectures have been implemented in CMOS technology. The first one reached a linearity of 0.03LSB of a 10 bit ADC for a frequency up to 10kHz, while the second one reached 0.15LSB for a frequency up to 400kHz.

Paper [56] proposes several architectures that include adaptive algorithms to generate a ramp stimulus with controlled slope. This paper also discusses possible degradation mechanisms. Moreover, the best two proposed architectures have been implemented and compared with the results of other work.

A dedicated ramp generator is also proposed in [57]. In this paper, a test interpretation mechanism is also presented but this aspect will be discussed next. The ramp generator is a transconductor that is loaded by an integrating capacitor. The slope of the ramp can thus be adjusted by tuning the voltage input of the transconductor. The authors propose to use an off-line manual calibration scheme. Two comparators are implemented on chip to detect when the ramp output is within the input range of the converter under test. By monitoring the comparator’s output, it is possible to determine the time in which the ramp has covered the ADC full scale range, and further adjust the transconductor input voltage to obtain the desired slope. This allows precise synchronization of the ramp to a counter that has a width of one more bit than the converter under test. Unfortunately, no data is provided in the paper on the performance of the resulting ramp.

2 • 2 . 1 . 3 Noise generation

Recently, a noise generator has been proposed for ADC testing [58]. The objective is to obtain a white noise generator, such that a faulty ADC is detected by an increase of the noise floor. The noise generator consists of a square wave filtered by a simple RC filter. An expo-

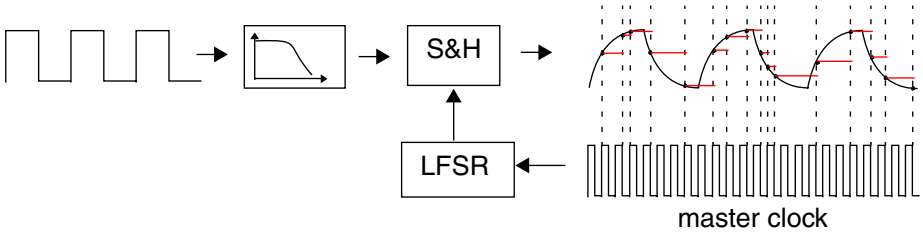


Figure 2-5: Noise generator based on a statistical sampler

nential shape periodic wave is obtained, that is further randomly sampled, accordingly to the output of a LFSR (Linear Feedback Shift Register). The necessary hardware is small and robust. Nevertheless, the white behaviour is limited to a bandwidth of 4 kHz.

2 • 2 . 1 . 4 Exponential generation

In [59], the authors propose an alternative Code Density Test (Histogram test) to determine static characteristics. Though it is not primarily targeted at BIST schemes, it tackles a similar issue. Indeed, the authors argue that it is often difficult to provide a sufficiently linear test stimulus to characterize high-standards converters. Hence, they propose to use several voltage steps filtered by an RC network to cover the whole ADC full-scale range. The theoretical code density can be calculated, just as for a classical histogram test, it only requires some more computational power for the test evaluation. However, the direct application of such a characterization scheme to BIST would require a deep study of the implementation shortcomings and the necessity of calibration.

Actually paper [60] propose two methods to use exponential signals to determine static linearity. The second one is a curve fitting like in [59] but the first one is a method that determines INL on a code-by-code basis. In this method, the time constant of the exponential is first calibrated by measuring the time necessary to reach known intermediate voltages. Then the ADC gain and offset errors are determined using the times at which the exponential test signals enters and leaves the ADC conversion range (i.e. the ADC full-scale). At last the INL at code Cx is determined by measuring the time Tx necessary to reach the code Cx. It can be calculated by subtracting the value of the exponential at time Tx from the theoretical voltage corresponding to code Cx. Notice, though, that the exponential signal should be slow in

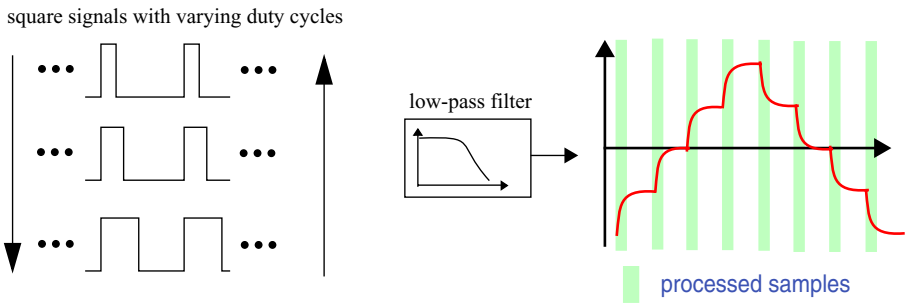


Figure 2-6: Exponential stepped signal equivalent to a ramp

order to reach a high precision. Furthermore, the fact that the INL has to be determined on a code-by-code basis greatly limit the applicability of the method to high resolution converters.

In turn, Roy *et al.* present in [61] an exponential shaped test stimulus for application in the well-known Logic-Vision BIST scheme [62]. The idea is to use pulse width modulation to encode 5 different DC levels digitally. Using an RC network to low-pass filter the digital waveform, the corresponding DC levels can be retrieved. Alternating the PWM codes as shown in Figure 2-6, a waveform with exponential steps is obtained. The digital PWM is proposed to be performed on-chip, while the RC filtering would be done off-chip, with hand selected resistors and capacitors. This would thus require two extra pins, and a BOST (Built-Out Self-Test) would be obtained. Note that the RC network has to be external because absolute component value in CMOS technology can exhibit unacceptably large dispersion. For the proposed BOST scheme, only the settling part of the exponential steps would be used, which translates to an increase of test time, as the plateau of the steps have to be discarded.

2 • 2 . 2 Test interpretation

Test interpretation and evaluation are almost as important as test stimulus generation. Indeed, though the mechanisms are known (because they are used for characterization), they usually cannot be implemented on-chip due to the required memory and processing power. For instance, a DSP unit can be used to calculate a Fourier transform only if it is already

available on-chip. Hence, we will focus at this point on the clever solutions that have been proposed in the literature to implement simplified functional test evaluation.

Among the solutions that focus on reducing the hardware dedicated to test data analysis, the work of Gordon Roberts's team can once again be stressed. Indeed, they have proposed solutions to extract some dynamic parameters in association with their sine-wave generation mechanism. In [63], they compare three possible solutions. The first one is straightforward. It comprises the implementation of an FFT engine. Though it provides good precision, it is not affordable in the majority of cases (if a DSP is not available on-chip). The second one consists of using standard linear regression to perfrm a sine-fit on the acquired data. The same master clock is used for the sampling process and the test stimulus generation. The input frequency is precisely known, which avoids the necessity of using a non-linear four-parameter search. The precision of the SNR calculation is similar to that obtained using FFT, but less hardware is required. However, some multiplications need to be performed in real-time and some memory is also required to tabulate the values of the sine and cosine at the test stimulus frequency. The third and last proposed solution is to use a digital notch filter to remove the test signal frequency component and calculate the noise power and a selective band-pass filter to calculate the signal power. The required hardware to implement this method is less than for the other two solutions, as no memory is needed to tabulate cosine values and no real-time multiplication is required. The price to be paid is a small reduction in SNR precision and that the test time is slightly increased to account for the filter settling time. Actually, the more selective the filter, the better the SNR precision but the higher the settling time. Extensions of this work [64] also showed that it was possible to extract harmonic distortion and inter-modulation distortion with similar digital filtering.

Apart from dynamic testing, some solutions have also been proposed to interpret on-chip the results of a code density test. One of them is that of De Vries *et al.* [65]. Their solution is targeted at a slow ramp code density test. What they propose is to monitor only the LSB, arguing that a transition between two codes for a slow ramp input is always defined by a change in the LSB. This is true only if the converter non-linearity is taken into account. However, if noise (thermal and jitter) variance is significant with respect to the quantization step, the principal assumption does not hold true and a toggling between adjacent codes can

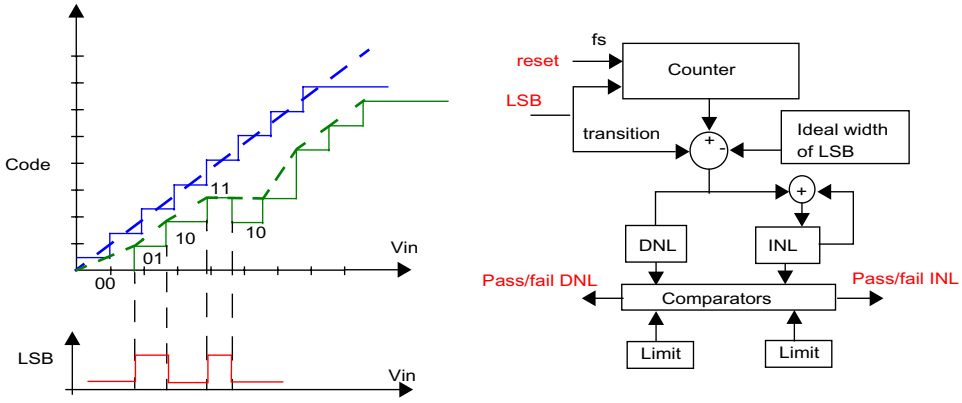


Figure 2-7: On-chip INL and DNL checking by monitoring LSB

be seen at code transitions. The authors propose to use a digital low-pass filter to remove most of the noise. Then, a simple counter accumulates the number of samples between two consecutive LSB changes. This gives a measure of the code DNL. Similarly, the DNL values are accumulated to get the INL for each code. Both measured INL and DNL values are compared directly to an ideal value stored on-chip. If the measured values exceed an allowable amount, a fail flag is sent as a BIST result. This paper also provides a statistical analysis to evaluate the expected probability of failed good devices and passed bad devices, as a function of the counter width (i.e. the number of samples per code).

Wen and Lee have proposed a similar scheme [57]. They use a digitally controlled ramp with one more bit of resolution than the ADC under test. A transition between two codes is determined by monitoring the converter LSB. Then, simple INL and DNL detectors are derived that compare the ADC output with a counter that is synchronized with the input ramp. The main limitation of the proposed scheme is that it is limited to a precision of 0.5 LSB. On the other hand, only simple logic gates are used, and the area overhead associated with the detectors is very low. However, the paper does not contemplate possible error mechanisms such as noise or input ramp non-linearity.

The work realized at the LIRMM by Michel Renovell's team is worthy of consideration. They have done a good job to minimize the hardware necessary to implement an histogram test. In [66], they first state that the ramp histogram is much more efficient than a sine-wave

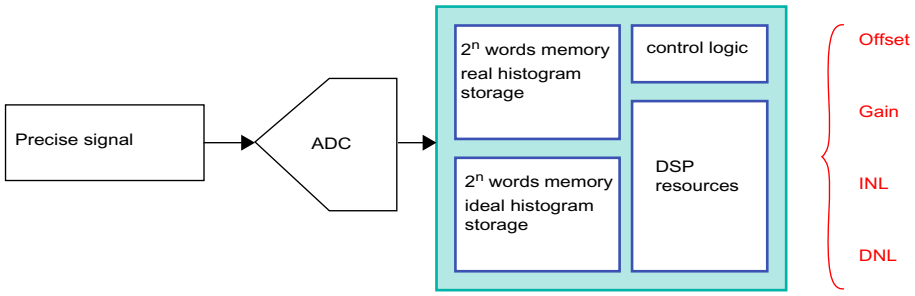


Figure 2-8: Generic hardware required to perform an histogram test

(or other) histogram from a hardware point of view. Indeed, the tabulation of the ideal results for a linear ramp histogram only requires two words: one for the two extreme codes (that are more excited due to the designed over-range of the ramp), and one for the intermediate codes, that all have the same density. Then, in [67,68], they propose a full implementation, with optimized hardware resources. They propose to decompose the test sequentially, not only for the type of measurements (gain, offset, DNL and INL) but also for the codes. In other words, DNL and INL evaluation are carried out on a code by code basis: only one code is considered per run. They implement the proposed hardware together with a 6bit FLASH ADC, and obtain a quite reduced 6.7% area overhead. Obviously, this sacrifices much test time compared to the case where only one run was necessary, because 2N runs are now required (N being the converter number of bits). Hence, this scheme should be limited to converters with relatively low resolution. Indeed, the authors point out that a complete test of a 14bit converter at a sampling frequency of 1MHz would take 5h22mn, which is totally unaffordable. By contrast, the test of an 8bit converter at a 100MHz sampling frequency would require only 50ms. Moreover, they conclude this article opening a possible trade-off between extra hardware and test time. Indeed, a p-after-p code sequence evaluation could be used instead of code after code evaluation.

Last but not least, Bozena Kaminska's team has developed a BIST scheme based on the servo-loop method [69]. In their method, the ADC output is made to oscillate between two reference codes. A triangular wave is generated by a relaxation oscillator controlled by the ADC under test output. Actually, a current source charges a capacitor while the ADC output code is lower than the upper specified code. Once this specified code is reached, another cur-

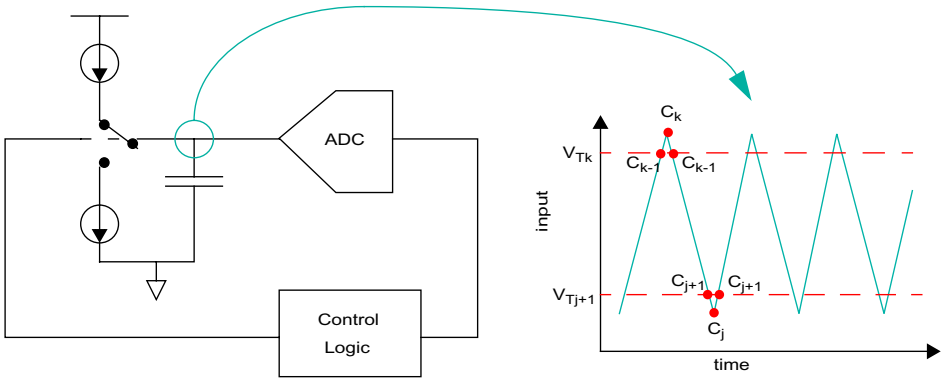


Figure 2-9: A BIST application of the servo-loop principles

rent source discharges the capacitor until the lower reference code is reached, and so on. The frequency of oscillation is directly proportional to the voltage difference between the transitions associated with the specified codes. Hence the DNL and INL can easily be derived by measuring the oscillation frequency. It is worth noticing that it is quite easy to measure a frequency, because any linear filtering will not alter the result whenever the fundamental frequency is preserved. Hence, it is quite easy to ship the test signal out of the chip even in embedded systems, through buffers and busses, without losing precision on the test result. Moreover, the influence of white noise can also be averaged out if the frequency is measured over a sufficiently large number of samples. In the servo-loop method, however, the oscillation is filtered out and the test output is the DC voltage component of the oscillation, which has to be measured precisely. This is a fundamental difference, because it allows one to use quite an imprecise integrator. Indeed, if the oscillations are restricted to adjacent codes and the ramp is locally linear, the DC component of the oscillation coincides with the average between the two transition voltages involved. However, the oscillation frequency depends on the slope of the integrator. Therefore, the global linearity of the integrator is important. Actually it should be better than the ADC under test.

2 • 3 MODEL-BASED TEST

One of the main limiting factors for the direct application of functional test to BIST schemes is the amount of data that has to be acquired and processed. This obviously has an impact on the processing power required (including memory) and on the test time. However, test is not the same as characterization and a large number of researchers have postulated that in some cases good fault coverage could be obtained with a test that is far from being exhaustive.

2 • 3 . 1 Fundamentals of the model-based approach

The model-based test approach has been developed mainly by Stenbakken and Souders but other researchers have then followed their path and a large number of papers describe most of the advantages and drawbacks of this approach [70-74]. The idea consists of building a parametrized model such that the number of parameters is much lower than the number of measurement to be performed. Hence, only a subset of measurement is necessary to determine the parameters and the rest of the measurements can be extrapolated using the model.

The model-based approach relies on the assumption that the performance of a circuit is correlated with a small number of core parameters. Hence, if one knows these correlations, the performance evaluation can be performed by determining the core parameters. The set of correlations between the core parameters and the performance measurements actually forms the model.

The relation between performance and core parameters can be non-linear. However, a commonly used method to simplify non-linear problems is to consider that only small variations occur around the nominal operating point (set by design). Hence, a first order approximation can lead to sufficiently accurate results. That is the basis of the linear modelling.

Though the concept of model-based test is relatively simple, it implies two different tasks that have to be detailed:

- How to retrieve the model parameters and evaluate the performance
- How to determine the model, which implies the determination of the core parameters and their correlations to the performance measurements

Given a number M of specifications [s] to be tested, the model-based testing approach assumes that they can be linearly related to a number P of parameters [x]. We can thus write

$$[s] = [A][x] + [s_0], \quad \text{(2-1)}$$

where [s_0] is the vector of the nominal specification measurements. Matrix [A], of size M*P, is the linear model of the circuit.

If P is less than M, the system is over-dimensioned and only a subset [s_b] of P specification measurements would be necessary to determine the model parameters [x].

$$[s_b] = [A_b][x] + [s_{b0}] \Rightarrow [x] = \left[A_b^{-1}\right]\left([s_b] - [s_{b0}]\right) \quad \text{(2-2)}$$

Once the model parameters are determined, it is easy to determine the specifications that were not measured through Eq (2-1).

Due to noise considerations and the limited precision of the specification measurements, it may be necessary to perform the measurements over a set wider than P. The selection of the number of specifications to be measured and which of all the possible subsets has to be chosen is an optimization problem.

The most important point of the model-based approach is without doubt the determination of the model (i.e. matrix [A])

One of the ways to derive an efficient model consists of identifying the mechanisms that can potentially impact the specifications that have to be tested for. This method is known as *a-priori* modeling. Obviously this requires knowledge of the exact circuit architecture and implementation together with a deep understanding of its functioning. Even more, statistics on the process variations should also be available, as most parametric failures are due to unexpected drift of some of these parameters. A systematic approach for the model derivation would then consist of performing a sensitivity analysis around the normal operating point. All parameters that impact the specifications would be selected to form the final model. The main shortcoming of this approach is that the sensitivity analysis is limited to the parameters that have been identified by the designer. An unidentified degradation mechanism may thus produce test escapes.

On the other hand, the model can also be derived in an empirical manner. From a statistically significant set of devices, an empirical model is retrieved by singular value decompo-

sition. The number of devices that have to be characterized fully to generate the model put a fundamental limit on the maximum achievable model order. Let S be the matrix of M raws and P columns representing the measurements performed on the set of P devices. Each column correspond to one device. Let also S_0 be the vector average of the P columns of S. ΔS is the matrix obtained by subtracting S_0 from each column of S. Model A is obtained by singular value decomposition of ΔS, namely

$$\Delta S = ADV^T. \quad \textbf{(2-3)}$$

Matrix D is the matrix that contains the singular values of ΔS. Though A and S_0 will form the model corresponding to Eq (2-1), the singular values of ΔS also serve to optimize the model order. Indeed, A and V are unitary matrices that just define a projection from the space defined by the set of specifications S to the space defined by the eigenvectors corresponding to the singular values of D. Hence, all the information about the sensitivity of the specifications to the model parameters is contained in matrix D. The lowest singular values correspond to parameters that influence the specifications to a lower extent. Hence, a possible optimization of the model order would consist in selecting only the parameters whose singular value are above the variations related to measurement noise. In terms of the model, it would consist of selecting the columns of A that correspond to the set of selected singular values. The model quality is determined by a lack-of-fit figure of merit.

The main advantage of such an approach is that it can easily be generalized as the methodology does not require any particular knowledge of the circuit under test. That is why it is called *blind* modelling. However, the modelling method still implicitly assumes that the variations are small around an ideal operating point. By contrast with the sensitivity analysis approach, the empirical modelling provides no insight into the validity range of the linear assumption.

Nevertheless, in [70], Stenbakken and Souders built a model for a 13-bit ADC out of the exhaustive INL measurements of 50 devices. Thanks to that model, they managed to predict the INL of 77 unknown devices by measuring the INL at only 64 codes (out of 8192), with a maximum error of 0.08 LSB.

2 • 3 . 2 An application of the model-based approach to BIST

A model-based BIST scheme that is worth of mention is without doubt the one proposed by Roy and Sunter [62]. Accordingly to Stenbakken, it could be classified as a-priori modelling. Indeed, it consists of considering the ADC transfer function as a third order polynomial. This is a very coarse assumption, but these researchers showed that it was a valid assumption for most of high-resolution ΣΔ modulators. Based upon this assumption, they developed a very simple test to determine the polynomial parameters. As seen in Figure 2-10 a ramp stimulus is used as an input and the ADC output is integrated over each of the four quarters that divide the time necessary to reach the ADC full-scale. Only four signatures have to be processed with low speed arithmetic to retrieve the polynomial parameters or the related gain error, offset, 2nd and 3rd order distortion.

One may wonder how a model as simple as a 3rd order polynomial could reliably represent the rich behaviour of ΣΔ modulators, but the fact is that this BIST scheme is actually commercialized and used in the industry. The authors propose a very simple test to retrieve the coefficients of the third order polynomial, which is none other than model parameter identification. It consists of submitting the ADC under test to a ramp input covering the full-scale, and accumulating the output samples over four regions dividing the full-scale. Four signatures, S_0, S_1, S_2 and S_3 are thus obtained, which would correspond to four measurements, and simple arithmetic is then used to retrieve performance specifications such as gain, offset, 2nd harmonic amplitude and 3rd harmonic amplitude.

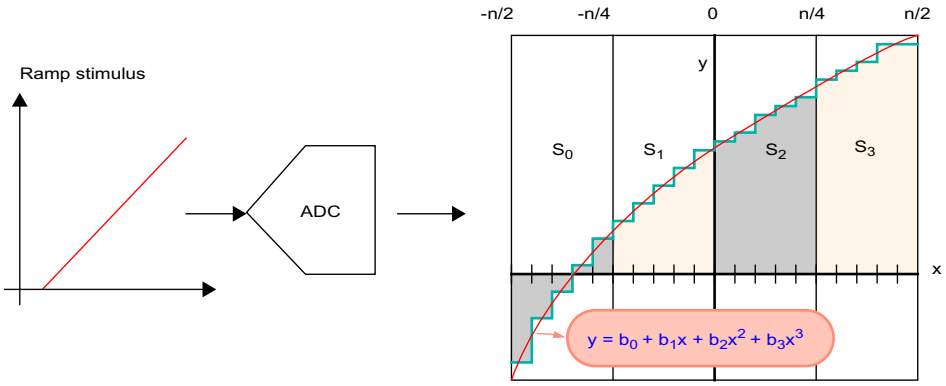


Figure 2-10: Test with a 3rd order polynomial model

Let the polynomial representing the transfer function be

$$y = b_0 + b_1 x + b_2 x^2 + b_3 x^3 . \tag{2-4}$$

The authors demonstrate that the coefficients of the polynomial can be written as a function of the signatures

$$\begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & 0 & \frac{-4}{3n} & 0 \\ 0 & \frac{4}{nr} & 0 & \frac{-16}{3nr} \\ 0 & 0 & \frac{16}{nr^2} & 0 \\ 0 & 0 & 0 & \frac{128}{3nr^3} \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} \tag{2-5}$$

$$\begin{bmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 \\ -1 & 3 & -3 & 1 \end{bmatrix} \begin{bmatrix} S_0 \\ S_1 \\ S_2 \\ S_3 \end{bmatrix}$$

The relationship between the model parameters (the b_is) and the performed measurements is linear and is written in a matrix format, according to the previous sub-section. From the model parameters, performance specifications can be retrieved. Indeed, the third order polynomial transfer function leads to

$$\begin{aligned} offset &= \frac{1}{n}\left(B_0 + \frac{2}{3}B_2\right) \approx \frac{B_0}{n} \\ gain &= \frac{4}{nr}\left(B_1 + \frac{2}{3}B_3\right) \approx \frac{4B_1}{nr} \\ A_{harm2} &= \frac{B_2}{B_1 + \frac{2}{3}B_3} \approx \frac{4B_2}{nr} \\ A_{harm3} &= \frac{2B_3}{3\left(B_1 + \frac{2}{3}B_3\right)} \approx \frac{8B_3}{3nr} \end{aligned} \tag{2-6}$$

The reader should notice that the relationships between the harmonic amplitudes and the model parameters are not linear. Nevertheless, if we take first order approximations on the right hand side of Eq (2-6), we can write everything according to the model-based formalism as

$$\begin{bmatrix} S_0 \\ S_1 \\ S_2 \\ S_3 \\ offset \\ gain \\ A_{harm2} \\ A_{harm3} \end{bmatrix} = [A] \begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix}. \qquad \textbf{(2-7)}$$

Matrix A could be calculated explicitly from Eq (2-5) and Eq (2-6) but it would require some matrix inversion. However, the reader should notice that the relationships already available correspond to those that are necessary to perform the test. Indeed, the subset of measurements actually performed is $\{S_0,S_1,S_2,S_3\}$; this can be mapped onto the intermediate step $\{B_0,B_1,B_2,B_3\}$. This step corresponds to equation Eq (2-2) in previous sub-section Then, matrix A is used to map the model parameters back onto the measurement space (according to Eq (2-1)) but more specifically onto the unknown subset {*offset, gain,* A_{harm2}, A_{harm3}}.

Hence, the conclusions of this example are twofold:

- Ad-hoc tests other than direct specification measurements can be designed to retrieve the model parameters in a simple and reliable way (i.e. the tests signatures have a simple relationship with the parameters)
- The validity range of the linear approximation relating the tests signatures and the model parameters can be improved by the use of ad-hoc tests. Even more, once the behavioral parameters have been identified, the relationship between the model parameters and the performance specifications does not need to be linear anymore.

2 • 4 ΣΔ SPECIFIC TESTS

We have described in the previous section some DfT techniques that apply to black-box ADCs and that can thus be considered for ΣΔ modulators. However, the case of ΣΔ modulators in somewhat particular in the sense that a ΣΔ ADC consists of a ΣΔ modulator followed by a decimation filter. It is a very peculiar structure that was built specifically to take advantage of the major robustness of digital circuitry. Hence, an important part of the conversion job is realized by the digital filter and the modulator in itself requires relatively few components. Considering the ΣΔ ADC as a black box is possibly not the optimum solution. It could be possible to test the digital filter using well-known DfT schemes, and to test the modulator as a stand alone part.

Despite the attractiveness of dedicated test solutions for ΣΔ modulators, only a few papers can be found in the literature.

One of the first papers [75] that tried to take advantage of the ΣΔ modulator structure takes as an example a double-loop bandpass modulator. The authors propose to reconfigure the modulator in test mode as shown in Figure 2-11. The two loops of the modulator are split and the two resonators are reconfigured in a unity gain feedback loop. The test consists of sending an identical test stimulus (typically a sine-wave) to the two resonators and compare their output, that should be identical. This comparison is carried out re-using the modulator comparator: the two resonator outputs are subtracted and compared with the tolerance window (defined by two DC levels) in a sequential manner (with one level on the rising edge of the clock and with the other on the falling edge). A fault analysis considering single shorts, stuck-open and stuck-on faults in the switches as well as 50 to 200% deviations in the capacitor values was carried out and showed that the fault coverage depended on the tolerance window but converged to 100% for small window. A shortcoming of this technique, however, is that global parametric defects or even soft defects may be difficult to detect. Indeed, if a defect affects the two resonators in the same way, the comparison will always be good but the modulator may deviate from its specifications. On the other hand, this test is very simple, can be performed with any input signal, and does not require extra hardware apart from some control logic.

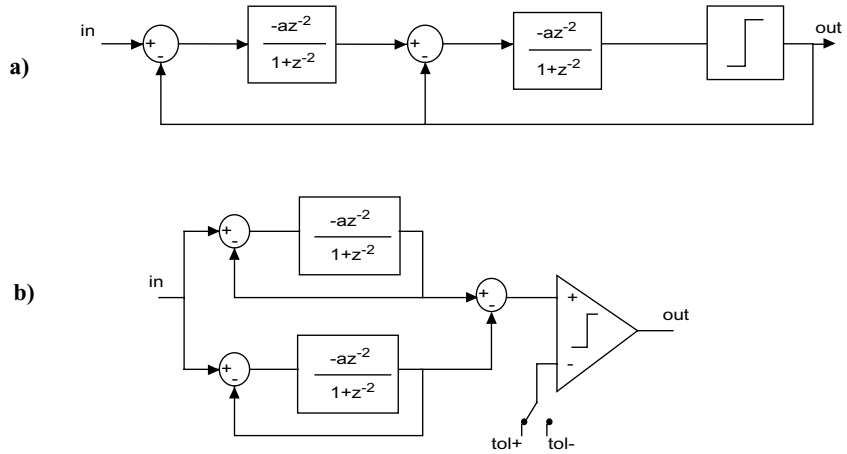


Figure 2-11: a) double-loop bandpass ΣΔ modulator; b) reconfiguration in test mode

In [76], The authors focus on the detection of integrator leakage in a second-order ΣΔ modulator. Indeed, integrator leakage is an important concern in ΣΔ modulators and mostly in cascaded ones. Integrator leakage is directly related to the DC gain of the amplifier used to build the loop integrators, and is thus likely to be affected by faults occurring in the amplifiers. The interest of their proposal is that they use as a test stimulus a pseudorandom digital sequence that is sent to the modulator through its feedback DAC. This avoids the use of a precise test stimulus and enables cheap on-chip signal generation. On the other hand, the test response analyser requires an exhaustive exploration of the frequency-domain response so as to determine the spectrum regions that are most sensitive to leakage.

The same authors made another interesting proposal, focusing on the stimulus generation [77]. They argued that the test stimulus generation scheme proposed in [48] could be used for ΣΔ modulators without the need for any anti-aliasing filter. They proposed to use a stored bit-stream of the same order as the modulator under test and to send it to the modulator through its feedback DAC but with an attenuation coefficient. Hence, the power spectrum is shifted down for both the encoded sine-wave and the input bit-stream quantization noise. The consequence is that the input quantization noise should be buried in the output quantization noise at the output and thus enable a classical spectral analysis. A shortcoming of this

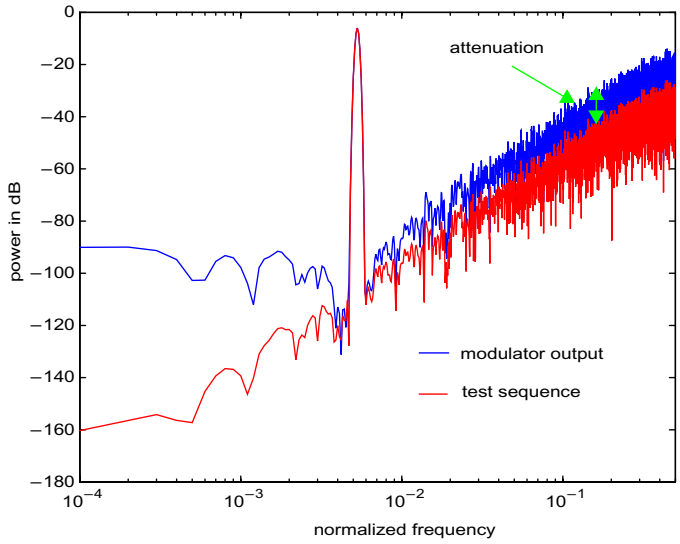


Figure 2-12: Input and output of the modulator under test

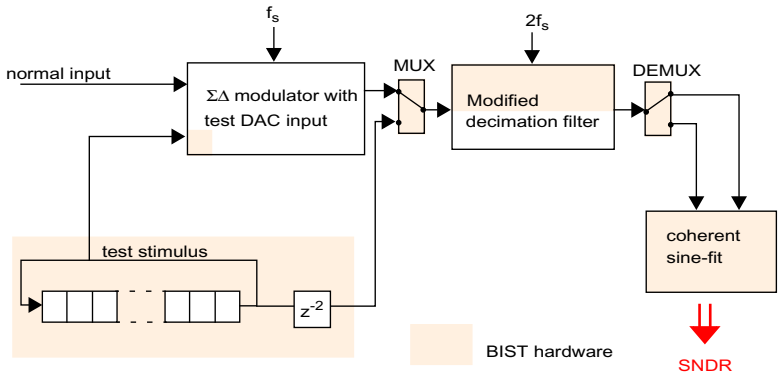


Figure 2-13: Digital sine-fit BIST setup

approach may be that the dynamic behaviour of the modulator is not the same for a continuous input signal as for a digital sequence, so that the results of the THD test may be biased.

In [78] a similar idea is followed, as can be seen in Figure 2-13 that shows the BIST setup. The test stimulus is a sine-wave encoded in a ΣΔ bit-stream of one order higher than the modulator under test and stored in a recycling register (a 3rd order bit-stream is used in the paper to test a 2nd order modulator). The test stimulus is sent to the modulator through a dedicated one-bit DAC that provides a 1/4 attenuation with respect to the feedback DAC.

The goal of this attenuation is not to obtain a lower noise base-band like in [77] but to avoid integrator saturation due to the presence of high power quantization noise in the test signal together with the test sine-wave. Apart from the stimulus generation, a clever sine-fitting algorithm is proposed that makes use of the available decimation filter. The decimation filter has to be designed with one order more than what would in principle be necessary, has to work at twice the modulator frequency and uses two extra bits for internal calculations. This makes it possible, by use of time multiplexing to process in parallel the modulator output bit-stream and the delayed test signal. The sine-fitting algorithm is then simplified due to the fact that the modulator output signal can be compared with the corresponding in-phase pure reference signal. After gain and offset corrections, the SFDR is extracted. The method shows good results in simulation and is able to detect most faults. However, the fact that the test stimulus contains a significant amount of quantization noise limit the capability to detect correctly detect faults that produce distortion.

In [79], the authors propose to apply the concept of Oscillation-Based Test to ΣΔ modulators. Indeed, they argue that a modulator contains the elements necessary to make a sustainable oscillator: the loop filter and a non-linear element (the comparator and the feedback DAC) to control the oscillation amplitude. Hence, the area overhead due to the application of OBT should be minimum. Nevertheless, high level simulations showed that the oscillator built out directly from the ΣΔ modulator was easily locking into limit-cycle behaviors, that masked the presence of errors. Indeed, the very principle of OBT is to detect faults in the circuit through the deviation of the oscillation frequency and/or amplitude from the nominal (expected) one. Hence, if the ΣΔ oscillator locks into a limit cycle, the oscillation frequency and amplitude may remain the same over a non-negligible range of operating conditions. In other words, the same oscillation could be produced for different values of capacitor ratios. To solve this issue, the authors determined that it was necessary to add some elements so as to transform the filtering function, as can be seen in Figure 2-14.

By doing so, the resulting oscillator is much more immune to limit cycles and the sensitivity to circuit faults is recovered. However, one concern with OBT in general is that it is mostly devoted to the detection of catastrophic faults in the switches or parametric faults in the capacitor ratios. That could be sufficient in some cases where the spot defect model can

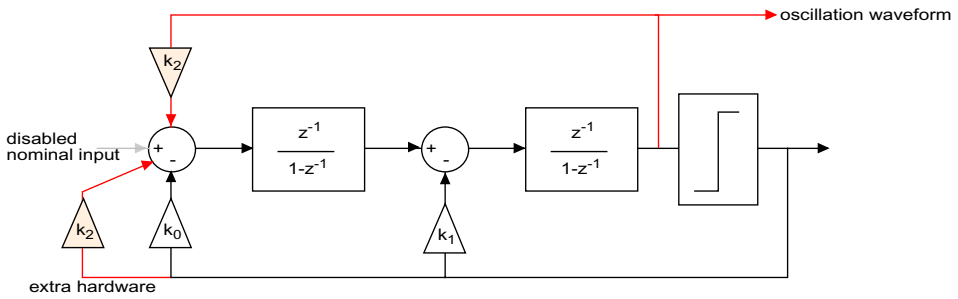


Figure 2-14: OBT applied to a 2nd order modulator

fully apply. In more complex situations where the environmental stress conditions have to be taken into account, some other kind of faults would appear. Furthermore, in most sub-micron processes, the spot defect model may not be sufficient to describe all the possible shortcomings that can affect analog designs. For instance, the performance of some ΣΔ modulators is greatly related to the DC gain of the amplifiers, which could in turn be affected by a wide variety of process variations. These kinds of parametric faults are unlikely to be detected by OBT.

De Venuto *et al*. proposed in [80] to use an alternative input point to test ΣΔ modulators. The intention is to inject a test signal at the input of the modulator quantizer. This test signal is processed by the modulator just like the quantization noise. In that sense, the authors argue that they can determine the modulator Noise-Transfer Function accurately. Although it is true that many defects or non-idealities can affect the modulator noise-transfer function and should thus be detected, other are intrinsically related to the input signal. The best example is given by those defects that cause harmonic distortion such as non-linear settling of the fist integrator. Such a defect would not be detected by the proposed method. Similarly, it is worth wondering if the input of a test signal at that point significantly alters the non-linear dynamics of the modulator under test. In particular, much care should be taken for high order modulators to ensure that they are not driven into instability. Nevertheless, the main advantage of the approach is that it is applicable, in principle, to any modulator architecture.

In [81], a divide-and-conquer approach is proposed by the author to detect the main degradation mechanisms in high-resolution cascaded ΣΔ modulators while relaxing test require-

ments. The main idea is that the performance of the modulator relies principally on the behaviour of the first integrator. Hence, it is proposed to test this integrator by reconfiguring it as an amplifier. Furthermore, the rest of the modulator is reconfigured to form a lower-order modulator and converts the error signal obtained from the first integrator (reconverted in an amplifier). Guidelines are given in the paper to build signatures related to the DC gain and the settling of the first integrator but are not explicitly justified. In the same paper, a description is given of the design of a prototype that includes interesting DfT features: buffers are added at the outputs of the integrators to provide monitoring and OTAs are replaced by swopamps to enable modulator reconfiguration and test signal injection at internal nodes. Electrical simulations show that these features can be implemented without much impact on block specifications.

Partial results of the work developed in this thesis have already been published [83-90].

Table I: summary of test techniques applied to ΣΔ modulators

	Pros.	**Cons.**
Characterization		
Static parameters: Histogram Servo-loop	Gives access to gain and offset errors, INL and DNL	Exhaustive characterization requires a large amount of time INL and DNL should be related to transitions in ΣΔ modulators Requires the input of a precise stimulus
Dynamic parameters: Sine-fit FFT	Provide important datasheet specifications (SNR, THD, ENOB, …)	Requires complex DSP Requires the input of a precise stimulus
Functional Test		
Roberts [63-64]	Provides a solution to precise on-chip stimulus generation Digital filter solution to relax data analysis	Requires a DSP on-chip The area overhead associated with stimulus generation may be large The re-use of on-chip resources makes concurrent test of other SoC parts difficult

Table I: summary of test techniques applied to ΣΔ modulators

Ong [77]	The test stimulus is an unfiltered ΣΔ digital sequence	The test signature aspect is not solved The potential effect of unfiltered high-frequency noise in the input on the result validity is not addressed
Rolindez [78]	The test stimulus is an unfiltered ΣΔ digital sequence A sine-fit is performed on-chip by adapting the decimation filter	The test sequence cannot use the same DAC as the modulator Some defects do not affect the SNDR obtained with digital sequences in the same way as with sine-waves
Defect-oriented Test		
Reconfiguration [75]	No extra hardware is required Any input signal can be used	Requires a strong reconfiguration of the modulator. May be difficult to generalize to other architectures. The calculation of test coverage for any input is difficult to perform
OBT [79]	No test stimulus is required The data analysis is generic as the signatures are always amplitude and frequency A good methodology has been developed to apply the solution to any architecture with relative effort	The calculation of test coverage for faults other than capacitor ratio errors is difficult
Noise Transfer Function [80]	The test stimulus does not have to be as precise as the modulator The methodology is applicable to any modulator	The defect coverage may be low as some non-idealities do not impact the Noise-transfer Function The validity of the approach should be better demonstrated
Pseudo-random [76]	The input is digital and relatively cheap to produce on-chip	The validity of the heuristic model obtained through simulation is questionable Potential fault masking Only integrator leakage is addressed
Divide-and-Conquer [81]	Relax test requirements by focusing on building blocks	Does not provide justification for the proposed test signatures.
Model-based Test		

Table I: summary of test techniques applied to ΣΔ modulators

Model-based test Standard approach [70-73]	Relaxes the number of required measurements A good methodology exists.	The model is linear and performs well for small variations but may be limited for other defects. The methodology is based on standard specification measurements: it requires a precise stimulus and a DSP.
Ad-Hoc Model-based BIST [61-62]	The test stimulus can be partially generated on-chip. The data analysis is very simple and can be performed on-chip. Important specifications can be derived	The model is taken a-priori and not justified: its validity range may be questionable. Only four parameters are obtained: gain, offset, 2^{nd} order distortion and 3^{rd} order distortion. The test stimulus generation still requires off-chip components
Design-based BIST [83-90]	The test stimulus is digital The test requires few resources and simple modulator modifications The test signatures can be used for silicon-debug The test strategy can easily be integrated in the design flow The model is a validated-by-design behavioral model The validity has been proven for cascaded modulators of 1^{st} and 2^{nd} order sections	Research is still necessary to test more behavioral parameters. The extension of the approach to other modulators would require further research.

3

THE PROPOSED TEST APPROACH

In this chapter the principles of our test methodology for ΣΔ converters will be presented. The first section describes the test proposal, its philosophy, what motivates the approach and also discusses its particular implications. The second, in turn, is more practical and details the method followed to reach the defined purposes. It also settles the common framework necessary for a good understanding of the detailed test descriptions that will be presented in the next two chapters.

CHAPTER 3

3 • 1 DESCRIPTION OF THE IDEA

Analog-to-Digital converters are becoming more and more difficult to characterize, as their resolution and sampling frequency increase at a steady rate. In particular, for those based on ΣΔ modulation, the main shortcoming for functional test is the complexity of performance measurements. Indeed, ΣΔ converters commonly reach high resolutions (up to 24 bits), which impose the use of the highest resolution test stimuli and reference voltages and huge data acquisition and processing. Innovative solutions are thus required.

Our goal is to determine the main characteristics of the ΣΔ modulators building blocks. In that sense, our proposal can be seen as a particular case of model-based test, which has been seen to offer a high potential for test cost reduction. Instead of a linear model built from a small set of devices, we simply use a block-level behavioural model. Similarly, the proposal can be seen as a "divide-and-conquer" approach, although we will see later that the modulator is not physically divided in building blocks during test. Another way to present it is to speak of "design-based test" as in [82], because the parameters that we want to determine are precisely block-level "design parameters".

3 • 1 . 1 Motivations

To illustrate the idea behind the proposal, let us consider Figure 3-1, where a design flow and different test flows are represented. For linear circuits, analytical functions that relate the circuit performance to transistor parameters can usually be calculated manually or with symbolic analysis tools. The design space can thus be explored efficiently to find the optima of a design cost function. Due to the nonlinear feedback no such relations can be found for ΣΔ modulators. Indeed, the non-linear dynamics of ΣΔ modulators make analytical studies overwhelmingly complex. No closed-form expression can thus be derived that relates performance figures like THD or SNR to design parameters. On the other hand, electrical simulations of a complete ΣΔ modulator are far too long to allow design-space exploration. Hence, designers have been forced to build behavioral models in a variety of high level languages like Matlab (and its Simulink extension) [35, 24], VHDL-AMS, and even standard VHDL [36], etc. These models decompose modulators into functional macros that

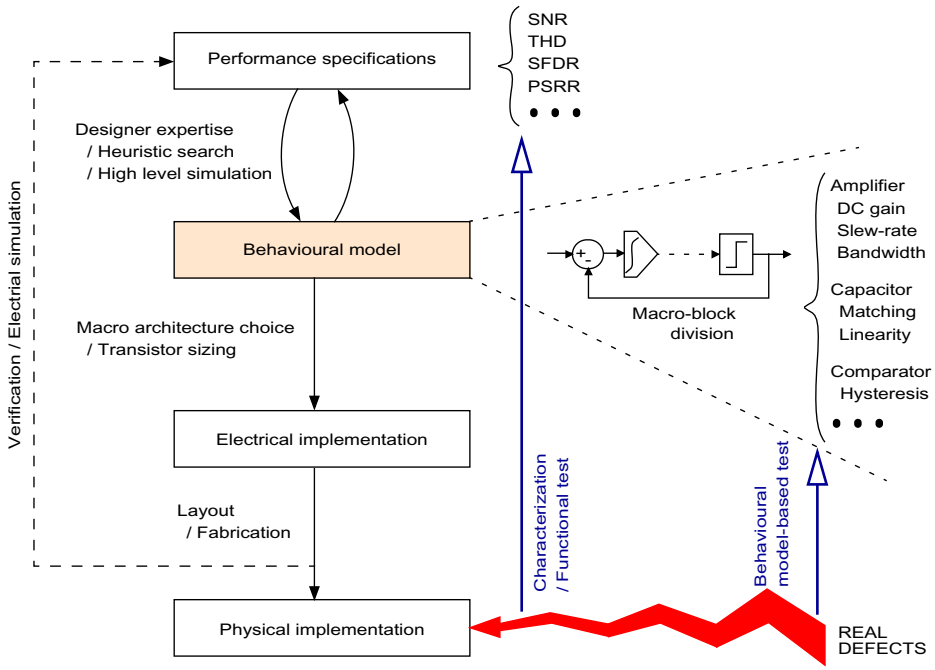


Figure 3-1: Behavioural model in the design and test flow

take into account most of the effects that are known to influence performance [38]. The validity of the model for test purpose is thus ensured by the fact that it is used precisely to explore the design space over a wide range of values. Furthermore, the model elaboration does not represent any extra cost for the test approach.

From a structural test viewpoint, the behavioral parameters are related to the different macros (i.e. building blocks) that are used to describe the model: integrators, comparators, switches... They are the design variables that the designer is used to managing. The test is thus closely linked to design and the test outcome is directly meaningful to the designer. Testing circuit macros has the advantage of providing some insight into the circuit failure mechanisms. By providing fault diagnosis at the macro level, such a test approach can also be useful for silicon debug.

From a functional test viewpoint, determination of the behavioral parameters that characterize performance degradation mechanisms would allow one to test the modulator performance indirectly. The relation between behavioral model parameters and performance may

be non-linear and quite complex. Nevertheless, it is usually well-known and well-understood by the designer. The success of a test based on a model depends on the level of confidence associated with it. Hence, the quality of the behavioral model is of utmost importance as it will set a higher limit on the achievable confidence in the test results.

3 • 1 . 2 Implications of the approach

3 • 1 . 2 . 1 The link with performance

As a matter of fact, our test proposal define the pass-fail region in the test signature space. What we intend is that the test signature space should be equivalent to the design variable space (i.e. the behavioural parameter space). However, for the majority of circuits, the design space is not equivalent to the performance space: the performance associated with a particular design point can be determined but a particular performance point cannot be associated with a unique design point.

As a result, the pass-fail region defined on the test signature space can be mapped onto the design space and onto the performance space, but the specifications (which can be seen as pass-fail limits in the performance space) cannot necessarily be mapped onto a unique region ofthe design space and consequently on the test signature space. This is illustrated in Figure 3-2.

On the other hand, the actual design is carried out in the design space and what defines both the final performance and the nominal test signatures is the point that has been selected in the design space, as seen in Figure 3-2. As a result, it makes sense to define the test limits in the design space close to the selected design point, because it corresponds to what has actually been fabricated. By testing the main block characteristics, we can ensure that the circuit conforms to what has been designed (which means that it is likely to be defect-free).

A functional test considers the performance specifications as the test pass-fail limits. It will thus accept any circuit in the valid design space, even if it is far from what has been effectively designed. This will limit the yield escapes as all good performers are accepted but it may represent a reliability issue.

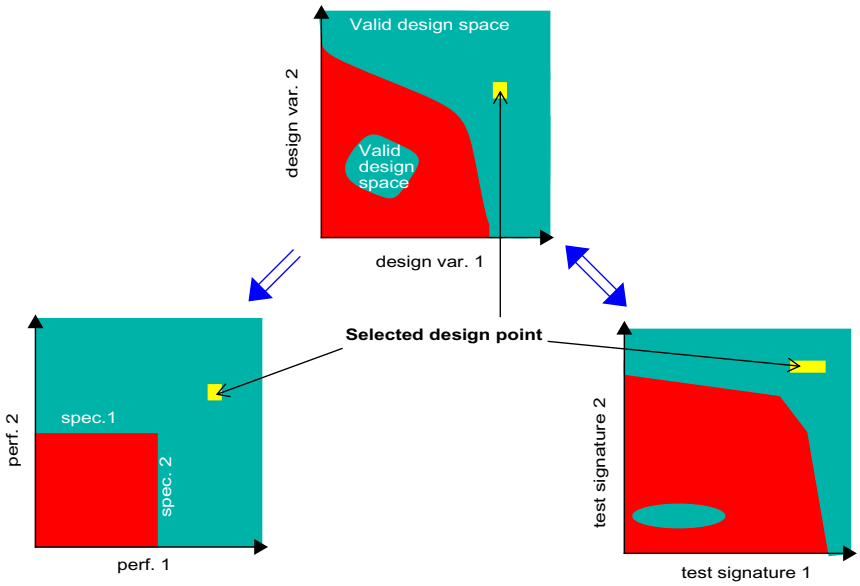


Figure 3-2: Relation between design space, performance space and test signature space

These concerns are particularly justified for ΣΔ modulator as their performance exhibit a very non-linear relation with respect to some behavioral parameters. For instance, it can be seen in Figure 3-3 that under certain conditions, the SNDR of a ΣΔ modulator could exhibit a singularity peak for a given value of amplifier gain-bandwidth product. If the SNDR specification is 90 dB, it can be seen that the valid design space comprises the singularity peak. Obviously, a designer would never select the design point at the singularity. In turn, he would select a point in a larger region with lower sensistivity, and provide some guard-band. By testing the amplifier GBW (directly or indirectly), it is possible to check if the modulator is in the desired region. In turn, a functional test of the SNDR would accept the modulator located at the singularity peak.

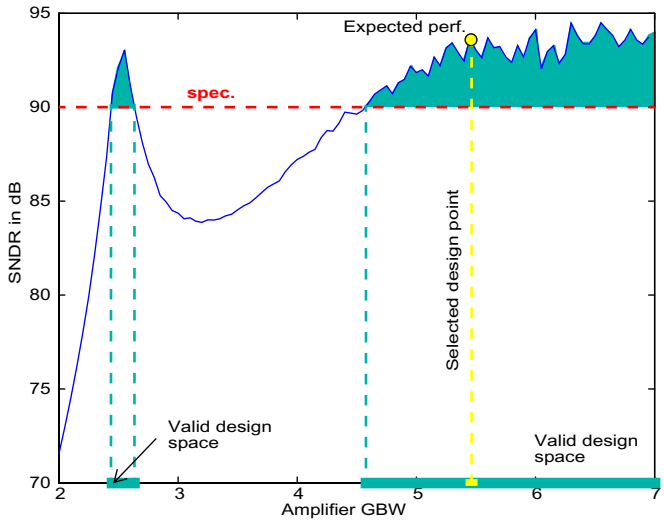


Figure 3-3: Impact of 1st amplifier Gain-Bandwidth product on the SNDR of a 2-1 cascaded ΣΔ modulator

3 • 1 . 2 . 2 The link with defects

In the previous sub-section, we have dealt with the capability of the test to infer if the performance meet the specifications. This is obviously a functional test viewpoint. Nevertheless, the test proposal can also be considered from a defect-oriented viewpoint. In that case, we have to question the ability of the behavioral model to be at a level of abstraction that is sufficiently low to represent the defect-induced faults accurately.

The behavioral model has been designed so as to take into account most of the parameters that influence the performance of the circuit. It can be assumed that any physical defect that will impact the circuit performance should also express itself at the behavioral level. Notice that this is an implication and not an equivalence: there may be physical defects that have an expression at the behavioral level but do not affect the circuit performance. In an attempt to bring IFA (Inductive Fault Analysis [14,13]) to analog and mixed-signal circuits, Mani Soma argues in [15] that the only way to handle parametric defects in analog circuits is to gather them into fault classes related to the functionality of the basic building blocks. Otherwise, the fault dictionary that should be simulated would be far too long. This naturally leads to behavioral model-based test.

However, we should consider what could be the reasons for missing some defects that have an impact on performance, and we should contemplate them in the definition of the test signature in order to minimize this defect masking:

- The behavioral model is incomplete. This point meets the considerations in the previous section about the model quality.
- The defect breaks the signal flow. If the tests are designed exclusively to devise the macro parameters, they may not detect a failure in the signal flow that would corrupt the results. However, such defects are likely to be catastrophic, such that very simple test could be added to check coarse functionality.
- The defect alters a block such that it does not correspond to its macro model. Once again, such defects are likely to be catastrophic and easily detectable, as they affect the integrity of the model.
- The defect increases the complexity of a block. This would be a subtle failure mechanism, that would change the operation of a block slightly while maintaining its coarse behavior. For instance, one can imagine a defect that alter the compensation of an amplifier. If the amplifier was modeled by a single pole approximation, the defect could put the circuit out of the validity range of the behavioral model, while producing acceptable functional results.

3 • 1 . 2 . 3 The way to determine the block parameters

Another important issue is the type of tests to be performed. In the linear modelling approach discussed in the previous chapter, the tests performed on the device were considered as a subset of the whole set of specifications. The model, in some way, depicts the correlations that exist between the specifications and aims at reducing redundancy. For instance, for an ADC, only some transitions are characterized and the model estimates the maximum value of INL and DNL. In the case of design-based test, however, the aim is to determine the parameters of the main building blocks which in turn allow one to extrapolate the circuit performance. Hence, the tests performed on the device may be completely different from classical specification tests, being tailored to determine block parameters. This obviously add an important degree of freedom to the approach, which has the potential to bring important benefits in term of test cost. The downside is that those additional tests cannot be provided using

a systematic approach. They have to be invented and this requires a deep understanding of operation of the behavioral model. For instance, as was pointed out in Section 2 • 3 . 2, Roy and Sunter propose in [62] a technique that requires one to generate only four simple signatures to derive important parameters such as gain, offset, second and third harmonic distortion.

The use of a behavioural model for test purposes should not be restricted to functional testing. What we expect is to consider the behavioral model as a vehicle to enhance circuit testability, not only from a production test viewpoint. The designer should study the possibility of modifying the circuit so as to enable innovative tests that could allow one to determine the model parameters accurately and simply. The circuit is no longer considered as a black-box.

3 • 2 THE PROPOSED METHOD

The aim of this section is to establish the basics for the next two chapters that will describe the proposed digital test set in detail.

Almost as important as the test philosophy is the manner in which to carry it out. It would be useless to develop a model-based test where determination of the model parameters would be as costly as direct characterization of the converter. In the following, the main issues and trade-offs regarding low-cost test derivation are discussed.

3 • 2 . 1 Tests constraints

Production test-time is an important parameter in the cost equation associated with a product, and many papers have focused on reducing it. Nevertheless, other costs are relevant, such as diagnosis cost, in-field test cost, high precision ATE investment, etc. In order to tackle these issues, we decided to restrict the tests to those that would be good candidates for a BIST implementation. This obviously requires simple test stimulus and simple test interpretation. Moreover, another constraint is to minimize any modifications of the modulator topology so that the test solutions can be included easily in the existing design flows. Hence, our test constraints can be summarized as:

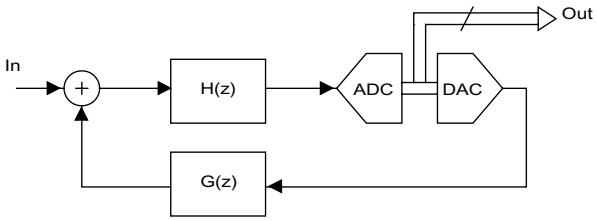


Figure 3-4: Generic representation of a ΣΔ modulator

- digital test stimulus
- simple signature generation
- stimulate the whole modulator signal path
- maintain the modulator topology and the integrity of the building blocks

Figure 3-4 shows a schematic of a generic ΣΔ modulator. Whatever the exact implementation of the loop filter, the principle of operation is always the same: a coarse quantization is performed and the quantized signal is fed back to the input through a DAC. The loop filter shapes the quantization noise out of the baseband so that it can be filtered out. In many cases, the quantizer has only one bit of resolution; it is actually a single comparator. The associated feedback DAC consists only of switches that sample the full-scale reference voltages. Hence, we foresee the possibility of using the feedback DAC to send a digital test stimulus to the modulator. An obvious drawback of such a test stimulus is its very low resolution, but it has two advantages that may overweigh it. The first is that it allows digital interfacing, so that a precise analog signal generator is not needed for the test. This opens the door to the use of digital ATE and also to interfacing to an IEEE 1149.1 test bus in cases where the modulator is embedded in a complex circuit such as SoC. The second advantage is that the stimulus sent to the modulator exactly matches the full-scale reference voltages so that the modulator output bitstream can be directly related to the digital test stimulus (sent to the DAC), enabling precise relative measurements. This means that if the reference voltage exhibits a slow variation in time (with respect to the modulator sampling frequency), the test stimulus exactly matches this drift, so that the measurements are valid while the levels remain in the acceptable range of operation.

In order to facilitate interpretation of the test results, the generation of the output signatures has to be simple and low-cost. Although ΣΔ modulators are usually used in conjunction with a decimation filter, its nature and specifications may vary to a great extent. Even more, at some stage of its fabrication, the ΣΔ modulator may not be associated with a filter. Some ΣΔ modulators are shipped as ADC converters with embedded decimation filters but many times the modulator is shipped as a single part and the filtering is performed in another chip. Hence, in order to extend the test capability beyond board level (system) test or in-field test, we should not rely on the decimation filter to carry out the test. Our proposal is based on the use of simple counters and possibly low-speed arithmetic to perform most of the signature generation. Obviously, in a partial BIST approach, the signature generation could be realized in software within the ATE.

Finaly, an important constraint that we imposed on ourselves was to limit the impact of the DfT modifications on the circuit topology. Indeed, the industry is often reluctant to modify parts that have been proven good. In that sense, DfT solutions requiring a profound modification of the circuit are often discarded. The DfT adaptation has to be seen as an add-on feature that can easily be adapted to known design flows and even to IP blocks (i.e. the addition of buffers, new analog connections, new topologies, new amplifier structures, etc... should be avoided). As a consequence we focused on modifying the circuitry to the least extent, and if possible always on the digital side, acting on the switch controls.

With these three guidelines (constraints), a low-cost and fully-digital DfT solution for ΣΔ modulators could be designed, with little or no adverse impact on performance.

3 • 2 . 2 Test description

In 1991, Schreier and Snelgrove published a very interesting paper entitled: “ΣΔ modulation is a mapping” [32], arguing that the relation between the input and the output can be seen as a projection. Extrapolating this sentence from a structural test point of view we can write: “ΣΔ modulation should be a mapping”. We thus form the hypothesis that defects could alter this mapping. Summarizing the idea, the test development consists of finding a suitable digital input sequence and the modulator operating conditions such that the average

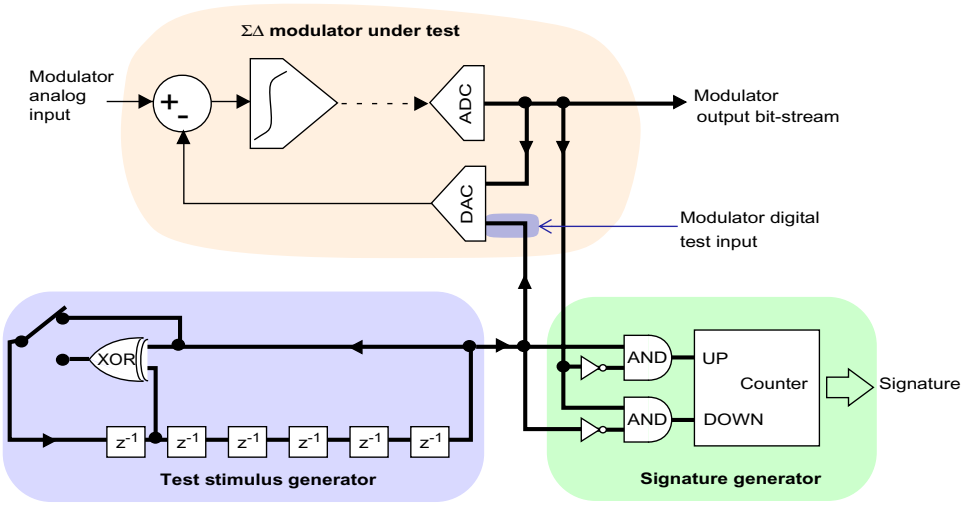


Figure 3-5: Generic sheme of the proposed test setup

of the output bitstream is sensitive to the behavioral parameter under test and an efficient signature can be built.

The digital tests that will be described in the nest two chapters can be implemented using the setup of Figure 3-5. The test stimuli are digital and can be generated on-chip or by a digital tester. Those digital stimuli are then sent to the modulator under test through the feedback DAC during the sampling phase. During the integrating phase, the feedback DAC is driven by the modulator output, as usual. That time-multiplexed use of the DAC is symbolized in Figure 3-5 by an extra input. During test mode, the modulator analog input is disabled.

As a general test signature, we propose the result of accumulating a certain number of samples, and subtraction of the input and output sequences. This requires only few logic gates and an up-down counter. However, the reader should notice that the test decision has necessarily to be taken in the model parameter space. Indeed, the calculation of explicit performance figures would require simulation of the behavioral model. For silicon-debug purposes, the behavioral signatures should be shifted off-chip. But for test purpose, we will show that tolerance windows can be designed for each behavioral signature.

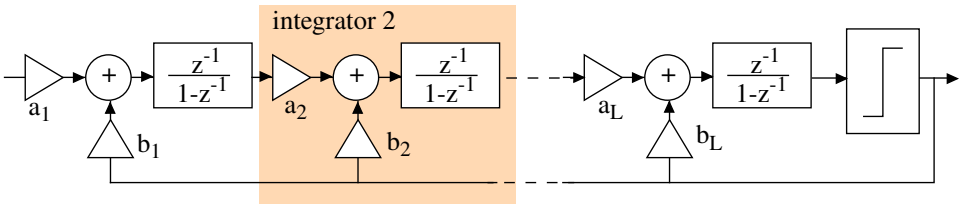


Figure 3-6: Direct extension of the feedback structure to modulators of order higher than 2

The different tests will thus be described according to three points:

- Definition of the digital input sequence.

  For each proposed test, the nature of the digital test stimulus will be detailed.

- Modification of the modulator operating conditions

  The modifications required for each test will be defined.

- Elaboration of the test signature

  The elaboration of the test signature will be described and its relation to the behavioural parameters will be demonstrated.

3 • 2 . 3 Application range

As was said in Chapter 1, high order single-stage modulators usually exhibit stability issues and they require architectures that are more complex than the direct implementation of Figure 3-6. Indeed, such a straightforward implementation is likely to lead to situations where the integrator outputs become unbounded or rise to unpractical levels. Moreover, although they may exhibit a stable range of operation, the analytical determination of such a stability range is cumbersome.

For that reason, cascaded modulators are and have been widely used to implement high order modulators. The stages usually comprise 2^{nd} and 1^{st} order modulators, mainly because these modulators are unconditionally stable and their architecture is simple.

In our behavioral-model-based test approach, we aim to determine behavioral parameters using simple and reusable tests. In that sense, we focus our research mainly on 2^{nd} and 1^{st} order modulators, because the results could be used for an entire cascaded modulator.

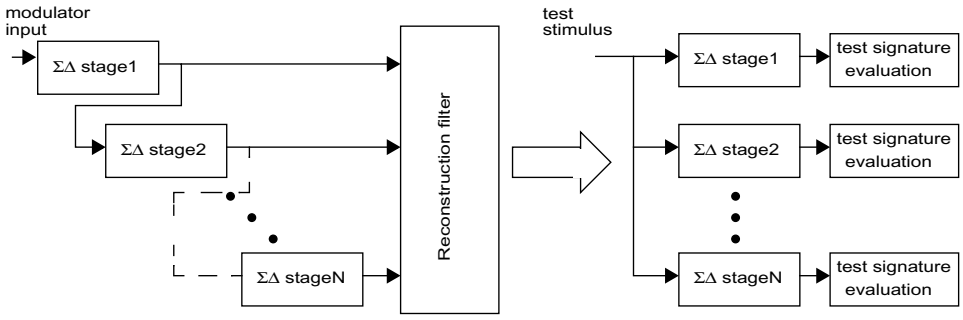


Figure 3-7: Parallel testing of a cascaded ΣΔ modulator

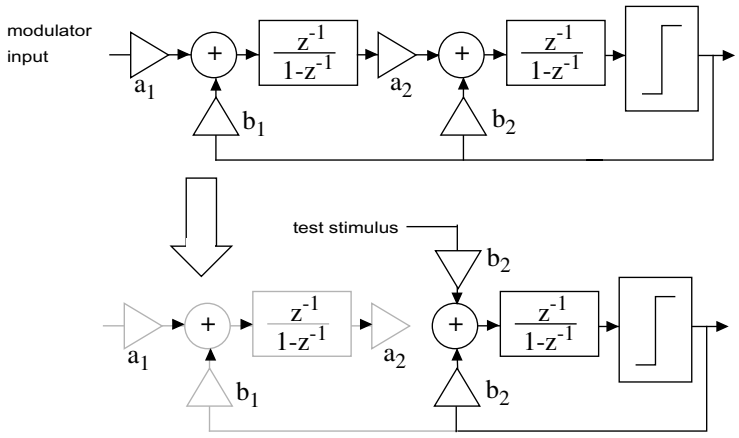


Figure 3-8: Reconfiguration of a 2nd order modulator as a 1st order modulator, for test purpose

Indeed, the different stages can be disconnected and tested in a parallel manner, as seen in Figure 3-7.

Moreover, a 2nd order modulator can easily be reconfigured as a 1st order modulator to enhance its testability, as shown in Figure 3-8. This is of particular interest when the tests target defects in the second integrator of the ΣΔ modulator, as will be seen in the following chapters. In that way, the tests developed for 1st order modulators can be used to test defects in the second integrator of the reconfigured 2nd order modulators.

Whenever possible, we try to extend the results obtained to higher order architectures. But the decomposition principle described above, that enables one to test for defects in the integrators situated deeper in the ΣΔ loop, cannot be generalized for any architecture.

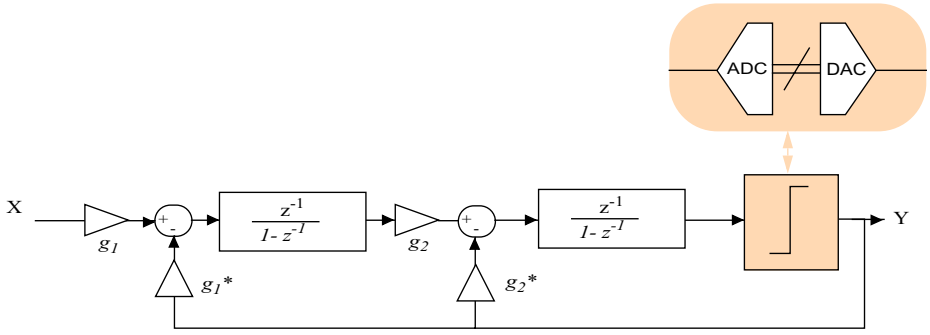


Figure 3-9: Discrete-time representation of a 2nd order ΣΔ modulator

Indeed, high order architectures usually include some local feedback or feedforward paths that may impede the reconfiguration of the modulators into lower order ones.

3 • 2 . 4 Normalization issues

Up to now, we have been saying that the chosen test stimulus is a digital sequence. Nevertheless, the standard input of a ΣΔ modulator is analog and not digital. Actually, the digital test sequence has to be converted to analog by a Digital-to-Analog Converter (a DAC). Many ΣΔ modulators use a single-bit quantizer in the feedback loop, and hence the feedback signal is generated by a single-bit DAC that consists only of a couple of switches that sample two reference voltages. These two reference voltages (V_{ref} and $-V_{ref}$ in a differential implementation) define the modulator Full-Scale.

This apparent simplicity leads to some confusion between the digital sequence - which has two logical levels: 0 and 1 - and its analog version, at the output of the DAC - which also has two levels: V_{ref} and $-V_{ref}$. The reader should thus be aware that when we consider digital sequences as test stimulus, we implicitly override the Digital to Analog conversion of the sequence. Actually, the mathematical description of the tests is based on the commonly used z-domain representation of ΣΔ modulators. Figure 3-9 shows the example of a second order modulator.

Notice that in this representation, the quantizer is sketched as a unique block that gathers both the coarse ADC and the feedback DAC. This obviously reinforces the confusion

between digital and analog sequences because the output of the z-domain model, quoted Y, is analog. Hence, in what follows, we will refer to the sequences as their representation in the analog discrete-time domain (the z-domain), unless it is explicitly specified otherwise. Whether the digital test sequence is sent to the modulator through an extra 1-bit DAC or re-using the modulator feedback DAC will be discussed in the following chapter.

This consideration leads us to another important aspect of the common mathematical framework which is normalization. As was said above, the two reference levels used by the feedback DAC further define the modulator Full-Scale. Indeed, the input of the modulator cannot be higher than the maximum feedback signal, otherwise the stability of the structure would be compromised. Though it would be possible to describe the modulator using real analog levels, it is easier to normalize all the internal levels such that all modulators can be described in a similar way. The convention in that case consists of normalizing Vref to 1. Hence, the input signal has to remain in the range [-1;1] and the normalized Full-Scale is thus equal to 2. Notice that our digital sequences, in their normalized analog representation, use two levels: 1 and -1. Similarly, in order to describe the modulator in the frequency domain we will use a normalized frequency of 1. Hence, dynamic parameters like bandwidth and slew-rate will be expressed relatively to that normalized frequency.

4

TEST FOR STATIC PARAMETER DETERMINATION

In this chapter, several tests for the static behaviour of the integrators in a ΣΔ modulator are described. Actually, the tests proposed in this chapter address the determination of the integrator leakage and the non-linearity of the amplifier DC gain.

The guidelines given in Chapter 3 have been followed in most of the cases, but the exceptions will be specified. In each case, the impact on the performance of the parameter of interest is discussed. The test description is sustained by a theoretical justification and followed by a validation process through simulation.

The next chapter is built on the same pattern and will be devoted to the tests proposed for determining dynamic behavioural parameters.

4 • 1 INTEGRATOR LEAKAGE

In the discrete-time domain, the operation realized by an integrator is a cumulative sum: the output at instant n is the sum of the output at instant $n-1$ and the input sample at instant $n-1$ or n, depending on wether it is a delaying integrator or not. To perform this sum, the integrator output at instant $n-1$ has to be memorized until instant n. Ideally, this analog memory function is lossless and the transfer function of the delaying integrator can be written as

$$\frac{z^{-1}}{1-z^{-1}}. \tag{4-1}$$

For a non-delaying integrator, the numerator in Eq (4-1) would be 1.

In real cases, the integrator output cannot be held exactly and an systematic error is introduced: only a fraction p (close to one) of the ideal voltage is available at instant n. This effect, known as integrator leakage, modifies the integrator transfer function such that a pole error is introduced. Thus,

$$\frac{z^{-1}}{1-pz^{-1}}. \tag{4-2}$$

In a switched-capacitor implementation, integrator leakage is produced by the finite DC gain of the operational amplifier. The lower the DC gain, the higher the leakage. Indeed, a simple study of the integrator in Figure 4-1 shows that

$$\Delta p = 1 - p \approx \frac{b}{A_{DC}} \qquad b = \frac{C_i}{C_f}. \tag{4-3}$$

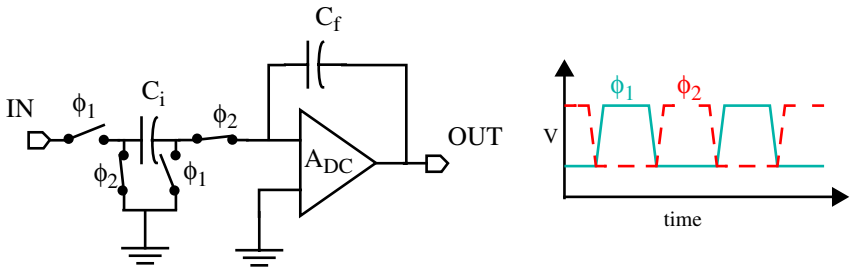


Figure 4-1: Switched-capacitor integrator scheme

Hence, any physical defect or environmental condition that may affect the amplifier DC gain will automatically have an adverse impact on integrator leakage.

4 • 1 . 1 Impact on modulator performance

The impact of integrator leakage on the performance of a ΣΔ modulator depends on the Over-Sampling Ratio (OSR) and on the modulator architecture. Integrator leakage changes the quantization noise shaping produced by the ΣΔ loop. Actually, for a L^{th} order single-stage modulator, the output should be of the form

$$Y = z^{-L}X + (1 - z^{-1})^{L}E, \tag{4-4}$$

where X is the input signal and E is the quantization noise introduced by the low-resolution quantizer. In a traditional approximation, this quantization noise is considered as a uniform white noise over the range [-Δ/2;Δ/2] where Δ is the quantization step. In the presence of leakage in one integrator, this shaping becomes

$$Y = z^{-L}X + (1 - pz^{-1})(1 - z^{-1})^{L-1}E, \tag{4-5}$$

which can also be written,

$$Y = z^{-L}X + (1 - z^{-1})^{L}E + \Delta p z^{-1}(1 - z^{-1})^{L-1}E \tag{4-6}$$

Therefore, the modulator output contains the shaped quantization noise plus a contribution of the quantization noise shaped to order L-1, and scaled by the factor $\Delta p = 1 - p$ introduced in Eq (4-3).

This improperly shaped noise is said to have leaked into the base-band of the ΣΔ converter. Hence, the performance degradation depends on the amount of leakage: the higher Δp the higher the excess noise. But it also depends on the converter OSR. For low oversampling ratios, the contribution of the L^{th} order noise may still dominate over the $(L-1)^{th}$ order noise. However, for high OSRs, the $(L-1)^{th}$ order noise is likely to dominate the total noise, limiting the theoretical SNR. This is graphically illustrated in Figure 4-2. The quantization noise of a 3rd order modulator with a leaky integrator is represented. It can be seen that, at high frequencies, the quantization noise follows a 3rd order shape (i.e. the straight line of 60dB/decade in the figure) while at lower frequencies, a 2nd order noise appears (i.e. a straight line of 40dB/decade). A corner frequency can be defined at the intersection of these

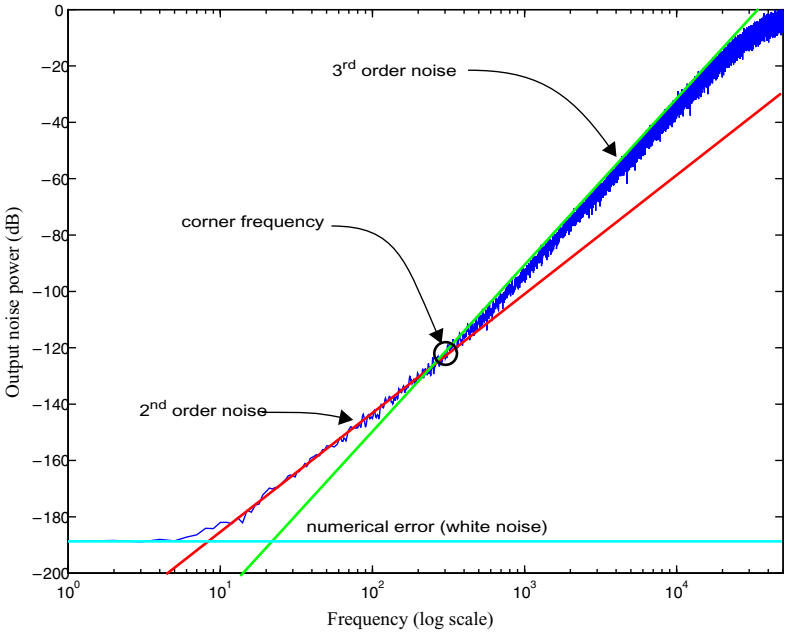


Figure 4-2: Output noise spectrum of a 3rd order ΣΔ modulator with a leaky integrator

straight lines. If the OSR of the ΣΔ converter is set such that cut-off frequency of the decimation filter is higher than the corner frequency, integrator leakage will have little impact on the SNR as the dominant noise contribution is the 3rd order noise, as expected. In turn, if the OSR is set such that the filter cut-off frequency is lower than the corner frequency, the actual SNR of the obtained modulator may be significantly lower than expected. The corner frequency is more descriptive than rigorous as the noise spectral density should be integrated in the signal band, but it still gives a good overview of the impact of integrator leakage.

Actually, it can be shown [41] that, to a first order approximation, the performance degradation should not exceed 3dB if the amplifier DC gain is greater than the OSR. That is a coarse rule of thumb but it gives a good insight into the leakage requirements for single stage ΣΔ modulators. A more detailed description of the problem can be found in [38, 42] that comes up with a generic closed form of the excess noise in dB

$$\Delta P_{noise} = 10\log\left(1 + \frac{\Delta p^2 M^2 L}{\pi^2} \times \frac{2L+1}{2L-1}\right) \quad \textbf{(4-7)}$$

where M is the OSR of the modulator.

This result stands for single stage modulators. For cascaded modulators, on the other hand, the integrator leakage has a more important impact. Indeed, the reconstruction of the signal assumes that no leakage is present and the reconstruction error introduces more uncanceled noise. Let us recall the generic expression of the reconstruction filter described in Section 1 • 1 . 4 . 2, namely

$$Y = \sum_{i=1}^{n} \left(z^{\left(-\sum_{j=i+1}^{n} L_j\right)} (1 - z^{-1})^{\left(-\sum_{k=1}^{i-1} L_k\right)} Y_i \right) \tag{4-8}$$

with,

$$\begin{aligned} Y_1 &= z^{-L_1} X + (1 - z^{-1})^{L_1} E_1 \\ &\cdots \\ Y_i &= -z^{-L_i} E_{i-1} + (1 - z^{-1})^{L_i} E_i \end{aligned} \tag{4-9}$$

Considering that an integrator is leaky in stage f, Eq (4-8) has to be modified as

$$\begin{aligned} Y = z^{\left(-\sum_{i=1}^{n} L_i\right)} X + (1 - z^{-1})^{\left(-\sum_{i=1}^{n} L_i\right)} E_n \\ + \Delta p z^{\left(-1-\sum_{j=f+1}^{n} L_j\right)} (1 - z^{-1})^{\left(1-\sum_{k=1}^{f} L_k\right)} E_f \end{aligned} \quad . \tag{4-10}$$

In the case of single stage modulators, the quantization noise leaking into the base-band was shaped by an order L-1 and scaled by a factor Δp. In the case of cascaded modulators, the quantization noise leaking into the base-band is also scaled by a factor Δp but shaped by an order

$$\left(\sum_{k=1}^{f} L_k \right) - 1 , \tag{4-11}$$

where f is the stage that contains the leaky integrator. Clearly, the leakage appearing in the first stage of a cascade modulator will degrade the performance to a greater extent than the

leakage appearing in further stages. Indeed, if the leakage appears in the first stage, the quantization error leaking into the base-band is of the form

$$\Delta p(1-z^{-1})^{-(L_1-1)}E_1\,. \tag{4-12}$$

As cascaded modulators are used to avoid stability issues for high order ΣΔ modulators, they usually rely on unconditionally stable stages, which are 2nd and 1st order ΣΔ modulators. From an integrator leakage point of view, it is important to maximize the shaping order of the leaking noise, which is equivalent to maximizing L_1. That is why a second order modulators is usually used in the first stage of a cascaded modulator.

The reader should notice that we have considered only one leaky integrator for both single-stage and cascaded modulators. In the case that we need to consider several leaky integrators, which could be interesting for modelling global defects, the different contributions should be summed and cross terms in the expressions of the form

$$\prod_{i=1}^{L}[(1-z^{-1})+\Delta p_i z^{-1}] \tag{4-13}$$

should be considered. Notice however that the terms involving more than one Δp scaling are unlikely to dominate the quantization noise unless the DC gain of the amplifier is very low.

Provided that we know the way in which the leakage modifies the quantization noise shaping, it is possible to take this shaping modification into account in the reconstruction filter so as to eliminate the noise excess due to the reconstruction error. This means that the integrator leakage can be calibrated in cascaded modulators. However, such a calibration requires that the value of the pole error Δp be evaluated. If such a calibration is carried out, the modulator performance degradation due to leakage can be improved up to the level of an equivalent single stage modulator with leakage, that is

$$\Delta p(1-z^{-1})^{-(L_{tot}-1)}E_1\,. \tag{4-14}$$

Another unwanted effect associated with integrator leakage is that of limit cycles. Limit cycles are periodic sequences that are stabilized by integrator leakage such that they remain unchanged for a small range around the DC level corresponding to their mean value. It is shown in [30] that, for a 1st order modulator, the widest of these limit-cycle ranges is the one that corresponds to the limit cycle of mean value 0, that is a [1 -1 1 -1 1 -1 1 -1 ...] output

bit-stream. Actually, this limit cycle is shown to be stable for input DC values x (normalized to full-scale) in the range

$$\frac{-\Delta p}{2-\Delta p} \le x \le \frac{\Delta p}{2-\Delta p} \qquad \textbf{(4-15)}$$

4 • 1 . 2 Proposed tests for leakage detection[1]

Although it may not seem natural, we begin with the case of 2nd order ΣΔ modulators instead of 1st order modulators. The reason is that, despite its architectural simplicity, the behaviour of a first order modulator is difficult to study. Indeed most analytical studies of ΣΔ modulators are based on a linearization of the non-linear element: the coarse quantizer. In that approximation, the quantizer is replaced by an additive noise source modelling the quantization error. This noise source is assumed to be independent of the input signal, uniformly distributed across the feedback DAC quantization step and with a white spectrum. However, Bennett demonstrated in [20], that such an approximation is valid only under a number of conditions:

- The input does not overload the modulator
- The quantizer step is small
- The joint probability density function of the input signal at different sample time is smooth

These conditions are almost never fulfilled for any practical ΣΔ modulator, but the point is that for order higher than 2, the quantization noise can be considered sufficiently random and sufficiently white such that the linearization of the quantizer give at least an insight into the expected performance. However, the correlation between the input signal and the quantization noise in 1st order modulators is too strong to allow the use of the linear approximation.

1. *Here, a brief description of each test is provided. Theoretical justifications will be given in next sub-section*

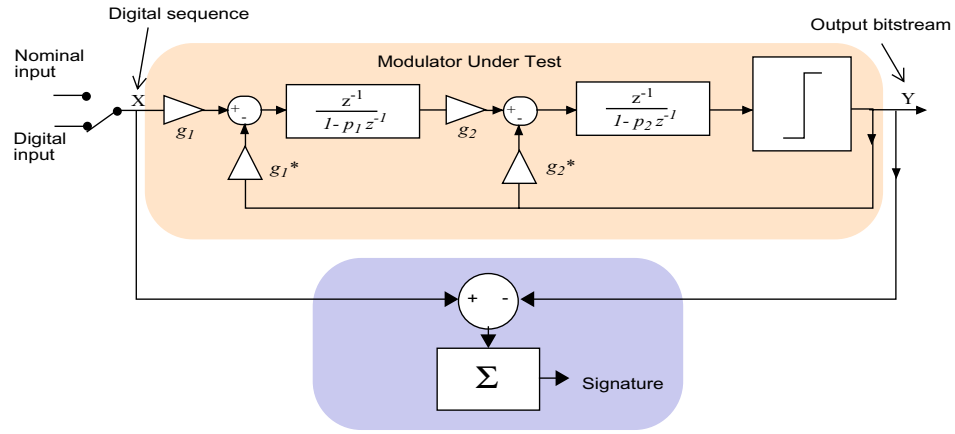


Figure 4-3: Diagram of the proposed test for first integrator leakage in a second-order ΣΔ modulator

4 • 1 . 2 . 1 Second order modulator

Figure 4-3 shows the proposed test structure. The input sequence corresponds to signal X and the output bitstream to signal Y. Following what was said in previous chapter, we can describe the test as follows (a theoretical demonstration will be provided further):

- Digital input sequence: a periodic sequence of mean value Q that is different from 0.

  Considering that a digital sequence is described as its analog version, accordingly to what was said in previous chapter, the mean value of a sequence of period L can be written as,

$$Q = \frac{1}{L}\left(\sum_{i=1}^{L} x_i\right) \qquad \textbf{(4-16)}$$

  For example, a digital input sequence [1 1 1 0] would have an analog representation of the form [1 1 1 -1] and thus a mean value of Q=1/2

- Modifications of the modulator operating conditions: the normal input is disabled and the digital input is enabled. It has been said in previous chapter that the digital input is obtained by re-using the feedback DAC during both the sampling and the integrating phase. This test input is symbolized by a multiplexer in Figure 4-3, considering the test sequence as the analog equivalent of the digital sequence.

- Test signature: it is the sum over a number N of samples of the difference between the input sequence and the output bitstream. For a 2nd order modulator it is given by,

$$s_1 = \sum_{i=1}^{N} x_i - y_i \approx 2NQ\Delta p_1 \pm 3\sqrt{\frac{2}{3}} \quad \textbf{(4-17)}$$

where Δp_1 is the pole error of the first integrator as defined in Eq (4-3).

Actually, an input-referred offset o would modify the signature output

$$s_1 \approx 2NQ\Delta p_1 + N \times o \pm 3\sqrt{\frac{2}{3}} \quad \textbf{(4-18)}$$

To get rid of it, it is possible to run a second acquisition with a sequence of mean value $-Q$ (i.e. the opposite of the first sequence), giving a test signature,

$$s_2 \approx -2NQ\Delta p_1 + N \times o \pm 3\sqrt{\frac{2}{3}} \quad \textbf{(4-19)}$$

The final result can be obtained by subtracting the second signature from the first:

$$s = s_1 - s_2 \approx 4NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}} \quad \textbf{(4-20)}$$

There is no a-priori restriction on the input sequence, except that it must be different from 0. Actually, it should be maximized in order to get the best sensitivity of the signature to the integrator leakage. We will see in the following that signal range considerations compel us to restrict the mean value of the sequence to less than 0.7. Hence, we propose to use a short sequence with Q=2/3. Such a sequence is of the form [1 1 1 1 1 -1].

4 • 1 . 2 . 2 Multibit first order modulator

As was said before, linearizing the coarse quantizer in the case of a 1st order modulator does not makes much sense. Indeed, the quantization error is strongly correlated to the input signal, which breaks one of the fundamental conditions stated by Bennett in applying the linear approximation.

However, in the case of multibit 1st order modulators, the multibit quantization helps to decorrelate the quantization error from the input signal. Hence, a test similar to that for a 2nd order modulator can be implemented for these modulators as follows:

- Digital input sequence: a periodic sequence of mean value Q greater than one half of the quantizer step Δ_{DAC}.

$$|Q| > \frac{\Delta_{DAC}}{2} \tag{4-21}$$

The quantizer step can be calculated from the number of bits L_{DAC} of the quantizer, as,

$$\Delta_{DAC} = \frac{2}{2^{L_{DAC}} - 1} \tag{4-22}$$

- Modifications of the modulator operating conditions: the normal input is disabled and the digital input is enabled.
- Test signature: it is the sum over a number N of samples of the difference between the input sequence and the output bitstream. It will have the form,

$$s_1 = \sum_{i=1}^{N} x_i - y_i \approx NQ\Delta p \pm \frac{3\sqrt{\frac{1}{3}}}{2^{L_{DAC}-1}}. \tag{4-23}$$

As for the case of a 2nd order modulator, the impact of an eventual input-referred offset on the signature can be compensated. For two acquisitions with digital input sequences of mean value Q and -Q, two signatures s_1 and s_2, respectively, are obtained. The final signature would be,

$$s = s_1 - s_2 \approx 2NQ\Delta p \pm \frac{6\sqrt{\frac{1}{3}}}{2^{L_{DAC}-1}}, \tag{4-24}$$

where Δp is the integrator pole error.

The reader should notice that while the input stimulus is a digital sequence and thus exhibits only two levels (1 and -1), the output bitstream comes from a multibit quantizer and in our normalized representation is thus multi-valued (with a number 2^m of levels, m being the number of bits of the quantizer). This does not have theoretical implications but has an impact on the implementation of the signature analyzer. This will be discussed in a posterior chapter.

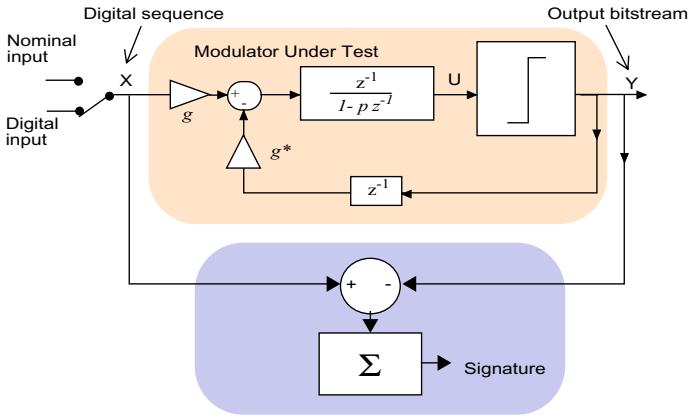


Figure 4-4: Diagram of the proposed test for first integrator leakage in a first-order single-bit ΣΔ modulator

4 • 1 . 2 . 3 Single-bit first-order modulator

For single-bit 1st order modulators, the quantizer linearization does not hold anymore. Actually, Schreier and Temes [32] showed that a 1st order ΣΔ modulation is a mapping, i.e. a projection. The main implication of this in our case is that if a digital sequence is used as a test stimulus, the modulator output will follow that sequence. This effect is even strengthened by integrator leakage, which means that we will see no difference between the modulator output mean value and the input sequence mean value.

What we propose is thus to modify the modulator during the test mode by adding an extra delay in the digital part of the feedback path, as shown in Figure 4-4. The rest of the procedure is similar to the one described for a second order modulator. Theoretical justification will be provided further.

- Digital input sequence: we limit the digital test sequences to periodic sequences of period L and of the form,

$$\begin{bmatrix} 1 & 1 & \dots & 1 & -1 \end{bmatrix} \\ \begin{bmatrix} -1 & -1 & \dots & -1 & 1 \end{bmatrix} \quad \textbf{(4-25)}$$

with a number *L*-1 of 1s and one -1 (conversely of -1s and 1). The sequence period *L* must be strictly higher than 5. This implies that the magnitude of its mean value *Q* is greater than 3/5.

- Modifications of the modulator operating conditions: the normal input is disabled and the digital input is enabled. An extra delay is added in the feedback loop.
- Signature elaboration: it is the sum over a number N of samples of the difference between the input sequence and the output bitstream.

$$s_1 = \sum_{i=1}^{N} x_i - y_i \approx \frac{2N\Delta p}{\ln\left(\frac{3L-5}{L-5}\right)} = \frac{2N\Delta p}{\ln\left(\frac{1+5Q}{-3+5Q}\right)} \pm 2 \quad \textbf{(4-26)}$$

Here again, performing two acquisitions s_1 an s_2 with opposite sequences allows to get rid of an eventual input-referred offset. The final signature is,

$$s = s_1 - s_2 \approx \frac{4N\Delta p}{\ln\left(\frac{3L-5}{L-5}\right)} = \frac{4N\Delta p}{\ln\left(\frac{1+5Q}{-3+5Q}\right)} \pm 4 \quad \textbf{(4-27)}$$

An alternative to the test described above is to use an input sequence that is similar to the one described above, but where the -1 (conversely the 1) is replaced by a 0. This oblige us to deviate from the constraints set in Chapter 3 as the 0 is not an available output of the feedback DAC. Nevertheless, we will see in Chapter 6 that such a modification can easily be implemented. The advantage, on the other hand, is that the extra delay in the feedback loop is no longer necessary. In that case, the result for two acquisitions with opposite sequences takes the form,

$$s = s_1 - s_2 \approx \frac{2N\Delta p}{\ln\left(\frac{3L-2}{L-2}\right)} = \frac{2N\Delta p}{\ln\left(\frac{2Q+1}{2Q-1}\right)} \pm 2 \quad \textbf{(4-28)}$$

In this case, L has to be strictly higher than 2 (i.e. Q>0.5).

4 • 1 . 2 . 4 Extension to modulators of order greater than 2

In the case of modulators of order higher than 2, it is likely that the quantization error issufficiently decorrelated from the input signal that the quantizer linearization give a good result for the modulator behavior. Actually, there are no alternative analytical methodology to study the frequency response of a high order modulator.

Hence, we suggest that the test proposed for a second order modulator could be valid to determine integrator leakage in high order modulators. Integrator leakage modifies the quan-

tization noise shaping NTF(z) such that the noise in the baseband of the modulator increase. Due to the ΣΔ modulation loop, the Signal Transfer Function STF(z) is related to NTF(z). Hence a change in NTF(z) induces a change in STF(z). The underlying assumption in the proposed test is that there is a deviation in the modulator output mean value from the input mean value. In terms of the frequency domain, it means that the limit of STF(z) when z tends to 1 is a function of integrator leakage, i.e.

$$\lim_{z \to 1} STF(z) = f(\Delta p_1, \ldots, \Delta p_i, \ldots, \Delta p_L) \quad \textbf{(4-29)}$$

We should make a Taylor series expansionof the function f and see which integrator leakage(s) (if any) modify the STF to a first order.

Our first guess, extrapolating the results for the second order modulator, is that only the first integrator leakage will impact the mean value of the output. However, the application of this test requires the study of the particular architecture and no general conclusion can be drawn on its applicability.

4 • 1 . 3 Leakage test theoretical justification

This sub-section presents analytical proof for the signatures proposed above as well as for the restrictions that may have been put on either the test sequence or the modulator operating conditions.

4 • 1 . 3 . 1 Second order modulator

The goal of this section is to establish the relationship between the signature and the loss of the first integrator. For this, we will make use of a linearized model of the modulator. Despite the fact that this model fails to represent all the effects observed in the modulator behavior, we will verify by simulation that it gives sufficient insight in our case.

Let us consider the discrete-time domain modulator model of Figure 4-3. For the analytical study, the quantizer is linearized and replaced by a gain element and zero mean additive noise, as can be shown in Figure 4-5.

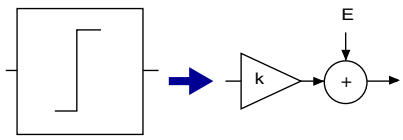


Figure 4-5: Quantizer linear model

For a more detailed study, the reader should refer to the work of Ardalan *et al.* [33].

From this model we obtain

$$\begin{aligned}&[1+z^{-1}(-p_1-p_2+kg^*_2)\\&+z^{-2}(p_1p_2+kg_2g^*_1-p_1kg^*_2)]Y\\&=kg_1g_2z^{-2}X+[1+z^{-1}(-p_1-p_2)+p_1p_2z^{-2}]E\end{aligned} \tag{4-30}$$

In the ideal case, the integrators have no loss and thus $p_1=p_2=1$. Therefore, in order to fit the second order ideal behaviour, that is,

$$Y = z^{-2}X + (1-z^{-1})^2 E \tag{4-31}$$

we must ensure by design that

$$\begin{aligned}kg_1g_2 &= 1\\kg^*_2 &= 2\\kg_2g^*_1 &= 1\end{aligned} \tag{4-32}$$

One possible solution is $g_1=g_2=g^*_1=g^*_2=0.5$, as presented in [26], which leads $k=4$.

The counter output is the sum of the modulator output over N samples. By interpreting Eq (4-30) in the time domain, and noticing that

$$\sum_{j=1}^{n} w(j-1) = \sum_{j=1}^{n} w(j) + w(0) - w(n) \tag{4-33}$$

we obtain, using Eq (4-32),

$$[\Delta p_1(2+\Delta p_2)+1]\sum_{n=2}^{N+1} y(n) = \sum_{n=2}^{N+1} x(n-2) \qquad \textbf{(4-34)}$$

$$-[\Delta p_1(2+\Delta p_2)](y(1)-y(N+1))$$

$$-[\Delta p_1(1+\Delta p_2)-\Delta p_2](y(0)-y(N))$$

$$+[\Delta p_1\Delta p_2-1](e(1)-e(N+1))$$

$$+[\Delta p_1\Delta p_2-\Delta p_2-\Delta p_2+1](e(0)-e(N))$$

$$+[\Delta p_1\Delta p_2]\sum_{n=2}^{N+1} e(n)$$

Here, we have introduced Δp_1 and Δp_2 that stand for *(1-p_1)* and *(1-p_2)* respectively.

The previous equation can be greatly reduced if we notice that

$$\sum_{n=2}^{N+1} x(n-2) = NQ \qquad \textbf{(4-35)}$$

if N is a multiple of the input sequence period. Moreover, for N large, the term

$$\sum_{n=2}^{N+1} e(n) \qquad \textbf{(4-36)}$$

should be bounded, as the mean value of the error term is zero.

The remaining terms on the right hand side of Eq (4-34) are also bounded, and independent of N. Thus, if we consider that $\Delta p_1=\Delta p_2=0$ for these terms, then Eq (4-34) reduces to,

$$\sum_{n=2}^{N+1} y(n) \approx \frac{(NQ-(e(1)-e(0))+(e(N+1)-e(N)))}{[\Delta p_1(2+\Delta p_2)+1]}. \qquad \textbf{(4-37)}$$

If Δp_1 and Δp_2 are small, we obtain

$$s_1 = \sum_{n=2}^{N+1} x(n) - \sum_{n=2}^{N+1} y(n) \approx 2NQ\Delta p_1 . \qquad \textbf{(4-38)}$$

Therefore, the signature is directly sensitive to the integrator loss, as was stated in Eq (4-16). The theoretical basis of the proposed test is thus justified. Notice that the inclusion of an input-referred offset has been obviated for the sake of brevity.

The precision on the determination of Δp_1 is limited by the quantization noise terms e in Eq (4-37). Taking into account the input referred offset cancellation the following expression is obtained,

$$s = 4NQ\Delta p_1 + \sum_{i=1}^{8} e_i \tag{4-39}$$

where the terms e_i are random variables representing the quantization noise. Assuming that the quantization noise is gaussian-like,

$$e \sim N\left(0, \left(\sigma_e^{\,2} = \frac{FS^2}{12}\right)\right) \tag{4-40}$$

and the sum of eight quantization noise terms is also gaussian-like with,

$$\sum_{i=1}^{8} e_i \sim N\left(0, \left(\sigma^2 = \frac{8FS^2}{12}\right)\right) \tag{4-41}$$

The term FS stands for the modulator Full-Scale which, in our case, is equal to 2 as the feedback levels are normalized to 1 and -1.

The integrator leakage can be determined within a confidence interval of $\mp 3\sigma$, and hence, from Eq (4-39) and Eq (4-41), we can write

$$\Delta p_1 = \frac{s}{4NQ} \pm \frac{6\sqrt{\frac{2}{3}}}{4NQ} \tag{4-42}$$

From a test viewpoint, it is important to determine the number of points that have to be summed to detect unexpected leakage. This can be done using Eq (4-42). Let us assume that the nominal expected leakage is,

$$\Delta p_{nom} = \frac{b}{A_{DCnom}}. \tag{4-43}$$

The leakage begins to be detected when the term $4NQ\Delta p_1$ in Eq (4-39) is greater than the 3σ error. Thus,

$$4NQ\Delta p_1 > 6\sqrt{\frac{2}{3}} \Leftrightarrow N > \frac{3\sqrt{\frac{2}{3}}}{2Q\Delta p_1} \tag{4-44}$$

The number of samples required to detect the expected leakage given by Eq (4-43) will be

$$N_{test} \approx 1.23 \times \frac{A_{DCnom}}{bQ} \tag{4-45}$$

For a 60dB nominal DC gain and a 0.5 integrator gain, a test with the proposed [1 1 1 1 -1] sequence would require two acquisitions of 3690 samples. Notice that these samples are acquired at the modulator bitstream speed.

Notice that the above demonstration has been carried out supposing that the second order modulator has been designed to fulfill the ideal 2nd order noise shaping of Eq (4-31). However, optimization considerations may lead designers to use branch coefficients in the integrators that do not lead to the ideal 2nd order shaping. For instance, if coefficient g_1 and g_1* of Figure 4-3 are not made equal, it modifies the gain of the modulator. Programmable gains are sometimes implemented to adapt the input signal to the modulator full-scale. Nevertheless, it can be shown that the proposed test always leads to a signature that is sensitive to the first integrator leakage. Considering the generic diagram of Figure 4-3 and a linearized quantizer with effective gain k, it can be written

$$Y = \frac{kg_1g_2z^{-2}X + (1-p_1z^{-1})(1-p_2z^{-1})E}{(1-p_1z^{-1})(1-p_2z^{-1}) + kg^*{}_1g_2z^{-2} + kg^*{}_2(1-p_1z^{-1})} \tag{4-46}$$

The leakage signature senses how the modulator output deviates from the input on average. Hence taking the limit of Eq (4-46) when z tends to 1, we obtain,

$$\overline{Y} = \frac{kg_1g_2\overline{X} + (\Delta p_1)(\Delta p_2)\overline{E}}{(\Delta p_1)(\Delta p_2) + kg^*{}_1g_2 + kg^*{}_2(\Delta p_1)} \tag{4-47}$$

where,

$$\begin{aligned} \overline{Y} &= \lim_{z \to 1} Y \\ \overline{X} &= \lim_{z \to 1} X = Q \\ \overline{E} &= \lim_{z \to 1} E \end{aligned} \tag{4-48}$$

Considering that the integrators pole errors are small, a first order Taylor development leads to

$$\overline{Y} \approx \frac{g^*{}_1}{g_1}\left(1 - \frac{g^*{}_2}{g^*{}_1g_2}(\Delta p_1)\right)\overline{X} + \frac{(\Delta p_1)(\Delta p_2)\overline{E}}{kg^*{}_1g_2}. \tag{4-49}$$

It can be seen that the modulator gain is actually g_1^*/g_1, and hence the test signature should be modified as

$$s = \sum_{i=1}^{N}\left(x_i - \frac{g_1}{g^*_1}y_i\right) \approx N\frac{g^*_2}{g^*_1 g_2}(\Delta p_1)Q - N\frac{g_1(\Delta p_1)(\Delta p_2)\bar{E}}{k g^{*2}_1 g_2}. \quad \textbf{(4-50)}$$

Notice that the main term of the signature is independent of the quantizer's effective gain, which is quite interesting as this parameter can only be determined by simulation in most cases.

4 • 1 . 3 . 2 First order multibit modulator

Supposing that the quantizer linear approximation can be used, the discrete-time model depicted in Figure 4-6 is obtained. Notice that the effective gain of a multibit quantizer is one, that is, it is equal to the quantizer actual gain.

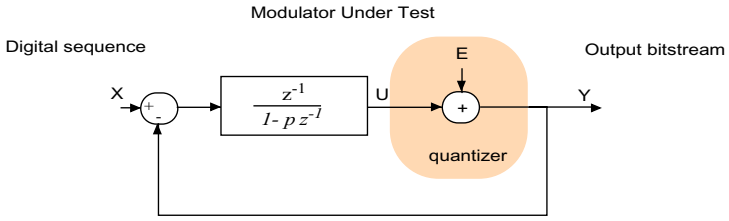


Figure 4-6: z-domain representation of a linearized first-order multibit ΣΔ modulator

We can write

$$Y(1+\Delta p z^{-1}) = z^{-1}X + (1 - z^{-1} + \Delta p z^{-1})E. \quad \textbf{(4-51)}$$

Using the same considerations as for a second order modulator, we obtain

$$\sum_{n=2}^{N+1} y(n) \approx \frac{NQ - (e(0) - e(N))}{[1+\Delta p]}, \quad \textbf{(4-52)}$$

where N, the number of summed samples, is a multiple of the input sequence period.

In the case of low integrator leakage, Δp is small and the test signature can be written as

$$s_1 = \sum_{n=2}^{N+1} x(n) - \sum_{n=2}^{N+1} y(n) \approx NQ\Delta p \quad . \quad \textbf{(4-53)}$$

Therefore, the signature is directly sensitive to the integrator loss. The theoretical basis of the proposed test is thus justified. Notice that the inclusion of an input-referred offset has been obviated for the sake of brevity.

Like in the case of the 2nd order modulator, the precision of the leakage determination is driven by the quantization noise terms in Eq (4-52). We can thus repeat a similar study.

Taking into account the input referred offset cancellation, we have an expression of the form

$$s = 2NQ\Delta p + \sum_{i=1}^{4} e_i \,, \tag{4-54}$$

where the terms e_i are random variables representing the quantization noise. Assuming that the quantization noise is gaussian-like, with

$$e \sim N\left(0, \left(\sigma_e^{\,2} = \frac{\Delta_{DAC}^{\,2}}{12}\right)\right), \tag{4-55}$$

we have that the sum of eight quantization noise terms is also gaussian-like, with

$$\sum_{i=1}^{4} e_i \sim N\left(0, \left(\sigma^2 = \frac{4\Delta_{DAC}^{\,2}}{12}\right)\right). \tag{4-56}$$

Let us recall that the term Δ_{DAC} stands for the quantizer step, which in our case is equal to

$$\Delta_{DAC} = \frac{2}{2^{L_{DAC}} - 1}, \tag{4-57}$$

where L_{DAC} is the number of bits of the quantizer.

Hence, the integrator leakage can be determined within a confidence interval of $\mp 3\sigma$,

$$\Delta p = \frac{s}{2NQ} \pm \frac{3\sqrt{1/3}}{NQ\left(2^{L_{DAC}-1}\right)} \tag{4-58}$$

Let us now justify the limitation on the input sequence mean value. It has been shown in [32] that 1st order ΣΔ modulation is a projection. This means that the modulator response to a digital sequence is the same digital sequence. This can be demonstrated through the behavioral equation of the modulator

$$u_{n+1} = u_n + x_n - Quant(u_n)\,, \tag{4-59}$$

where *Quant* represents the quantization function, x is the input sequence and u is the integrator output. The term $Quant(u_n)$ corresponds to the modulator output y_n.

We want to solve Eq (4-59) in the particular case where x is a digital sequence. In this case, it can be written that

$$Quant(x_n) = x_n . \tag{4-60}$$

An obvious solution to Eq (4-59) is

$$u_n = x_{n-1} + \alpha \qquad \forall n , \tag{4-61}$$

where α is such that

$$Quant(x_{n-1} + \alpha) = Quant(x_{n-1}) , \tag{4-62}$$

which is equivalent to

$$\alpha \in [\frac{-\Delta_{DAC}}{2}, \frac{\Delta_{DAC}}{2}] \tag{4-63}$$

Δ_{DAC} being the quantizer step.

By replacing the u_is using Eq (4-61) in Eq (4-59), the solution is easily verified. The integrator output strictly follows the input sequence with a one-sample delay. The term α accounts for the integrator initial condition. The modulator output $y_n=Quant(u_n)=x_{n-1}$ follows the input, as was stated in [32]. In the presence of integrator leakage, however, this behavior is slightly altered. Indeed, the leakage can be seen as a small perturbation that tends to push the integrator output (denoted U in Figure 4-6) towards zero. The modulator output will follow the input while $Quant(u_n)=x_{n-1}$. This condition is not fulfilled when the decrease due to integrator leakage is such that u_n excites a transition other than the two extreme ones. Nevertheless, it can be shown that in some cases this condition is never broken and the output always follows the input, losing any sensitivity to integrator leakage.

While the pattern is maintained, $Quant(u_n)=x_{n-1}$ and the integrator output can be expressed as

$$u_{n+1} = pu_n + x_n - x_{n-1} \tag{4-64}$$

Therefore, if the input sequence x has a period of L samples, the decay over one period can be expressed as

$$u_{(k+1)L+j} = p^L u_{kL+j} + \beta_j$$
$$\beta_j = \sum_{i=0}^{L-1} p^i (x_{j-1-i} - x_{j-2-i}) \qquad j \in [1,L] \tag{4-65}$$

The terms β_j can be calculated exclusively from the input sequence. It can thus be seen that the integrator leakage actually pushes the integrator output towards zero through the term p^L, but the actual decay also depends on β. Actually, β can counteract the effect of p^L. If β is positive for a negative u_n, there may be a stable solution U such that,

$$U_j = u_{kL+j} = u_{(k+1)L+j} \qquad \forall k$$
$$U_j = \frac{\beta_j}{1-p^L} \tag{4-66}$$

For that solution to be stable, it must satisfy Eq (4-62), that is,

$$(Quant(u_j^s) = x_{j-1}) \Leftrightarrow \begin{cases} u_j^s > 1 - \dfrac{\Delta_{DAC}}{2} & \text{if} \quad x_{j-1} = 1 \\ u_j^s < -1 + \dfrac{\Delta_{DAC}}{2} & \text{if} \quad x_{j-1} = -1 \end{cases} \tag{4-67}$$

In order to ease the interpretation for any sequence, the study can be restricted for values of p close to 1 (small leakage). Then, by taking $p=1-\Delta p$, we obtain

$$\lim_{\Delta p \to 0} U_j = \frac{-\sum_{i=1}^{L-1} i(x_{j-1-i} - x_{j-2-i})}{L} = -Q + x_{j-1} \tag{4-68}$$

In this case, the condition for the output sequence to follow the input sequence (Eq (4-67)) becomes

$$|Q| < \frac{\Delta_{DAC}}{2}. \tag{4-69}$$

Notice that for a one-bit quantizer $\Delta_{DAC}=2$ and the stability condition is always fulfilled, meaning that for any input sequence, the output will always follow the input. That is consistent with the result of [32].

4 • 1 . 3 . 3 First order single-bit modulator

In the case of a single-bit modulator, the linear model does not apply in any way and its behavior is better described by non-linear dynamics. As was seen in the case of the multibit modulator study, if a digital sequence is applied at the input of a single-bit 1^{st} order modulator its output bitstream follows the input, whatever the value of the integrator leakage. This effect has been described in [32] and is verified using Eq (4-69). Therefore the mean value of the modulator output will follow the mean value of the input sequence for any value of the integrator leakage. And the test that can be applied to 2^{nd} order modulators is thus insensitive to leakage for 1^{st} order single-bit modulators.

Conceptually, it seems that the feedback is too tight to allow any deviation from the input sequence. As the first order modulator under normal operating conditions is very robust to non-idealities, what we propose is to relax the feedback and bring the modulator out of its normal operation, in over-range. For this to be done, we have to include an extra delay in the feedback path.

Then, the same procedure is used to evaluate the integrator leakage. A sequence with a non-zero mean value is fed to the modulator, and the mean value of the output bitstream depends on the integrator leakage. Nevertheless, the reasoning to derive this relation is not as simple as for the second order modulator as the linear model cannot be used. Actually, the mean value of the output bitstream turns out to be a complex non-linear function of the integrator leakage. Fortunately, a Taylor development of this function for a small leakage will simplify its evaluation.

The reasoning that has to be followed to derive the relation between the integrator leakage and the output bit stream mean value is similar to the one that was carried out to derive the validity range of input sequences in the case of a multibit modulator. In the ideal case of an integrator with no leakage, the output bitstream of the modified modulator is periodic and its mean value is equal to the input sequence mean value. Moreover, the integrator output u_n follows a periodic pattern on three levels,

$$u = \gamma + \begin{cases} 2 \\ 0 \\ -2 \end{cases} \qquad |\gamma| < 2 \tag{4-70}$$

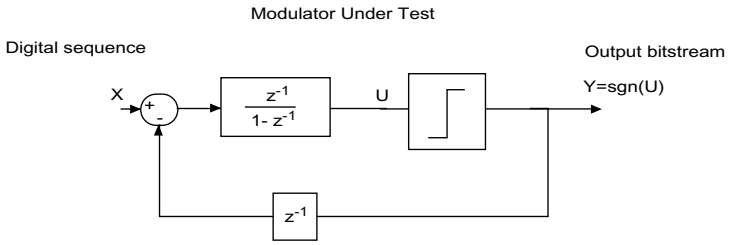


Figure 4-7: z-domain representation of a first-order single-bit ΣΔ modulator with an extra delay in the feedback path.

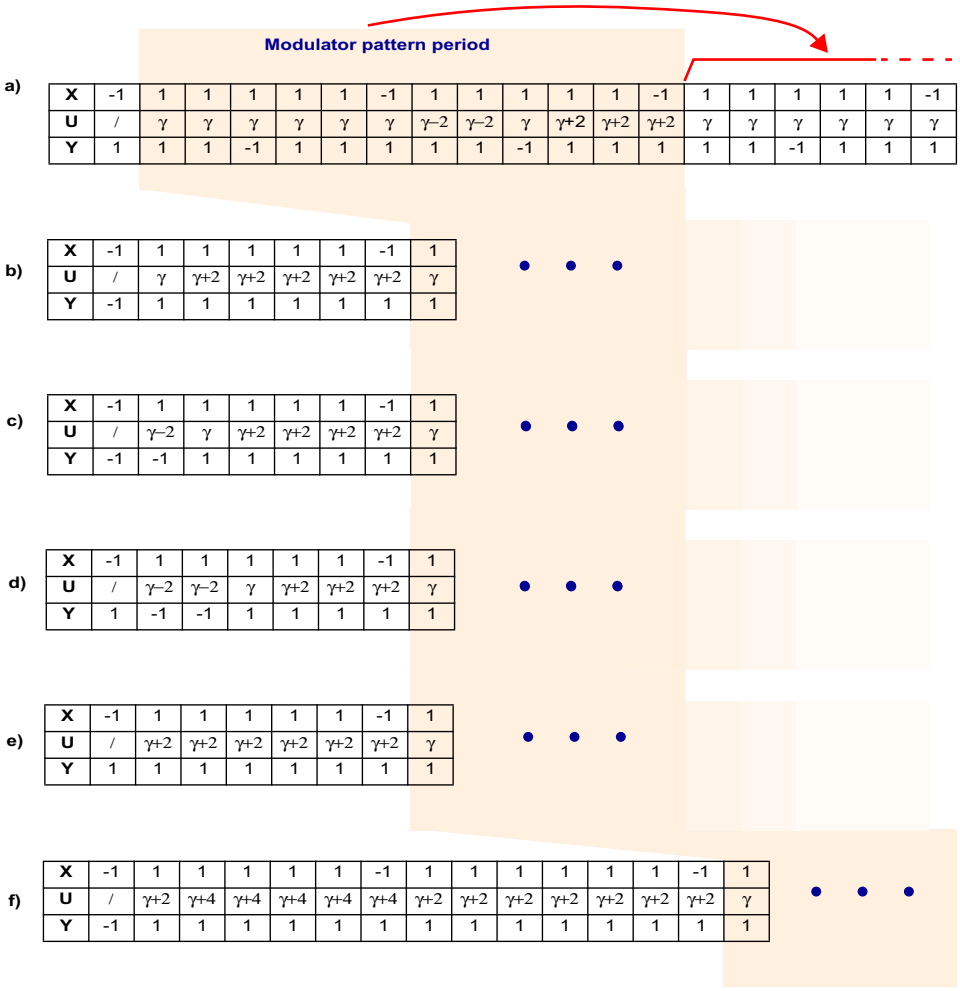
If the integrator is leaky, a decay will be superimposed to that pattern, just like in the case of the multibit modulator.

However, in the case of the multibit modulator it was possible to solve the modulator equation for finding the output pattern. But when an extra delay is introduced in the feedback loop, it becomes very difficult to derive a general solution for any input sequence. Therefore, we limit our study to sequences of the form L-1 "1s" and 1 "-1". For such sequences, it can be shown, doing a case analysis in the time domain, that the integrator output follows a fixed pattern. This case study has been carried out using the difference equation that represents the modified modulator of Figure 4-7:

$$u_{n+1} = x_n + u_n - \mathrm{sgn}(u_{n-1}) \qquad \textbf{(4-71)}$$

For instance, consider a [1 1 1 1 1 -1] input sequence for six cases of the modulator initial state. The modulator initial state is defined by the integrator output at instant 0 and the sign of the integrator output at instant -1. This case study is represented in Figure 4-8. Extrapolating these six cases, it can be seen that the integrator output locks into a fixed pattern after few periods of the input sequence.

The integrator pattern for a generic input sequence is thus of the form shown in Figure 4-9. This pattern period (of length $2L$) begins with L samples at a central level γ that is strictly positive and less than 2. The 2 next samples are at γ-2 and are thus negative. The following sample brings the integrator output back to the central level γ and the remaining L-3 samples are at level γ+2. The modulator output is equal to the sign of the integrator output, $y_n=sign(u_n)$, and consists of L "1s", 2 "-1s" and L-2 "1s". The modulator output mean value is thus $(L\text{-}2)/L$, which is equal to the input sequence mean value Q.



a)

X	-1	1	1	1	1	1	-1	1	1	1	1	1	-1	1	1	1	1	1	-1
U	/	γ	γ	γ	γ	γ	γ	γ−2	γ−2	γ	γ+2	γ+2	γ+2	γ	γ	γ	γ	γ	γ
Y	1	1	1	-1	1	1	1	1	1	-1	1	1	1	1	1	-1	1	1	1

b)

X	-1	1	1	1	1	1	-1	1
U	/	γ	γ+2	γ+2	γ+2	γ+2	γ+2	γ
Y	-1	1	1	1	1	1	1	1

c)

X	-1	1	1	1	1	1	-1	1
U	/	γ−2	γ	γ+2	γ+2	γ+2	γ+2	γ
Y	-1	-1	1	1	1	1	1	1

d)

X	-1	1	1	1	1	1	-1	1
U	/	γ−2	γ−2	γ	γ+2	γ+2	γ+2	γ
Y	1	-1	-1	1	1	1	1	1

e)

X	-1	1	1	1	1	1	-1	1
U	/	γ+2	γ+2	γ+2	γ+2	γ+2	γ+2	γ
Y	1	1	1	1	1	1	1	1

f)

X	-1	1	1	1	1	1	-1	1	1	1	1	1	1	-1	1
U	/	γ+2	γ+4	γ+4	γ+4	γ+4	γ+4	γ+2	γ+2	γ+2	γ+2	γ+2	γ+2	γ+2	γ
Y	-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 4-8: **Time-domain case study for a [1 1 1 1 1 -1] input sequence**
a) initial condition: $0<u_0=\gamma<2$ and $sgn(u_{-1})=1$;
b) initial condition: $0<u_0=\gamma<2$ and $sgn(u_{-1})=-1$;
c) initial condition: $-2<u_0=\gamma-2<0$ and $sgn(u_{-1})=-1$;
d) initial condition: $-2<u_0=\gamma-2<0$ and $sgn(u_{-1})=1$;
e) initial condition: $2<u_0=\gamma+2<4$ and $sgn(u_{-1})=1$;
f) initial condition: $2<u_0=\gamma+2<4$ and $sgn(u_{-1})=-1$;

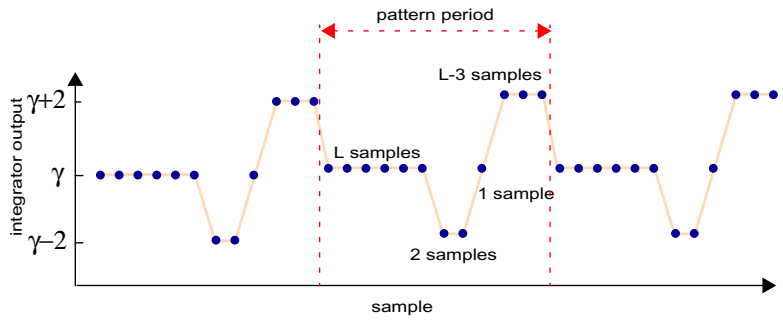


Figure 4-9: Pattern followed by the integrator output

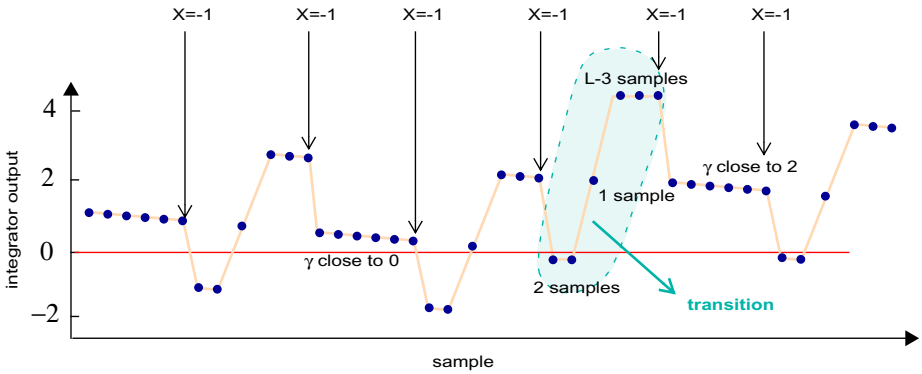


Figure 4-10: Transition pattern for the case of a leaky integrator

For a leaky integrator, a small decay perturbs the ideal pattern. If this decay is sufficient to make the central level γ cross zero, the pattern is broken and the modulator output is modified. When the central level crosses zero, the integrator output exhibits transitions of the form shown in Figure 4-10. This transition (of length *L*) brings the central level (γ in Figure 4-9) back to 2, and the integrator output enters in a new cycle of decaying patterns. The first two samples of this transition are close to zero but negative. The third sample is close to 2 and the following *L*-3 samples are close to 4. Then the modulator output during the transition is 2 "-1s" and *L*-2 "1s" and its mean value is (*L*-4)/*L*.

Thus, the counter output measuring the deviation of the output bitstream from the input bitstream can be written as

$$s_1 = LN_{tran}\frac{L-2}{L} - LN_{tran}\frac{L-4}{L} = 2N_{tran}, \tag{4-72}$$

where N_{tran} is the number of transitions over the record length N. In order to calculate N_{tran} explicitly, the number of pattern periods necessary for the central level to decay from 2 to 0 must be found.

Let u_{2jL} be the integrator output at the beginning of a pattern period. From the z-domain model of Figure 4-4, it can be shown that the integrator output at the beginning of the next pattern period will be

$$\begin{aligned} u_{(j+1)2L} &= p^{2L}u_{j2L+j} + \alpha \\ \alpha &= -2 + 2p^{L-2} + 2p^{L-3} - 2p^{L} \end{aligned} \tag{4-73}$$

If α compensates for the decay due to the term p^L, the modulator can lock into a stable pattern, just as has been seen for the multibit 1st order modulator. This occurs if the solution U of the equation

$$U = p^{2L}U + \alpha \tag{4-74}$$

is of the right sign. As u_{j2L} must correspond to a positive output, the lock condition can be written

$$U = \frac{\alpha}{1-p^{2L}} > 0\,. \tag{4-75}$$

By taking the limit of this value when p tends to 1, it becomes

$$\lim_{p \to 1} U = \frac{5-L}{L} > 0 \Leftrightarrow L < 5\,. \tag{4-76}$$

Therefore, in order to get sensitivity to integrator leakage, that is, for the modulator not to lock into a fixed pattern, a sequence of length greater than 5 should be used.

If u_{mid} is the value of the medium level just after a transition, the integrator output after k pattern periods is

$$u_{2kL} = p^{2kL}u_{mid} + \alpha\frac{1-p^{2kL}}{1-p^{2L}}\,. \tag{4-77}$$

Actually, the transition will bring the central level to a value u_{mid} that is slightly lower than 2. This level can be calculated, taking into account the fact that the first point in the transition in Figure 4-9 is zero. It becomes

$$u_{mid} = -2 + 2p^{L-2} + 2p^{L-3}. \tag{4-78}$$

Then, the number of pattern periods between two transitions is the solution of $u_{2kL}=0$, which is, using Eq (4-77)

$$k = \left\lceil \frac{\ln\left(\frac{\alpha}{\alpha - (1-p^{2L})u_{mid}}\right)}{2L\ln(p)} \right\rceil. \tag{4-79}$$

Therefore, N_{tran} can be written as

$$N_{tran} = \left\lfloor \frac{N}{2kL+L} \right\rfloor \tag{4-80}$$

taking into account the fact that the pattern period has a length of $2L$ samples and a transition of L samples. The counter output can thus be written explicitly using Eq (4-79) and Eq (4-80) as

$$s_1 = 2\left\lfloor \frac{N}{2L\left(1+\left\lceil \frac{\ln\left(\frac{-2+2p^{L-2}+2p^{L-3}-2p^{L}}{-2+2p^{L-2}+2p^{L-3}-2p^{L}-(1-p^{2L})(-2+2p^{L-2}+2p^{L-3})}\right)}{2L\ln(p)} \right\rceil\right)} \right\rfloor \tag{4-81}$$

This is a strongly non-linear function of p, but it can be simplified, assuming that $\Delta p=1-p$ is small. In this case,

$$s_1 \approx \frac{2N\Delta p}{\ln\left(\frac{5-3L}{5-L}\right)} \tag{4-82}$$

Here again, if a small input-referred offset is present at the modulator input, the result will be modified slightly. Actually, the offset contribution has to be taken into account in the calculation of α in Eq (4-73). If *off* is the input referred offset, we obtain

$$\alpha = -2 + 2p^{L-2} + 2p^{L-3} - 2p^{L} + off\frac{1-p^{2L}}{1-p} \tag{4-83}$$

This new α has thus to be considered in Eq (4-79). Nevertheless, some care must be taken if the offset compensates the decay. Taking a close look at the lock condition (consid-

ering the new α in the unequality of Eq (4-75)), a domain (*off, p*) may exist where the modulator output locks to the input sequence. Over this domain, the term in the logarithm of the numerator in Eq (4-79) would become negative. This is not numerically valid and Eq (4-79) does not make sense either. Indeed, if the modulator output locks to the input sequence, there are no transitions. Mathematically, *k* tends to infinity and the counter output to zero. That is consistent with what was said, as the output locks into the fixed pattern which has a same mean value as the input.

If the input referred offset is sufficiently small, one can still use a first order approximation

$$s_1 \approx \frac{2N\Delta p}{\ln\left(\frac{5-3L}{5-L}\right)} + Noff \tag{4-84}$$

Here again, performing two acquisitions s_1 and s_2 with two opposite sequences will allow one to compensate for the offset, and we should thus have

$$s = s_1 - s_2 = \frac{4N\Delta p}{\ln\left(\frac{5-3L}{5-L}\right)} \tag{4-85}$$

and also

$$s' = s_1 + s_2 = 2Noff \tag{4-86}$$

A drawback of this method is that, as two opposite sequences are used, the input referred offset will tend to compensate the leakage effect for one of the two. Thus, the linearity of the counter output may be severely compromised. Another solution could be to calculate the parameters using two sequences of different lengths (L_1 and L_2) but of the same sign, providing that their mean values have a sign opposite to the offset. In that case, the strong non-linearity does not occur, and we obtain

$$s = s_1 - s_2 = 2N\Delta p\left(\frac{1}{\ln\left(\frac{5-3L_1}{5-L_1}\right)} - \frac{1}{\ln\left(\frac{5-3L_2}{5-L_2}\right)}\right) \tag{4-87}$$

and

$$off = \frac{s_1 \ln\left(\frac{5-3L_1}{5-L_1}\right) - s_2 \ln\left(\frac{5-3L_2}{5-L_2}\right)}{N\left[\ln\left(\left(\frac{5-3L_1}{5-L_1}\right) - \ln\left(\frac{5-3L_2}{5-L_2}\right)\right)\right]}. \quad \textbf{(4-88)}$$

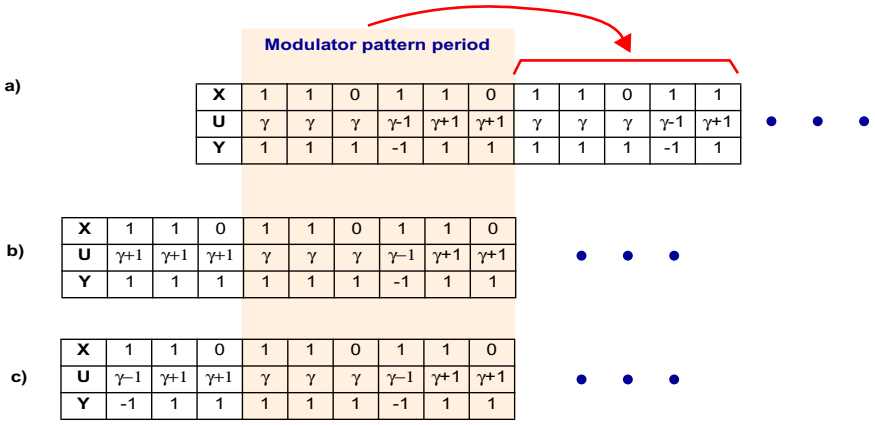
Considering Eq (4-72), the precision of the leakage evaluation is determined by the number of sensed transitions. Suppose that the leakage produces a transition every 1000 samples, the same number of transitions will be sensed if N+1 samples are acquired as if N+999 samples are acquired. This rounding operation is neglected to achieve the linearized signature of Eq (4-85). For small leakages and no input-referred offset, this rounding operation is thus the major precision-limiting factor. If we consider that an error of 1 sensed transition can occur, we can thus re-write Eq (4-85) taking into account the error

$$s = s_1 - s_2 = 2(N_{tran1} \pm 1) + 2(N_{tran2} \pm 1) = \frac{4N\Delta p}{\ln\left(\frac{5-3L}{5-L}\right)} \pm 4 \quad \textbf{(4-89)}$$

An alternative has also been introduced in Section 4 • 1 . 2 . 3 that consists in using test sequences of the form [1 1 1 1 ... 1 0] (and [-1 -1 - 1 ... -1 0] to cancel input referred offset) of period L. It has been said that for such sequences, it is not necessary to add a delay in the feedback path of the modulator. A case analysis in the time domain shows that the modulator output for an ideal integrator is periodic of period 2L with a number 2L-1 of “1” and 1 “-1”. Such a case analysis can be seen in Figure 4-11 where a [1 1 0] input sequence is considered for 3 values of the integrator initial condition. Extrapolating these three cases, it can be seen how the integrator output (and consequently the modulator output) settles into a periodic pattern after a few periods of the input sequence. The integrator output pattern period for a generic sequence of L-1 “1” and one 0 is represented in Figure 4-12.

Integrator leakage superimposes a decay on the global pattern. At a given instant, the maximum level γ+1 becomes less than 1. At the next 0 input, the integrator output becomes negative and a transition occurs. The form of the transition can be seen in Figure 4-13. After such a transition, the integrator output locks back into a pattern with γ=1.

The same demonstration synopsis as for the case of a conventional sequence and an extra delay in the feedback path can be followed:



X	1	1	0	1	1	0	1	1	0	1	1	
U	γ	γ	γ	γ-1	γ+1	γ+1	γ	γ	γ	γ-1	γ+1	
Y	1	1	1	-1	1	1	1	1	1	-1	1	

X	1	1	0	1	1	0	1	1	0	
U	γ+1	γ+1	γ+1	γ	γ	γ	γ−1	γ+1	γ+1	
Y	1	1	1	1	1	1	-1	1	1	

X	1	1	0	1	1	0	1	1	0	
U	γ−1	γ+1	γ+1	γ	γ	γ	γ−1	γ+1	γ+1	
Y	-1	1	1	1	1	1	-1	1	1	

Figure 4-11: **Time-domain case analysis. a) integrator initial condition 0<γ<1; b) integrator initial condition 1<γ+1<2; c) integrator initial condition -1<γ−1<0**

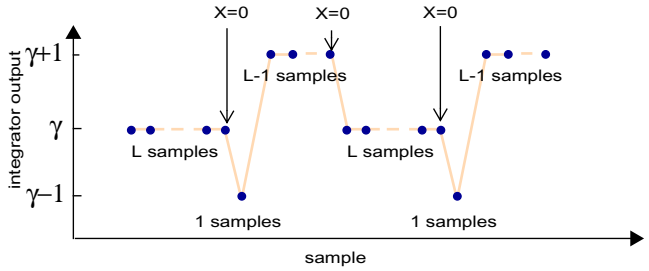


Figure 4-12: **Pattern followed by the integrator output**

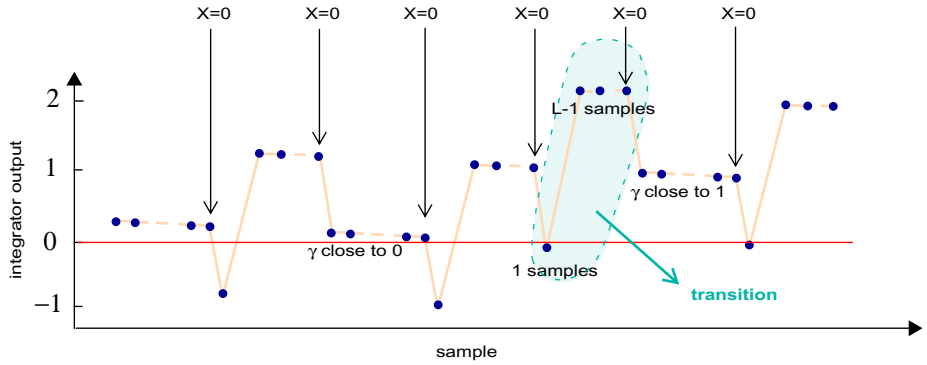


Figure 4-13: **Transition pattern at the integrator output for a leaky integrator**

i) the decay due to integrator leakage is calculated over one period of the integrator pattern.

ii) The number of pattern periods necessary to bring the central level γ from 1 (just after a transition) to 0 (just at the transition) is calculated

iii) The number of transitions in an acquisition register is evaluated which gives the expected signature

Indeed, the modulator output mean value over one period of the pattern is equal to *(L-1)/L*, which equals the input sequence mean value. The modulator output mean value over a transition is, in turn, (L-2)/L. Hence, the test signature is equal to

$$s_1 = LN_{tran}\frac{L-1}{L} - LN_{tran}\frac{L-2}{L} = N_{tran}\ , \qquad \textbf{(4-90)}$$

where N_{tran} is the number of transitions that occur during the acquisition. Following the above described synopsis, we obtain

$$s_1 = \left\lfloor \frac{N}{L\left(1 + \left\lceil \frac{\ln\left(\frac{-1-2p^{L}+2p^{L-1}}{-1-2p^{L}+2p^{L-1}-(1-p^{2L})\left(-1+2p^{L-1}\right)}\right)}{L\ln(p)} \right\rceil\right)} \right\rfloor \qquad \textbf{(4-91)}$$

In order to suppress partially the impact of the offset, another acquisition is performed with the opposite sequence and the difference between the two signatures can be calculated as

$$s = s_1 - s_2 \approx \frac{2N\Delta p}{\ln\left(\frac{3L-2}{L-2}\right)}. \qquad \textbf{(4-92)}$$

Similarly to what was said for the regular sequences (with no zero), the results from two acquisitions with different sequences (of length L_1 and L_2 respectively) can be combined to avoid the potential non-linearity related to the offset. The result obtained is similar to Eq (4-87):

$$s = s_1 - s_2 = N\Delta p\left(\ln\left(\frac{2-3L_1}{2-L_1}\right)^{-1} - \ln\left(\frac{2-3L_2}{2-L_2}\right)^{-1}\right) \qquad \textbf{(4-93)}$$

4 • 2 LEAKAGE TEST VALIDATION THROUGH SIMULATION

In this sub-section, we will provide a proof-of-concept for the previously proposed tests and check the validity of the assumptions realized in the theoretical analysis. Hence, we will simulate the z-domain models of the modulators using the MATLAB Simulink tool. The only non-ideal defects contemplated in the simulations presented here are the integrator leakages.

A more realistic approach is carried-out in a later chapter, considering complex behavioural models and simultaneous variations of the behavioural parameters of interest.

4 • 2 . 1 Second order modulator

◆ **Variation with the input sequence mean value**

We simulated 200 sequences with different mean value, for 3 values of Δp_1 (0, 0.05 and 0.1). The sequences were determined by choosing a random rational number and determining the corresponding sequence with the euclidian algorithm [30]. The reason for this is that this algorithm gives the most homogeneous periodic sequence, that is optimum to maintain the integrator output excursion as limited as possible (notice that these sequences correspond to the limit cycle of a first order ΣΔ modulator with a input DC value equal to our rational number Q). In this case p_2 was arbitrary fixed at 1. Moreover, for each point in the simulation, the initial conditions of the integrators were chosen randomly. The signature should ideally be computed over a number of samples multiple of the input sequence period in order to avoid any bias in the signature, as stated in Eq (4-35).

However it is not practical to compare the different signatures on the same figure for different number of acquired samples. Hence, the output bitstream was summed up over 5000 samples for all sequences.

Figure 4-14 represents the test signature versus the mean value of the input sequence. It appears clearly that the test signature exhibit a linear relationship with the input sequence mean value.The slope of this relation clearly depends on the integrator leakage. This is what we will show with the next simulations.

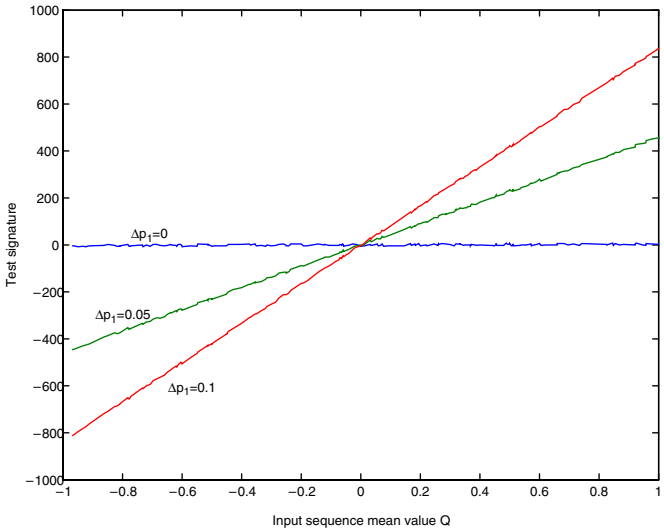


Figure 4-14: Test signature output as a function of the input sequence mean value

◆ **Variation with the leakage**

In order to verify the relationship between the first integrator leakage and the signature, we simulated 20 acquisitions over 6000 points, linearly sweeping the pole error Δp_1 from 0 to 0.05. The input sequence mean value is Q=2/3. Notice that Δp_1=0.05 corresponds, according to Eq (4-3), to an amplifier DC gain of only 20dB.

Figure 4-15 represents the signature output as a function of the pole error Δp_1. The cross markers correspond to the 20 simulated acquisitions. The red line corresponds to the expected signature, accordingly to Eq (4-38). It can be seen that the simulated signatures match very well the expected ones if the integrator leakage remains low (i.e. for small Δp), but deviates from the linear curve for higher leakages. This can be explained easily taking a look at the orange line that represents the expected signature before Taylor linearization of Eq (4-37). It can be seen that the simulated signatures perfectly match that curve, which means that the deviation actually comes from a second order effect.

Figure 4-16 represents the same thing as Figure 4-15 but in this case, the second integrator leakage was set to Δp_2=0.05. Once again it can be seen that the simulated signatures

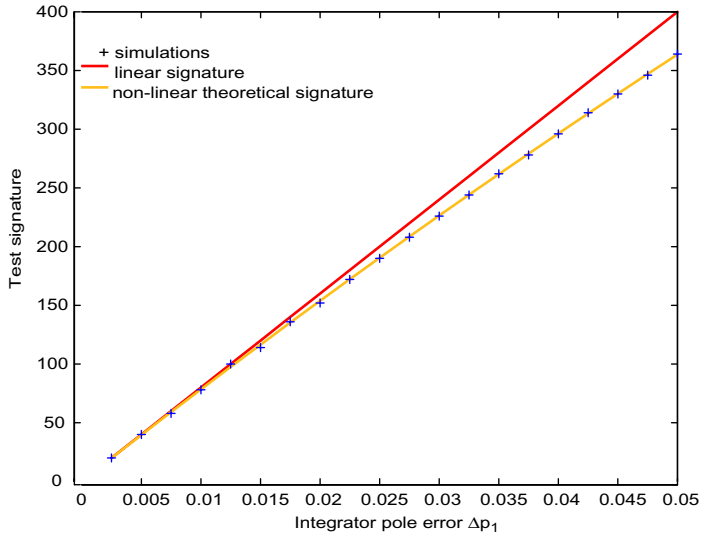


Figure 4-15: Test signature output as a function of the first integrator leakage (Δp_2=0)

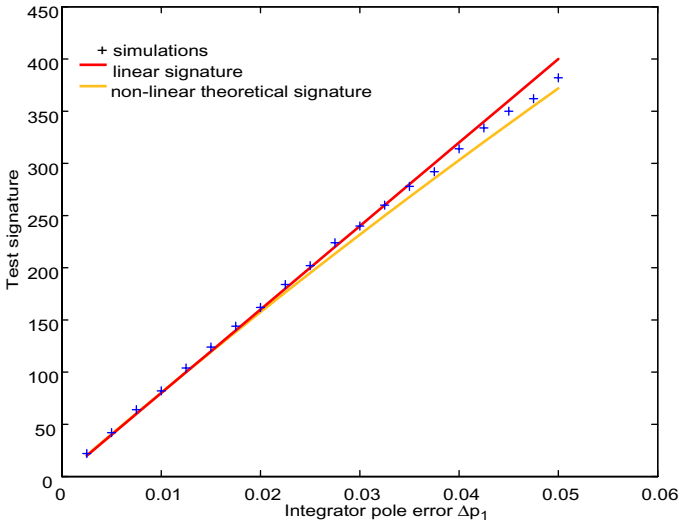


Figure 4-16: Test signature output as a function of the first integrator leakage (Δp_2=0.05)

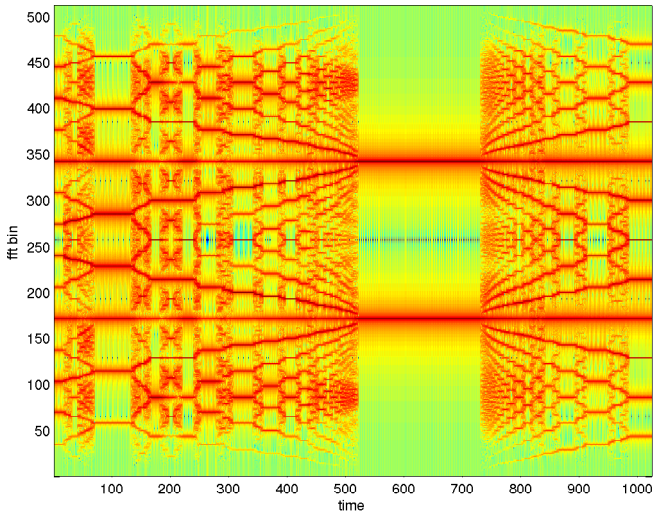


Figure 4-17: Evolution in time of the output bitstream spectrum for a [1 1 -1] input sequence

match very well the expected ones if the integrator leakage remains low (i.e. for small Δp). For higher leakages, the signature deviates slightly from the expected one. Notice however that the simulated signatures do not match the non-linear curve of Eq (4-38) as well as for Figure 4-15. This is due to the fact that the linearization of the quantizer is an approximation that still show its limits for second order modulators. Hence, we can justify those differences by a non-linear dynamic behaviour. In any case, it should be stressed that this slight differences do not produce a major deviation from the linear signature. On the contrary, the simulated signatures are closer to the linear signature than in the case of Figure 4-15.

In order to illustrate the "strange" non-linear dynamics of the 2nd modulator, take a look at Figure 4-17. It represents the evolution of the output bitstream spectrum with time for an input sequence [1 1 -1]. This figure was obtained acquiring 60000 samples of the output bitstream of a second-order modulator with Δp_1=10^{-5} and Δp_2=0.0666. Then the 60000 samples were divided in 1024 evenly-spaced registers of 512 points and the FFT was calculated for each register. Hence, in Figure 4-17, the horizontal axis represents the register index (i.e. the time) and the vertical axis represents the FFT frequency bin. The height of the FFT bin associated to a color ranging from the red for the highest tones to the blue for the lowest tones. A curious diagram is obtained that seems to indicate that the modulator output toggles

between well-defined periodic sequences. Indeed, it can be seen that for the time index from 500 to 700 approximately, the sequence has a well defined period of $f_s/3$ as two tones (in red) clearly appear at $f_s/3$ and $2f_s/3$ (f_s being the modulator sampling frequency that corresponds to bin 512). However at time index 100, the period of the sequence seems to be $f_s/9$. The evolution from one sequence to another seems to correspond to a kind of chaotic behavior.

◆ Variation with the number of points

In Figure 4-18, we represent the evolution of the signature as a function of the number of acquired points, in order to verify the evaluation error. For that we simulated a modulator with $\Delta p_1=10^{-3}$ and $\Delta p_2=0$ with a Q=2/3 input sequence. It is not necessary to repeat the acquisition for several number of points. Instead, we perform only one acquisition over a large number of points (100000) and vary the number of points for the signature computation by taking into account only the first N points of the 100000 acquired points.

We represent the mean value of the difference between the input and the output of the modulator instead of its sum. By doing so, the central result does not depends on the number of acquired points and the evaluation error is more readable. Actually, accordingly to Eq (4-42), the expected curve should follow,

$$s^* = 4Q\Delta p_1 \pm \frac{6}{N}\sqrt{\frac{2}{3}} \qquad \textbf{(4-94)}$$

Figure 4-18 shows the evolution of the alternative signature defined above with the number of acquired samples. Notice that the signatures were computed for values of N multiple of 96, which are multiple of 6 as required. Together with the simulation results, we represent the expected center value and the associated confidence interval of Eq (4-94). It appears clearly that the measurement error lies in between the calculated upper and lower bounds.

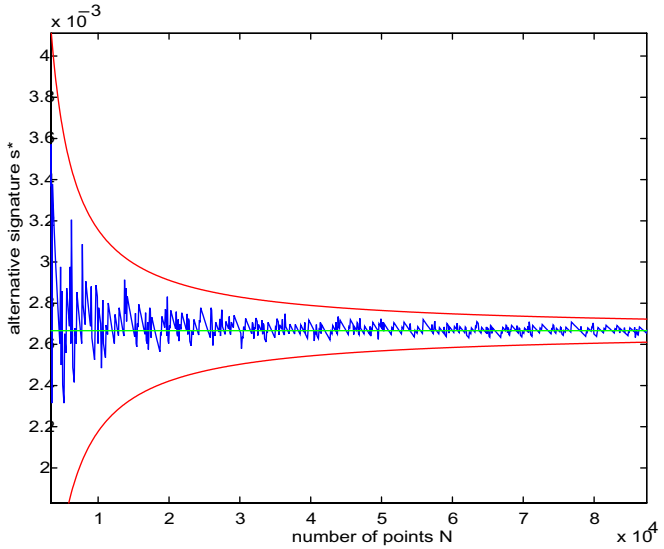


Figure 4-18: Evolution of the evaluation error with the number of samples.

4 • 2 . 2 Multibit first-order modulator

◆ **Variation with the input sequence mean value, verification of the Q limit**

The condition Eq (4-21) can be better understood by taking a look at Figure 4-19 and 4-20. Two modulators with 2-bit and 3-bit quantizers have been simulated over 5000 points for 200 input sequences with different mean value. The signature of Eq (4-24) is represented versus the mean value of the input sequence for three values of integrator leakage, namely Δp=0.1, 0.05 and 0. It can easily be seen that the three curves collapse to the leakage-free case for small input sequence mean values. This verifies the theory that the output bitstream follows the input sequence for sequences that respect the lock condition of Eq (4-21). Actually, it can be seen that the limit value correspond to $\frac{\Delta_{DAC}}{2}$ =2/3 and 2/7 respectively, as expected.

Moreover, it appears that when the lock condition is not fulfilled, the signature is sensitive to the integrator leakage. The quantizer linearization approximation shows its limit for a multibit first order modulator, in particular for low-resolution quantizers (this is

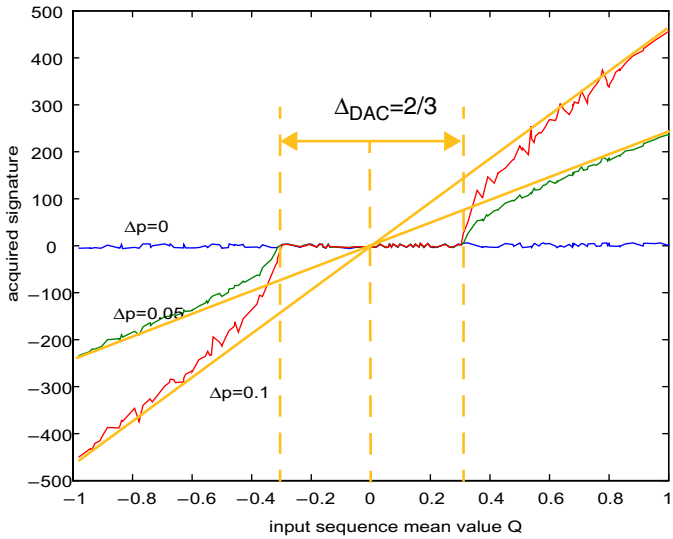


Figure 4-19: Test signature output as a function of the input sequence mean value, for a 2-bit modulator

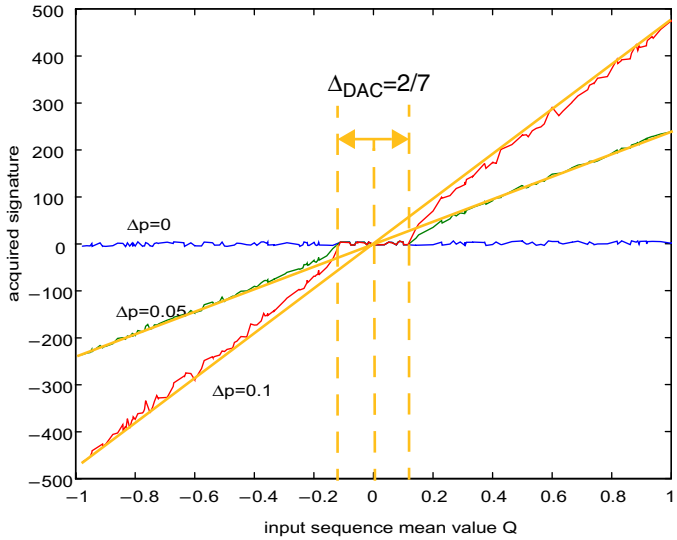


Figure 4-20: Test signature output as a function of the input sequence mean value, for a 3-bits modulator

coherent with Bennett conditions [20]). Hence, it seems that apart from the quantization noise error, the proposed signature will be limited by a systematic error of the form,

$$err = 2Nf(Q)\Delta p\,, \tag{4-95}$$

where *f(Q)* is a non-linear function of the input sequence mean value, which is much less than unity.

◆ **Variation with the leakage**

In order to verify the relationship between the first integrator leakage and the signature, we simulated 20 acquisitions over 6000 points, linearly sweeping the pole error Δp from 0 to 0.05.

Figure 4-21 and 4-22 represent the signature output as a function of the pole error Δ*p*, for a 3-bit quantizer and a 2-bit quantizer, respectively. The cross markers correspond to the 20 simulated acquisition. The red line corresponds to the signature predicted by Eq (4-24). It can be seen that the simulated signatures match the expected ones very well if the integrator leakage remains low (i.e. for small Δ*p*), but deviates from the linear curve for higher leak-

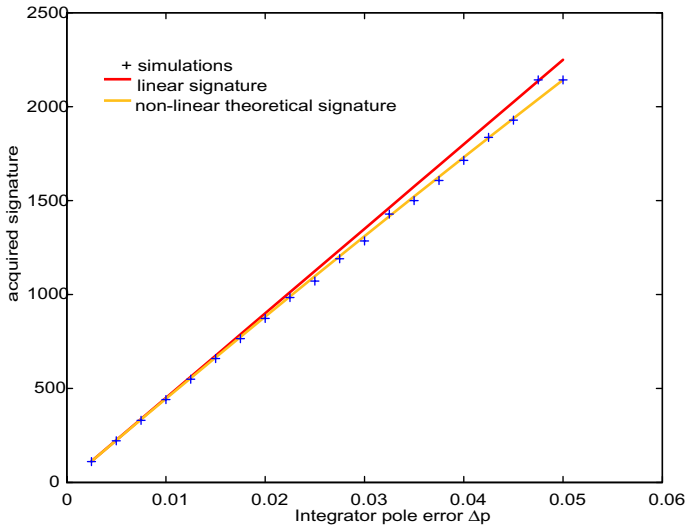


Figure 4-21: Test signature output as a function of the integrator leakage (Δp) for a 3-bit first-order modulator

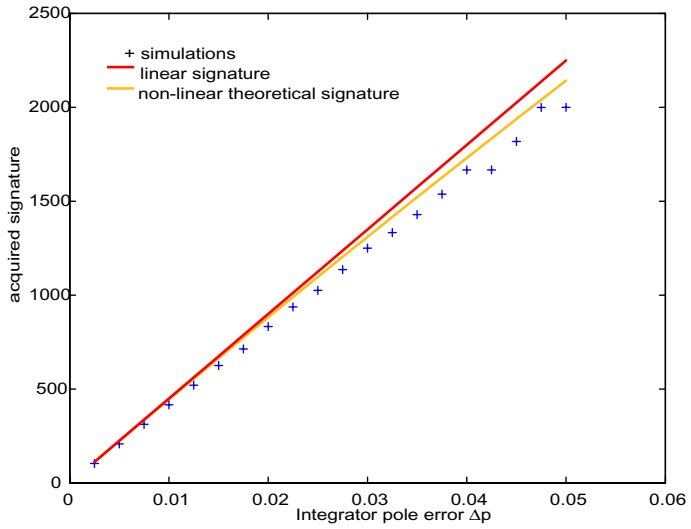


Figure 4-22: Test signature output as a function of the integrator leakage (Δp) for a 2-bit first-order modulator

ages. This can be partially explained by taking a look at the orange curve that represents the expected signature before Taylor linearization of Eq (4-52). It can be seen that the simulated signatures match that curve better. However, this expected non-linearity is not sufficient to explain the deviation. The remaining deviation is due to the error introduced in Eq (4-95) that manifests itself as a slope error for the signature, as was pointed out above. In accordance to what can be seen in Figure 4-19 and Figure 4-20, this slope error is more important for the lower quantizer resolution.

◆ **Variation with the number of points**

Figure 4-23 depicts the evolution of the signature as a function of the number of acquired points. Once again, a 2-bit and a 3-bit first-order modulator were simulated, with Δp=0.995. The input sequence was set to Q=2/3. The red line represents the expected signature according to Eq (4-24). It can be seen that, as we quoted above, the expected signature overestimates the actual signature. This puts an upper limit on the achievable precision. Indeed if the signature is used to evaluate Δp, the increase of the number of points will help to reduce the noise related error but not the systematic error. Fortunately, this systematic

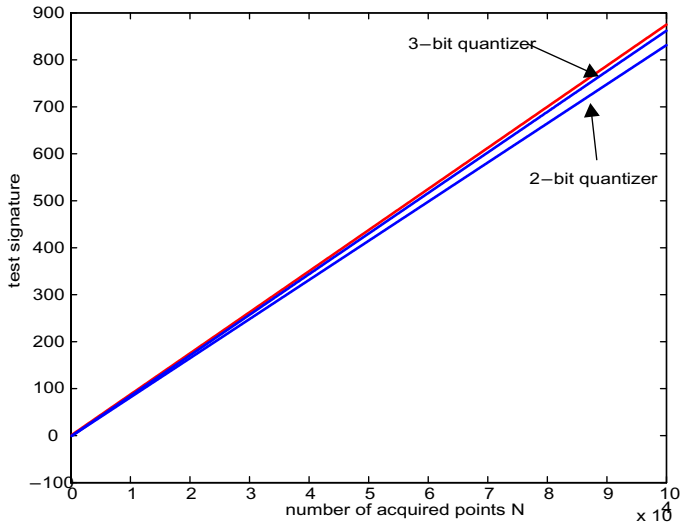


Figure 4-23: Test signature as a function of the number of acquired points for a 3-bit quantizer and a 2-bit quantizer

error is not fixed but is proportional to the leakage Δp, as stated in Eq (4-95). Hence, we can say that the leakage can be determined within a relative precision. This relative precision depends on the mean value of the input sequence and the resolution of the coarse quantizer. Figure 4-24 shows a set of curves that represent the evolution of this relative error as a function of the input sequence, for quantizers with a number of bits from 2 to 4. It appears that the relative error is lower for high test sequence mean values and for the higher number of bits. Actually, if the input sequence mean value is higher than 0.7, the relative error is lower than 10%, even for a 2-bit quantizer.

If we aim only at detecting the nominal pole error and not at measuring it, the number of points to be acquired has to be calculated such that the signature rise just above the random noise. In that case, the relative measurement error is just below 100%. Hence, from a test viewpoint, this relative error limit is not relevant. If this scheme is used to measure the integrator leakage for calibration purposes, however, this error may affect the results. Anyway, if the sequence is properly chosen, the leakage can be determined with a relative error lower than 10%, which should rise significant improvement on the calibrated modulator.

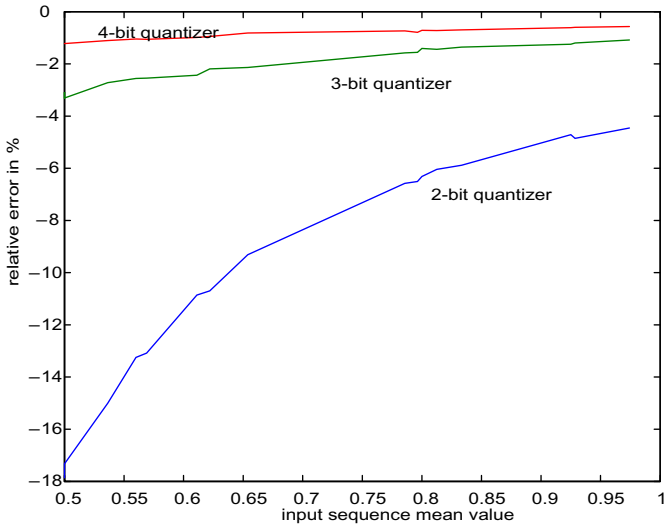


Figure 4-24: Relative error on the measurement of Δp as a function of the input sequence mean value Q.

4 • 2 . 3 Single-bit first-order modulator

◆ **Verification of the pattern**

The objective of these first simulations is to verify that the pattern depicted in Figure 4-9 and 4-10 are produced in simulations. For that, we simulated a first-order single-bit modulator for different values of leakage. It is important to remember that a restriction was put on the type of input sequences (see Eq (4-25)).

Figure 4-25 represents the evolution of the integrator output for a sequence of L=6, for pole errors Δp=0, Δp=0.001, and Δp=0.005. It shows that the integrator output actually suffers a decay that leads to periodic transitions, as explained in section 4 • 1 . 3 . 3. The decay is a function of the integrator leakage, such that more transitions occur for higher Δp. A zoom over the pattern period for the three cases shows that the leakage does not change the periodic pattern, which corresponds to Figure 4-9. Another zoom on the transitions shows that the pattern predicted in Figure 4-10 is also respected.

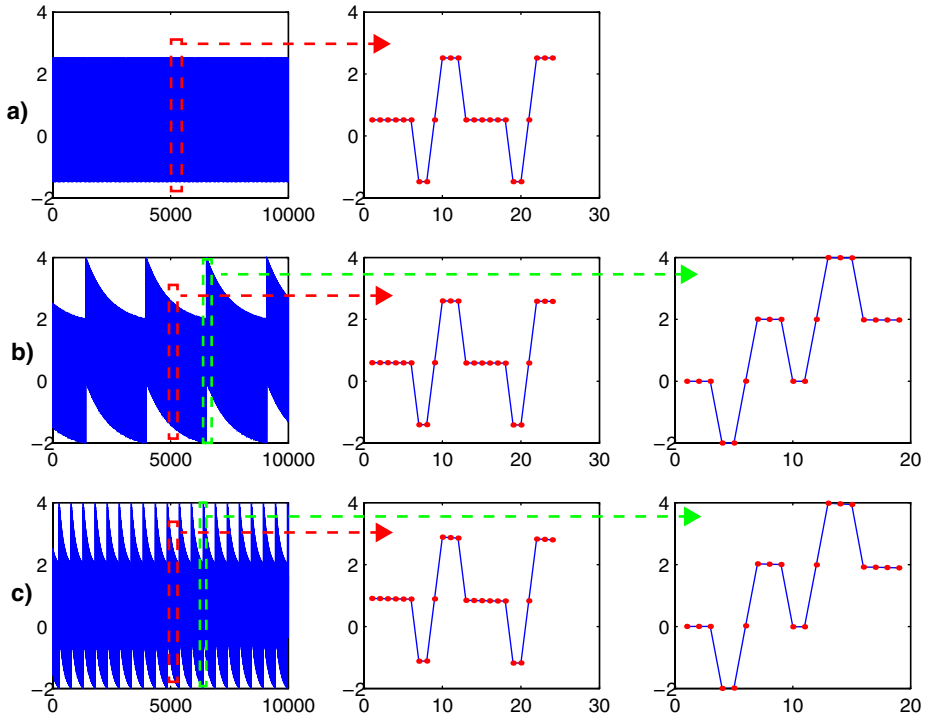


Figure 4-25: Integrator output, for a 1st order single-bit modulator.
a) leakage-free modulator: global view, zoom on the pattern
b) Δp=0.001: global view, zoom on the pattern, zoom on the transition
c) Δp=0.005: global view, zoom on the pattern, zoom on the transition

◆ **Variation with the input sequence period**

To produce Figure 4-26, we simulated a modulator over 10000 points for different values of the input sequence period and for three values of the integrator leakage, namely Δp=0.001, 0.005 and 0.01. The solid line stands for the expected signature computed accordingly to Eq (4-26) for every case while the markers are the simulated signatures. The lock condition of Eq (4-76) is verified, as the signature is zero for sequences of period L less than 5. For sequences with L greater than 5, the signature is sensitive to leakage.

◆ **Variation with the leakage**

The variation of the signature as a function of the integrator leakage can be seen in Figure 4-27 and 4-28 for an input sequence of periods L=6 and L=11, respectively. The num-

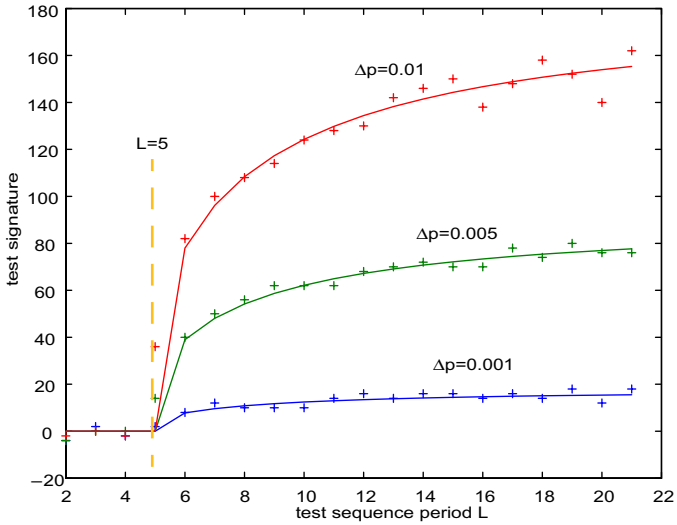


Figure 4-26: Test signature versus test sequence period L, for a 1st order single-bit modulator.

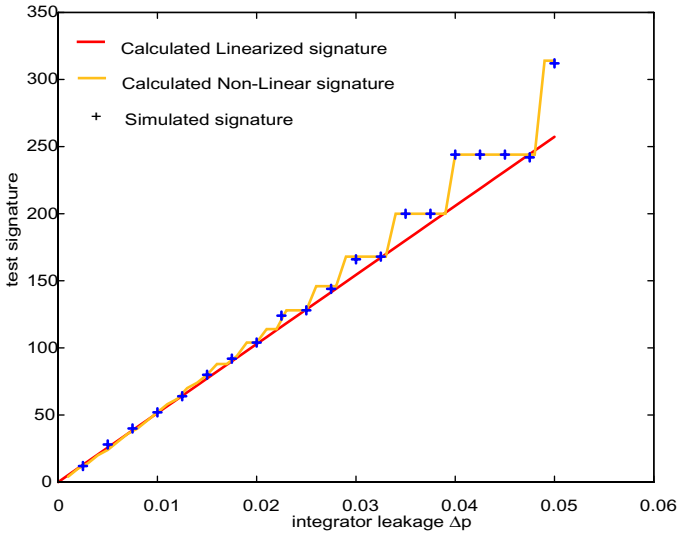


Figure 4-27: Test signature versus integrator leakage, for an input sequence of L=6

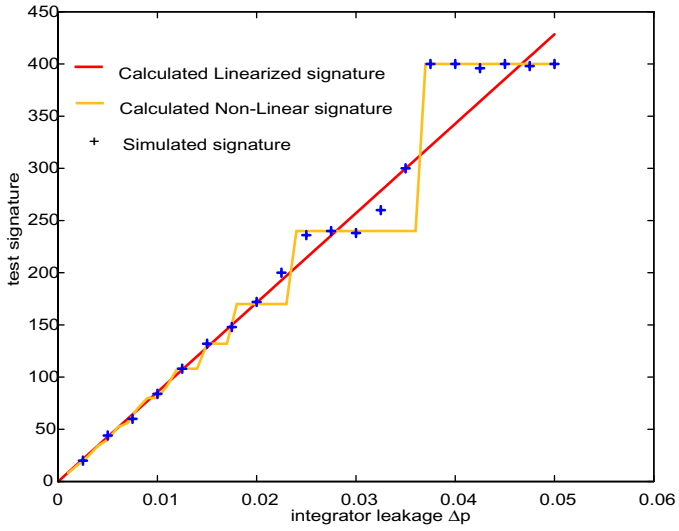


Figure 4-28: Test signature versus integrator leakage, for an input sequence of L=11

ber of acquired points was set to N=6600. The solid red curves represent the expected linear signature of Eq (4-26) while the orange curves represent the non-linear function predicted by Eq (4-81). It can be seen that the linear approximation leads to good results for small Δp (i.e. low leakages) and the matching is very good with the non-linear function. However, it seems likely that the evaluation error associated to the linear approximation dominate over the quantization noise.

◆ **Variation with the number of points**

In Figure 4-29, we represent the evolution of the signature as a function of the number of acquired points. For that we simulated a modulator with $\Delta p=10^{-3}$ with a $L=7$ input sequence. It is not necessary to repeat the acquisition for several number of points. Instead, we perform only one acquisition over a large number of points (100000) and vary the number of points for the signature computation by taking into account only the first N points of the 100000 acquired points.

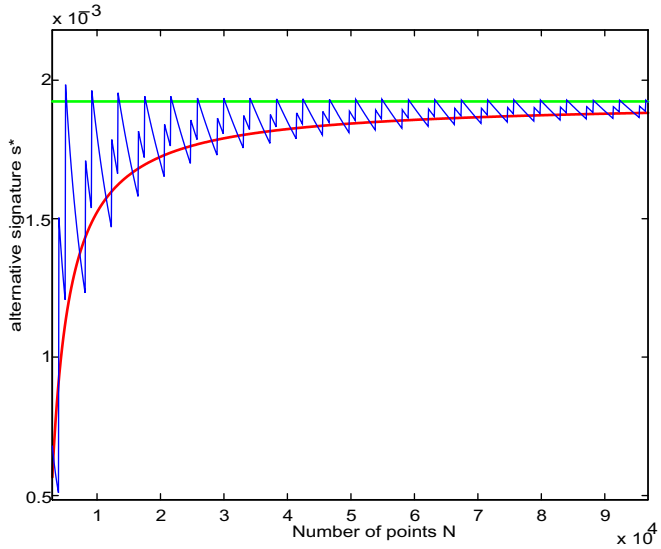


Figure 4-29: Evolution of the evaluation error with the number of samples.

We represent the mean value of the difference between the input and the output of the modulator instead of its sum. By doing so, the central result does not depends on the number of acquired points and the evaluation error is more readable. Actually, accordingly to Eq (4-89), the expected curve should follow,

$$s^* = \frac{4\Delta p}{\ln(8)} \pm \frac{4}{N} \qquad \textbf{(4-96)}$$

Figure 4-29 shows the evolution of the alternative signature defined above with the number of acquired samples. Notice that the signatures were computed for values of N multiple of 70, which are multiple of L=7 as required. Together with the simulation results, we represent the expected center value (in green) and the associated confidence interval (in red) of Eq (4-96). The measurement error corresponds the calculated bounds to a reasonable extent.

◆ Impact of the offset

It was explained in sub-section 4 • 1 . 3 . 3 that an input-referred offset can modify the expected signature. In order to compensate for such an offset, we proposed to use two opposite sequences and to subtract the two obtained signatures such as to eliminate the linear part of the offset contribution, just as in the case of a second-order modulator. However, the

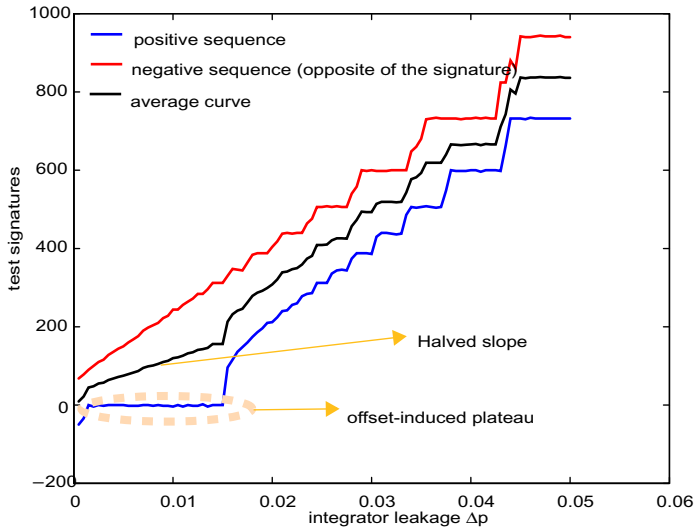


Figure 4-30: Test signature versus integrator leakage, for an input sequence of L=6 and its opposite, and an input-referred offset of 0.003.

impact of an input referred offset on the signature is not linear when leakage is present, as it modifies the lock condition (see Eq (4-75) and Eq (4-83)). This translates into the fact that the offset can compensate for the decay due to leakage such that the signature is no longer proportional to leakage but is equal to zero. This can be seen in Figure 4-30 which shows the same simulation as Figure 4-27 but with the introduction of an input-referred offset of 0.003. Moreover, a second acquisition was run with the opposite sequence, and the opposite of the obtained signature is also represented. It appears that a positive offset can compensate for the decay and provokes the unwanted “plateau” in the signature only for sequences with a positive mean value. Hence, when the signature is computed using Eq (4-27) (subtracting the result obtained for a positive sequence and its opposite) the plateau is converted in a region with a slope of half the expected value. This can be seen in Figure 4-30 as the black (average) curve represents this signature. Notice that the individual signatures obtained for the positive sequence and its opposite have been multiplied by two so that they can be represented on the same scale as the combined signature in Figure 4-30. As the offset is not known a-priori, it can be said that the test will exhibit a 50% relative error in the worst case

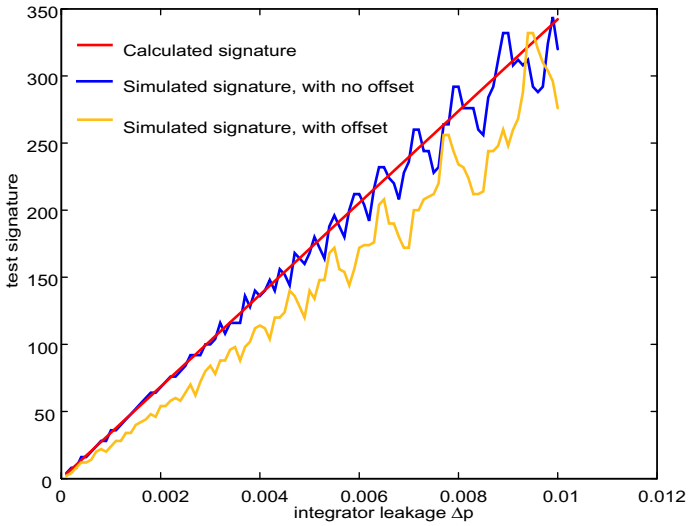


Figure 4-31: Second test signature versus integrator leakage, for input sequences of L=6 and L=11, with and without an input-referred offset of 0.003.

(i.e. the leakage is evaluated to one half of what it actually is). This can appear as a very limiting factor, but from a detection point of view it is not that critical. Indeed, it can lead one to underestimate the leakage by 50% which is equivalent to overestimating the amplifier DC gain by 6dB. It is unlikely that such a deviation in the DC gain would be critical for the performance of the modulator.

In order to circumvent the issue of the input-referred offset, a second signature was proposed in Eq (4-87). Figure 4-31 represents that signature, computed for input sequences of period L=6 and L=11, respectively, versus the integrator leakage. This figure has been limited to the region where the plateau could be seen. Each acquisition was performed over 66000 points in order to let the non-linearities dominate the evaluation error. Indeed, it can be seen that for the higher values of the pole error Δp, the signature exhibits a quite non-linear behaviour. This has to be related to the steps that could be seen in Figure 4-27 and 4-28, as this alternative signature is a combination of such curves for two different test sequences. Moreover, we can also see that the input-referred offset impact is not totally suppressed for that alternative. Despite the fact that globally, the linearity for this signature is better than for than for the previous one, the offset still manifests itself as a slope error with respect to the

expected signature. In that sense, the worst case relative precision on the determination of the pole error Δp can be estimated to be around 15% for the 0.003 offset in Figure 4-31.

4 • 2 . 4 Alternative test for the leakage of a 1st order single-bit modulator

Another test has been proposed for the integrator leakage of a 1st order single-bit modulator in Section 4 • 1 . 2 . 3. It is very similar to the previous one. Actually, it only differs in that the input sequence is of the form [1 1 1 .. 0] instead of [1 1 1 .. -1]. With this modification, we have shown that no extra-delay is required in the feedback loop. The same validation flow is thus followed.

- **Verification of the pattern**

The objective of these first simulations is to verify that the pattern depicted in Figure 4-12 and 4-13 are followed in simulations. For that, we simulated a first-order single-bit modulator for different values of leakage.

Figure 4-32 represents the evolution of the integrator output for a sequence of L=4 (i.e. [1 1 1 0]), with pole errors Δp=0, Δp=0.001 and Δp=0.005. It shows that the integrator output actually suffers a decay that leads to periodic transitions The decay is a function of the integrator leakage, such that more transitions occur for higher values of Δp. A zoom over the pattern period for the three cases shows that the leakage does not change the periodic pattern, which corresponds to Figure 4-12. Another zoom on the transitions shows that the pattern predicted in Figure 4-13 is also respected.

- **Variation with the input sequence period**

To produce Figure 4-33, we simulated a modulator over 10000 points for different values of the input sequence period and for three values of the integrator leakage, namely Δp=0.001, 0.005 and 0.01. The solid curve represents the expected signature computed according to Eq (4-28) for every case while the markers are the simulated signatures.

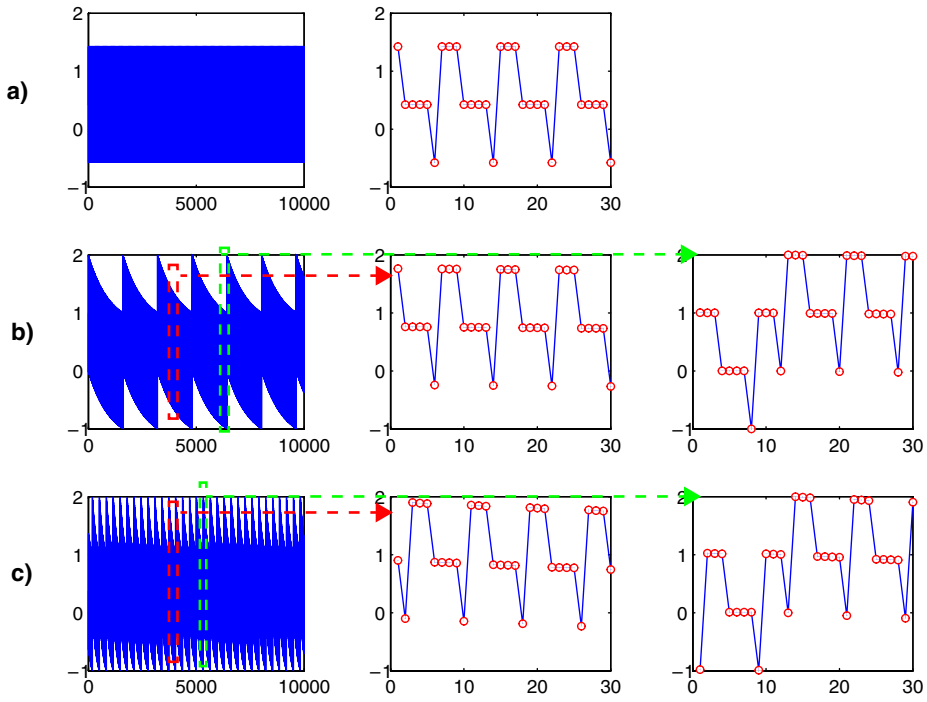


Figure 4-32: Integrator output, for a 1st order single-bit modulator.
a) leakage-free modulator: global view, zoom on the pattern
b) Δp=0.001: global view, zoom on the pattern, zoom on the transition
c) Δp=0.005: global view, zoom on the pattern, zoom on the transition

◆ **Variation with the leakage**

The variation of the signature as a function of the integrator leakage can be seen in Figure 4-34 and 4-35 for input sequences of periods L=4 and L=7 respectively. The number of acquired points was set to N=10000. The solid red curves represent the expected linear signature of Eq (4-28) while the orange curves represent the non-linear function predicted by Eq (4-91). Note that the linear approximation leads to good results for small Δp (i.e. low leakages) and the matching is very good with the non-linear function. The linear approximation is valid for small leakages because the steps of the non-linear function are smaller than the ± 4 error associated with the quantization noise. However, the evaluation error associated with the linear approximation dominate over the quantization noise for large values of

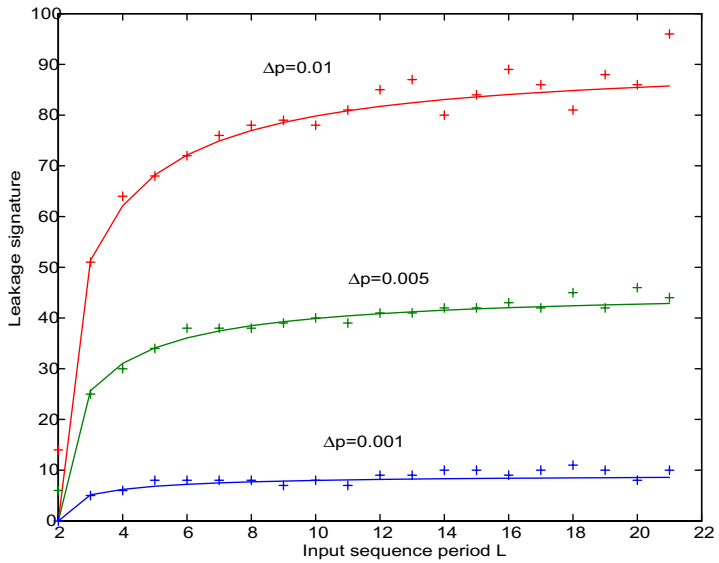


Figure 4-33: Alternative test signature versus test sequence period L, for a 1st order single-bit modulator.

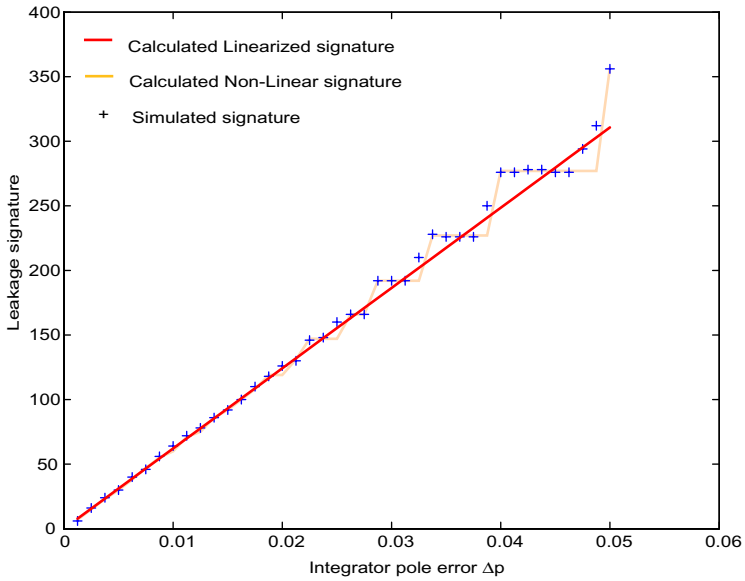


Figure 4-34: Test signature versus integrator leakage, for an input sequence of L=4

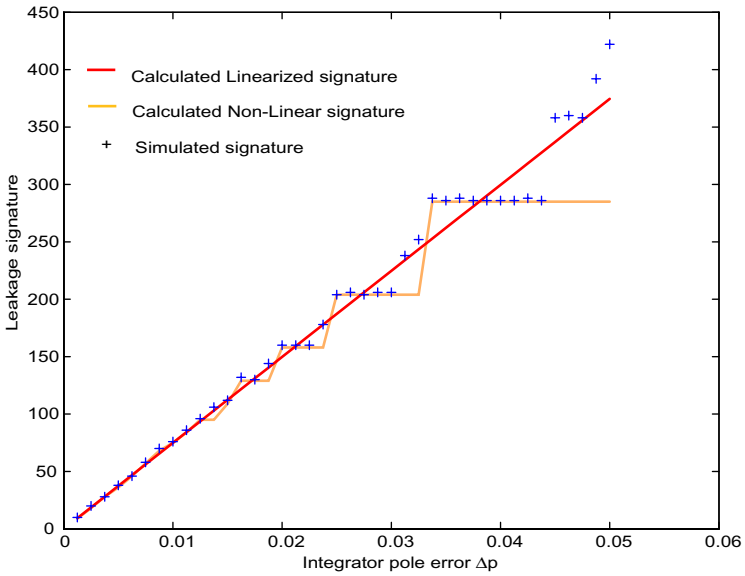


Figure 4-35: Alternative test signature versus integrator leakage, for an input sequence of L=7

leakage. The worst case error due to non-linearity is around 15%, which is equivalent to a 1.4dB error in the estimation of the amplifier's DC gain.

◆ Variation with the number of points

In Figure 4-36, the evolution of the signature as a function of the number of acquired points is represented. For that we simulated a modulator with $\Delta p=10^{-3}$ with a L=4 input sequence. It is not necessary to repeat the acquisition for several number of points. Instead, we perform only one acquisition over a large number of points (100000) and vary the number of points for the signature computation by taking into account only the first N points of the 100000 acquired points.

We represent the mean value of the difference between the input and the output of the modulator instead of its sum. By doing so, the central result does not depends on the number of acquired points and the evaluation error is more readable. Actually, accordingly to Eq (4-28), the expected curve should follow

$$s^* = \frac{2\Delta p}{\ln(5)} \pm \frac{2}{N}. \qquad \textbf{(4-97)}$$

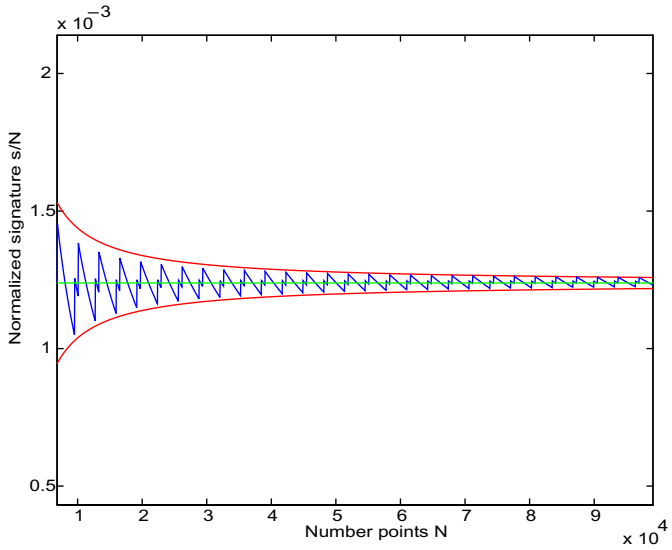


Figure 4-36: Evolution of the evaluation error with the number of samples.

Figure 4-36 shows the evolution of the alternative signature defined above with the number of acquired samples. Together with the simulation results, we represent the expected center value (in green) and the associated confidence interval (in red) of Eq (4-97). The measurement error corresponds with the calculated bounds.

◆ **Impact of the offset**

As the mechanism underlying the two proposed leakage tests is very similar, an input-referred offset also causes the same kind of non-linear phenomenon that has been described above. In order to illustrate this effect, a simulation was performed varying the integrator leakage for a 1st order modulator with an input-referred offset of 0.3% of the full-scale. The alternative test was performed with a [1 1 1 1 0] (L=5) sequence and its opposite ([-1 -1 -1 -1 0]) over N=10000 samples.

Figure 4-37 is constructed in the same manner as Figure 4-30 and the results are very similar. The input-referred offset can compensate for the leakage-related decay of the integrator output for one of the two sequences (the positive sequence for a positive offset). This corresponds to the “plateau” that appears on the blue curve of Figure 4-37: the signature is equal to zero over a range of pole errors.

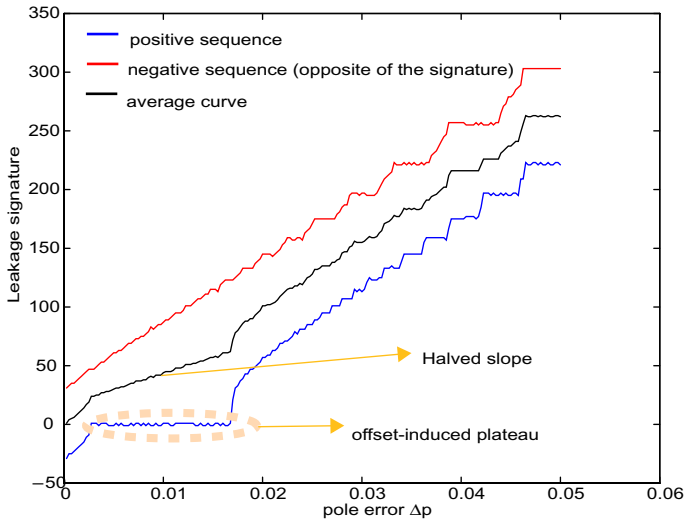


Figure 4-37: Signature versus integrator leakage for the alternative leakage test, in the presence of an offset.

4 • 3 AMPLIFIER NON-LINEAR DC GAIN

We said in a previous section that the amplifier finite DC gain generates a pole error in the integrator and modifies the Noise Transfer Function such that some quantization noise leaks into the modulator baseband. Though this is the main limitation related to the amplifier gain, it is not unique. Indeed, in real implementations, the DC gain of an amplifier is given as the value of the derivative of its DC transfer function for a half-scale input (a zero input in a differential implementation). Nevertheless, this small-signal value of DC gain is not constant over the whole output range. This is particularly true with newer processes, which tend to reduce the supply voltage and consequently the usable linear range.

One of the functions that can be used to represent the transfer function of an amplifier is the hyperbolic tangent. Indeed, such a function presents a linear shape close to zero but varies continuously up to the saturations levels. We could write y the relationship between the DC output of an amplifier and a DC input x as

$$y = sat \times \tanh\left(A_{DC0}\frac{x}{sat}\right), \tag{4-98}$$

where A_{DC0} is the specified DC gain for a zero input and *sat* is the saturation level of the amplifier.

The DC gain over the whole signal range can thus be written as

$$A_{DC}(x) = \frac{\partial y}{\partial x} = A_{DC0} \times \left(1 - \tanh\left(A_{DC}\frac{x}{sat}\right)^2\right). \tag{4-99}$$

Instead of expressing it as a function of the input voltage, whose range is very limited, it is usually expressed as a function of the amplifier output. We obtain the following relation

$$A_{DC}(y) = A_{DC0} \times \left(1 - \left(\frac{y}{sat}\right)^2\right). \tag{4-100}$$

It appears that parameter *sat* (the saturation level) drives the non-linearity of the amplifier DC gain.

In real implementations, the amplifier gain may not be accurately modelled by the hyperbolic tangent function, and the variation of the DC gain may be driven by more factors than just the saturation level. However, it is not possible to contemplate all the possibilities for gain variation. Hence, we decided to model DC gain non-linearity as

$$A_{DC}(y) = A_{DC0} \times \left(1 - \left(\frac{y}{a_{NL}}\right)^2\right). \tag{4-101}$$

where the parameter *sat* has been replaced by another coefficient, namely a_{NL}. This allows us to decorrelate the DC gain non-linearity from the effective saturation of the integrator. Notice that, for convergence issues in simulations, the integrator saturation *sat* should be strictly lower than the non-linear coefficient a_{NL}. Indeed, clipping the integrator output to $\pm sat$ ensures that the DC gain calculated using Eq (4-101) is always greater than zero.

4 • 3 . 1 Impact on the modulator performance

The major impact of amplifier non-linear DC gain occurs for the first integrator. Indeed, for others integrators in the modulator, the integrator output is normally quite decorrelated from the input signal. Hence, for these integrators, the impact of amplifier DC gain non-linearity can be seen as slight increase in the integrator pole error, due to the fact that the effective amplifier DC gain has to be considered instead of the DC gain for a zero output.

Nevertheless, such a modification will only increase quantization noise leakage slightly. Indeed, the effective gain will be mainly determined by the DC gain at a zero output in most cases. In other words, if the DC gain for a zero output of the amplifier is high, its non-linearity will not be noticeable.

On the other hand, the first integrator output is still strongly correlated with the input signal. As a consequence, the error associated with the amplifier gain at an instant n is correlated with the input signal value at an instant n. This produces distortion. In [38], a study of the distortion generated by a non-linear DC gain is reported. Assuming that a single-stage modulator of order L exhibits an ideal transfer function, we have

$$Y = z^{-L}X + (1 - z^{-1})^{-L}E. \tag{4-102}$$

The first integrator input can be written

$$I_1 = X - Y = (1 - z^{-L})X - (1 - z)^{-L}E, \tag{4-103}$$

and the first integrator output as

$$U_1 = \frac{bz^{-1}}{1 - z^{-1}}I_1 \tag{4-104}$$

Considering that the modulator input X is a sine-wave of amplitude A and a small frequency f_b with respect to the modulator sampling frequency f_s, we can consider the behaviour of the modulator when z tends to 1. Taking a first order Taylor series expansion of z^{-1} leads to more manageable expressions

$$z^{-1} = e^{-i2\pi\frac{f_b}{f_s}} \approx 1 - i2\pi\frac{f_b}{f_s} \tag{4-105}$$

Neglecting the quantization error, we obtain,

$$x(n) = A\cos\left(2\pi\frac{f_b}{f_s}n\right)$$

$$i_1(n) = 2\pi L\frac{f_b}{f_s}A\sin\left(2\pi\frac{f_b}{f_s}n\right) \quad \textbf{(4-106)}$$

$$u_1(n) = bLA\cos\left(2\pi\frac{f_b}{f_s}n\right)$$

These expressions show the low frequency content of the integrator input and output when a sine-wave is applied to the ideal modulator. These results can be used as the base to calculate the harmonic contents of the integrator referred to its input. Indeed, we can consider the gain non-linearity as a perturbation of the ideal results and thus use the expressions Eq (4-106) to determine the fundamental frequency components. Considering the integrator of Figure 4-1 as an example, the difference equation can be written

$$u(n) = \frac{Ab}{A+1+b}i(n) + \frac{A+1}{A+1+b}u(n-1)\,. \quad \textbf{(4-107)}$$

Assuming that the amplifier gain A is high, this reduces to

$$u(n) = b\left(1-\frac{1+b}{A}\right)i(n) + \left(1-\frac{b}{A}\right)u(n-1)\,. \quad \textbf{(4-108)}$$

Furthermore, taking into account that the non-linearity of the DC gain is small in Eq (4-101), we obtain,

$$u(n) = b\left(1-\frac{1+b}{A_{DC0}\left(1+\left(\frac{u(n)}{a_{NL}}\right)^2\right)}\right)i(n) + \left(1-\frac{b}{A_{DC0}\left(1+\left(\frac{u(n)}{a_{NL}}\right)^2\right)}\right)u(n-1) \quad \textbf{(4-109)}$$

For a slow sine-wave input, we can approximate *u(n-1)* to *u(n)* and calculate the harmonic content of the integrator output using Eq (4-106). The perturbed integrator output can thus be written

$$u(n) \approx bLA\cos\left(2\pi\frac{f_b}{f_s}n\right) \quad \textbf{(4-110)}$$
$$+\frac{b}{A_{DC0}}\times\left(\frac{bLA}{a_{NL}}\right)^2\frac{LA}{4}\left[2\pi(1+b)\frac{f_b}{f_s}\sin\left(6\pi\frac{f_b}{f_s}n\right)+b\cos\left(6\pi\frac{f_b}{f_s}n\right)\right]$$

It appears that a third order harmonic is created by the non-linear DC gain of the amplifier. When referred to the modulator input, the amplitude of this harmonic can be written as

$$\left\|A_3\right\| = \frac{bLA}{4A_{DC0}}\left(\frac{bLA}{a_{NL}}\right)^2, \quad \text{(4-111)}$$

whenever $2\pi f_b/f_s<<1$.

In the case of a 2nd order modulator like that proposed by Boser and Wooley in [26], which is widely used as a first stage in cascaded modulators and for which b=0.5, the third harmonic amplitude associated with a half-scale (A=0.5) input sine-wave reduces to

$$\left\|A_3\right\|_{dB} = -(A_{DC0})_{dB} - 20\log(32) - 40\log(a_{NL}). \quad \text{(4-112)}$$

4 • 3 . 2 Description of the proposed test

The test that we propose to check the linearity of the amplifier DC gain is valid for the first integrator of a second order ΣΔ modulators. Second order modulators are usually preferred as a first stage in cascaded modulators because of their lower leakage requirements. The non-linearity of the DC gain has a significant impact on the modulator performance only for the first integrator. Therefore, a test for DC gain non-linearity for first order modulator is not of much relevance in practice.

The proposed test is similar to what was done to test integrator leakage. Actually, it relies on performing two leakage tests with sequences with different mean value and checking if the two obtained signatures are proportional.

The test can thus be described as follows:

- Digital input sequences: apply two periodic sequences of mean value Q_1 and Q_2, different from 0.
- Modifications of the modulator operating conditions: the normal input is disabled and the digital input is enabled
- Signature elaboration: this is the relation between the sums over a number N of samples of the difference between the input sequence and the output bitstream for the two sequences.

$$s = \frac{\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_1}}{\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_2}} = \frac{2NQ_1\Delta p \times f(a_{NL}, Q_1)}{2NQ_2\Delta p \times f(a_{NL}, Q_2)} = \frac{Q_1}{Q_2} \times \frac{f(a_{NL}, Q_1)}{f(a_{NL}, Q_2)} \quad \textbf{(4-113)}$$

where Δp is the pole error of the first integrator, as defined in Eq (4-3)

Here again, an input referred offset can compromise the results and two more acquisitions can be performed with sequences of mean value -Q_1 and -Q_2. In this case we obtain

$$s = \frac{\left[\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_1} - \left(\sum_{i=1}^{N} x_i - y_i\right)_{-Q_1}\right]}{\left[\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_2} - \left(\sum_{i=1}^{N} x_i - y_i\right)_{-Q_2}\right]} \quad \textbf{(4-114)}$$

$$= \frac{4NQ_1\Delta p \times f(a_{NL}, Q_1) \pm 4}{4NQ_2\Delta p \times f(a_{NL}, Q_2) \pm 4} \approx \frac{Q_1}{Q_2} \times \frac{f(a_{NL}, Q_1)}{f(a_{NL}, Q_2)} \pm \frac{Q_1}{NQ_2\Delta p}\left(\frac{1}{Q_1} + \frac{1}{Q_2}\right)$$

It should be noticed that this test is redundant with the leakage test. Hence, we can consider that the leakage test already provides the results for the sequence of mean value Q_1 and only one other sequence has to be used.

The signature proposed above requires that we perform a division. This division does not have to be performed at modulator speed and could thus be carried out at a relatively low cost. However, if it is desirable to avoid this division, an alternative test signature can be used

$$s^* = \left[\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_1} - \left(\sum_{i=1}^{N} x_i - y_i\right)_{-Q_1}\right] - \frac{Q_1}{Q_2}\left[\left(\sum_{i=1}^{N} x_i - y_i\right)_{Q_2} - \left(\sum_{i=1}^{N} x_i - y_i\right)_{-Q_2}\right] \quad \textbf{(4-115)}$$

$$= 4NQ_1\Delta p[f(a_{NL}, Q_1) - f(a_{NL}, Q_2)] \pm 6\left(1 + \frac{Q_1}{Q_2}\right)\sqrt{\frac{2}{3}}$$

However, this alternative signature is proportional to both the nominal DC gain (through the term Δp) and its non-linearity (through the difference between the terms $f(a_{NL},Q_i)$).

Hence, if there is a non linearity, its magnitude may not be correctly estimated if the nominal DC gain is not determined a-priori with sufficient precision. This means that, in order to evaluate DC gain non-linearity, the real (measured) integrator leakage has to be taken into account in Eq (4-115) and not only the expected one. On the other hand, this is congruent with the functional impact of the DC gain non-linearity: the magnitude of the distortion induced by a given DC gain non-linearity (a_{NL}) greatly depends on the nominal DC gain, according to Eq (4-112).

The multiplication by the coefficient Q_1/Q_2 in Eq (4-115) can be handled very simply if: i) the sequences are chosen such that Q_1/Q_2 is a power of two, ii) the acquisitions for sequence Q_2 and Q_1 are performed over different numbers of points such that,

$$\frac{N_2}{N_1} = \frac{Q_2}{Q_1} \tag{4-116}$$

With this modification, the multiplication becomes unnecessary.

4 • 3 . 3 Theoretical justification

Equation (4-20) shows that the signature for a leakage test is proportional to the mean value of the input sequence. Nevertheless, we will see that the integrator output mean value is proportional to the input sequence mean value. As a consequence, the effective DC gain of the amplifier is a function of the input sequence mean value. This means that the effective integrator leakage depends on the input sequence mean value

$$\Delta p = \Delta p(Q)\,. \tag{4-117}$$

Let us consider the first integrator in a modulator of order L. This integrator has a gain b and its associated amplifier DC gain is defined by Eq (4-101). Let U be the integrator output.

The error that is produced at the output of the integrator due to the finite (non-linear) gain of the amplifier can be written as

$$er_{out}(u) \approx \frac{bu}{A_{DC}(u)} = \frac{bu}{A_{DC0}\left(1-\left(\frac{u}{a_{NL}}\right)^2\right)}\,. \tag{4-118}$$

The average of the error due to integrator leakage referred to the modulator input, can be written as

$$er_{NL_Q} = \frac{1}{A_{DC0}} \int_{-\infty}^{\infty} \left(\frac{u \times pdf(u)}{1 - \left(\frac{u}{a_{NL}}\right)^2} \right) du \,, \tag{4-119}$$

where *pdf(u)* is the probability density function of the integrator output.

We have seen above that for low frequency input signals and neglecting the quantization error, we can write

$$U = bLX \,. \tag{4-120}$$

We can assume that for a digital input sequence, this relation still holds true for the low-frequency part of the signal. Hence, we have

$$\overline{U} = bL\overline{X} = bLQ \tag{4-121}$$

which defines the relation between the integrator output average and the input sequence mean value. This shows the consistency with the results found for the integrator leakage in the previous section. Indeed, if there is no non-linearity (a_{NL} is infinite), the average input referred error reduces to,

$$er_{NL_Q} = \frac{1}{A_{DC0}} \int_{-\infty}^{\infty} (u \times pdf(u)) du = \frac{\overline{U}}{A_{DC0}} = \frac{bLQ}{A_{DC0}} \,. \tag{4-122}$$

For a second order modulator with b=0.5, and for the definition of the pole error in Eq (4-3), we obtain

$$er_{NL_Q} = 2Q\Delta p \,. \tag{4-123}$$

This average error is equal to the average of the difference between the modulator input and its output.

On the other hand, in the case that non-linearity is present, this input referred error cannot be calculated without a knowledge of the probability density function of the integrator output (*pdf(u)*). Even if such a function were known, the integral in Eq (4-119) may not be calculated explicitly. Hence, it is not straightforward to evaluate the value of a_{NL}, and we recommend designing the test (i.e. to choose the required number of samples to be acquired) according to high-level simulation results.

In order to simplify the problem, an equivalent DC gain could be used to evaluate the expected signature. For instance, we can consider that the modulator behaves as if its DC gain were constant and equal to its actual value for the mean of the integrator output, that is,

$$A_{DCeq} = A_{DC}(\overline{U}) = A_{DC0}\left(1 - \frac{\overline{U}^2}{a_{NL}^2}\right). \quad \textbf{(4-124)}$$

In that case, we would have

$$er_{NL_Q} = \frac{1}{A_{DCeq}} \int_{-\infty}^{\infty} (u \times pdf(u))du = \frac{\overline{U}}{A_{DCeq}} = \frac{bLQ}{A_{DC0}\left(1 - \frac{(bLQ)^2}{a_{NL}^2}\right)}, \quad \textbf{(4-125)}$$

and the test signature would reduce to

$$s = \frac{er_{NL_{Q2}}}{er_{NL_{Q1}}} = \frac{Q_2}{Q_1} \times \frac{a_{NL}^2 - (bLQ_1)^2}{a_{NL}^2 - (bLQ_2)^2}. \quad \textbf{(4-126)}$$

Nevertheless, simulations show that this approximation clearly underestimates the impact of the non-linearity on the signature. This is easily understood by taking a closer look at Eq (4-119). Let us consider that *pdf(u)* is symmetrical around its mean value. The effective gain cannot be chosen as the gain value at the mean integrator output because the part of the *pdf* above the mean value is weighted by an error more important than the part of the *pdf* below the mean value. Hence, the worst-case effective gain could be chosen as the gain value for an integrator output above its mean value

$$A_{DCeq} = A_{DC0}\left(1 - \frac{(|\overline{U}| + \delta)^2}{a_{NL}^2}\right) \quad \textbf{(4-127)}$$

Simulations show that a value of δ of 0.6 gives quite good matching.

4 • 4 VALIDATION OF NON-LINEAR DC GAIN TEST THROUGH SIMULATIONS

In order to illustrate the influence of non-linear amplifier DC gain on the ΣΔ modulator behaviour, we realized a first simulation similar to that of Figure 4-14. A 2nd order ΣΔ mod-

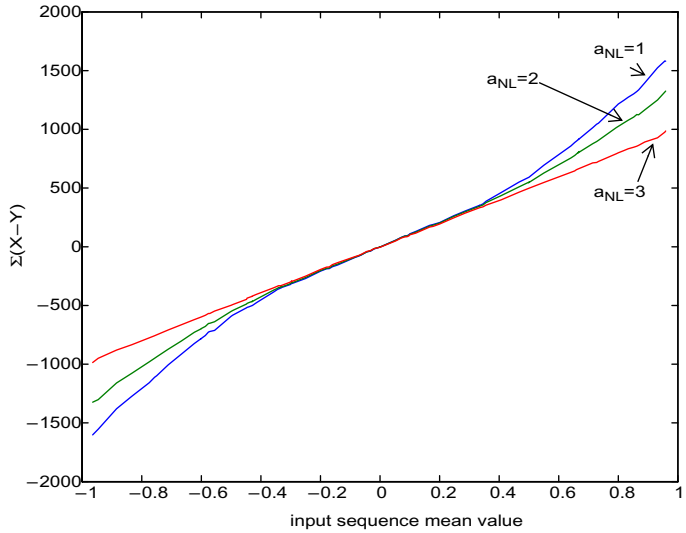


Figure 4-38: Sum of difference between the modulator output and the input sequence, for 3 values of the DC gain non-linear parameter a_{NL}

ulator was simulated over N=10000 points each for 100 different input sequences whose mean value cover the modulator full-scale [-1;1]. These 100 simulations were carried out for 3 values (1,2,3) of the parameter a_{NL} that define the non-linear amplifier DC gain. Figure 4-38 represents the sum over the 10000 simulated points of the difference between the modulator output bit-stream and the input sequence, against the input sequence mean value.

It appears that, for a high value of a_{NL}, the modulator behaves as if the DC gain were linear and the difference between the output bit-stream and the input sequence average is a straight line related to the integrator leakage, as in Figure 4-14. Lower values of a_{NL} correspond to more non-linear DC gains and are seen to blend the straight line for higher values of input sequence mean values. This behaviour is as expected as higher input sequence mean values cause higher average integrator output mean value and thus lower effective amplifier DC gain.

The test signature in Eq (4-114) was designed to be independent of the value of the amplifier nominal DC gain. To validate this signature, the previous simulation is not suffi-

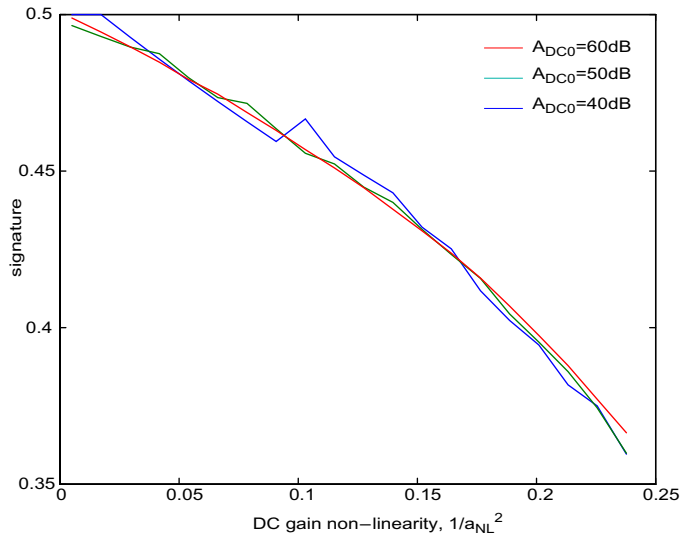


Figure 4-39: Proposed test signature as function of the DC gain non-linear parameter a_{NL} for 3 values of the nominal DC gain.

cient. Instead, the test as described in section 4 • 3 . 2 has to be carried out. That is what was done to elaborate Figure 4-39. Four input sequences were considered with mean values Q_1=1/3 and Q_2=2/3 and their opposite, respectively. For each input sequence, 200000 points were acquired and finally the signature was computed as specified in Eq (4-114). The swept parameter is a_{NL} which defines the non-linearity of the amplifier non-linear DC gain. Furthermore, the simulations were carried out for 3 values of the nominal DC gain 40dB, 50dB and 60dB.

The three curves obtained are superposed, so the first obvious result is that the signature is independent of the nominal DC gain, as expected. The only difference resides in the fact that the same number of points have been acquired for the three cases so the signature is more noisy for the higher values of the nominal DC gain. This is easily understood referring to section 4 • 1 . 3 . 1. For higher nominal DC gain, the sum of the difference between the input sequence and the modulator output is lower than for lower ones, but is still affected by the same quantization error range. Hence, the relative precision is lower. One way to avoid that undesirable effect is to perform the acquisition of a higher number of points for higher values of the nominal DC gain.

a)

b)

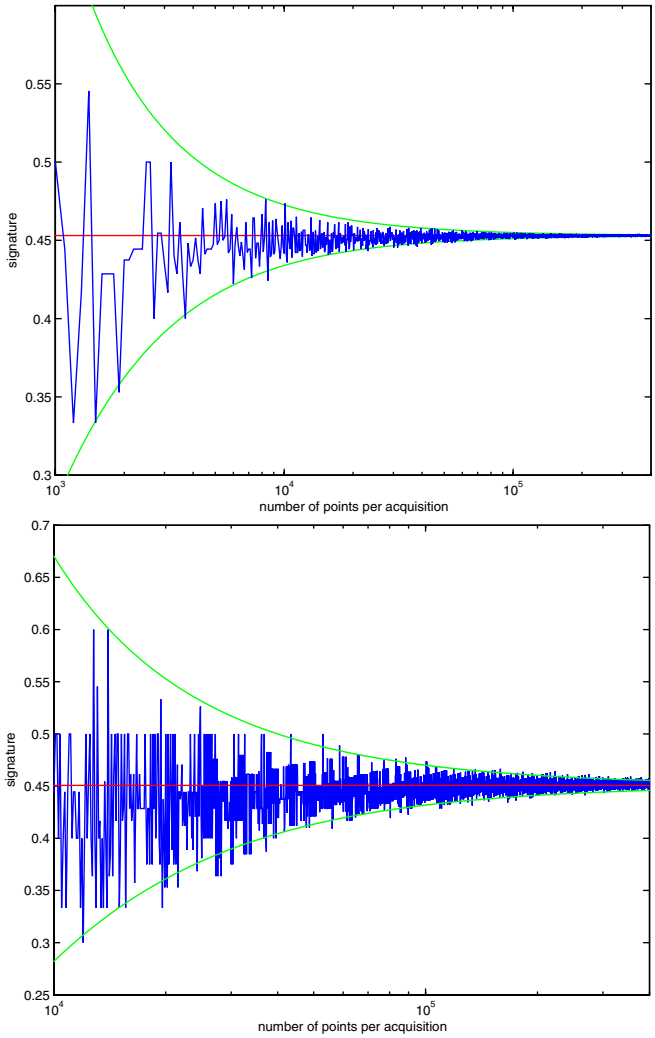


Figure 4-40: Proposed test signature as a function of the number of acquired points.
a) for a nominal DC gain of 40dB
b) for a nominal DC gain of 60dB

Finally, the precision of the signature as a function of the number of samples is depicted in Figure 4-40. Two simulations were realized over 400000 points for a modulator with $a_{NL}=3$ and a nominal DC gain of 40dB and 60dB respectively, using the same input sequences as above. Then, the signature was calculated for a subset of the output samples. Figure 4-40 represents the signature as a function of the length of the subset. It is clearly

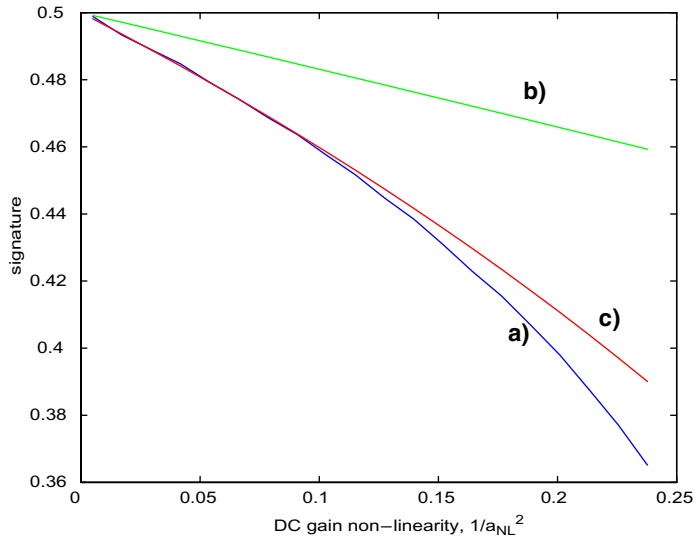


Figure 4-41: Proposed test signature as function of the DC gain non-linear parameter a_{NL}
a) acquired signature
b) calculated signature with (4-126)
c) calculated signature with (4-127) and δ=0.6.

seen that the precision of the signature improves with the number of points and follows the trend that could be expected considering the influence of quantization error in Eq (4-114). That expected trend is represented in Figure 4-40 by the two green curves.

Figure 4-41 represents the signature obtained for the lowest gain of Figure 4-39, and superposes the analytical closed forms proposed in the previous sub-section. It appears that calculating the signature using an equivalent gain at the mean integrator output (i.e. using (4-126)) clearly underestimates the impact of DC gain non-linearity on the proposed signature. Conversely, the modification proposed in (4-127) leads to more accurate results. Nevertheless, the signature deviation is also underestimated for important non-linearities (i.e. for small a_{NL}).

5

TEST FOR INTEGRATOR DYNAMICS

In this chapter, several tests for the dynamic behaviour of the integrators in a ΣΔ modulator will be described. Actually, the tests proposed in this chapter aim at the determination of the settling error, considering its linear and non-linear part. We use only two behavioural parameters (the Slew-Rate and GBW) to model the integrator at a high level. However these two parameters may not be sufficient to take into account the complexity of the integrator dynamics, including when it is defective. The settling error, on the other hand, is a concept that is independent of modelling and is thus better suited as a target for the proposed tests than the explicit behavioural parameters.

The guidelines given in Chapter 3 have been followed in most of the cases, but the exceptions will be specified. In each case, the test description is sustained by a theoretical justification and followed by a validation process through simulation.

At the end of the chapter the reader will find a summary of all the tests proposed in this chapter and in the previous one, followed by a discussion of the overall test set based upon

the simulation of the complete behavioural model of a 2-1 cascaded ΣΔ modulator. The aim of this simulation is to validate the approach and to show how the test set can detect the targeted parametric faults even when multiple faults are involved. Furthermore, it will show how the test pass/fail limits can be selected as a function of the test objectives.

5 • 1 DETERMINATION OF AMPLIFIER SETTLING ERRORS

Until now, we have considered only parameters related to static behaviour. Indeed, integrator leakage is related to the amplifier DC gain. This DC gain and its nonlinearity do not depends on the operating frequency. Nevertheless, ΣΔ modulators are inherently dynamic devices. Actually, their strength comes from the use of a high frequency of operation together with oversampling. Hence, it is legitimate to think that the dynamic properties of the building blocks will play an important role. In particular, the settling of the amplifiers used to build the integrators may be affected by defects in the circuit.

A commonly used approximation to study the behaviour of a modulator with non-ideal settling is the one-pole approximation together with a maximum output current limitation for the amplifier. In that case, the settling of the amplifier is determined by two parameters: its Gain-Bandwidth product and its Slew-Rate, labelled GBW and SR in the following. As was said in Chapter 3, these parameters are normalized to a sampling frequency of 1. In order to interpret the results in a real-world case, we must consider,

$$\begin{aligned} SR^* &= SR \times f_s \\ GBW^* &= GBW \times f_s \end{aligned} \qquad f_s = \frac{1}{T_s} \tag{5-1}$$

where SR^* and GBW^* are the real world Slew-Rate and Gain-BandWidth product, and f_s *is* the real sampling frequency. Parameters SR and GBW are the normalized (nondimensional) Slew-Rate and Gain-BandWidth product.

Let us take a look at the SC integrator in Figure 5-1

Let V_i be the voltage stored on capacitor C_1 at time 0, and V_o the integrator output at the end of the integrating phase, i.e. at time $T_s/2$. Three regions of operation can be considered:

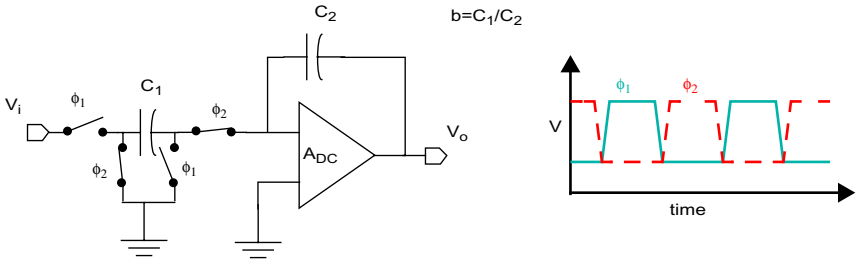


Figure 5-1: Switched-capacitor integrator scheme

- In the first region, the input voltage is sufficiently small such that the amplifier does not slew. The settling is determined only by the *GBW* and is exponential shaped. This can be written as

$$t_0 = \frac{b|V_i|}{SR} - \frac{1}{2\pi GBW} < 0$$
$$V_o = V_{o,n-1} + bV_i(1 - e^{-\pi GBW}) \quad \text{(5-2)}$$

  The first part of the equation sets the limits of the considered region and the second part makes explicit the integrator output. It is easily seen that the settling error is proportional to the input voltage.

- In the second region, the input voltage is so high that the amplifier slews over the whole integrating phase.

$$t_0 = \frac{b|V_i|}{SR} - \frac{1}{2\pi GBW} > \frac{1}{2}$$
$$V_o = V_{o,n-1} + SR \times \frac{1}{2} \times sign(V_i) \quad \text{(5-3)}$$

  Such a settling error is clearly non-linear, as the integrator output does not depend on the exact value of the input voltage.

- The last region is the intermediate zone between the previously described ones. The amplifier begins to slew but manages to return to the exponential settling at some point.

$$\frac{1}{2} > \left(t_0 = \frac{b|V_i|}{SR} - \frac{1}{2\pi GBW} \right) > 0$$
$$V_o = V_{o,n-1} + SRsign(V_i) \times t_0 + \ldots$$
$$\ldots + (bV_i - SRsign(V_i) \times t_0) \left(1 - e^{-2\pi GBW \times \left(\frac{1}{2} - t_0 \right)} \right) \quad \text{(5-4)}$$

In that case, the settling error is also non-linear.

The previous three equations simplify the settling behaviour. For more realistic simulations, the amplifier finite DC gain and output impedance should be taken into account as well as parasitic and load capacitances. However this analysis gives sufficient insight to understand the impact of settling error on performance, as well as the operating principle of the proposed tests.

5 • 1 . 1 Impact on the modulator performance

As can be seen from Eq (5-2), (5-3) and (5-4), the settling errors affect the update of the integrator. In that sense, it can be considered as a modification of the integrator gain. If the amplifier never slews, Eq (5-2) is always valid and this gain modification is independent of the input. However, in most cases, the amplifier slews for some input samples and the gain modification becomes non-linear. Hence, in general, the settling error can be seen as the superposition of a linear part and a non-linear part. The first one causes a change in the noise shaping function, while the second is a source of distortion.

5 • 1 . 1 . 1 Linear settling error

It is difficult to derive the impact on performance of the linear part of the settling error because it depends mainly on the integrator architecture. Indeed, as we have said above, the linear part of the settling error can be considered as an error in the integrator gain. Hence, for a single-bit first-order modulator, it has absolutely no impact on performance. Indeed, a modification of the integrator gain with respect to the nominal value only scales the modulator output but does not change its sign. As the quantizer senses the sign of the integrator output, the modulator output bitstream remains unchanged. A second order modulator is not

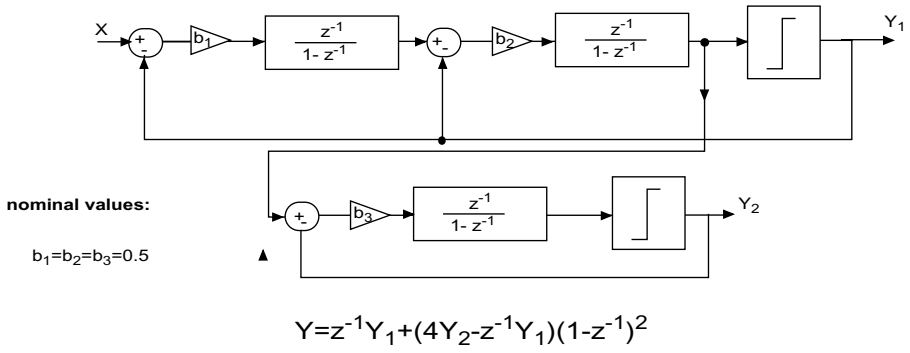


Figure 5-2: Diagram of a 2-1 cascade modulator

very sensitive to the first integrator gain either. Nevertheless, things change for cascaded modulators, that rely on the digital cancellation of all but the last stage quantization noise. Indeed, such a cancellation requires knowledge of the exact noise and signal transfer function of the different stages. A deviation from the nominal value would cause the noise cancellation unit to perform incorrectly and some noise shaped to an order lower than the overall modulator would leak into the baseband. In order to demonstrate this, we simulated a 2-1 cascade modulator as shown in Figure 5-2 and varied the first integrator gain (b_1) from 0.4 to 0.6. Notice that this would correspond to a 20% settling error which is very high. The input signal was a sine-wave with an amplitude of half the modulator full-scale.

Figure 5-3 shows the Signal to Noise and Distortion Ratio (SNRD) of the modulator for three value of the OSR: 32, 64 and 128. In each case, the modulator bitstream was filtered by a 4th order Chebytchev filter before decimation.

It can be seen that a variation of the integrator gain around its nominal value degrades the resulting SNRD, specially for a high OSR.

5 • 1 . 1 . 2 Non-linear settling error

The non-linear part of the settling error, however, causes more than an increase of the noise floor in the baseband of the modulator. Indeed, there is a strong correlation between the analog input value and the settling error. Nevertheless, it is not straightforward to refer

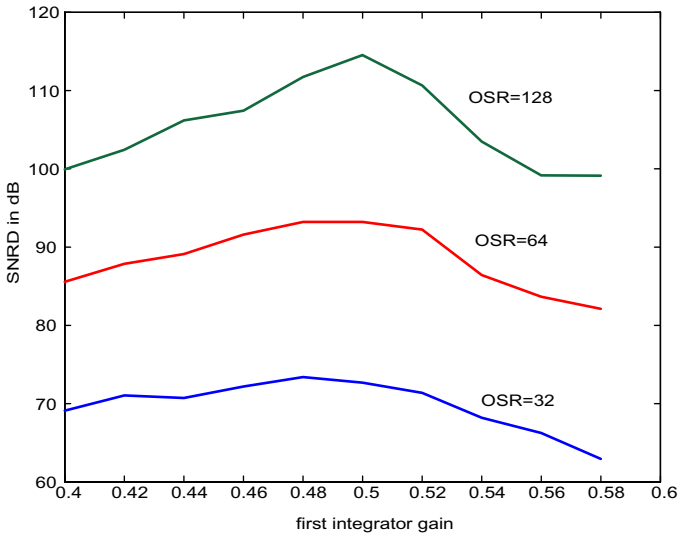


Figure 5-3: SNRD of a 2-1 cascaded modulator versus its first integrator gain

the settling error to the input of the modulator because the settling error applies to the integrator input, which is the difference between the modulator input and its output bitstream.

Nevertheless, a common approximation for the study of ΣΔ modulators is to consider that they use a high oversampling ratio and an anti-aliasing filter at its input, such that the input signal varies slowly with respect to the sampling frequency. In that sense, it is possible to reduce the study of ΣΔ modulators to DC input.

Let us suppose a DC input level *v*. Assuming that the modulator behaviour is close to ideal, the mean value of its output bitstream should be equal (or very close to) *v*. Hence, we can deduce the probability of occurrence of levels 1 and -1 in the output bitstream:

$$P_1 = \frac{1+v}{2}$$
$$P_{-1} = \frac{1-v}{2} \quad \text{(5-5)}$$

Hence, for a modulator input *v*, the integrator input oscillates between level *v+1* and *v-1*, with the probability of occurrence

$$P_{v-1} = \frac{1+v}{2}$$
$$P_{v+1} = \frac{1-v}{2} \quad \text{(5-6)}$$

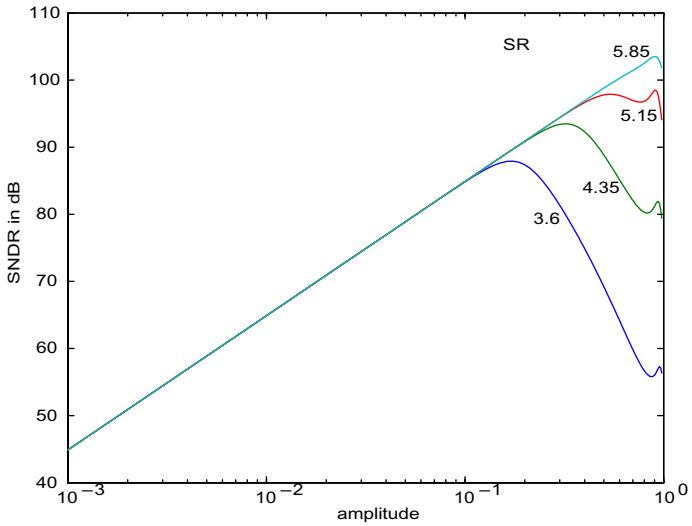


Figure 5-4: SNDR versus input sinewave amplitude, for different values of SR

The average settling error associated with level v and referred to the modulator input can thus be written

$$er_{input}(v) = \frac{1+v}{2} er_{v-1} + \frac{1-v}{2} er_{v+1} \quad \textbf{(5-7)}$$

The terms er_{v+1} and er_{v-1} are the settling errors associated with integrator input levels v+1 and v-1 respectively. These terms can be calculated analytically using Eq (5-2), (5-3) and (5-4).

Hence, we have obtained a DC approximation of the converter transfer function

$$f(v) = v + er_{input}(v) \quad \textbf{(5-8)}$$

This function can further be used to evaluate *a-priori* the expected distortion.

Figure 5-4 represents the evolution of the expected SNDR (Signal to Noise and Distortion Ratio) with the amplitude of the input sine-wave. It was built by distorting sine-waves of different amplitude using the transfer function of Eq (5-8) calculated for a GBW of 5 and four different values of the Slew-Rate (3.6, 4.35, 5.1, 5.85). Then random Gaussian noise (with σ=4.10^{-6}) was added to the distorted sine-wave so as to emulate the converter quantization noise and an FFT was realized in order to calculate the SNDR. This figure shows how the distortion reduces the SNRD for high input amplitudes. Moreover, the degradation is

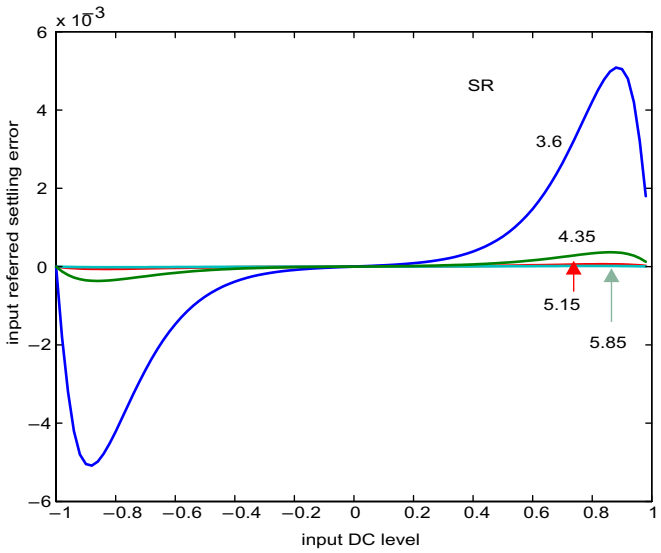


Figure 5-5: Input referred settling error versus DC input level (normalized to Full-Scale)

clearly seen to depend on the SR. As an illustration, Figure 5-5 represents the input referred settling error for the 4 simulated values of the SR and a GBW of 5.

In order to give a deeper insight into the impact of the settling error on modulator performance, we represent in Figure 5-6 the obtained SNRD over a grid of SR (from 4 to 7) and GBW (from 1 to 6) values, for four different amplitudes (0.9, 0.7, 0.5 and 0.1). Here again, a random Gaussian noise (with σ=4.10^{-6}) was added to the distorted sine-wave so as to emulate the converter quantization noise. It can be seen that the impact of the settling error on performance varies with the input amplitude. The acceptable SR/GBW region for an input amplitude of 0.5 is wider than the acceptable SR/GBW region for a 0.9 amplitude. Hence, the designer has to choose the SR and GBW values so as to optimize the performance/cost for a given amplitude. Indeed, $\Sigma\Delta$ modulators are often designed such that the maximum SNDR is achieved for amplitudes well below full-scale.

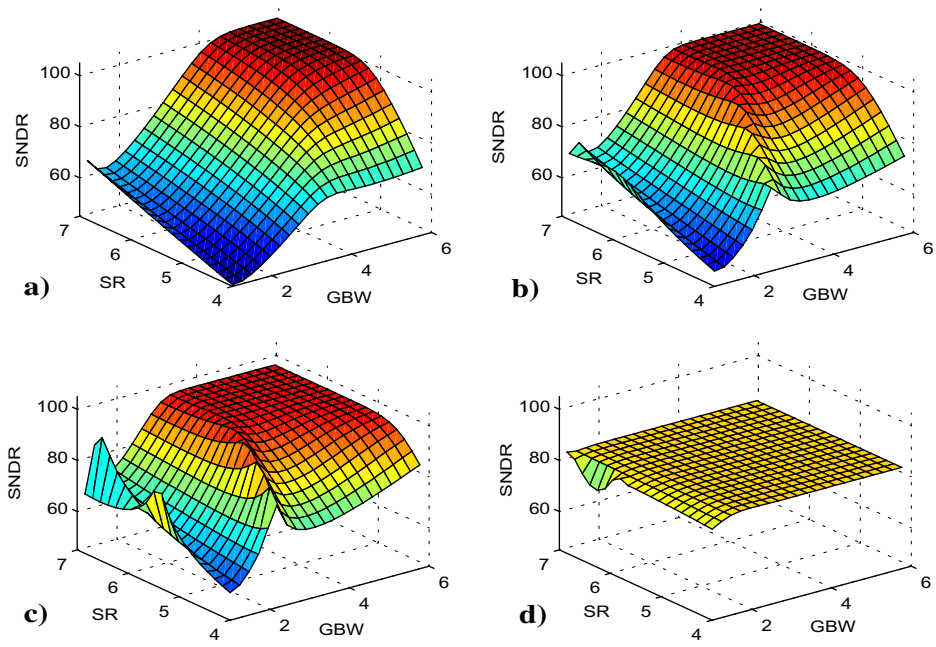


Figure 5-6: SNRD variation as a function of Slew-Rate and Gain-BandWidth product a) amplitude=0.9; b) amplitude=0.7; c) amplitude=0.5; d) amplitude=0.1

5 • 1 . 2 Description of the proposed test

5 • 1 . 2 . 1 Overall settling error

This test aims to determine the settling error of the first integrator of a ΣΔ modulator, for an integrator input level equal to 2. An input level equal to 2 is obtained when the input sample is equal to 1 and the feedback signal (i.e. the modulator output) is equal to -1. It is important to recall that this level 2 is normalized as explained in Chapter 3. Hence, in order to interpret it in the analog world, is should be multiplied by Vref. Moreover, this implicitly opens the door to another degree of freedom for the test: it can be realized for various reference voltage. In that case, the test allows one to determine the settling error associated with level 2, but that level 2 corresponds to different voltages in the real world implementation. Another degree of freedom for this test is the master clock frequency. By varying the frequency, it is possible to check the evolution of the settling error.

We can describe the test as follows:

- **Digital input sequence:** any digital periodic sequence. Its mean value can be chosen as 0, so as to avoid the influence of integrator leakage.
- **Modifications of the modulator operating conditions:** the normal input is disabled and the digital input is enabled. The clocking of the modulator is modified such that when the input sample is 1 (or conversely -1), the sampling and integrating phases last *k* times as long as when the input sample is -1 (or conversely 1). This is illustrated in Figure 5-7 for *k*=2.

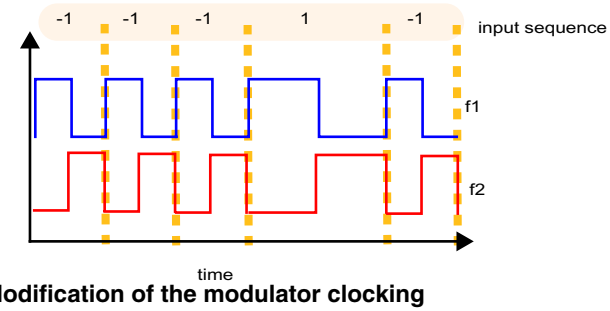


Figure 5-7: Modification of the modulator clocking

The implementation of such a feature will be detailed in the next chapter.

- **Signature elaboration:** it is based on the probability of occurrence of the levels 2 and -2 at the integrator input. Hence, the signature requires the acquisition of the number of occurrences of level 2 and level -2, for a test over *N* samples. An input level equal to 2 is obtained when the input sample is equal to 1 and the feedback signal (i.e. the modulator output) is equal to -1. And an input level equal to -2 is obtained when the input sample is equal to -1 and the feedback signal (i.e. the modulator output) is equal to 1. Let the number of occurrence of level 2 be

$$N_2 = \sum_{i=1}^{N} (x_i = 1) \bullet (y_i = -1), \qquad \textbf{(5-9)}$$

and the number of occurrence of level -2 be

$$N_{-2} = \sum_{i=1}^{N} (x_i = -1) \bullet (y_i = 1). \qquad \textbf{(5-10)}$$

The signature can be written as

$$er_2 = 2\frac{(N_2 - N_{-2})}{N_{-2}} \tag{5-11}$$

where er_2 is the settling error associated with level 2.

An input-referred offset could modify the signature output. To get rid of this, it is possible to run a second acquisition quoted with a star symbol (*) in order to differentiate it from the first acquisition. For that second acquisition, another sequence can be used (or not), but the required difference is on the clocking modification: for that second acquisition, the sampling and integrating phases instead last twice as long for a -1 input level as for a 1 input level. In that case, the signature can be written as

$$er_2 = 2\left[1 - \frac{\frac{N_2}{N} + \frac{N_{-2}^*}{N^*}}{\frac{N_{-2}}{N} + \frac{N_2^*}{N^*}}\right]. \tag{5-12}$$

In the case that the two acquisitions are made over the same number of points, an obvious simplification comes from N=N*, as N and N* disappear from the equation.

$$er_2 = 2\left[1 - \frac{N_2 + N_{-2}^*}{N_{-2} + N_2^*}\right] = \frac{\sum_{i=1}^{N}(y^*_i - x^*_i) - \sum_{i=1}^{N}(y_i - x_i) \pm 4}{N_{-2} + N^*_2}. \tag{5-13}$$

5 • 1 . 2 . 2 Non-linear settling error

With this test, we aim at determining the non-linear part of the settling error, which has been shown to be a source of non-linearity. For that we propose a test to evaluate the quantity

$$er_{NL} = er_2 - 2er_1, \tag{5-14}$$

which is the difference between the settling error associated with a level 2 at the first integrator input and two times the settling error associated with a level 1.

According to what was said in Sub-section 1.1, we can describe the test as follows:

- **Input sequence:** The test sequence has to use only 1 (conversely -1) and 0 levels. For instance, it could be [1 1 0 1 0 0 1] or [0 -1 -1 0 -1]. Hence, it requires a modification of the DAC during the test so as to manage three levels (1, 0 and -1).
- **Modifications of the modulator operating conditions:** the normal input is disabled and the digital input is enabled.
- **Signature elaboration:** it is based on the probability of occurrence of the levels 2 (conversely -2) at the integrator input. Hence, the signature requires the acquisition of the number of occurrences of level 2 and level -2, for a test over N samples. An input level equal to 2 is obtained when the input sample is equal to 1 and the feedback signal (i.e. the modulator output) is equal to -1. And an input level equal to -2 is obtained when the input sample is equal to -1 and the feedback signal (i.e. the modulator output) is equal to 1. The non-linear part of the settling error can be measured as

$$er_{NL} = \frac{\sum_{i=1}^{N} (y_i - x_i)}{N_2}. \quad \text{(5-15)}$$

An input-referred offset could modify the proposed signature. However, its contribution can be removed by running a second acquisition (labelled with a *) using the opposite input sequence. For instance, if a [1 0] sequence is used for the first acquisition, a [-1 0] has to be used for the second acquisition. In that case, we have

$$er_{NL} = \frac{\sum_{i=1}^{N} (y_i - x_i) - \sum_{i=1}^{N} (y^*_i - x^*_i) \pm 4}{N_2 + N^*_{-2}}. \quad \text{(5-16)}$$

5 • 1 . 3 Theoretical justification

5 • 1 . 3 . 1 Overall settling error

The theoretical justification of the proposed test relies on the fact that the settling error is a function of the integrator input. Hence, it is possible to consider the average of the settling errors as a DC perturbation on the modulator input. We thus have to consider the integrator

input node. Since a digital sequence is used as atest stimulus and the feedback signal is the modulator output bit-stream, the integrator input sees only three levels, associated with three settling errors.

$$\begin{array}{cc} 2 & er_2 \\ 0 & er_0 \approx 0 \\ -2 & er_{-2} \approx -er_2 \end{array} \quad \textbf{(5-17)}$$

Level 2 occurs when the test sequence input sample (x_i) is a 1 and the feedback sample (i.e. the modulator output y_i) is a -1. Level 0 occurs when the input sample and output sample are equal. Level -2 occurs when the test sequence input sample (x_i) is a -1 and the feedback sample (y_i) is a 1.

The error associated with level 0 is 0 because the integrator output does not change, and the error due to -2 is assumed to be the opposite of the error associated with 2 due to the symmetry of the fully differential implementations.

The mean value of the integrator input is, by definition,

$$\bar{I} = \int_{-\infty}^{\infty} i \times pdf(i)di, \quad \textbf{(5-18)}$$

where *pdf(i)* is the probability density function of the integrator input and *i* the integrator input.

The three levels at the integrator input (2, 0 and -2) can be associated with probabilities of occurrence (P_2, P_0 and P_{-2} respectively). The probability density function *pdf(i)* reduces to a distribution of the form

$$pdf(i) = P_2\delta(i-2) + P_0\delta(i) + P_{-2}\delta(i+2), \quad \textbf{(5-19)}$$

where δ is the Dirac distribution.

So the average of the integrator input simplifies to

$$\bar{I} = 2 \times P_2 + 0 \times P_0 + (-2) \times P_{-2} = 2 \times (P_2 - P_{-2}). \quad \textbf{(5-20)}$$

If an input-referred offset and settling error are present, the actual input levels are slightly modified and the integrator input average becomes

$$\bar{I} = (2 + er_2)P_2 + (0 + er_0)P_0 + (-2 + er_{-2})P_{-2} + off, \quad \textbf{(5-21)}$$

where *off* is an input-referred offset.

The feedback loop of a ΣΔ modulator tends to force the integrator input towards zero. Hence, using Eq (5-17) and Eq (5-21), we can write

$$\bar{I} = (2 + er_2)(P_2 - P_{-2}) + off = 0 . \quad \textbf{(5-22)}$$

Assuming a small offset, this can be automatically fulfilled for any input sequence by taking *P(2)=P(-2)*. In other words, the settling errors do not modify the DC behaviour of the modulator under test. This is due to the fact that the errors for 2 and -2 are opposite. Hence, if the probability of occurrence of levels 2 and -2 are equal, the average errors cancel each other. In order to retrieve sensitivity from these errors, the error symmetry (i.e. *er(2)=-er(-2)*) has to be broken.

To do so, we propose to modify the clocking control such that the sampling duration is set by the input level. If the input sample is 1, the sample is processed in *k* master clock periods instead of 1 clock period. Therefore, the settling error associated with level 2 is greatly reduced and can be approximated to 0 as the integrator has much more time to settle properly. Thus, Eq (5-21) becomes

$$\bar{I} = 2(P_2 - P_{-2}) + P_{-2}er_{-2} + off = 0 . \quad \textbf{(5-23)}$$

By definition, the first term in Eq (5-23) corresponds to the input sequence mean value minus the output bitstream mean value:

$$2(P_2 - P_{-2}) = \overline{X} - \overline{Y} . \quad \textbf{(5-24)}$$

Conversely, we can choose to use *k* periods for level -2 instead of for level 2. This case will be denoted by "*". For the same input sequence we obtain,

$$\overline{I^*} = 2(P^*_2 - P^*_{-2}) + P^*_2 er^*_2 + off = 0 \quad , \quad \textbf{(5-25)}$$

with

$$2(P^*_2 - P^*_{-2}) = \overline{X} - \overline{Y}^* . \quad \textbf{(5-26)}$$

By combining Eq (5-23) to Eq (5-26) and taking into account that er^*_2=$-er_{-2}$, the offset contribution can be removed. Hence, the settling error can be written as

$$er^*_2 \approx \frac{\overline{(Y^* - X^*)} - \overline{(Y - X)}}{P_{-2} + P^*_2} = 2\left[1 - \frac{P_2 + P^*_{-2}}{P_{-2} + P^*_2}\right]. \quad \textbf{(5-27)}$$

For a sum over *N* or *N** samples, let N_x or N_x* be the number of occurrence of *x*, it follows that

$$\begin{aligned} P_x &= \frac{N_x}{N} \\ P^*_x &= \frac{N_x^*}{N^*} \end{aligned} \quad . \tag{5-28}$$

The error on the measurement performed through Eq (5-27) is determined mainly by the numerical error in the numerator and the value of the denominator. Let us consider that the counts N_x and N_x* are realized with ± 1 precision. The real settling error can thus be written as

$$error_{\text{real}2} = er_2 \pm \frac{4}{N_{-2} + N_2^*} . \tag{5-29}$$

Hence, we can see that a key parameter concerning the measurement precision is *(N_{-2}+N_2*)*. Unlike for the evaluation of integrator leakage, it is difficult to relate the precision to the number of acquired points *N*. Indeed, it seems obvious that for a given sequence, the term (N_{-2}+N_2*) is proportional to *N*, but its exact value depends on the input sequence and on the modulator output. Hence, it is likely to vary with the input-referred offset and the settling error. Nevertheless, it would be interesting to evaluate *a-priori* (N_{-2}+N_2*) for two reasons. The first one, as explained above, is that it would allow one to estimate the number of points (*N*) required to reach a given precision. And the second reason, which puts stronger requirements on the precision of the evaluation of (N_{-2}+N_2*), is that it allows one to compute an alternative signature that does not require any division. Let N_e be the *a-priori* estimator of (N_{-2}+N_2*). Then we would have

$$s \approx \left(\sum_{i=1}^{N} (x_i - y_i) - \sum_{i=1}^{N} (x_i^* - y_i^*) \right) \approx N_e \times er_2 . \tag{5-30}$$

Notice that this alternative signature is less precise than the signature in Eq (5-27), because it is based on the approximation of the term (N_{-2}+N_2*) by N_e. This will contribute as a relative error on the evaluated settling error

$$\frac{\Delta er_2}{er_2} = \frac{\Delta s}{s} + \frac{N_{-2} + N_2^*}{N_e} . \tag{5-31}$$

In the case of first-order single-bit modulators, it can be calculated in the nominal case: without offset and with no settling error. Indeed, we have verified in Chapter 4 that the modulator output follows the input when the latter is a digital sequence. We have, using Eq (5-2),

$$y_{n+1} = x_n . \tag{5-32}$$

Hence, using Eq (5-9), we have

$$\begin{aligned} N_{-2} &= \sum_{i=1}^{N} (x_i = -1) \bullet (x_{i-1} = 1) \\ N_2{}^* &= \sum_{i=1}^{N} (x_i{}^* = 1) \bullet (x_{i-1}{}^* = -1) \end{aligned} . \tag{5-33}$$

So the expected values of N_2 and $N_{-2}*$ are proportional to the number of transitions from -1 to 1 in the input sequence. For a periodic sequence, the number of transitions from -1 to 1 is equal to the number of transitions from 1 to -1. The number of transitions for a sequence of period L can be written as,

$$n_{tran} = \frac{1 - \sum_{i=1}^{L} x_{i-1} x_i}{2}, \tag{5-34}$$

and the term of interest can thus be written as,

$$N_e = \frac{N}{L} \times n_{tran} = \frac{N}{2L}\left(1 - \sum_{i=1}^{L} x_{i-1} x_i\right). \tag{5-35}$$

Ideally, for a first order modulator we should thus choose a [1 -1] test sequence.

Nevertheless, it is known that this sequence is the natural limit cycle associated with zero and that integrator leakage makes it stable over a range of DC input levels around zero. As the settling error can be considered as an input-referred perturbation, it is possible that integrator leakage will make it undetectable. Nevertheless, if integrator leakage is previously tested, there should be no restriction on such a simple sequence.

For a second order modulator, however, we have found no direct relation between the input sequence and the term $(N_{-2}+N_2*)$. Simulations should thus be performed in order to find the sequences that maximize $(N_{-2}+N_2*)$.

If it is key to reach a given precision, the test can be designed such that samples are acquired until $(N_{-2}+N_2*)$ reaches the required value. The drawback of such an approach is that the uncertainty is transferred to the test time (i.e. the number of acquired samples N).

Another solution may consist of using a random zero-mean input sequence. With such a sequence, the modulator output at instant n should not be correlated to the input sample at

instant n and the probability of occurrence of level 2 (conversely -2) should be close to 1/4 as there are 4 combinations for the pair (input sample, output sample). Thus we would have

$$N_e = \frac{N}{2}. \tag{5-36}$$

Notice that if the input sequence is truly random, and the offset and settling errors remain small, the convergence of the term $(N_{-2}+N_2^*)$ to N_e also improves with the number of acquired samples. More concretely, we should consider the integrator input I as a random variable of a stochastic process. The probability density function (distribution) of I_k (the value of I at instant k) can be written

$$pdf(I_k) = \frac{1}{4}\delta(i-2) + \frac{1}{2}\delta(i) + \frac{1}{4}\delta(i+2) \tag{5-37}$$

Let L_k be the random variable defined as the occurrence of level 2 at the integrator input. Variable L_k is equal to 1 when I_k is equal to 2 and to 0 otherwise. We have the probability density function of L_k,

$$pdf(L_k) = \frac{1}{4}\delta(i-2) + \frac{3}{4}\delta(i). \tag{5-38}$$

The estimator N_e of the term $(N_{-2}+N_2^*)$ can be written as

$$N_e = \sum_{k=1}^{N} L_k + \sum_{k=1}^{N^*} L_k^* = \sum_{k=1}^{2N} L_k. \tag{5-39}$$

As the random variables are mutually independent, we have,

$$\begin{aligned} E(N_e) &= \sum_{k=1}^{2N} E(L_k) = \frac{N}{2} \\ \sigma^2(N_e) &= \sum_{k=1}^{2N} \sigma^2(L_k) = \frac{N}{2} \end{aligned}. \tag{5-40}$$

In order to take into account the different uncertainties, the simple signature proposed in Eq (5-30) can be written as

$$s = (E(N_e) \pm 3\sigma(N_e)) \times er_2 \pm 4 = \frac{N}{2} \times er_2 \pm \left(4 + 3er_2\sqrt{\frac{N}{2}}\right) \tag{5-41}$$

The error on the measurement of the settling error for a random input sequence and using Eq (5-41) (i.e., the simplified evaluation) is thus,

$$\Delta er_2 = \frac{8}{N} + \frac{6 \times er_2}{\sqrt{2N}} \tag{5-42}$$

5 • 1 . 3 . 2 Non-linear settling error

The justification of the test for the non-linear part of the settling error is based on the same considerations as for the overall settling error. For an input sequence with only 1s and 0s, the integrator input sees four levels and their associated settling errors:

$$\begin{array}{ll} 2 & er_2 \\ 1 & er_1 \\ 0 & er_0 \approx 0 \\ -1 & er_{-1} \approx -er_1 \end{array} \quad \textbf{(5-43)}$$

Hence, in the presence of an input referred offset (off), the integrator input mean value can be written:

$$\bar{I} = (2 + er_2) \times P_2 + (1 + er_1) \times P_1 + (0 + er_0) \times P_0 + (-1 + er_{-1}) \times P_{-1} + off\ . \quad \textbf{(5-44)}$$

Moreover, by definition, we have

$$\overline{X - Y} = \frac{1}{N} \sum_{i=1}^{N} x_i - y_i = 2P_2 + P_1 - P_{-1}\ . \quad \textbf{(5-45)}$$

Taking into account the simplifications on the settling errors in Eq (5-43), Eq (5-44) reduces to

$$\bar{I} = er_2 \times P_2 + er_1 \times (P_1 - P_{-1}) + \overline{X - Y} + off\ . \quad \textbf{(5-46)}$$

Due to the ΣΔ modulator feedback loop, the integrator input mean value is forced to zero. Moreover, we can assume that, if the input referred offset and the settling error are small, the output bitstream mean value is very close to the input sequence mean value. Hence, in a first order approximation we can write

$$[\overline{X - Y} \approx 0] \Leftrightarrow [(P_1 - P_{-1}) = -2P_2]\ . \quad \textbf{(5-47)}$$

Then, Eq (5-46)further reduces to

$$(er_2 - 2er_1) \times P_2 + \overline{X - Y} + off = 0\ . \quad \textbf{(5-48)}$$

If a second acquisition (quoted with a *) is performed with the opposite input sequence, we also have

$$(er^*_{-2} - 2er^*_{-1}) \times P^*_{-2} + \overline{X^* - Y^*} + off = 0. \quad \textbf{(5-49)}$$

Considering the simplifications on the settling errors in Eq (5-43), and combining these results with Eq (5-48), we obtain,

$$er_{NL} = er_2 - 2er_1 = \frac{\overline{Y - X} - \overline{Y^* - X^*}}{P^*_{-2} + P_2}. \tag{5-50}$$

For two acquisitions over N samples, this can be written more explicitly as Eq (5-16). Similarly to what has been said for the evaluation of the overall settling error, the main issue is the determination of the measurement precision, which depends strongly on the denominator term $(N^*_{-2}+N_2)$. Here again, if we were able to get a sufficiently precise estimator N_e of the denominator, we could build a simpler signature for the test

$$s \approx \left(\sum_{i=1}^{N} (x_i - y_i) - \sum_{i=1}^{N} (x_i^* - y_i^*) \right) \approx N_e \times er_{NL}. \tag{5-51}$$

Using random input sequences with only 0s and 1s (conversely -1s), the expected mean value and standard dispersion of N_e can be calculated similarly to what was done in the previous sub-section. Notice that if the probability of having a 0 or a 1 at the input is the same (1/2), the mean value of the random input sequence is 1/2. Hence, if the input referred errors are small, the mean value of the modulator output bitstream is also 1/2. Hence we have the following

$$\begin{pmatrix} \boldsymbol{X} & \boldsymbol{Y} \\ P(1) = \frac{1}{2} & P(1) = \frac{3}{4} \\ P(0) = \frac{1}{2} & P(-1) = \frac{1}{4} \end{pmatrix} \Rightarrow \begin{pmatrix} \boldsymbol{I} = \boldsymbol{X} - \boldsymbol{Y} \\ P(2) = \frac{1}{8} \\ P(1) = \frac{1}{8} \\ P(0) = \frac{3}{8} \\ P(-1) = \frac{3}{8} \end{pmatrix}. \tag{5-52}$$

Defining the variables L_k as in the previous sub-section, we obtain

$$\begin{aligned} E(N_e) &= \sum_{k=1}^{2N} E(L_k) = \frac{N}{4} \\ \sigma^2(N_e) &= \sum_{k=1}^{2N} \sigma^2(L_k) = \frac{N}{16} \end{aligned}. \tag{5-53}$$

In order to take into account the different uncertainties, the simple signature proposed in Eq (5-51) can be made more concrete as follows,

$$s = (E(N_e) \pm 3\sigma(N_e)) \times er_{NL} \pm 4 = \frac{N}{4} \times er_{NL} \pm \left(4 + \frac{3}{4} er_{NL}\sqrt{N}\right). \quad \textbf{(5-54)}$$

Hence, the uncertainty for the non-linear part of the settling error is,

$$\Delta er_{NL} = \frac{16}{N} + \frac{3er_{NL}}{\sqrt{N}} \quad \textbf{(5-55)}$$

It may also be possible to find an estimator N_e of the term $(N^*_{-2}+N_2)$ in the case of deterministic sequences, but it is not an obvious problem.

5 • 2 VALIDATION OF SETTLING ERROR TESTS THROUGH SIMULATION

5 • 2 . 1 Overall settling error

In order to validate the test proposed to determine the first amplifier settling error, a more complex model than the one presented in Figure 5-2 has to be used. Hence, we developed a simple amplifier model using standard Simulink blocks that implement Eq (5-2), (5-3) and (5-4).

◆ **Variation with the Slew-Rate and the GBW**

In this first set of simulations, we intend to show that the settling error measured through Eq (5-13) corresponds to the settling error expected for an input level of 2 and predicted by Eq (5-2), (5-3) and (5-4).

For that, we simulated a 1st and a 2nd order modulator over a grid of Slew-Rate and GBW. For each point of the grid, the expected settling error was calculated and two acquisitions over N=10000 points were run as explained in test description to obtain the measured settling error. The swept range for the GBW was the same for the 1st and 2nd order modulator: from 0.8 to 4. In turn, the range for the SR was 3.6 to 8 for the first order and 1.8 to 4 for the second order modulator. This change is due to the fact that the first integrator gain in the

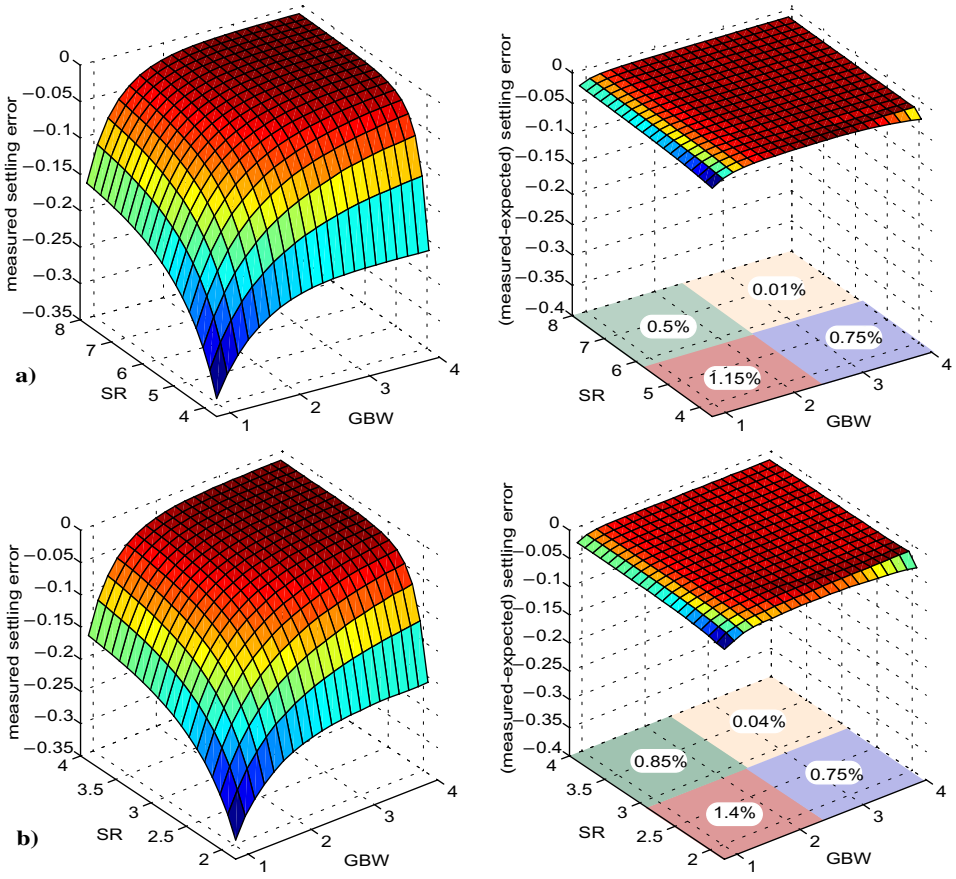


Figure 5-8: Evaluated settling error and its difference with the calculated settling error
a) for a first order modulator
b) for a second order modulator

2nd order modulator is set to 0.5, while it is set to 1 in the first order modulator. In both cases, the input sequence [1 1 -1 1 -1 -1] was used.

The results can be seen in Figure 5-8, which represents the measured settling errors and the difference with the expected (calculated) one, for both a 1st order modulator and a 2nd order modulator. It can be seen that the measured settling error is very similar for the first and second order modulators, which could be expected as the settling error is a characteristic of the amplifier. The difference between the measured and the calculated settling errors is represented with the same scale on the Z axis as the measured settling error itself. This allows one to verify easily that the matching is good between the calculated and measured

settling errors. Moreover, we have divided the SR/GBW grid in four quarters (for the sake of readability) and the maximum difference over each quarter is quoted on the figure. It is expressed as a percentage of the level (i.e. 2).

It can be seen that the precision of the proposed evaluation decreases slightly for the regions that present a high settling error. This is due to the fact that the settling error associated with the level processed in k samples is not negligible for those regions. For the simulations of Figure 5-8, k was set to 2. Figure 5-9 shows the difference between the calculated and measured settling errors in the case of a 1st order ΣΔ modulator with k=4. The differences between the measured settling error and the calculated settling error actually improve with k.

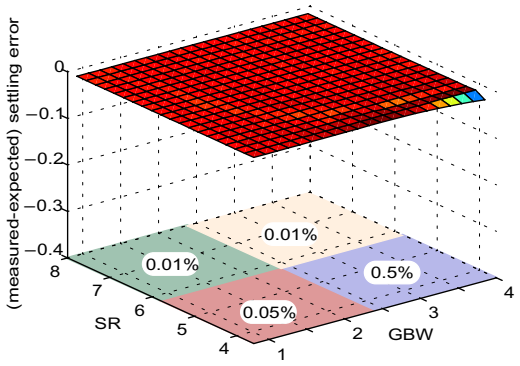


Figure 5-9: Measurement error for k=4

◆ **Variation with the input stimulus**

In the following, we intend to demonstrate the usefulness of the different signatures that have been proposed. To do so, we decided to drop the 3D representation of the settling error over a grid of SR and GBW value. For the sake of clarity, we prefer to represent the evolution of the settling error with the SR for 3 different values of the GBW, namely 1, 2 and 4.

Figure 5-10 shows the simulation results for a [1 1 -1 1 -1 -1] input sequence and a first order modulator. The solid curve corresponds to the calculated settling error, the circle markers to the error calculated with the originally proposed signature (Eq (5-13)) and the cross markers to the error calculated with the denominator approximation (using Eq (5-30)). For that input sequence, the estimator of $(N_{-2}+N_2^*)$ is, according to Eq (5-35), $N_e=2N/3$. It can be seen that the exact formula matches perfectly with the expected values (as was seen in the previous point). The matching of the alternative signature, based on the denominator approximation, is also very good for small settling errors. Larger settling errors are slightly overestimated, but that should not be critical from a test point of view.

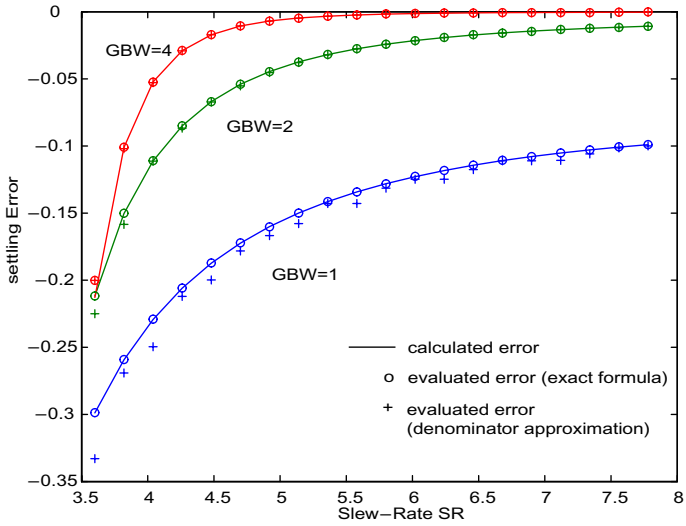


Figure 5-10: First order modulator settling error evaluation for a [1 1 -1 1 -1 -1] input sequence.

Figure 5-11 shows the same for a [1 -1] input sequence. For that sequence, the expected estimator of $(N_{-2}+N_2^*)$ is $N_e=N$. Here the matching is very good for the two signatures.

Finally, Figure 5-12 presents the results for a random input sequence. The expected estimator of $(N_{-2}+N_2^*)$ is $N_e=N/2$. In that case, the matching is similar to what was obtained in the case of the [1 1 -1 1 -1 -1] input sequence.

The following three figures represent the same results for a 2^{nd} order ΣΔ modulator. It can be seen clearly that the estimator N_e for deterministic sequences is not valid as the difference between the evaluated and the calculated error is high for both the [1 1 -1 1 -1 -1] and the [1 -1] input sequences. This could be expected as the estimator N_e was calculated assuming first order behaviour (i.e. that the modulator output bitstream follows the input sequence). The results appear to be better for the alternative signature with a [1 1 -1 1 -1 -1] sequence than with a [1 -1] sequence, but we could not find any reason for that. Hence, if the test sequence is a periodic sequence, the alternative signature should not be used for a 2^{nd} order modulator. On the other hand, the results drawn for a random sequence still hold true, as the matching is seen to be good for the two proposed signatures in Figure 5-12

.

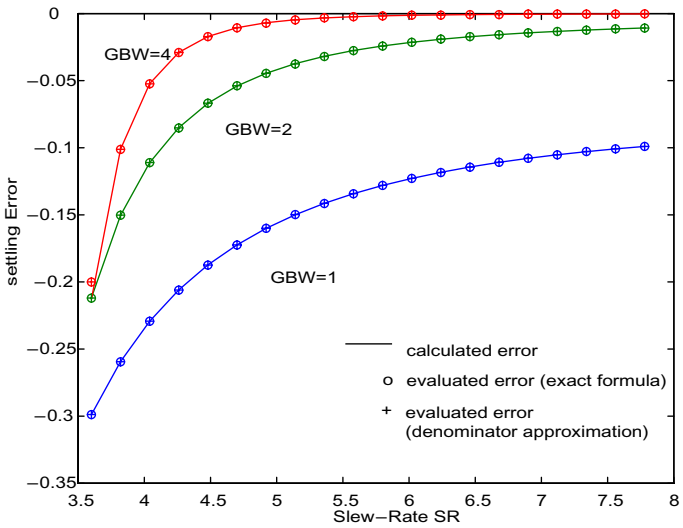


Figure 5-11: First order modulator settling error evaluation for a [1 -1] input sequence.

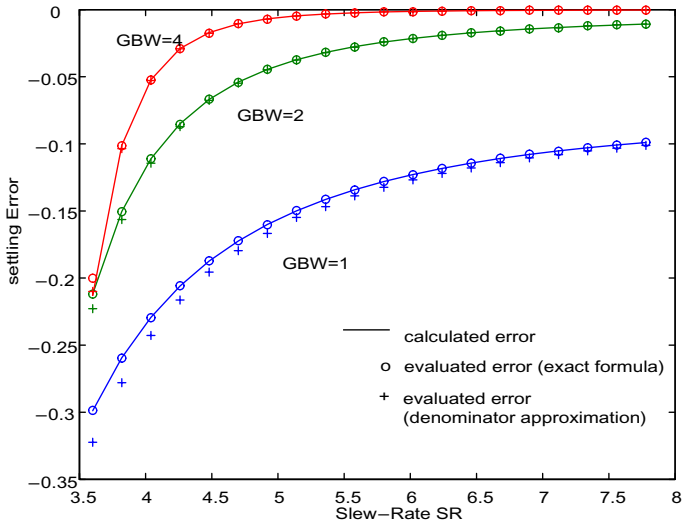


Figure 5-12: First order modulator settling error evaluation for a random input sequence.

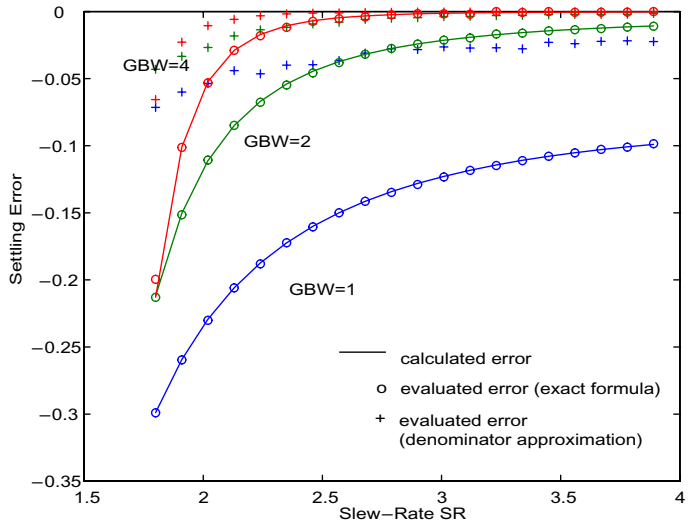


Figure 5-13: Second order modulator settling error evaluation for a [1 -1] input sequence.

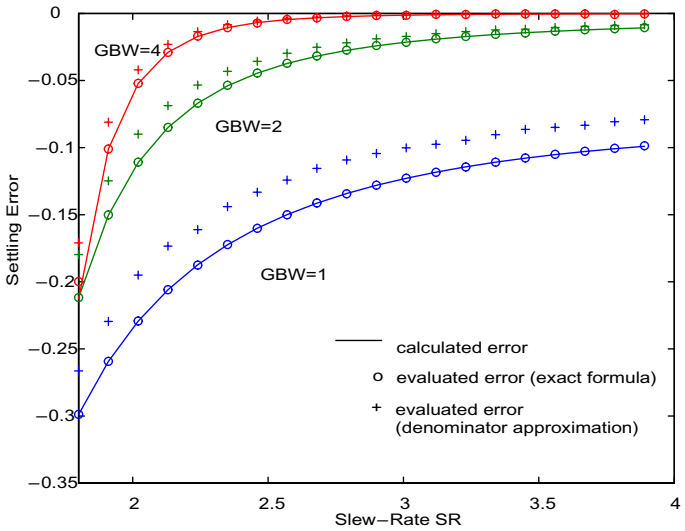


Figure 5-14: Second order modulator settling error evaluation for a [1 1 -1 1 -1 -1] input sequence.

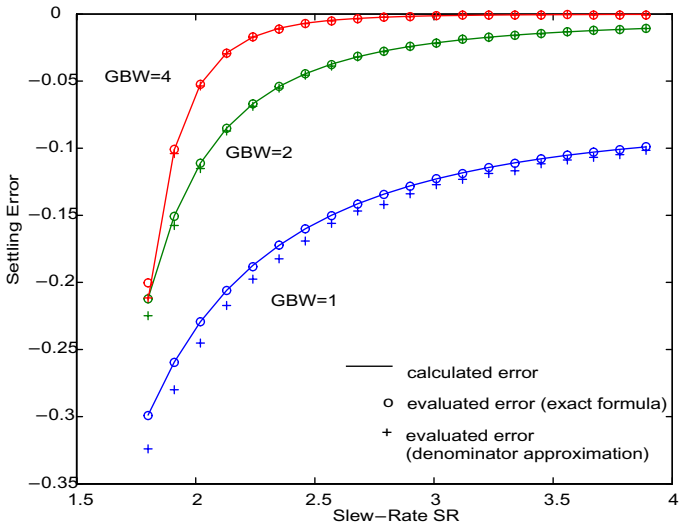


Figure 5-15: Second order modulator settling error evaluation for a random input sequence.

◆ **Variation with the number of points**

The objective of this last set of simulations is to check the evolution of the precision of the settling error evaluation with the number of points, for the proposed alternatives. For a 1st order modulator with SR=4 and GBW=3, three simulations were carried out over N=240000 points, for a [1 -1], a [1 1 -1], and a random input sequence. Figure 5-16 represents the evolution of the measured settling errors with the number of points. For each sequence, two settling errors were computed: the complete one (using Eq (5-27)) and the simplified one (using Eq (5-30)). On the figure is also represented the exact settling error and the confidence intervals, as calculated using Eq (5-29) and (5-42), for the complete evaluation and the simplified evaluation, in the case of the random input sequence. It can be seen that the results for the complete evaluation fit perfectly within the expected confidence interval for all three input sequences. In the case of the [1 1 -1] input sequence, however, the simplified evaluation signature seems to converge toward a value that is below the lower limit of the confidence interval. It is likely that the term N_e has been overestimated. On the other hand, the results for the simplified evaluation for a [1 -1] input sequence exactly fit the ones

for the complete evaluation, which means that the denominator term (N_{-2}+N_2*) in Eq (5-35) perfectly matches the expected N_e=N. Finally, the simplified evaluation for a random input sequence performs as expected. Indeed the results lie within the confidence interval calculated for a random sequence.

Figure 5-17 presents the results for a second order modulator. In that case, the simplified evaluation is only carried out for the random sequence, as we could not derive the estimator N_e of the term (N_{-2}+N_2*) for deterministic sequences. Moreover, the calculation of the confidence interval is also based on that estimator. That is why it is represented as a dotted curve for the [1 -1] and the [1 1 -1] sequences. It can be seen that the complete evaluation of the settling error gives good results. The calculated confidence interval is respected for the random sequence. However, it can be seen that the confidence interval for the [1 -1] sequence

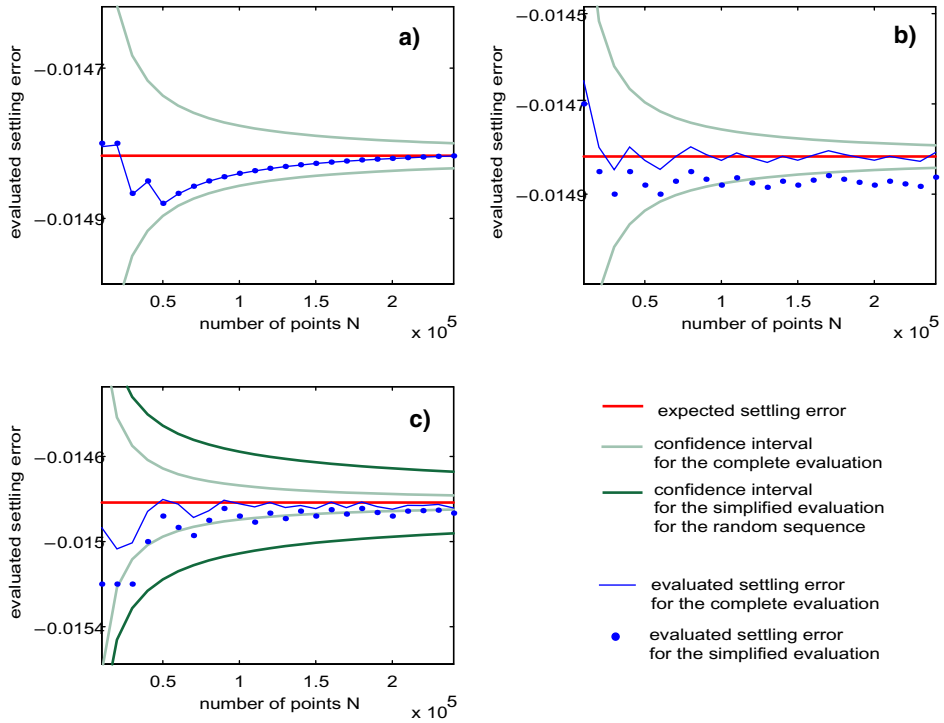


Figure 5-16: First order modulator settling error evaluation versus the number of acquired points
a) for a [1 -1] input sequence
b) for a [1 1 -1] input sequence
c) for a random input sequence

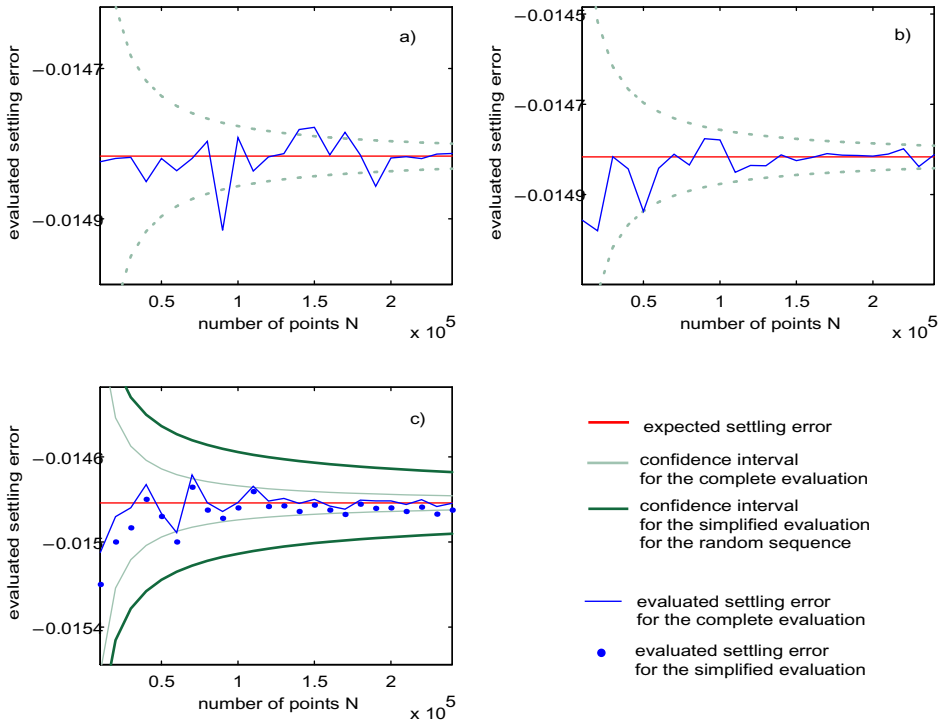


Figure 5-17: Second order modulator settling error evaluation versus the number of acquired points
a) for a [1 -1] input sequence
b) for a [1 1 -1] input sequence
c) for a random input sequence

does not hold true. This means that the term (N_{-2}+N_2*) can vary by a non-negligible amount with respect to N. In any case, the precision is good as the Y axis presents a very reduced range around the expected error.

5 • 2 . 2 Non-linear part of the settling error

◆ **Variation with the Slew-Rate and GBW**

The simulation performed here is similar to the one performed for the elaboration of Figure 5-8. A first-order and a second-order modulator are simulated over a grid of SR and GBW values, and the proposed test of the non-linear part of the settling error is applied.

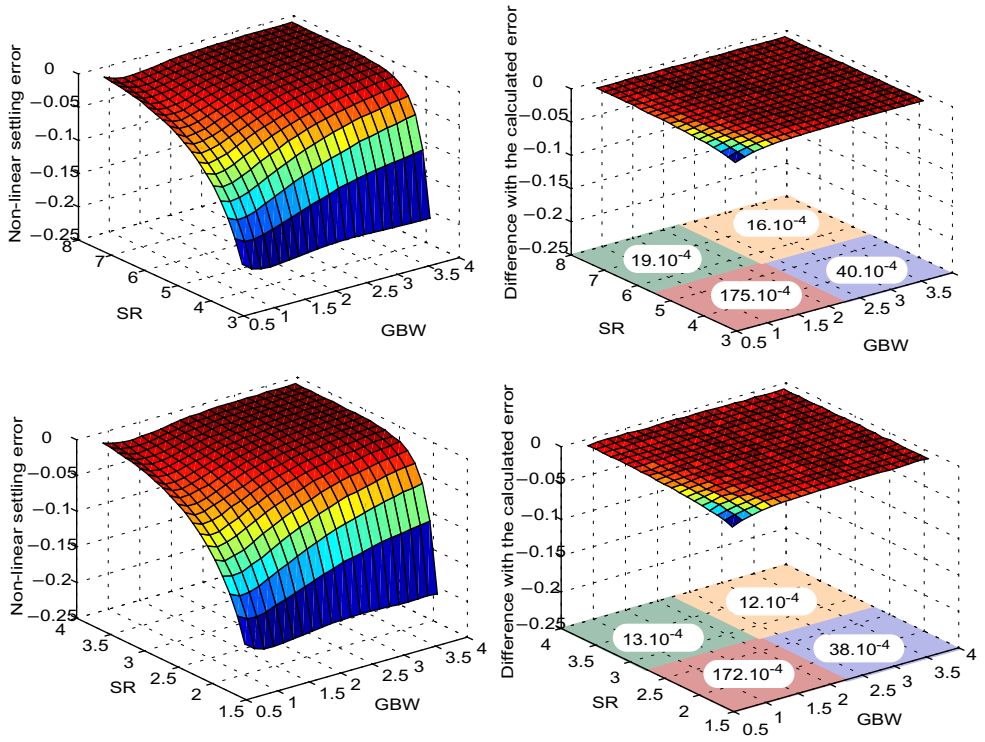


Figure 5-18: Evaluated non-linear settling error and its difference with the calculated non-linear settling error
a) for a first order modulator
b) for a second order modulator

Each acquisition was performed over N=10000 samples for random input sequences having only 1s and 0s or only -1s and 0s.

Figure 5-18 represents the measured non-linear settling error, using the complete measurement of Eq (5-16), and its difference with the calculated one (er_2-$2er_1$, using Eq (5-2), (5-3) and (5-4)), for both the first-order and the second-order modulators. Moreover, the SR/GBW grid has been divided into four quarters and the maximum difference over each quarter is quoted on the figure. It can be seen that a low error results from the proposed complete measurement. The maximum error is found for the highest values of the settling error. This is due to the fact that the approximation of Eq (5-47) stands for small values of the settling error. The results are very similar for the first-order and second-order modulators, as expected.

◆ **Variation with the number of points**

Similarly to what was done for the overall settling error, Figure 5-19 presents the evolution of the measured non-linear settling error with the number of acquired points, for a first-order and a second-order modulator. In both cases, the test was carried out for a [1 0] sequence, a [1 1 0] sequence and a random (between levels 1 and 0) sequence. The figures display the calculated settling error as a solid red curve and the evaluated settling error as a blue solid curve. In the case of the random sequence, the markers stand for the simplified evaluation that corresponds to Eq (5-55). Moreover, the confidence intervals have also been represented for the random sequence. In the case of the deterministic sequences (both [1 0] and [1 1 0]) we also represented by a dotted curve the confidence interval calculated for a random sequence in order to simplify the comparisons.

It can be seen that, for the first-order modulator, the evaluation with deterministic sequences provides good results, that are comparable to (and even better than) those obtained for a random sequence. For this latter, it can be noted that the results fit within the calculated confidence intervals. On the other hand, for a second order modulator, the deterministic sequences give poorer results than the random sequence. Anyway, the precision is seen to be good, as the excursion on the Y axis is still small.

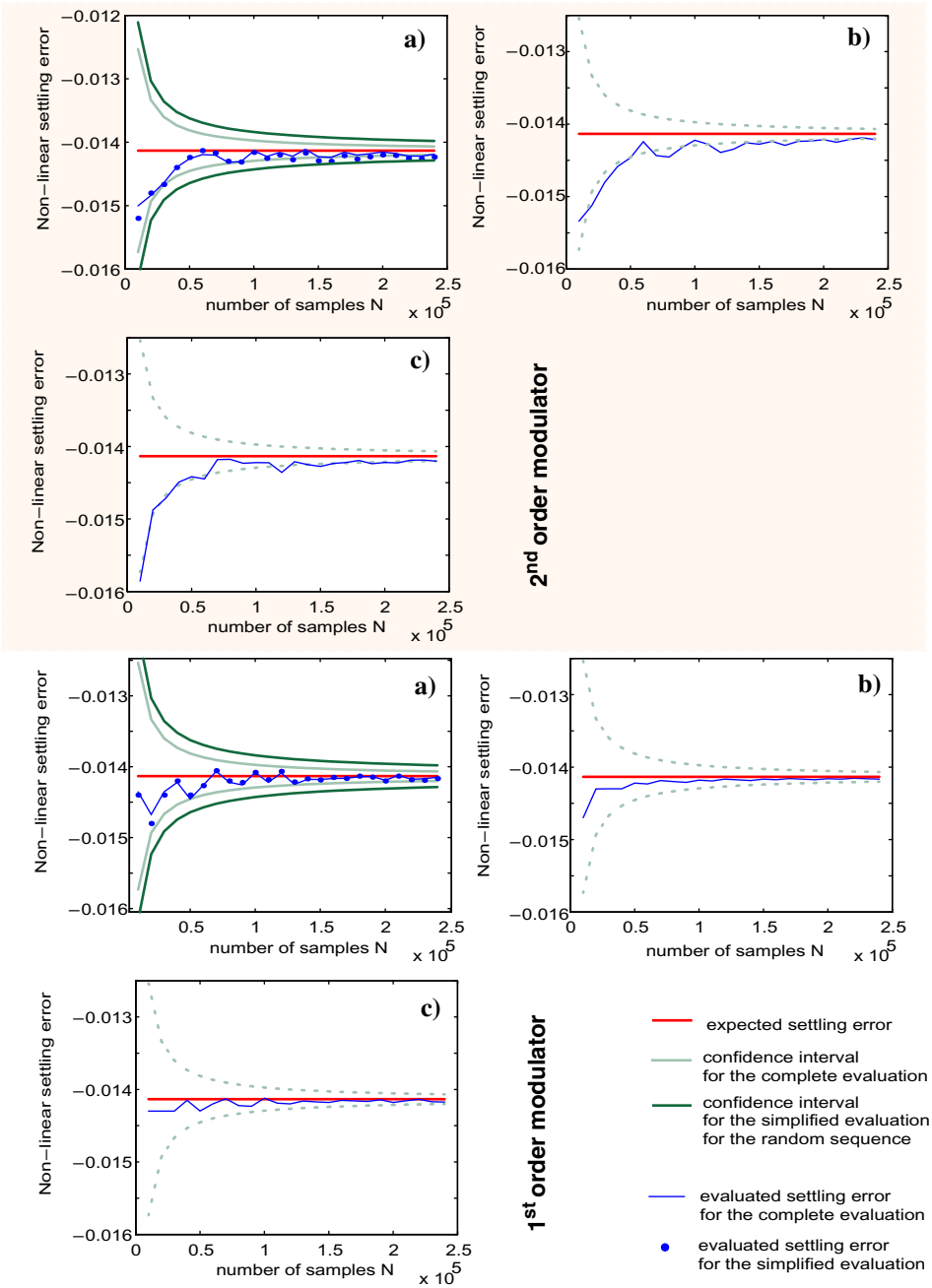


Figure 5-19: First and second order modulator settling error evaluation versus the number of acquired points
a) for a random input sequence
b) for a [1 -1] input sequence
c) for a [1 1 -1] input sequence

5 • 3 TESTS SUMMARY

In this chapter and the previous one, a number of tests have been proposed that target important behavioural parameters. Moreover, in some cases several test alternatives have been proposed for a given parameter as they offer different benefits and drawback.

The purpose of this section is to present in a table the most important information in order to facilitate the comprehension of the test set as a whole. Up to now, the tests have been considered individually as each is designed to target a different effect: integrator leakage, settling, etc. However, the approach described in Chapter 3 aims to determine most of the behavioural parameters to make sure that a modulator is defect-free. The different tests have thus to be considered as a test set.

As a matter of fact, if all the proposed tests are applied to a given modulator, the results will likely be correlated; on the one hand because several test target the same parameters as said before, and on the other hand because a catastrophic failure that cause the modulator to saturate will obviously fail all the tests. However, there is one particular case that has to be treated because the correlation it introduces between settling and leakage is intrinsic.

5 • 3 . 1 Test correction

Before proceeding with the test summary, a correction has to be introduced to one of the tests. In Section 5 • 1 . 2 . 2 it has been proposed to use a sequence with only 1s and 0s (or conversely -1s and 0s) instead of 1s and -1s. The purpose of this test is to test the non-linear part of the settling error.

However, a sequence composed only by 1s and 0s cannot have a zero mean value, making the test signature sensitive to integrator leakage. Actually, it was proposed in Chapter 4 to use a sequence with L-1 1s and one 0 as an alternative to the leakage test for a 1^{st} order modulator in order to avoid the introduction of an extra delay in the feedback loop. It appears clearly that there is a conflict between the tests that may lead to undesirable fault masking.

Fortunately, it is possible to circumvent this issue. Indeed, if the test is first performed at half the nominal clock frequency, it can be considered that the settling error is negligible. Hence, the test signature only contains the contribution of integrator leakage (at least to a first order approximation). Then if the test is performed at the nominal clock frequency, the deviation of the signature from the results obtained at the half-frequency account for the settling error contribution. Let us consider the test for a 2nd order modulator. Four signatures are obtained for the four acquisitions,

$$\begin{aligned} s1_{fs/2} &= \sum_{i=1}^{N}(y_i - x_i) = 2NQ\Delta p + off \pm 2 \\ s2_{fs/2} &= \sum_{i=1}^{N}(y_i - x_i) = (-2)NQ\Delta p + off \pm 2 \\ s1_{fs} &= \sum_{i=1}^{N}(y_i - x_i) = N_2(er_2 - 2er_1) + 2NQ\Delta p + off \pm 2 \\ s2_{fs} &= \sum_{i=1}^{N}(y_i - x_i) = -N^*_{-2}(er_2 - 2er_1) - 2NQ\Delta p + off \pm 2 \end{aligned} \quad \textbf{(5-56)}$$

As was seen previously, Q is the mean value of the test sequence, Δp is the pole error of the integrator under test, *off* is its input-referred offset, er_2 is the settling error associated with a 2 integrator input and er_1 is the settling error associated with a 1 integrator input. N_2 is the number of occurrence of a 2 integrator input (i.e the input sample is a 1 and the feedback sample is a -1) and N^*_{-2} is, conversely, the number of occurrence of a -2 integrator input (i.e. the input sample is a -1 and the feedback sample is a 1). The combinations of interest are thus

$$\begin{aligned} s1_{fs/2} - s2_{fs/2} &= 4NQ\Delta p \pm 4 \\ (s1_{fs} - s2_{fs}) - (s1_{fs/2} - s2_{fs/2}) &= (er_2 - 2er_1)(N_2 + N^*_{-2}) \pm 8 \end{aligned} \quad \textbf{(5-57)}$$

The only change with respect to the results obtained previously is that the absolute uncertainty on the settling error measurement has increased.

Hence, for the test with a deterministic sequence with only 1s (alternatively -1s) and 0s (that requires the evaluation of the number of occurrences of level 2 (-2) at the integrator input), the non-linear settling error signature (previously Eq (5-16)) becomes

$$er_{NL} = \frac{(s1_{fs} - s2_{fs}) - (s1_{fs/2} - s2_{fs/2}) \pm 8}{(N_2 + N^*_{-2})}, \quad \text{(5-58)}$$

where N_2 is the number of occurrences of a level 2 at the integrator input during the acquisition with a positive sequence at full-speed (corresponding to s_{1fs}) and N^*_2 is the number of occurrences of a level -2 at the integrator input during the acquisition with a negative sequence at full-speed (corresponding to s_{2fs}).

Similarly, for the test with pseudorandom sequences with only 1s (alternatively -1s) and 0s, the simplified signature (previously Eq (5-54)) becomes

$$s = (E(N_e) \pm 3\sigma(N_e)) \times er_{NL} \pm 8 = \frac{N}{4} \times er_{NL} \pm \left(8 + \frac{3}{4} er_{NL}\sqrt{N}\right). \quad \text{(5-59)}$$

5 • 3 . 2 Test list

In the following table, we summarize the characteristics of all the tests proposed in the thesis. This section is replicated in the floating appendix A, in order to facilitate referencing.

To avoid redundancy in the test comments, we recall to the reader that in the majority of cases, the test sequence is a digital sequence composed by 1s (corresponding to logic 1s) and -1s (corresponding to logic 0s). Some tests use sequences with analog 0s (and must thus use two bits to define the test sequence) but these cases will be specified in the table.

Similarly, most tests use two acquisitions to get rid of the impact of possible input-referred offsets. The test signature for each acquisition is the difference between the test sequence (x) and the modulator output bit-stream (y) accumulated over N samples. The final signature is taken as the difference between the result for the two acquisitions,

$$s = s_1 - s_2 = \left(\sum_{i=1}^{N} x_i - y_i\right)_1 - \left(\sum_{i=1}^{N} x_i - y_i\right)_2 \quad \text{(5-60)}$$

In some cases, a slightly more complex signature has to be generated but these particular cases are also specified in the table.

Table I: Test summary

nº	type	signature	equation ref.
1	leakage test for 2nd order	$s = 4NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}}$	(4-20) page 123
Stimulus: Any sequence of non-zero mean value Q (-Q). **Comments:** The influence of DC gain non-linearity may be noticed for the highest mean values.			
2	leakage test for 2nd order	$s = 4NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}}$	(4-20) page 123
Stimulus: A sequence with analog 0s of mean value Q (-Q). **Comments:** This test has to be run at half the nominal clock frequency to avoid settling errors.			
3	leakage test for 1st order single-bit	$s = \frac{4N\Delta p}{\ln\left(\frac{3L-5}{L-5}\right)} \pm 4$	(4-27) page 126
Stimulus: A digital sequence of length L with L-1 1s and only one -1, and its opposite. L must be greater than 5. **Comments:** An extra delay has to be introduced in the feedback loop. The offset may cause a strong non-linearity for either the positive or negative sequence, leading to a relative error on the leakage evaluation.			
4	leakage test for 1st order single-bit	$s = 2N\Delta p\left(\frac{1}{\ln\left(\frac{5-3L_1}{5-L_1}\right)} - \frac{1}{\ln\left(\frac{5-3L_2}{5-L_2}\right)}\right) \pm 4$	(4-87) page 142
Stimulus: Two digital sequences of length L_1 and L_2, with L-1 1s and only one -1, and their opposites. L_1 and L_2 must be greater than 5. **Signature:** The input/output difference accumulated over N samples. The sign of the offset has to be determined. The results obtained for the two sequences of opposite signs to the offset are combined **Comments:** An extra delay has to be introduced in the feedback loop. The obtained signature has lower sensitivity than the previous test			
5	leakage test for 1st order single-bit	$s = \frac{2N\Delta p}{\ln\left(\frac{3L-2}{L-2}\right)} \pm 2$	(4-28) page 126

Table I: Test summary

nº	type	signature	equation ref.
Stimulus: A digital sequence of length L with L-1 1s and only one 0, and its opposite. L must be greater than 2. The test must be carried out at half the sampling frequency to avoid settling errors. **Comments:** Analog 0s are used in the sequence. It is the same test as nº 3 but no extra delay has to be introduced in the feedback loop. The offset may cause a strong non-linearity for either the positive or negative sequence, leading to a relative error on the leakage evaluation.			
6	leakage test for 1st order single-bit	$s = N\Delta p\left(\frac{1}{\ln\left(\frac{2-3L_1}{2-L_1}\right)} - \frac{1}{\ln\left(\frac{2-3L_2}{2-L_2}\right)}\right)\pm 2$	(4-93) page 145
Stimulus: Two digital sequences of length L_1 and L_2, with L-1 1s and only one 0, and their opposites. L_1 and L_2 must be greater than 2. The test must be carried out at half the sampling frequency to avoid settling errors. **Signature:** The input/output difference accumulated over N samples. The sign of the offset has to be determined. The results obtained for the two sequences of opposite signs to the offset are combined **Comments:** The obtained signature has a lower sensitivity than the previous test			
7	leakage test for 1st order multi-bit	$s = 2NQ\Delta p \pm \frac{6}{2^{L_{DAC}-1}}\sqrt{\frac{1}{3}}$	(4-24) page 124
Stimulus: A sequence of mean value Q greater than half the quantizer step and its opposite. **Comments:** It is recommended to use a mean value significantly greater than half the quantizer step.			
8	DC gain non-linearity test for 2nd order	$s = s_1/s_2 = \frac{Q_1}{Q_2}\times\frac{f(a_{NL},Q_1)}{f(a_{NL},Q_2)} \pm \frac{Q_1}{NQ_2\Delta p}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)$	(4-114) page 173
Stimulus: Two sequences of non-zero mean value Q_1 and Q_2 and their opposites. **Signature:** It is the ratio of the leakage test signatures **Comments:** The same test as nº 1 is performed with two sequences. For a small mean value the result is proportional to the nominal DC gain while for a high mean value it is sensitive to DC gain non-linearity. The value of the signature is only sensitive to the non-linearity of the DC gain but not its uncertainty.			

Table I: Test summary

nº	type	signature	equation ref.
9	DC gain non-linearity test for 2nd order	$s = s_1 - \frac{Q_2}{Q_2} \times s_2 = 4NQ_1\Delta p[f(a_{NL}, Q_1) - f(a_{NL}, Q_2)] \pm 6\left(1 + \frac{Q_1}{Q_2}\right)\sqrt{\frac{2}{3}}$	(4-115) page 173
Stimulus: Two sequences of non-zero mean value Q_1 and Q_2 and their opposites. **Signature:** It is the scaled difference between the leakage test signatures. **Comments:** This signature does not requires a division but is function of the nominal DC gain and not only of its non-linearity.			
10	overall settling error test for any modulator	$er_2 = \frac{s_1 - s_2^* \pm 4}{N_{-2} + N^*_2}$	(5-13) page 191
Stimulus: A sequence of zero mean value. The period of the clock reference is doubled for a 1 input sample during the 1st acquisition and for a 0 input sample during the 2nd acquisition (*). **Signature:** Apart from the accumulated input/output difference**,** the number of occurrences of a level -2 (alternatively 2) at the integrator input has also to be acquired.			
11	overall settling error test for any modulator	$s = \frac{N}{2} \times er_2 \pm \left(4 + 3er_2\sqrt{\frac{N}{2}}\right)$	(5-41) page 197
Stimulus: A pseudorandom sequence of zero mean value. The period of the clock reference is doubled for a 1 input sample during the 1st acquisition and for a 0 input sample during the 2nd acquisition (*). **Comments:** The use of a pseudorandom sequence allows one to estimate *a-priori* the number of occurrences of a level -2 (alternatively 2) at the integrator input as being equal to N/4. The signature is thus much simpler but this approximation leads to an additional (small) relative error.			
12	non-linear settling error test for any modulator	$er_{NL} = \frac{(s_{1_{fs}} - s_{2_{fs}}) - (s_{1_{fs/2}} - s_{2_{fs/2}}) \pm 8}{(N_2 + N^*_{-2})}$	(5-58) page 214
Stimulus: A sequence with only 1s and analog 0s and its opposite. The clocking does not have to be modified as function of the input. Two more acquisitions have to be performed at half the nominal frequency. **Signature:** Apart from the accumulated input/output difference**,** the number of occurrences of a level 2 (alternatively -2) at the integrator input has also to be acquired. **Comments:** As the input sequence is not of zero mean value, the influence of the leakage has to be suppressed. For this reason the acquisitions are also performed at half the nominal frequency.			

Table I: Test summary

nº	type	signature	equation ref.
13	non-linear settling error test for any modulator	$s = (s1_{fs} - s2_{fs}) - (s1_{fs/2} - s2_{fs/2}) = \frac{N}{4} \times er_{NL} \pm \left(8 + \frac{3}{4} er_{NL}\sqrt{N}\right)$	(5-59) page 214
Stimulus: A pseudorandom sequence with only 1s and analog 0s, and its opposite. The clocking does not have to be modified as a function of the input. Two more acquisitions have to be performed at half the nominal frequency. **Comments:** The use of a pseudorandom sequence allows one to estimate as N/8 the number of occurrences of a level -2 (alternatively 2) at the integrator input. The signature is thus much simpler but this approximation leads to an additional (small) relative error.			

5 • 4 TEST SET SIMULATION

At this point, the proposed tests have been validated individually. For that purpose, all the behavioural parameters other than those directly involved in the tests were set to their ideal values. Nevertheless, it is legitimate to wonder if defects or drifts could alter more than one parameter significantly at a time, and if the proposed tests would be affected.

Ideally, a multi-dimensional analysis should be performed for each test, varying all the behavioural parameters over a large range but with a step that is sufficiently fine to distinguish meaningful variations. This would require a large number of simulations, which makes this approach prohibitive.

One of the benefits of the proposed approach is that it introduces much flexibility in the test design. This allows us to tailor the test as a function of the application need. On the other hand, such flexibility makes validation of the approach difficult. In this section, we perform a Monte-Carlo simulation at a behavioural level. This allows us to simulate a fairly large number of tests and to try several test set configurations. Let us make a brief summary of the tasks that are carried out in order to clarify what we intend with the simulation:

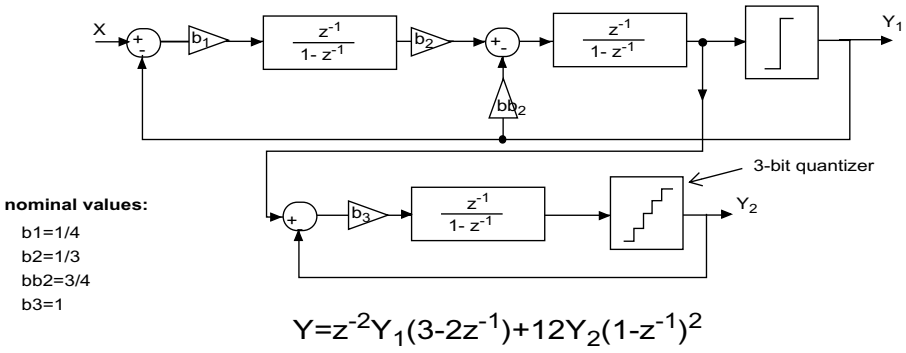


Figure 5-20: Diagram of a 2-1 cascade modulator

- Design of the demonstrator: a modulator architecture is selected and its behavioural parameters are selected in order to reach a given resolution. Guard bands are taken and a nominal variation range is defined for each parameter.
- Individual test design: a number of tests are proposed that cover the different proposals of the thesis. For each of these tests, the number of acquired points and the test pass/fail limit have to be defined.
- Test set selection: provided that some tests in the list are redundant (see Table I or Appendix A) and taking into account their specificities, several test sets can be defined.
- Fault simulation: A number of faults are simulated in a Monte-Carlo fashion. The results for the different test configurations can then be compared.

5 • 4 . 1 Modulator “design”

A 2-1 cascaded modulator like the one shown in Figure 5-20 has been chosen to perform the Monte-Carlo simulation. The first stage is a 2nd order single-bit modulator like the one proposed in [24] and the second stage is a 1st order 3-bit modulator.

For this architecture, the reconstruction filter is of the form

$$Y = z^{-2}(3-2z^{-1})Y_1 + 12Y_2(1-z^{-1})^2 \quad . \qquad \textbf{(5-61)}$$

Indeed, it is easily shown that such a reconstruction provides a noise shaping of third order as

$$Y = z^{-3}X + 12(1 - z^{-1})^3 E_2 \quad \textbf{(5-62)}$$

Notice that the final quantization error E_2 is the quantization error of the second stage and its associated power is thus

$$\sigma_{E_2}^2 = \frac{q^2}{12} = \frac{\left(\frac{FS}{2^3 - 1}\right)^2}{12} \quad \textbf{(5-63)}$$

We decided to set the oversampling ratio arbitrarily to 64. Hence, analytical calculation based on the above considerations tell us that the ideal resolution of the modulator should be around 16.5 bits for an ideal implementation.

As our goal is not to design a modulator for a real implementation but to give support to the validation of the proposed test set, we decided to choose adequate behavioural parameters by design-space exploration rather than detailed analytical calculations.

A number of 1000 simulations were performed varying the different parameters over a broad range and the obtained ENOB was calculated in each case for a half-scale input sine-wave. Then, the reduced set of the modulators that have an ENOB higher than a given target - say 15 bits - is isolated. The values of the behavioural parameters for this reduced set are retrieved; this provides the valid design space. Furthermore, the cloud of points of the ENOB versus any behavioural parameter can be represented, which gives an indication of the trend of the relationship between the parameter and ENOB. This information allows us to select a design point in the valid design space with some guard-band.

For instance, in our case, Figure 5-21 represents the ENOB against the 2nd amplifier DC gain. The upper limit of the cloud of points clearly indicates that lower DC gains limit the ENOB of the modulator. However, above a certain limit the impact of the DC gain becomes smaller than the quantization noise. Hence, the nominal DC gain for the 2nd amplifier has to be chosen, with some guard-band, in the range where the ENOB is not sensitive to its value. In Figure 5-21, it can be seen that a DC gain above 54 dB should be sufficient to reach an ENOB of 15.5bit. A DC gain of 65dB may thus provide a safe guard-band. The same can be done with the rest of parameters. Notice that considering the cloud of points on a single

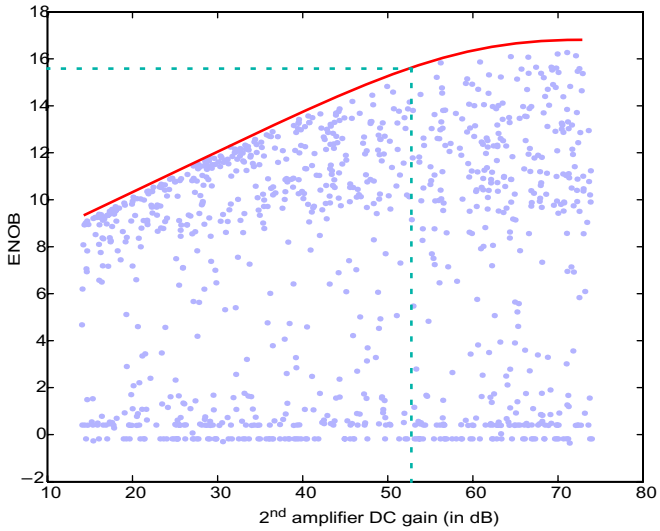


Figure 5-21: Cloud of points of the design space exploration representing the obtained ENOB versus the 2nd amplifier DC gain

dimension may be misleading. Indeed, the impact of some behavioural parameters cannot be considered without another. For instance, the pair Slew-Rate/GBW defines the settling of an amplifier and several couples may lead to a satisfactory result. In other words, it cannot be said that a given value of Slew-Rate is adequate without knowing the value of the GBW. This is illustrated in Figure 5-22 where the cloud of points of the ENOB is represented in three dimensions, versus the Slew-Rate and GBW of the first amplifier. The red circle markers emphasize the modulators (i.e. points of the cloud) having an ENOB greater than 15. On the X/Y view of the cloud of points, it can be seen that the red markers define a validity zone for the couple (SR/GBW) that is not a square: improving the Slew-Rate allows to relax the GBW and vice-versa. These types of trade-offs are very familiar to designers.

With the purpose of fault simulation in mind, we defined three variation ranges for each behavioural parameter:

- **Nominal range**

  During the design of a ΣΔ modulator, the characteristics of the analog macros (the behavioural parameters) are chosen in a zone where the simulated performance is

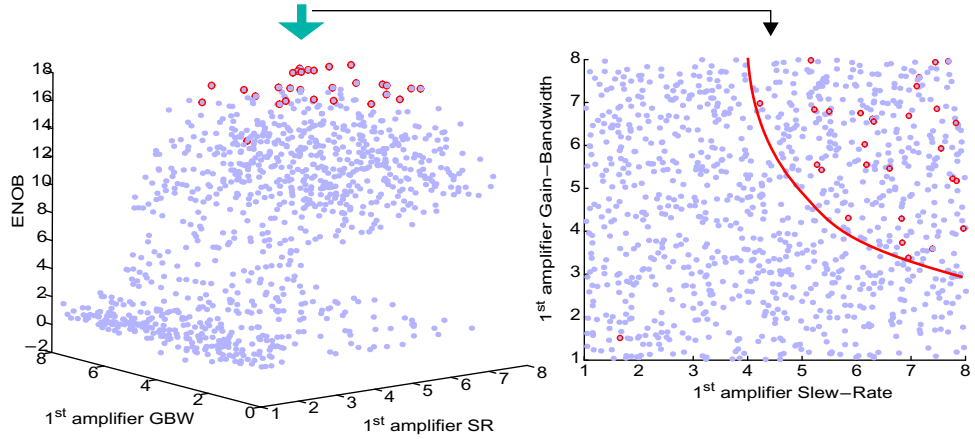


Figure 5-22: Cloud of points of the design space exploration representing the obtained ENOB versus the 1st amplifier Slew-Rate and Gain-Bandwidth

the desired one but also where the sensitivity to the variation of the parameters is reasonably small. For instance, it has been seen in Figure 1-17 that there may be singularities in the design space where performance reaches a very pronounced but very localized peak. It is not convenient to choose such a point for the actual design as any perturbation is likely to bring the modulator out of specifications. Actually, some guard-bands have to be considered in the choice of the design point to account for nominal process variations that will unavoidably translate into small variations of the behavioural parameters. Obviously, a skilled designer always tries to maximize the guard bands within the constraints of an area and power budget.

This last consideration is of importance from a test viewpoint, as will be seen further. Indeed, it means that a parameter variation larger than the the process corner (thus a parametric defect) may still lead to a modulator within the guard-band of the correct design-space. Such a modulator would perform correctly despite being defective.

- **Parametric range**

  In real-world applications, and in particular in harsh-environments, it is possible that the circuit will be used outside its certified operating conditions. As a result, the

behavioral parameters may be brought out of the nominal variation range. Corner simulations are performed during design to account for the worst case of process variations combined with temperature range and supply conditions. However, it is likely that if the operating conditions (temperature, supply voltage or both) are set slightly out of the expected range, circuit operation will still be maintained though performance may be affected. Hence, we define a parametric variation range for the behavioral parameters that extend the nominal range out of the design guard-bands. Notice that we have taken the example of a global temperature or supply drift to justify the introduction of the parametric range of variation but this does not mean that parametric variations are necessarily global. Indeed, a spot defect that would short the gate voltage of a p-type cascode transistor to ground may produce only a small parametric deviation in an amplifier.

- **Drastic variation range**

  A drastic variation range is also defined for each behavioural parameter to emulate the effects of possible "catastrophic" defects. The word catastrophic is in quotation marks because it is usually associated with catastrophic faults that significantly impact circuit performance or even functionality. Nevertheless, what we intend to consider here are defects that severely impact the analog macros of the modulator. However, as will be seen later, this does not mean that the induced fault need to be necessarily considered as a functional catastrophic fault for the modulator.

The three selected variation ranges for each parameter are displayed in Table II. Notice that dimensional parameters (like for instance the Slew-Rate) are normalized to the modulator Full-Scale and/or sampling frequency.

Further simulations of nominal modulators show that the ENOB obtained for a half-scale input sine-wave varies between 15.2 and 15.5 bits, which means that the selected guard-bands effectively provide a slight resolution improvement over the 15 bit target.

Table II: Behavioural parameters variation ranges

parameters	nominal range	parametric range	drastic range
1st amplifier DC gain A1 (dB)	[65;68]	[40;60]	[5;30]
1st integrator coefficient b1	1/4 +/- 0.1%	1/4 +/- 0.1%	1/4 +/-[20;40]%
1st amplifier Gain-Bandwidth product GBW1 (dB)	[6;6.2]	[3;4.5]	[0.5;2.5]
1st amplifier Slew-Rate SR1 (dB)	[6.5;6.7]	[3;4.5]	[0.5;2.5]
1st amplifier input-referred noise Vn1	$[1;2].10^{-5}$	$[10^{-5};10^{-4}]$	$[1;6].10^{-4}$
1st amplifier feedback capacitance Cf1 (pF)	10 +/- 20%	[1 ; 10]	[0.1 ; 1]
1st amplifier clipping value sat1	[3 ;3.2]	[1;3]	[0.5;1]
1st amplifier DC gain non-linearity a_{NL1}	[8;9.5]	[2.5;8]	[1;2]
1st integrator offset o1	+/- 0.1%	+/- 0.2%	+/- [5;10]%
2nd amplifier DC gain A2 (dB)	[65;68]	[40;60]	[5;30]
2nd integrator direct coefficient b2	1/3 +/- 0.1%	1/3 +/- 0.1%	1/3 +/-[20;40]%
2nd integrator feedback coefficient bb2	3/4 +/- 0.1%	3/4 +/- 0.1%	3/4 +/-[20;40]%
2nd amplifier Gain-Bandwidth product GBW2 (dB)	[5;5.2]	[2.5;4.5]	[0.5;2]
2nd amplifier Slew-Rate SR2 (dB)	[6;6.2]	[3;5]	[0.5;2]
2nd amplifier input-referred noise Vn2	$[1;2].10^{-5}$	$[10^{-5};10^{-4}]$	$[1;6].10^{-4}$

Table II: Behavioural parameters variation ranges

parameters	nominal range	parametric range	drastic range
2nd amplifier feedback capacitance Cf2 (pF)	1 +/- 20%	[0.1 ; 1]	[0.01 ; 0.1]
2nd amplifier clipping value sat2	[3 ;3.2]	[1;3]	[0.5;1]
2nd amplifier DC gain non-linearity a_{NL2}	[8;9.5]	[2.5;8]	[1;2]
2nd integrator offset o2	+/- 0.1%	+/- 0.2%	+/- [5;10]%
3rd amplifier DC gain A3 (dB)	[40;43]	[10;30]	[5;10]
3rd integrator coefficient b3	1/4 +/- 0.1%	1/4 +/- 0.1%	1/4 +/-[20;40]%
3rd amplifier Gain-Bandwidth product GBW3	[4;4.2]	[2;3]	[0.5;1]
3rd amplifier Slew-Rate SR3 (dB)	[6.5;6.7]	[3;4.5]	[0.5;2.5]
3rd amplifier input-referred noise Vn3	$[1;2].10^{-5}$	$[10^{-5};10^{-4}]$	$[1;6].10^{-4}$
3rd amplifier feedback capacitance Cf3	0.1 +/- 20%	[0.01 ; 0.1]	[0.001 ; 0.01]
3rd amplifier clipping value sat3	[2 ;2.3]	[1.2;2.2]	[0.5;1]
3rd amplifier DC gain non-linearity a_{NL3}	[4;4.5]	[2.5;4]	[1;2]
3rd integrator offset o3	+/- 0.1%	+/- 0.2%	+/- [5;10]%

5 • 4 . 2 Individual test design

A large number of tests will be applied to this modulator in order to cover most of our proposals:

- **Test 1:** 1st amplifier leakage test with a Q=1/5 sequence [1 -1 1 -1 1] (nº1 in Table I)
- **Test 2:** 1st amplifier leakage test with a Q=3/4 sequence [1 1 1 1 1 1 -1] (nº1 in Table I)
- **Test 3:** 1st amplifier leakage test with a Q=2/3 sequence [1 1 0] (nº2 in Table I)
- **Test 4:** 2nd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (nº3 in Table I)
- **Test 5:** 2nd amplifier leakage test with a Q=3/4 sequence [1 1 1 1 1 1 -1] (nº3 in Table I)
- **Test 6:** 2nd amplifier leakage test with a Q=2/3 sequence [1 1 0] (nº5 in Table I)
- **Test 7:** 2nd amplifier leakage test with a Q=4/5 sequence [1 1 1 1 0] (nº5 in Table I)
- **Test 8:** 3rd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (nº7 in Table I)
- **Test 9:** 1st integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (nº10 in Table I)
- **Test 10:** 1st integrator settling error test with a pseudorandom sequence (nº11 in Table I)
- **Test 11:** 1st integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (nº12 in Table I)
- **Test 12:** 2nd integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (nº10 in Table I)
- **Test 13:** 2nd integrator settling error test with a pseudorandom sequence (nº11 in Table I)
- **Test 14:** 2nd integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (nº12 in Table I)

- **Test 15:** 3rd integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (nº10 in Table I)
- **Test 16:** 3rd integrator settling error test with a pseudorandom sequence (nº11 in Table I)
- **Test 17:** 3rd integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (nº12 in Table I)
- **Test 18:** 2nd amplifier leakage test (nº4 in Table I), combining the results from test 4 and test 5
- **Test 19:** 2nd amplifier leakage test (nº6 in Table I), combining the results from test 6 and test 7
- **Test 20:** DC gain non-linearity of the 1st amplifier (nº8 in Table I), combining the results from test 1 and test 2
- **Test 21:** DC gain non-linearity of the 1st amplifier (nº9 in Table I), combining the results from test 1 and test 2

Apart from these tests, a functional test is also applied that consists of measuring the ENOB obtained for a half-scale input sine-wave.

The next thing to be done is to select the number of points of the acquisition for each one of the proposed tests together with the pass-fail limit. In order to select these two related parameters, two different criteria can be followed: The defect-oriented criteria and the performance-oriented criteria.

5 • 4 . 2 . 1 Defect-oriented criteria

The defect-oriented approach relies on the fact that the manufactured modulators should always fit within the bounds defined by process corners. In that sense, anything outside normal process variation should be considered as a defect. This can seem severe because some of these defects may not cause any significant performance degradation. However, two things must be pointed out. If a parameter is outside the process corners it means that something has gone wrong and this is a potential reliability issue. Furthermore, for a mature man-

ufacturing process the yield should be high, which means that the probability of such small deviations is reduced. In that sense, what could be considered as yield escapes from a performance viewpoint should remain limited.

In order to design the tests with the defect-oriented criteria, the number of points and the pass/fail limit should be taken such that the signature for the worst-case parameter within the nominal range should be above the associated confidence interval.

Let us take an example. We want to test the leakage of the first integrator with an input sequence of mean value Q=1/5. According to what was said in the previous chapter, and taking into account the fact that the first stage of the modulator does not lead to an ideal 2nd order function, the signature of the leakage test should be (refer to Eq (4-49))

$$s = 6NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}} \approx \frac{6}{5}N\Delta p_1 \pm 5 \qquad \textbf{(5-64)}$$

Taking into account the fact that integrator leakage, in our behavioural model, is related to the amplifier DC gain in the form

$$\Delta p = \frac{1+b}{A_{DC}}, \qquad \textbf{(5-65)}$$

the number of samples required to get a signature above 6 (more than the uncertainty) for the lowest nominal DC gain (i.e. 65dB) is,

$$N = \frac{6}{6Q} \times \frac{A_{DC_{1min}}}{1+b_1} = 7114 \qquad \textbf{(5-66)}$$

In this case, the test pass/fail limit should be set to 6+5=11 such that no modulator within the nominal range can be discarded by the test. However, the test designer may require a more selective test. Indeed, due to the +/- 5 uncertainty on the signature, an amplifier with a gain of only 57dB may pass the test. Indeed, we have

$$s = 6NQ\Delta p_{bad} - 5 = 6 \times 7114 \times \frac{1}{5} \times \frac{1+\frac{1}{4}}{10^{(57/20)}} - 5 \approx 10\,. \qquad \textbf{(5-67)}$$

In our case, we opted to perform the test over 24000 points in order to get more precision. The new test limit is then, for the worst-case DC gain in the nominal range,

$$lim = 6NQ\Delta p + 5 = 6 \times 24000 \times \frac{1}{5} \times \frac{1+\frac{1}{4}}{10^{(65/20)}} + 5 \approx 24 \quad \textbf{(5-68)}$$

With this new limit we can calculate simply that only an amplifier with a gain above 62dB may pass the test.

The number of samples and nominal pass-fail limits for each test could be calculated analytically as described above. However, we have seen that it is not possible to derive a closed analytical expression for the test of the non-linear DC gain of the 1st amplifier. To circumvent this issue, we applied the test flow to several modulators within the nominal range with a number of acquired samples deliberately large for each test. With the results in hand, it is possible to scale down the number of points in the same proportion as the signature. For instance, if a signature of 200 is obtained for an acquisition over 100000 points, the test could be performed over 10000 points to obtain a signature of 20 that would be sufficient for test purposes.

Criteria other than the measurement precision also influence the choice of the number of samples. For instance, as was proposed in Eq (4-115), the non-linearity of the DC gain could be tested as the scaled difference between leakage signatures for two different input mean values. As was proposed, this scaling can be performed at no cost whenever since

$$N_1 Q_1 = N_2 Q_2 \quad \textbf{(5-69)}$$

Similarly, in the case of the leakage test for a first order modulator, we proposed in Eq (4-87) to combine the results obtained from two different sequences to obtain a signature whose linearity would not be affected by an input referred offset. This signature requires that the acquisitions realized with the different sequences be performed on the same number of samples.

The selected number of points and test limits can be found in Table III.

5 • 4 . 2 . 2 Performance-oriented criteria

Even if it may or may not be significant in a real manufacturing procees (such concern is beyond the scope of this thesis), the defect-oriented criteria do sacrifice functional yield for reliability. Indeed, some functionally correct modulators may be discarded because some of

their behavioural parameters are outside of the nominal expected range but still within the valid design space. This is possible because guard-bands were taken for the choice of the nominal parameters. Such a deviation is a potential reliability issue but at the time of the test it gives a good performance. Some would thus argue that discarding these modulators is losing yield and thus money.

It is possible to change the focus of the test proposal in order to obtain more performance-oriented results. Indeed, the number of points and the test limits may be chosen according to the valid design space instead of the nominal variation range.

For our purpose, we decided to keep the same number of points for each test and only to relax the test limits according to the performance-oriented criteria. In that way the results of the test set simulation, as will be seen further, can be processed simply for the two criteria by comparing the obtained set of signatures to either set of limits.

In order to determine the performance-oriented signatures we considered from the 1000 simulated modulators only the subset of those that have an ENOB higher than 15bits. The maximum signatures obtained for this subset are taken as new performance-oriented test limits. These test limits are also quoted in Table III.

Table III: Test limits

Test	Number of acquired points	Defect-oriented Test limit	Performance-oriented Test limit
1	24000	24	82
2	9600	26	86
3	100000	286	1104
4	19200	46	9802
5	19200	44	12802
6	18000	26	54
7	18000	28	74
8	1200	29	1600
9	100000	$2.3\ 10^{-4}$	0.016

Table III: Test limits

Test	Number of acquired points	Defect-oriented Test limit	Performance-oriented Test limit
10	100000	16	798
11	100000	$2.8\ 10^{-4}$	0.014
12	100000	$7.1\ 10^{-4}$	0.15
13	100000	32	7270
14	100000	4.8 10-4	0.14
15	10000	0.11	19992
16	10000	492	19998
17	10000	0.11	2.3
18	/	12	192
19	/	6	10
20	/	1.25	3.8
21	/	4	62

The last four lines in Table III do not show the number of points because these tests re-use the results obtained for other acquisition. Similarly, the number of points for test 3 is unusually large because such an acquisition with a [1 1 0] sequence at half the clock frequency is also necessary for test 11.

5 • 4 . 2 . 3 Comments on the optimization of the test limits

Relaxing the test limits on all the parameters at a time clearly opens the door to test escapes. Indeed, the performance-oriented limits are set to the maximum value reached by the signatures for the set of good-performing modulators. This is equivalent to considering the impact of the different parameters on performance individually, which is a best-case approach. Let us take a simple example. Consider that a given modulator with a first amplifier DC gain of 60dB reaches 15 bits and another modulator with a 2^{nd} amplifier slew-rate of 3 also reach 15 bits. This does not imply that a modulator with both a first amplifier DC gain of 60dB and a 2^{nd} amplifier slew-rate of 3 both reach 15bits.

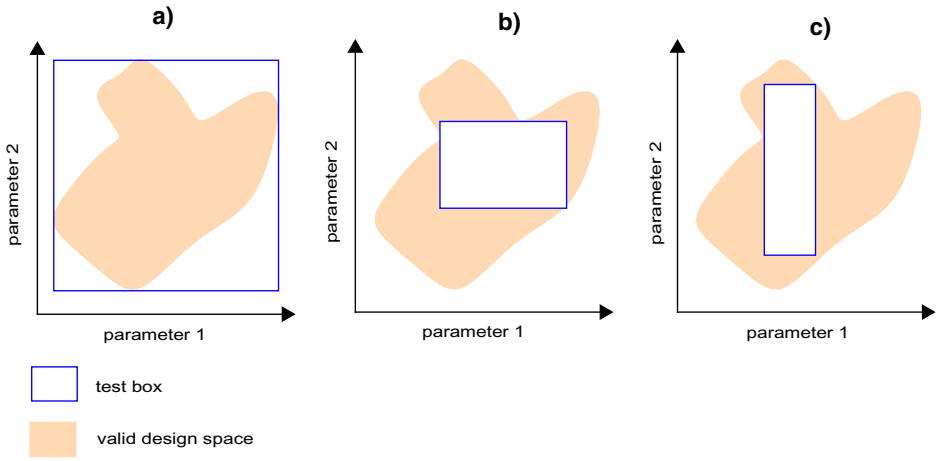


Figure 5-23: Test box versus valid design space
a) the test box contains the valid design space
b) and c) the test box is contained in the valid design space

To be rigorous, some correlations should be introduced between the signatures to make the final pass-fail decision. These correlations would intend to match the surface of the valid design space in the behavioural parameters space. Such correlation could be determined as proposed in [92] but this would definitely complicate the approach.

We do not have this problem with the test based on the nominal limits. The reason is that the parameters'nominal variations can be seen as a small n-dimensional perturbation box around the nominal design point, with n being the number of behavioural parameters. Due to the design guard-bands, it can be assumed that this box fits entirely within the valid design space.

Following the same image, the way we have selected the performance-oriented test limits is equivalent to selecting the smallest box that contains the valid design space. A better solution would consists of finding the largest box that fits within the design space, minimizing the number of poor performers that pass the test, while also minimizing the number of good performers that fail the test. Unfortunately, there is not an obvious solution to this problem. As a matter of fact, Figure 5-23 displays a small diagram that helps understand that such a solution is not unique.

Depending on the application, there may be a trade-off between test escapes and functional modulators overkill. A interesting path for further research would be to study the optimization of the pass-fail limit for all the parameters.

5 • 4 . 3 Test flow selection

As was said previously, some of the tests introduced above are redundant because they target the same behavioural parameters. Alternative tests were introduced to offer more flexibility to the test designers mainly in terms of implementation. Hence, we will consider several test flows.

5 • 4 . 3 . 1 The complete test flow

One of the objective of fault simulation is to verify how the proposed test set behaves when more than one parameter is varied at a time. Hence, we will primarily consider the behaviour of the set of 21 tests proposed above.

5 • 4 . 3 . 2 Test flow with no analog 0s

Some of the proposed tests require the introduction of analog 0s in the test sequence. This implies a modification of the DAC to implement this capability and requires that the test sequence is defined by two bits. If such a modification is not desired, a test flow can be considered that target all the proposed parameters but with purely digital sequences:

- **Test 1:** 1st amplifier leakage test with a Q=1/5 sequence [1 -1 1 -1 1] (n°1 in Table I)
- **Test 2:** 1st amplifier leakage test with a Q=3/4 sequence [1 1 1 1 1 1 -1] (n°1 in Table I)
- **Test 4:** 2nd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (n°3 in Table I)
- **Test 8:** 3rd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (n°7 in Table I)
- **Test 9:** 1st integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (n°10 in Table I)

- **Test 12:** 2nd integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (n°10 in Table I)
- **Test 15:** 3rd integrator settling error test with a deterministic sequence [1 1 -1 1 -1 -1] (n°10 in Table I)
- **Test 20:** DC gain non-linearity of the 1st amplifier (n°8 in Table I), combining the results from test 1 and test 2

5 • 4 . 3 . 3 Test flow with simple counter signatures

Some tests require the computation of "complex" signatures that need a divider. This may not be practical for full-BIST on-chip implementation. Hence, we will also consider a test flow that does not require such divisions:

- **Test 1:** 1st amplifier leakage test with a Q=1/5 sequence [1 -1 1 -1 1] (n°1 in Table I)
- **Test 2:** 1st amplifier leakage test with a Q=3/4 sequence [1 1 1 1 1 1 -1] (n°1 in Table I)
- **Test 4:** 2nd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (n°3 in Table I)
- **Test 8:** 3rd amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (n°7 in Table I)
- **Test 10:** 1st integrator settling error test with a pseudorandom sequence (n°11 in Table I)
- **Test 13:** 2nd integrator settling error test with a pseudorandom sequence (n°11 in Table I)
- **Test 16:** 3rd integrator settling error test with a pseudorandom sequence (n°11 in Table I)
- **Test 21:** DC gain non-linearity of the 1st amplifier (n°9 in Table I), combining the results from test 1 and test 2

5 • 4 . 3 . 4 Test flow with no input-dependent clocking

The overall settling error tests that have been proposed require that the reference clock of the modulator be modified as a function of the input sample. Indeed, the reference clock period should be doubled for the 1 input samples (alternatively the -1s). We will show in the next chapter how this can be done on-chip at a reasonable cost but in any case, the designer may want to avoid such modification. The following test set substitutes the non-linear settling error tests by the overall settling error tests. As those tests require sequences with analog 0s, the leakage test that makes use of analog 0s has also been preferred for the 2^{nd} integrator. This avoids the introduction of an extra delay in the feedback loop. The test flow is as follows:

- **Test 1:** 1^{st} amplifier leakage test with a Q=1/5 sequence [1 -1 1 -1 1] (n°1 in Table I)
- **Test 2:** 1^{st} amplifier leakage test with a Q=3/4 sequence [1 1 1 1 1 1 -1] (n°1 in Table I)
- **Test 6:** 2^{nd} amplifier leakage test with a Q=2/3 sequence [1 1 0] (n°5 in Table I)
- **Test 8:** 3^{rd} amplifier leakage test with a Q=2/3 sequence [1 1 1 1 1 -1] (n°7 in Table I)
- **Test 11:** 1^{st} integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (n°12 in Table I)
- **Test 14:** 2^{nd} integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (n°12 in Table I)
- **Test 17:** 3^{rd} integrator non-linear settling error test with a Q=2/3 sequence [1 1 0] (n°12 in Table I)
- **Test 21:** DC gain non-linearity of the 1^{st} amplifier (n°9 in Table I), combining the results from test 1 and test 2

5 • 4 . 3 . 5 Comments on test flow optimization

Similar to what was said for the selection of the test limits, it would be interesting to study the optimization of the test flow. A rigorous approach to test flow optimization is a Ph.D. subject in itself [93]. Moreover, optimization must be done with respect to a given cost

function that has to be minimized. The construction of the cost function is not necessarily straightforward. Test metrics such as test escapes and yield loss should be considered, as well as the test resources requirements, the test time, etc.

As an example, a simple algorithm such as the one depicted in Figure 5-24 may be used. However, such an algorithm cannot be carried out during the design phase because it would require a prohibitive number of realistic fault simulations. It would make more sense to implement such an optimization algorithm for the production line.

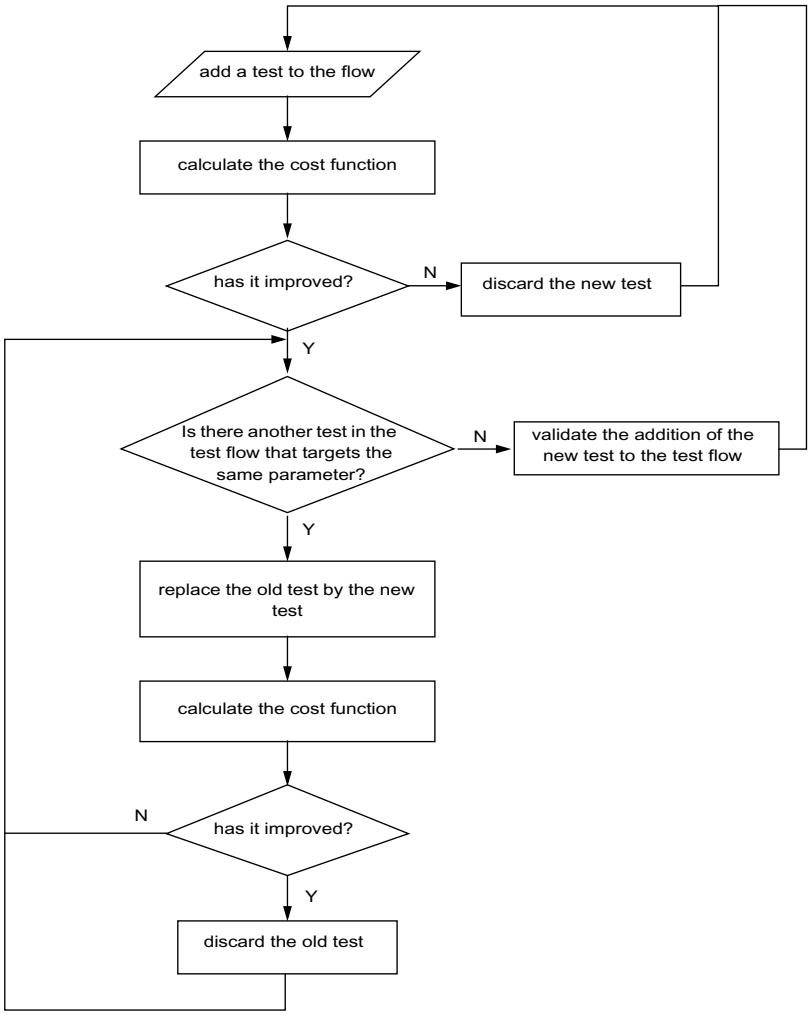


Figure 5-24: Ad-hoc test flow optimization algorithm

5 • 4 . 4 Fault simulation

5 • 4 . 4 . 1 Definition of the simulation

In many design flows, Monte-Carlo simulation is performed to evaluate the impact of mismatch and/or process variations on a circuit. For such simulation, statistics have to be provided by the foundry that reasonably match the distribution of the parameters measured in a production environment. However, what we propose is not to make a realistic Monte-Carlo simulation. Indeed, this would make little sense as it would be realistic only for a given implementation. In turn, we will define a kind of Monte-Carlo simulation at behavioral level and see how the proposed test set behaves.

It would be possible to vary all the behavioural parameters independently and over a broad range, like we did for exploring the design space. However, such an option would lead to a wide majority of the modulators having more than one parameter outside their nominal range. Our behavioural model of the modulator is defined by 26 behavioural parameters in total. Assuming that we define a broad variation range for each parameter and that the nominal range represents 50% of this range, the probability to obtain a nominal modulator would be

$$P = 0.5^{26} = 1.5 \times 10^{-8}. \quad \textbf{(5-70)}$$

Instead, we opted to define an ad-hoc fault list, associating a probability of occurrence to each fault. For that, as was seen in Table II, three variation ranges have been defined for each behavioural parameter.

It is neither possible nor desirable to make a realistic fault simulation at a behavioural level. It is not possible because a realistic fault simulation would require one to extract fault classes and statistics from layout level tools or silicon failure analysis. Furthermore, it is not desirable for our purpose because realistic faults may not cover all the cases that we want to study. Indeed, in a realistic manufacturing process, it is likely that the yield may be quite high. This means that the parameters of the large majority of the modulators are within their nominal variation range. A number of modulators would also present catastrophic defects (like opens and shorts) that would be easily detected by the proposed test set but also by a

relaxed functional test. For our validation purpose, we concentrate mostly on those modulators that present parametric failures. For that, we defined four equally-probable categories:

- Nominal: All the parameters are selected within the nominal range.
- Global parametric drift: One or more parameters of the three integrators are selected in the parametric range. For instance, the three DC gains, the three slew-rates or the three pairs clipping-value/DC gain non-linearity. The rest of the behavioural parameters are selected in the nominal range. A total of 9 equally-probable combinations were considered.
- Local parametric drift: One or more parameters of one of the three integrators are selected in the parametric range. The rest of the behavioural parameters are selected in the nominal range. A total of 36 equally-probable combinations were considered (around 12 for each amplifier).
- Drastic drift: One or more parameters of one of the three integrators are selected in the drastic variation range. The rest of the behavioural parameters are selected in the nominal range. A total of 42 equally-probable combinations were considered.

One thousand modulators were simulated in a MonteCarlo way, randomly selecting one category and then one fault type within this category.

5 • 4 . 4 . 2 Test metrics

Let us clarify the different metrics that we will use to illustrate the test results. First of all, we define defect-oriented metrics. For this, take a look at Figure 5-25.

- **The test escapes ratio** is defined as the number of defective modulators that are targeted by the test set and that unexpectedly pass the test over the total number of defective modulators that are targeted by the test set.

$$\frac{N_5}{N_1 + N_5}. \tag{5-71}$$

- **The total test escapes ratio** is defined as the number of defective modulators that pass the test (both expectedly and unexpectedly) over the number of defective modulators.

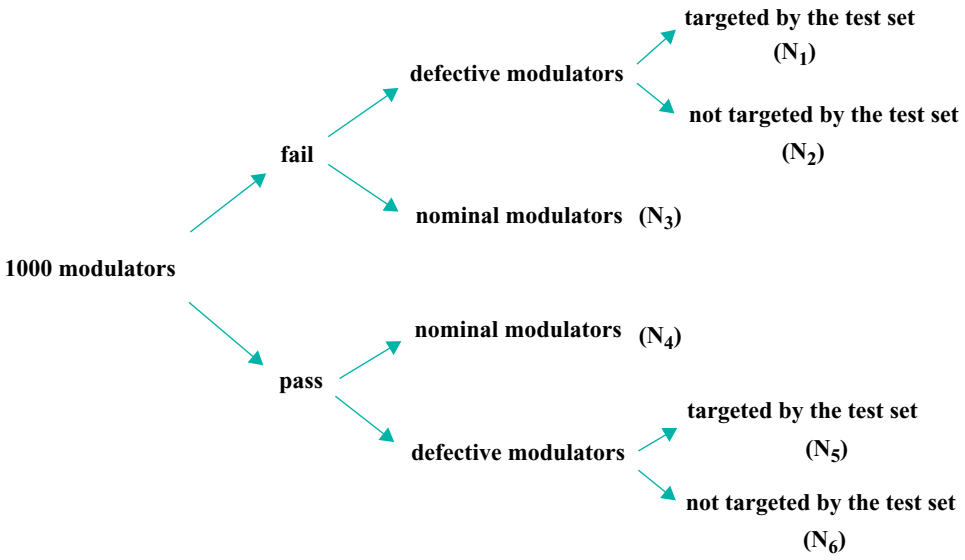


Figure 5-25: Diagram of the test results partitioning.

$$\frac{N_5 + N_6}{N_1 + N_2 + N_5 + N_6}. \tag{5-72}$$

- **The yield escapes ratio** is defined as the number of nominal modulators that fail the test over the number of nominal modulators.

$$\frac{N_3}{N_3 + N_4}. \tag{5-73}$$

- **The test added value** is defined as the number of defective modulators that are not targeted by the test set and that unexpectedly fail the test over the total number of defective modulators that are not targeted by the test set.

$$\frac{N_2}{N_2 + N_6}. \tag{5-74}$$

Similarly, we define two performance-oriented metrics:

- **The good performers rejection ratio** is defined as the number of modulators with more than 15 effective bits that fail the test over the total number of modulators with more than 15 effective bits.

- **The poor performers acceptation ratio** is defined as the number of modulators with less than 15 effective bits that pass the test over the total number of modulators with less than 15 effective bits.

Notice that the values obtained for these metrics should not be used to extrapolate quantitative conclusions because the probabilities of occurence of the different defects are arbitrary and not realistic. Nevertheless, our purpose is to uncover interesting qualitative trends.

5 • 4 . 4 . 3 Results for the complete test flow with the defect-oriented criteria

After applying the 21 tests to the 1000 modulators with the test limits proposed in the second column of Table III, a number of 450 modulators have passed the test set and 550 have failed. Figure 5-26 shows the histogram of the ENOB obtained for the 1000 modulators together with the histogram of the ENOB of the modulators that have passed the test set.

Two conclusions can be drawn from this graph. The most striking is possibly that many good performers have been discarded by the proposed test set. The good performers rejection ratio is of 28%. Another is that all bad performers have been discarded and few poor

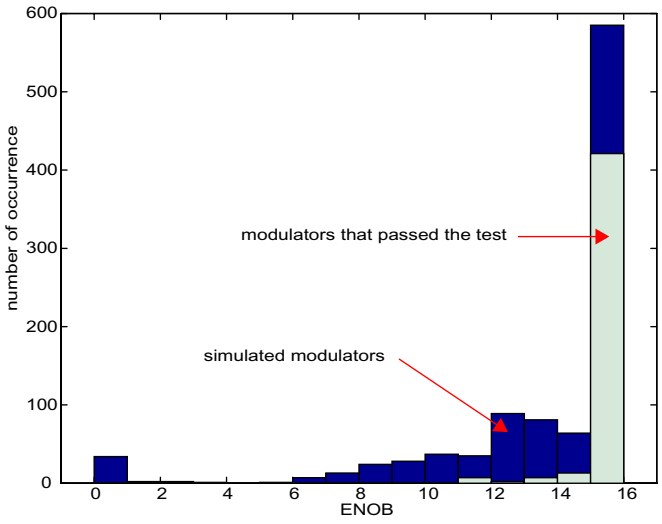


Figure 5-26: Histograms of the ENOB obtained for the 1000 simulated modulators and for the subset of the modulators that passed the test set

performers have been accepted: 13 in the 14bit bin (i.e. 14<ENOB<15), 7in the 13bit bin, 2 in the 12bit bin and 7 in the 11bit bin. The poor-performers acceptation ratio is of 6.9%.

These effects can easily be explained by the fact that we are looking at a defect-oriented test through the prism of a functional gradation. The histogram of the ENOB is a functional measurement so Figure 5-26 implicitly pre-suppose a correlation between the results of the test proposal and the results of the functional test. This correlation obviously exists but is not total.

Many good performers have been discarded because they actually present a parametric drift that is higher than what was expected for a nominal variation. In other words these parts are defective. Nevertheless, defective parts even with strong parametric deviations may still be in the design-space of valid modulators, as was explained above. This is specially true if large design guard-bands had been taken. Notice that the large number of good performers that have been discarded may not be realistic: the fault simulation that we have performed has generated a fairly large number of modulators with small parametric drifts. More concretely, only 6% of the modulators with more than 15 effective bits that have failed the test correspond to modulators that exhibit a drift in the first integrator. This is not surprising as it is well known that the errors introduced in the integrators located further in the loop are partially shaped to high frequencies. As a result, the first integrator has the highest requirements while further integrators are more relaxed and are thus very likely designed with large guard-bands. 29% of the modulators with more than 15 effective bits that have failed the test correspond to modulators that present amplifier(s) DC gain non-linearity higher than the nominal. Once again, it can be said that the nominal range for this parameter was designed with a lot of margin.

On the other hand, the poor performers that have been accepted correspond to parameter deviations that are not contemplated by our proposal. More concretely, 5 of the 21 poor performers that have passed the test are modulators that present deviations in the integrator branch coefficients. The rest corresponds to excess thermal noise in the amplifiers.

If we want to evaluate the test set results with more defect-oriented metrics, we can say several things.

First of all, it can be verified that none of the nominal modulators has been discarded. The yield escapes ratio is 0. This is of utmost importance because it means that the test set does not impact the yield.

If only the subset of faults that are targeted by the proposed test set is considered, it can be seen that the test set detected 93.7% of the faults. The remaining 6.3% of test escapes ratio correspond to parametric drifts of the first amplifier DC gain non-linearity. Moreover these drifts do not significantly impact performance because the ENOB obtained for the modulators that correspond to these 6.3% is greater than 15bits. This means that the proposed tests are not accurate enough to detect such small variations. One solution could be to perform the tests over a larger number of samples. To verify this assumption, one of the test-escape modulators was re-simulated performing test 1 and test 2 with ten times more points (240000 and 64000 respectively). The signature obtained for test 21 (calculated from the results of test 1 and 2) is 18 while the same signature computed for a nominal modulator leads to a result of 7. Hence, it can be concluded that the test for DC gain non-linearity should have been performed over a larger number of points in order to detect small parametric deviations outside the nominal range.

Hence, it can be concluded that the test performs as expected even when several parameters are varied at a time.

Some defects that were not targeted by the test set are also detected. It is legitimate to think that the proposed digital tests, that rely on the proper functioning of ΣΔ modulation, are likely to detect catastrophic faults even if they are not directly caused by one of the parameters that are targeted. As a matter of fact, it can be seen in Figure 5-26 that the test set discarded all the faulty modulators with an ENOB below 11 bits. Among these discarded modulators, some correspond to faults that were not expected to be detected. To be more precise, 22.4% of the faults that were not directly targeted by the test set have been detected (i.e. the test added value ratio is 22.4%). 80% of these 22.4% correspond, as expected, to drastic variation of some parameters (mainly branch coefficients, noise figures and 2^{nd} and 3^{rd} amplifier clipping value) and 20% correspond to parametric variations.

5 • 4 . 4 . 4 Results for the complete test flow with the performance-oriented criteria

For the performance oriented criteria, the obtained signatures are compared with the limits of the 3rd column of Table III. From these limits, it can already be said that the third integrator settling does not influence in a large extent the performance of the overall modulator. Indeed, the functional limits for tests 15, 16, 17 are very high and practically all the modulators will pass such tests.

Figure 5-27 is the same as Figure 5-26 but for the results obtained with the performance-oriented test limits. It can be seen how no good performers have been discarded with the new test limits (i.e. the good performers rejection ratio is 0). On the other hand, the number of poor performers that pass the test is significantly increased: 34 instead of 13 in the 14bit bin (i.e. 14<ENOB<15), 22 instead of 7 in the 13bit bin, 43 instead of 2 in the 12bit bin and 7 in the 11bit bin. The poor performers acceptation ratio has increased to 25.3%. 63% of these poor performers correspond to parameters that were explicitly targeted by the proposed tests. This observation must be related to the way in which we selected the test limits for the performance-oriented criteria. Indeed these test limits were set to the maximum signature obtained for modulators with an ENOB higher than 15bits, which corresponds to case

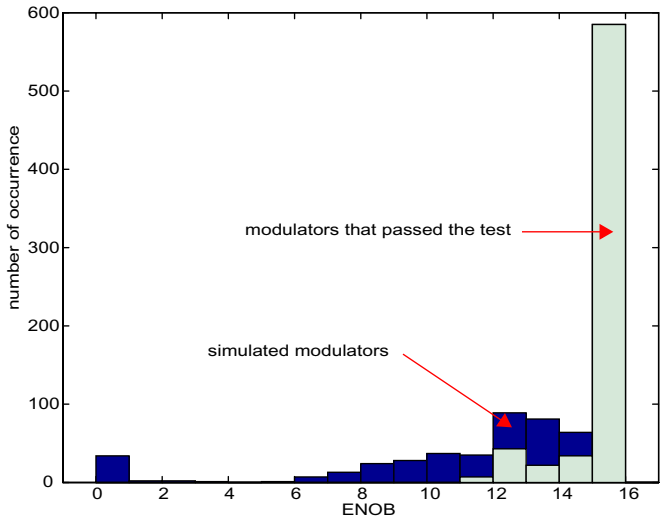


Figure 5-27: Histograms of the ENOB obtained for the 1000 simulated modulators and for the subset of the modulators that passed the test set with performance-oriented limits

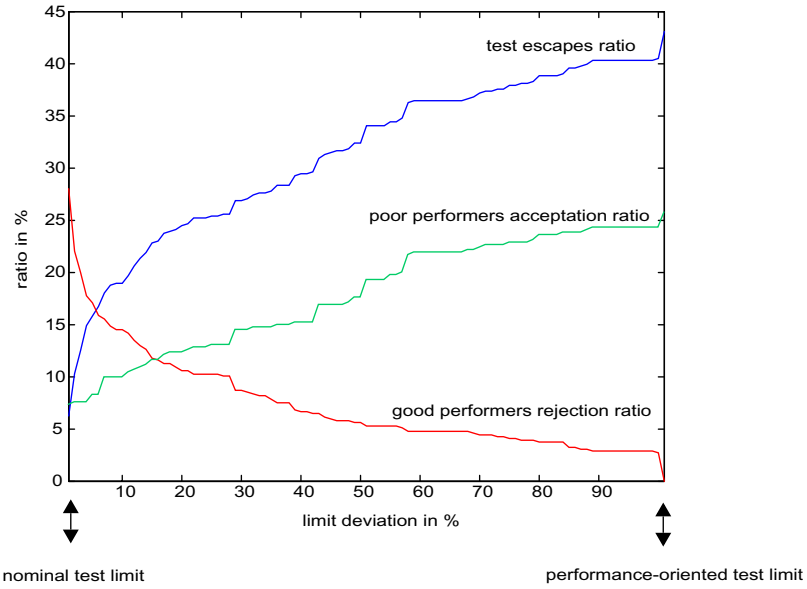


Figure 5-28: Evolution of two test metrics as function of the test limits:
- the test escapes ratio
- the good performers rejection ratio

a) in Figure 5-23. Moreover the relationship between a given parameter and the performance may not be monotonous. For instance, a modulator with an amplifier of GBW=2 may give an ENOB of 15.5 bits while another with a GBW=3, which is in principle better, may give an ENOB of 14.6dB. If we set the settling error test limit to admit the first modulator it is likely that the second one will also pass the test.

As was said in section 5 • 4 . 2 . 3, it may be more judicious to select the test limits at an intermediate point between the defect-oriented criteria and the performance-oriented criteria. As an illustration of this concern, Figure 5-28 represents the evolution of the test escapes ratio, the good performers rejection ratio and the poor performers acceptation ratio as a function of the test limit. For all the parameters a relative deviation between the defect-oriented limit and the performance oriented limit was considered. The choice of an optimum point depends on the application-related cost function.

5 • 4 . 4 . 5 Results for the other test flows

We also applied the reduced test flows proposed in section 5 • 4 . 3 to the 1000 simulated modulators. Table IV gives a summary of the metrics obtained for the different test flows with the two criteria for the test limits (defect-oriented and performance-oriented).

First of all, it is important to note that the figures in the table must be considered taking into account the type of fault simulation that has been carried out. The test escapes ratio can seem unusually large with the performance oriented criteria, but this is because many defective devices are actually good performers. Similarly, the number of poor performers accepted is also fairly large because the fault simulation was designed to produce many parametric faults. Particularly relevant is the fact that none of the test flows discards nominal modulators.

In the same column that gives the test escapes ratio we have quoted the minimum and the average ENOB of the modulators that correspond to these test escapes. The same has been done in the column that gives the poor performers acceptation ratio. Notice that these figures do not have the same meaning

The poor performers that passed the test include modulators that have defects that are not explicitly targeted by the proposed tests. What we intend to show is that the different test sets are able to detect all the catastrophic failures, even if they do not correspond to a targeted parameter. This is possible because all the proposed tests rely on a proper functioning of the ΣΔ modulation. Indeed, it can be seen that for all the test sets with the defect-oriented criteria, the worst modulator that passed the test has an ENOB of 11.2bits and the average ENOB of these poor performers is 13.5bits.

The test escapes correspond to modulators that could have been detected by the test set because they exhibit a deviation in one of the targeted parameters. Hence, what we indirectly intend to show with the associated ENOB figures is that these modulators have not been detected because the deviations are small and have little impact on the modulator. As a matter of fact, it can be seen that, for all but one of the proposed test flows with the defect-oriented criteria, the test escapes correspond to good performers. This means that these undetected defects are defects that effectively stand within the design guard-bands. These defects may possibly be detected by increasing the precision of the related tests (i.e. the

number of acquired points). This assumption has been verified in a particular case in section 5 • 4 . 4 . 3, for a defect that affected the DC gain non-linearity of the 1st amplifier.

For the test flow with no input-dependent clock modification, though, one of the test escapes has an ENOB of 12.9bits. A detailed scrutiny of the results show that this modulator has a drastic variation in the GBW of the 2nd amplifier. In principle, such a defect should be detected by the settling error test of the 2nd amplifier. However, as the test flow does not make use of input-dependent clocking, the selected settling error test was test 14 (n°12 in Table I). This test target the non-linear part of the settling error and is thus not totally equivalent to the overall settling error test. In the majority of cases, a defect in the amplifier settling is very likely to cause a non-linear settling error. However, for this particular test escape, the defect only affected the GBW while maintaining a high Slew-rate. As a result, the settling error is mostly linear even if it is much slower than nominal (see Eq (5-2)). Hence, we can say that this particular test escape could be expected. The rest of the test escapes for this test flow all have an ENOB above 15bits, like the other test flows.

From the rest of the figures given in the table, we can conclude that all the test flows perform in a similar way. This demonstrates that the different test proposals for a given parameter are self-consistent.

Table IV: Summary of test flow results

test limits	test flow	yield escapes ratio	total test escapes ratio	test escapes ratio min(ENOB) / mean(ENOB)	test added value ratio	good performers rejection ratio	poor performer acceptation ratio min(ENOB) / mean(ENOB)
nominal	complete	0%	25.2%	6.3% 15.1 / 15.4	22.4%	28%	6.9% 11.2 / 13.5
nominal	no analog 0s	0%	28.3%	9.6% 15.1 / 15.4	19.9%	24.3%	7.2% 11.2 / 13.5
nominal	simple signatures	0%	28.1%	9.4% 15.1 / 15.4	19.9%	24.6%	7.4% 11.2 / 13.5
nominal	no input-dependent clocking	0%	26.3%	6.6% 12.9 / 15.4	19.4%	27%	7.4% 11.2 / 13.5
perf.	complete	0%	57.8%	43.1% 12.3 / 14.8	1.5%	0%	25.3% 11.2 / 13.4
perf.	no analog 0s	0%	65%	52.9% 8.2 / 14.4	1.5%	0%	38% 8.2 / 13.1
perf.	simple signatures	0%	65%	52.9% 8.2 / 14.4	1.5%	0%	38% 8.2 / 13.1
perf.	no input-dependent clocking	0%	58.6%	44.2% 12.3 / 14.8	1.5%	0%	26.8% 11.2 / 13.4

6

PRACTICAL IMPLEMENTATION CONCERNS

In many cases, Design-for-Testability proposals that can be found in the literature put much emphasis on their high fault coverage or on the accuracy of their performance measurements. Others also focus on test time reduction. However, a very important aspect that is sometimes overlooked is that of practical implementation. Moreover, many techniques that claim to be BIST schemes are indeed only partial BIST in the sense that only data processing or test stimulus generation is carried out on-chip. In other cases, the implementation is technically possible but the extra area dedicated to test hardware is larger than the circuit under test. Finally, some proposals do not consider how sensitive the test hardware could be to defects and how this could impact yield

This chapter will thus address practical concerns with respect to the tests proposed in the two previous chapters. Despite the fact that implementation is often considered as secondary in many proposals, it is precisely in that aspect that our proposal unveils most of its potential. Indeed, we will show how both test stimulus generation and test data analysis can be

carried out on-chip with robust and low-cost circuitry. However, we do not pretend to provide a unique solution because the optimum implementation will always depend on the architecture and the application. Instead, we will sketch general guidelines for the most critical points.

6 • 1 THE TEST STIMULUS

The proposed test stimuli are digital sequences that are then converted to analog by either re-using or replicating the feedback DAC (possibly with some modification) as will be seen later. The analog sequence seen by the modulator under test are thus two-valued and they are either periodic (with a short period) or pseudo-random. In any cases they remain within the modulator full-scale.

6 • 1 . 1 Stability considerations

The first consideration that should be made with respect to the use of a test stimulus concerns the stability of the modulators. ΣΔ modulators are designed to process slowly varying inputs and most stability studies have been performed assuming DC inputs. It is far from straightforward to determine how a modulator behaves when submitted to a digital sequence.

As our tests apply only to 1^{st} and 2^{nd} order modulators, stability concerns are indeed much relaxed. Modulators of 1^{st} order are known to be unconditionally stable for any input that does not overload the modulator (i.e. for any input within the modulator's full-scale). Hence, using test sequences whose mean value remains strictly below the full-scale should be sufficient. In principle, this is equivalent to saying that anything except an "all 1" (or "all -1") sequence can be used. Nevertheless, some guard-band should be taken to accommodate an eventual input-referred offset.

Modulators of 2^{nd} order are not unconditionally stable. An example of a non-overloading input that drives a 2nd order modulator into instability is given in [24]. Fortunately, it was proven in [25] that 2^{nd} order modulators are stable for any input that can be represented as a finite sum of sine-waves. Being periodic sequences, our test stimuli can thus be repre-

sented as a Fourier series in the discrete-time domain, that is to say a finite sum of sine-waves.

There is thus no conceptual impeachment to the use of digital sequences in both 1st and 2nd order modulators. Anyway, some care should be taken with practical limitations. Stability implies that the output of the integrator(s) remains bounded, but the exact value of this bound is important in practical implementation as integrator output swing is limited. The integrator output excursion during the test mode should thus remain similar to the expected output swing under normal operation. As was said in Chapter 1, the calculation of these-bounds has concentrated much research effort even for DC inputs. We thus decided to limit our verification to simulation. There is an exception which is the case of the leakage test for 1st order single-bit modulators. Indeed, in Section 4 • 1 . 3 . 2 we have shown that the integrator output varies between -2 and 4 for a positive sequence, and between -4 and 2 for a negative sequence. Under normal operation, the output of the integrator should remain between -2 and 2 for any non-overloading input. This difference is due to the inclusion of an the additional delay in the feedback path during test mode. Notice that the alternative test proposed in Section 4 • 1 . 2 . 3 uses a 0 instead of a -1 and does not require additional delay in the feedback path. In this case, the integrator excursion during test mode is the same as during normal operation.

For the rest of the cases, it can be shown by simulation that test sequences tend to force higher internal states at the integrator output than the equivalent DC levels. As an example, Figures 6-1 and 6-2 show the maximum value reached by the first integrator output for both a DC input and a digital sequence, as a function of their mean values. The simulated modulator in Figure 6-1 is ideal and second-order with the structure proposed in [26]; it uses single branch integrators with a 0.5 gain. We will refer to it as modulator A. The simulated modulator in Figure 6-2 uses a single branch integrator with a 0.25 gain as a first integrator and a two branch integrator of gains 1/3 for the signal branch and 0.25 for the feedback branch. This modulator was proposed in [24]. We will refer to it as modulator B. This modulator does not exactly fulfill the conditions for an ideal 2nd order modulator because its coefficients have been rounded to small fractions for implementation purposes. Linearizing the

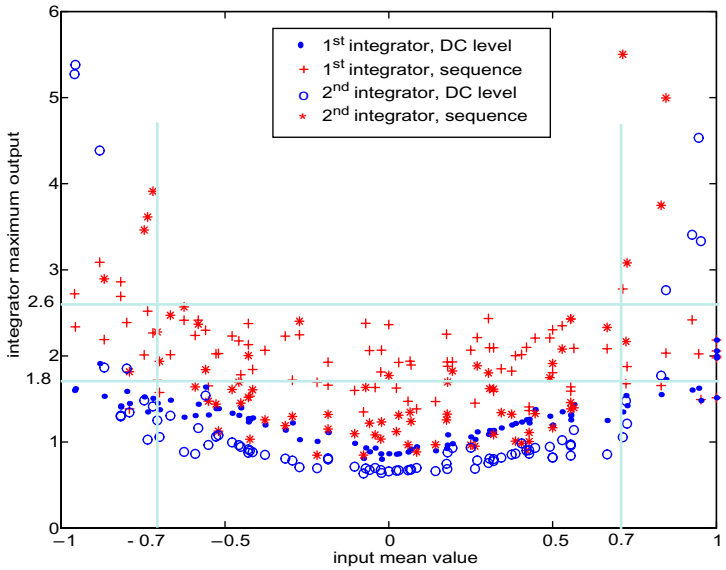


Figure 6-1: Maximum integrator outputs as a function of modulator A input

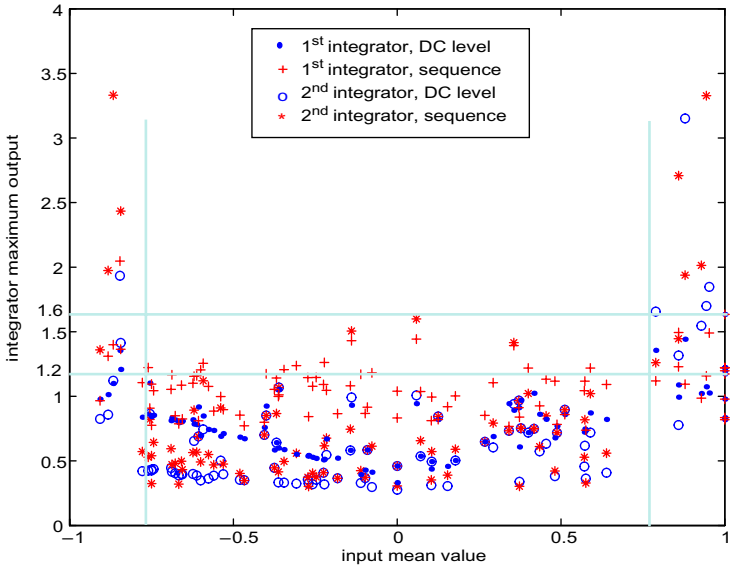


Figure 6-2: Maximum integrator outputs as a function of modulator B input

quantizer as explained in Chapter 1, the difference equation that governs the modulator can be written as

$$Y\left[(1-p_1z^{-1})(1-p_2z^{-1})+\frac{k}{12}z^{-2}+\frac{k}{4}z^{-1}(1-p_1z^{-1})\right]= \frac{k}{12}z^{-2}X+(1-p_1z^{-1})(1-p_2z^{-1})E \quad \text{(6-1)}$$

The effective gain k of the quantizer settles to about 16/3. However, the leakage signature does not depend to first order on the quantizer's effective gain. Considering that the leakage signature senses the average of the output minus the input, we have

$$s = N\times \lim_{z\to 1}(X-Y) = N\frac{\left[\Delta p_1\Delta p_2+\frac{k}{4}\Delta p_1\right]}{\Delta p_1\Delta p_2+\frac{k}{12}+\frac{k}{4}\Delta p_1}\lim_{z\to 1}(X)\approx 3NQ\Delta p_1, \quad \text{(6-2)}$$

where Q is the input sequence mean value, that is,

$$Q = \lim_{z\to 1}(X) \quad \text{(6-3)}$$

For modulator A, note that the integrator outputs reach values close to 1.8 for DC levels below 0.7. In turn, if digital sequences are used as the inputs, the integrator outputs reach values close to 2.6 (44% higher than with DC levels). For modulator B, the integrator outputs reach 1.2 for DC inputs below 0.8 while they reach 1.6 for digital sequences with mean value below 0.8 (20% higher than with DC levels).

Thus, we conclude that the use of digital sequences lead to internal states that are higher than the states reached by the modulator during normal operation in a proportion that depends on the architecture. Fortunately, several solutions can be proposed to cope with this.

6 • 1 . 1 . 1 Addressing the test requirements during design

The test of the modulator with digital sequences must be considered during the design phase and the modulator appropriately scaled for both test and normal operation. This solution is the most interesting but introduces new trade-offs in particular for the design of the first integrator (which usually is the most demanding). A straightforward solution would consist of selecting the modulator full-scale in order to accommodate properly the modulator's internal states within the amplifier's output range during test mode. Selecting a lower

full-scale has other implications than its effects during test mode: it relaxes settling and linearity requirements for the amplifier but increases the noise requirements.

During normal operation it is desired that the internal states remain within the linear range of the amplifier. However, the linearity requirements for the output range may be relaxed significantly during test mode. As the output range of the amplifier is not limited to its linear range, this extra non-linear part of the output range may be sufficient to accommodate the test-mode requirement and provide satisfactory results. It should thus be verified during the design phase if it is really necessary to modify the amplifier for test purposes.

Let us illustrate this with an example. Consider that we have in our libraries an amplifier with a 5V supply and a linear differential output range of 6V such that its DC gain at 0V is 60dB, and its DC gain at 3V (and -3V) is 57dB. In principle, during the design of the modulator, the full-scale will be chosen as large as possible such that the integrator state remains entirely in the linear part of the amplifier output range for normal operation. Taking a look at Figure 6-1, modulator A could be designed with a differential full-scale of [-1.5V; 1.5V] such that DC inputs within 70% of the full-scale do not suffer distortion. In the case of modulator B (see Figure 6-2), in turn, selecting a full-scale of [-2.5V; 2.5V] would allow to process DC inputs up to 0.8 without significant distortion. With such limits, it could be thought that tests with digital sequences could not be performed with the nominal full-scale. Nevertheless, some care has to be taken because the amplifier output range is not limited to its linear part. Actually, the amplifier mentioned above is likely to clip at the supply rail, which represents a clipping at +/-5V differential. The strong non-linearity of the amplifier characteristic above the nominal linear output range may or may not affect the results of the proposed tests and high level simulations should thus be performed to take the adequate decision.

The full-scale of modulator A is set to 3V while the full-scale of modulator B is set to 5V. Hence, normalizing the model parameters to a [-1;1] full-scale we have the parameters in Table I

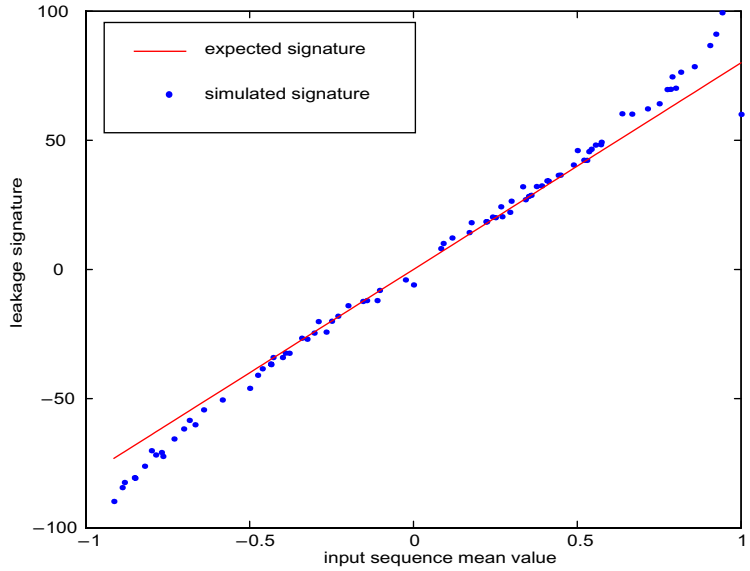


Figure 6-3: Modulator A 1st integrator leakage signature as a function of the mean value of the input sequence

Table I: normalization of the amplifier parameters

parameters	modulator A	modulator B
Full-scale	1	1
amplifier gain	60dB	60dB
Clipping value	5/1.5=3.333	5/2.5=2
DC gain non-linearity a_{NL}	2.83	1.70

Figures 6-3 and 6-4 represent the signature of the first integrator leakage test for the modulators described above. In both cases, we can see that the simulated signature is quite close to the expected one for input sequences with mean values far from the modulator full-scale. More precisely, it can be seen that the simulated signature deviates from the expected one for mean values above 0.5 for modulator A and above 0.7 for modulator B. On the other hand, this phenomenon has already been described in Chapter 4 and is actually the basis of the test for the non-linearity of the first amplifier DC gain. Hence, it can be con-

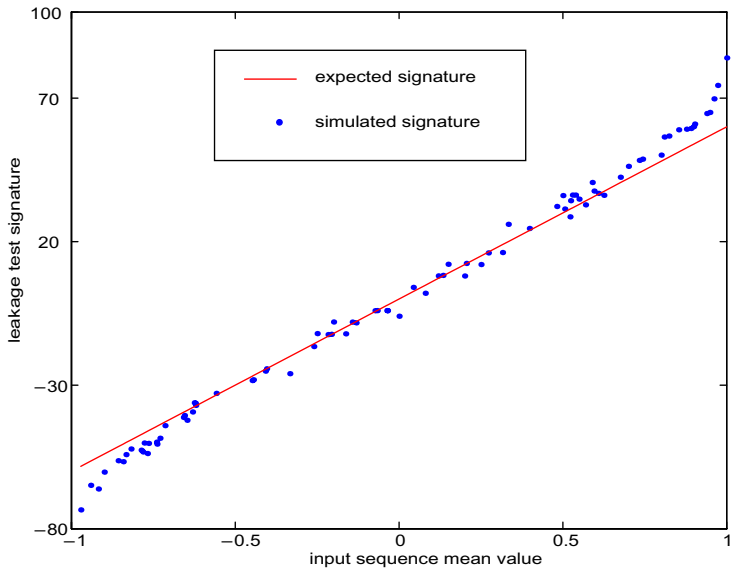


Figure 6-4: Modulator B 1st integrator leakage signature as a function of input sequence mean value

cluded that the leakage test as well as the DC gain non-linearity test could be performed for these two modulator examples without any particular modification.

Similarly, Figures 6-5 and 6-6 show the settling error signature obtained using Eq (5-13) (see test 10 in appendix A) by varying the slew-rate of the amplifier for a fixed value of the GBW. Furthermore, the test was carried out using 3 pseudorandom sequences generated by Linear Feedback Shift Registers (LFSR) of three different lengths. It can be seen that for both modulators, the measured settling error closely matches the expected one and that there is no significant difference between the 3 LFSRs (actually the results are superimposed).

6 • 1 . 1 . 2 Changing the full-scale in test mode

As was said above, a straightforward solution would be to use a smaller full-scale to accommodate the larger excursion of internal states when using digital sequences. If the resulting design trade-offs are not acceptable for normal operation, the modulator full-scale may be decreased during test only. This is an interesting solution if the voltage references are set externally. Otherwise, the impact of an on-chip voltage scaling should be evaluated.

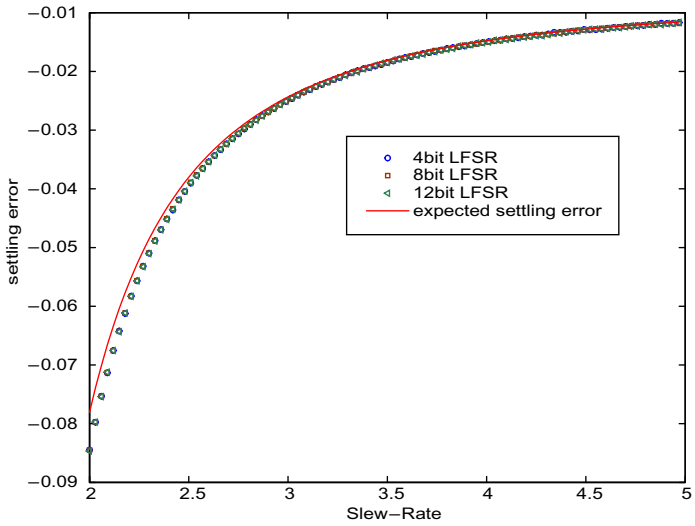


Figure 6-5: Modulator A settling error signature as a function of the 1st integrator Slew-rate.

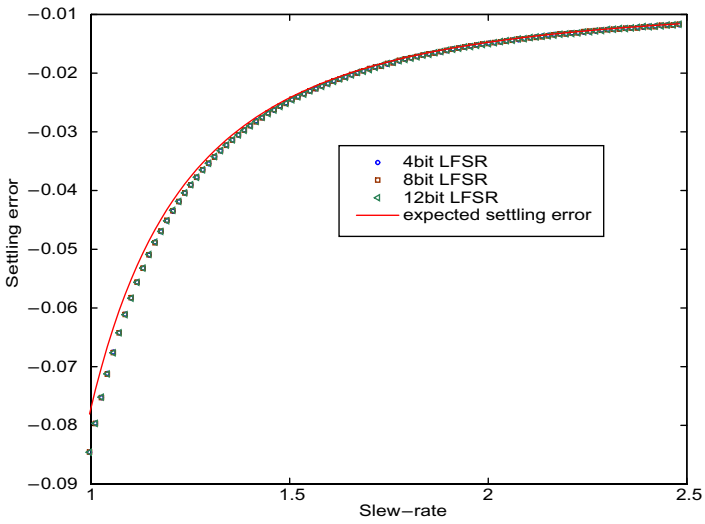


Figure 6-6: Modulator B settling error signature as a function of the 1st integrator Slew-rate.

Once again, this would make the noise contribution more significant during test mode. As the proposed tests are all based on DC measurements, this could be solved by a major averaging if necessary. Reducing modulator full-scale has no impact on the leakage tests but things are different for the DC gain non-linearity (that has much to do with the integrator output range) and the settling error. Indeed, if the full-scale is reduced the requirements on these two parameters are lower. There is thus a trade-off between test sensitivity and the value of the internal states, that can be resolved for every particular architecture through high-level simulations.

6 • 1 . 1 . 3 Coefficient scaling in test mode

Acting on the modulator coefficients also varies the internal states. Hence the modulator coefficients could be modified during test mode. This solution should obviously be contemplated during the design phase, as it would require the inclusion of extra switches to disconnect (or) some unit capacitors in test mode. How to properly modify the modulator should be studied is each case.

For instance, the modulator with 0.5 integrator gains proposed above (modulator A), could be modified during test mode such that the first integrator has a gain of 0.25 (one half of the nominal gain). This could be done by disconnecting one half of the sampling capacitor. The obtained modulator would not have a second order transfer function. Simulations show that the quantizer effective gain settles to approximately 8/3. The modified transfer function would become

$$Y = \frac{z^{-2}X + 3(1-z^{-1})^2 E}{3 - 2z^{-1}}. \qquad \textbf{(6-4)}$$

Nevertheless, it can be shown that the leakage signature of the first integrator would be of the form

$$s = \left(\sum_{i=1}^{N} x_i - y_i\right)_{Q} - \left(\sum_{i=1}^{N} x_i - y_i\right)_{-Q} = 8NQ\Delta p_1, \qquad \textbf{(6-5)}$$

for a test performed with sequences with mean values Q and -Q.

As seen in Figure 6-7, the maximum output reached by the integrators is much reduced for the modified modulator compared with the nominal case of Figure 6-1. Actually, the

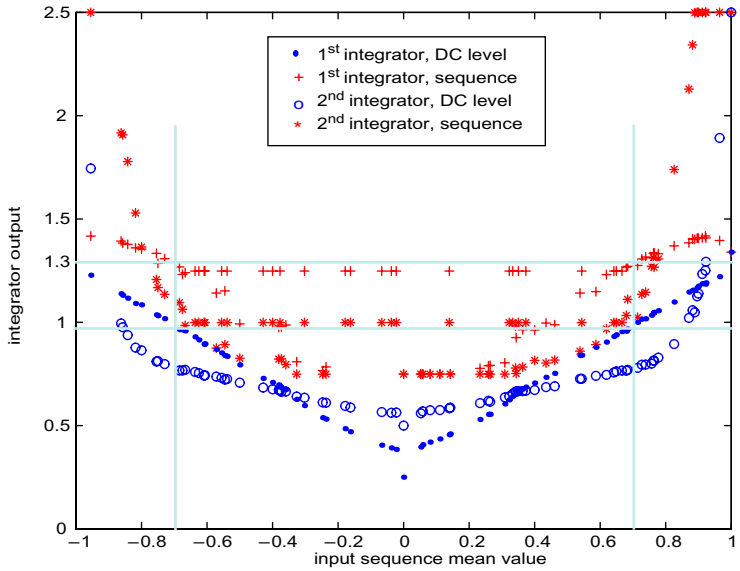


Figure 6-7: Maximum integrator outputs as a function of the modified modulator A input

maximum integrator output reached for digital sequences in the modified modulator is below the maximum output reached by DC levels in the nominal modulator: in particular, it is below 1.3 for mean values in the range [-0.7; 0.7].

Figure 6-8 shows the signature of the leakage test as a function of the mean value of the input sequence , for modulator A but with a clipping value set to 1.6 instead of 3.3 according to Table I. The same test is performed for the modulator with and without the scaling of the first integrator gain. It appears clearly that the leakage signature follows the expected one over a larger range of sequences for the scaled modulator than for the nominal one.

In conclusion, the use of digital sequences as test stimuli does not cause instability in 1^{st} or 2^{nd} order modulators but may increase the requirements on the output range of the amplifier. Nevertheless, we have shown that neither integrator clipping nor DC gain non-linearity affect the leakage test results significantly for input sequences with a small input mean value and that the deviation of the signature for higher mean values may allow one to test for these effects. Similarly, it appears that the settling error test can be performed correctly without modifications. Anyway, the proposed tests should be simulated (at high level) for any partic-

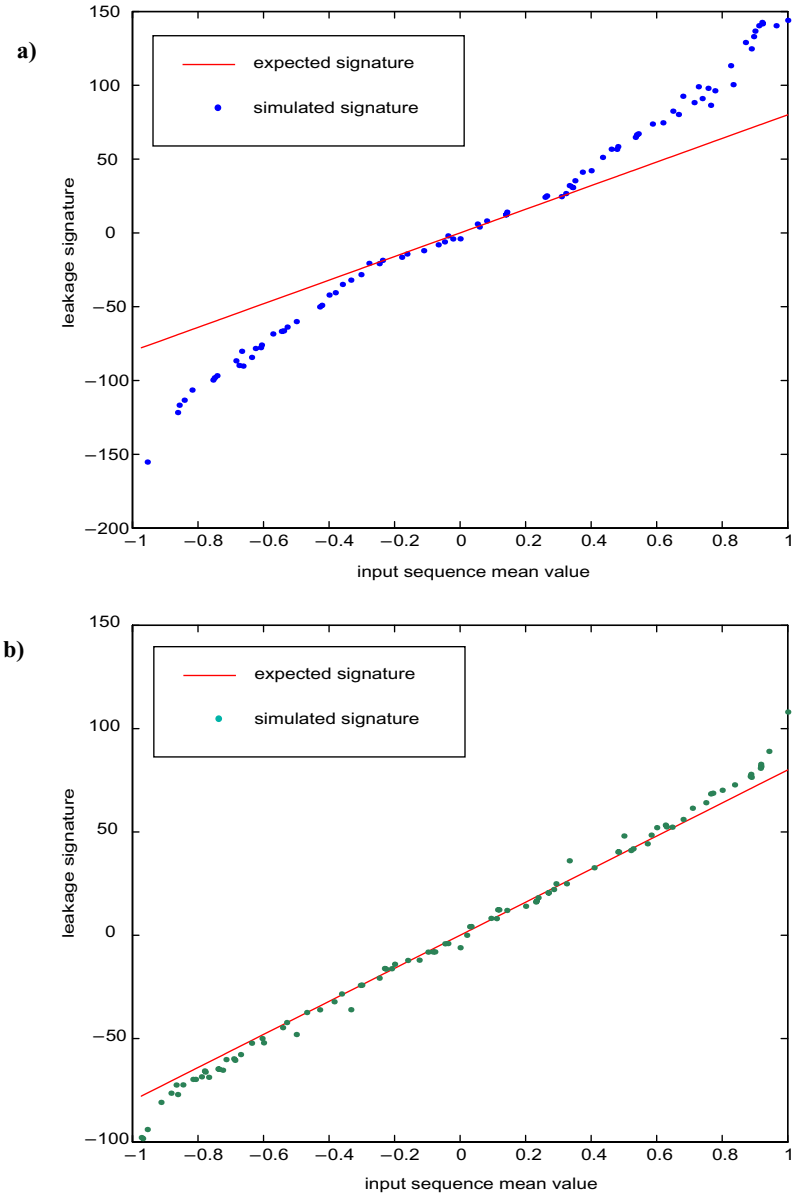


Figure 6-8: Modulator A (with clipping at 1.6) 1st integrator leakage signature as a function of the input sequence mean value
a) 1st integrator with the nominal 0.5 gain
b) 1st integrator with the scaled 0.25 gain

ular architecture and implementation in order to see whether it is necessary or not to introduce integrator gain scaling or full-scale reduction during test mode.

6 • 1 . 2 Input sequence generation

The on-chip generation of the test stimuli also has to be addressed.In order to test the amplifier DC gain, the digital periodic sequence can be stored in a recycling register, which will require a number of memory elements equal to the sequence period. For instance, a test sequence [1 1 1 1 1 -1] would require a 6-bit register. The stimulus for testing the amplifier settling errors is a pseudo-random sequence. It could be generated by a LFSR [91]. An m-bit register provides a repeating random sequence of length 2^m-1. That sequence has a systematic offset of $1/(2^m-1)$. The most important characteristic of the pseudo-random sequence is that the correlation of three consecutive samples should be close zero. Hence, a relatively small LFSR could be used, which opens the door to the reuse of the recycling register, as seen in Figure 6-9. The control signal c allows the user to select between the periodic and the pseudo-random signal. If more than one sequence is desired, multiplexers could be used to add or remove the required number of latches from the register. Nevertheless, the same feedback cannot be used for any register length to generate pseudorandom sequences. Figure 6-9 shows a possible feedback configuration for a six-bit register. However, other register lengths may require more than 1 XOR gate and the XOR input location (called the tap location) may also vary. For instance, a 12-bit LFSR requires at least 4 XOR gates. A generic implementation would be that of Figure 6-10. An XOR gate is associated with each

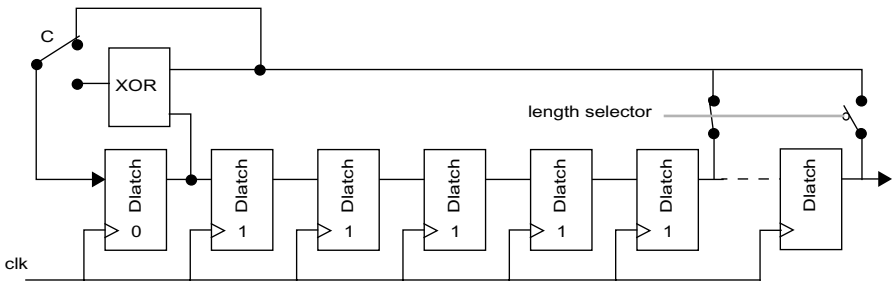


Figure 6-9: Test sequence generator.

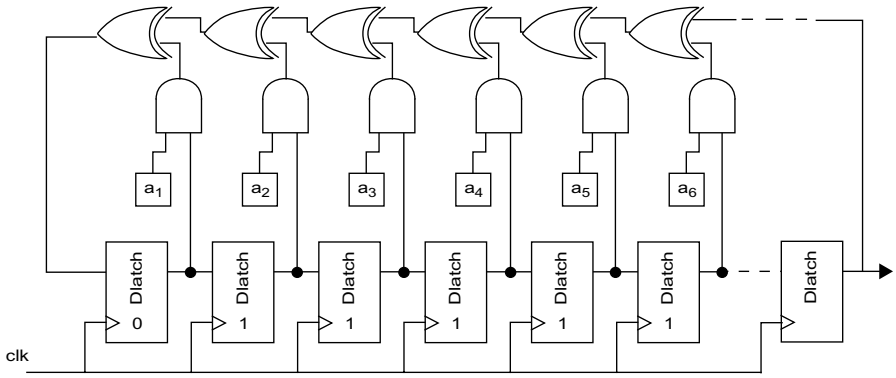


Figure 6-10: Generic LFSR

latch but can be enabled or disabled. Indeed, if parameter a_i is set to 0 the XOR gate i is bypassed. For a given register length L, there is usually more than one feedback configuration (a_i combination) that gives a pseudorandom sequence of maximum length 2^L-1. Table II shows the valid a_i combinations for some register length. Notice that for each combination of a_i that appear in the table, the combination of a_{L-i} 's is also valid.

Table II: LFSR feedback configuration for maximum length sequences

register length L	feedback coefficients that are set to 1
3	a_2(1 XOR gate)
4	a_3 (1 XOR gate)
5	a_3 (1 XOR gate) a_2, a_3, a_4 (3 XOR gates) a_1, a_3, a_4
6	a_5(1 XOR gate) a_1, a_4 a_5 (3 XOR gates) a_2, a_3 a_5
7	a_4 (1 XOR gate) a_4, a_5, a_6 (3 XOR gates) a_2, a_5, a_6 a_2, a_4, a_6 a_1, a_4, a_6 a_3, a_4, a_5 a_2, a_3, a_4, a_5, a_6 (5 XOR gates) a_1, a_2, a_4, a_5, a_6
...	...

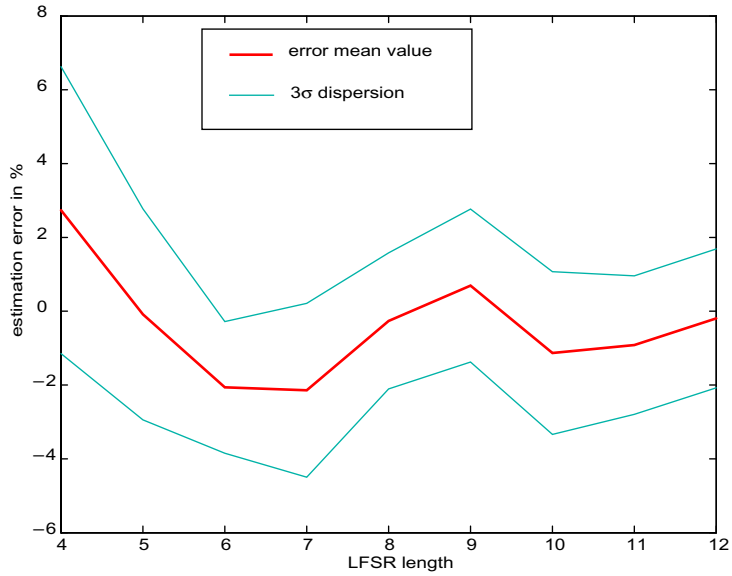


Figure 6-11: Estimation error of the number of occurrences of level 2, as a function of the LFSR length

If the LFSR has been correctly designed to reach a maximum length pseudo-random sequence, any initialization is valid except an all-zero.

In order to demonstrate that pseudorandom sequences can be used efficiently to generate the settling error signature, a 2^{nd} order modulator is simulated using as input the pseudorandom sequence produced by a LFSR. The length of the LFSR is varied from 4 to 12, taking in each case a feedback configuration that ensures a maximum length sequence. For each LFSR length, the settling error test is performed 100 times on the modulator, randomly varying the modulator behavioral parameters (1^{st} and 2^{nd} amplifier DC gain, slew-rate, bandwidth...). According to the settling error test proposed in Section 5 • 1 . 3 . 1 (and corresponding to test 11 in Appendix A), a random sequence is used because it enables one to estimate *a priori* the probability of the occurrence of level 2 at the input of the first integrator. This allows one to infer the settling error directly from the deviation of the output bit-stream average from the input sequence average. Hence, Figure 6-11 represents the error (in %) produced by the a-priori estimation of the number of occurrences of a level 2 at the

integrator input, as a function of the LFSR length. Actually, what is represented is the mean value of the error for the 100 cases simulated for each LFSR length, together with the 3σ interval. Note that the error remains below 7% in any case. Notice also that the error on the estimation of the number of occurrence of a level 2 at the integrator input translates to a relative error on the evaluation of the settling error. It can be easily assumed that determining the settling error with a 7% precision should be sufficient for most tests. It is thus likely that the use of a LFSR will not be the limiting factor for a settling error test, at least for small values of the settling error. This is corroborated by simulating a settling error test with a 5-bit LFSR, varying the 1st amplifier slew-rate. Figure 6-12 a) shows the settling error evaluated through Eq (5-13) which, at first sight, perfectly matches the settling error calculated analytically. Figure 6-12 b), in turn, shows the relative error produced by the proposed evaluation. It appears clearly that the error remains below 7% except when settling errors are very small and the measurement error is dominated by quantization noise.

Provided that the input sequence is conceptually similar to the modulator feedback signal, it has similar requirements in terms of synchronization. More concretely, it should be ensured that the input sequence does not vary during the clock phase(s) where it is sensed (this will be addressed further). The best option possibly consists of adding an edge-triggered D-latch that will sample and hold the input test sequence according to the relevant internal clock edge.

In any case, it is clear that in the case that the test sequences were generated on-chip, the required hardware will only represent a few logic gates. In particular, it is interesting to compare our requirements with those of the work proposed in [48]. In order to generate a multitone sine-wave, the authors propose to store a portion of a ΣΔ modulator bit-stream in a recycling register and filter the digital signal issued by a well-designed return-to-zero differential buffer. Even without considering the analog filter, the authors had to use a 1024-bit register to obtain a signal with 60dB of SFDR. Our proposal requires two orders of magnitude less hardware, considering only the digital part.

Such a small digital circuit is undoubtedly more robust than the circuit under test but for high reliability applications, the small size of the used register would even permit the use of TMR (Triple Modular Redundancy) without a large impact in terms of area.

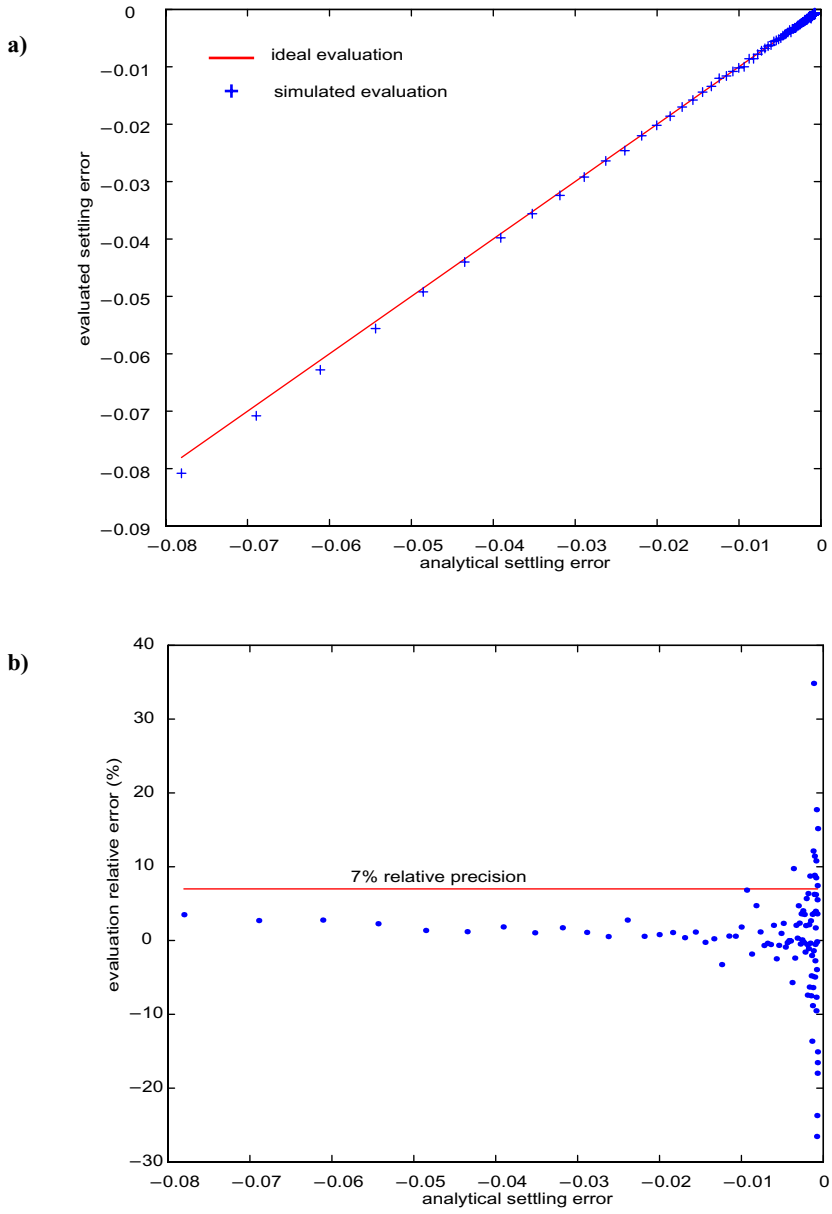


Figure 6-12: Test of the settling error
a) evaluated settling error
b) evaluation relative error

6 • 2 THE RESPONSE ANALYSER

The implementation of the response analyser depends on the level of integration which is required. As was commented above, the proposed test set can be seen as a solution that enables the use of low-cost digital tester. In that sense, the modulator output bit-stream can be acquired and processed in software to build the test signatures. At a higher-level of integration, the signature can be computed on-chip but shifted out for test decision. This could be the case for a modulator embedded within a SoC, where an on-chip micro controller could be used to take the test decision. Finally, the signature could be computed on-chip and compared to a pass-fail limit stored in an on-chip register.

6 • 2 . 1 Signature counters

The signature elaboration consists of summing the input sequence and subtracting the output over a given number of samples. Hence, it only requires an up/down counter and some logic gates, as shown in Figure 6-13. A multiplexer can also be introduced to invert the inputs of the signature analyser. The proposed tests require that two acquisitions be performed in order to cancel input-referred offsets. Subtracting the two signatures can be done using a single counter and simply inverting its inputs.

The sizing of the counter has to be considered with care. Indeed, it is possible to evaluate what should be the final value of the counter as a function of the worst case that must be measured. For instance, a leakage test could be designed so as to obtain a signature of 10 in the nominal case. Let us say that this nominal case corresponds to an 80dB amplifier gain. If the counter is sized to 100, the signature will saturate for amplifier gains below 60dB

However, the input-referred offset has to be taken into account as it may saturate the counter before the end of the evaluation. This issue can be circumvented by implementing a modulo counter. In that case, the size of the counter has to be set higher than the worst-case signature. This would be an adequate choice whenever the worst case can be defined with great confidence. In the case depicted above, a modulo 128 counter may be used. The nominal counter output would be 10 and the counter output for a 60dB gain would be 100. How-

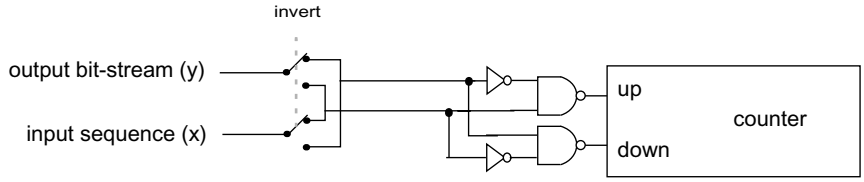


Figure 6-13: Hardware required for the signatures

ever, a defect causing a DC gain of 725 (57.2 dB) would give an output counter of 10, being wrongly interpreted as an 80dB gain. The modulo counter solution is thus prone to fault masking.

It may thus be more judicious to implement a saturating counter and set its length according to the maximum allowable offset. If an offset representing 10% of the full-scale is allowable and a given test requires the acquisition of 100000 points, a 14 bit counter would be adequate.

Notice that a unique counter may be used if all the tests are implemented sequentially. In that case, the counter has to be sized according to the most demanding case. Nevertheless, in cascaded modulators it may be interesting to test the different stages in parallel in order to save test time. In that case, one counter per stage should be implemented.

In the case that the settling error tests are implemented with deterministic sequences, it has been shown that it is necessary to acquire the number of occurrences of a level -2 (or level 2 for the second acquisition) at the integrator input. A level -2 occurs at instant *n* at the integrator input if and only if the input sequence sample at instant n is a -1 (a digital 0) and the modulator output a 1 (a digital 1). Hence, the counter necessary to acquire this number of occurrence could be implemented as in Figure 6-14. The length of this counter can be set to handle a maximum final count of *N*, where *N* is the number of acquired points. Indeed, the integrator input has zero mean. This implies that, for one acquisition, the number of occurrence of level -2 cannot be greater than *N*/2. Similarly, for the second acquisition (necessary to get rid of the input-referred offset), the number of occurrence of level 2 cannot be greater than *N*/2. Hence, the final value of the counter at the end of the two acquisition cannot be greater than N. Notice that this is the worst case as it supposes that the number of occurrences of a level 0 is null, which is highly improbable.

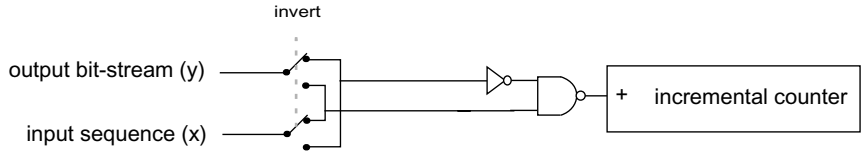


Figure 6-14: Counter of level 2 (-2) number of occurrences at the integrator input

Notice that the leakage test for a multi-bit modulator requires us to implement an accumulator with a multibit input instead of a counter. This obviously requires more hardware than for a single-bit modulator. Moreover, the summing operation has to be realized at the modulator's speed and a combinational implementation is thus likely.

6 • 2 . 2 Using a decimation filter

Our aim has been to design simple digital tests for ΣΔ modulators, with the goal of being as general as possible. From the architectural point of view, the proposed tests are valid for any cascade of 1^{st} and 2^{nd} order sections. Research is still necessary to extend the tests to generic architectures. However, the proposal is not limited by the actual usage of the modulator. The digital tests were designed with cost-effectiveness in mind. The objective was to provide a full-BIST implementation that would be suitable even for stand-alone ΣΔ modulators, which is the most demanding case as the test hardware has to be compared with the modulator alone.

Nevertheless, for ΣΔ converters (that gather a ΣΔ modulator and a decimation filter), the resources available on-chip may be exploited for test purpose. Indeed, it has been repeated throughout the manuscript that the test are designed such that the signatures sense the deviation of the output bit-stream mean value from the input sequence mean value. Hence, as the mean value of the input sequence is known *a-priori*, all the relevant information is present in the DC component of the output bit-stream. The task realized by the signature up/down counters is nothing more than filtering the quantization noise and tones in the output bit-stream to isolate the DC components. For instance, it has been pointed out in Section 4 • 1 . 3 . 1 that the number of acquired points should be ideally chosen such that it is a multiple of the input sequence length, in order to minimize the signature error. The reason for this can

be easily interpreted in the frequency domain. The operation realized by the counter is actually a sinc (cardinal sinus) filtering, which takes the following form in the z-domain,

$$\frac{1 - z^{-N}}{1 - z^{-1}}, \tag{6-6}$$

where N is the number of averaged points.

If N is chosen such that it is a multiple of the selected test sequence period, it implies that the sinc filter implemented by the counter has zeros at all multiples of the input sequence fundamental frequency. Hence, the contribution of the input sequence harmonics in the test signature are efficiently filtered.

This new frequency-domain focus on the signature leads to a natural question: if the goal of the counter is mainly to remove the quantization noise, would not it be more efficient to use the converter decimation filter? Indeed, the decimation filter is designed specifically to remove the modulator quantization noise. It is likely that it performs the desired filtering operation better than a first order filter (i.e. a counter).

The only drawback is that the decimation filter is usually not programmable and is not optimized for any input sequence period. This is a particular concern for low OSR, as it is possible that the fundamental frequency of the test sequence fall into the base-band. One solution to this issue could be to add a first order filter at the decimation filter output that would take the average of the required number of samples. For example, if the input sequence is of length 6, the number of filter output samples to be averaged could be 6 (or any multiple of 6).

Whether the decimation filter is adequate or not to build signature is a matter of the required sensitivity of the output bit-stream DC component. Let us take an example. The leakage test signature for an ideal second order modulator is

$$s_1 = \sum_{i=1}^{N} (x_i - y_i) = 2NQ\Delta p_1 + N \times off\,. \tag{6-7}$$

This signature can be interpreted in terms of DC components. Assuming that the decimation filter is good enough to isolate the DC level of the modulator output bit-stream, the filter output can be written as

$$\begin{aligned} \overline{Y} &= Q - 2Q\Delta p_1 + off \\ Q &= \overline{X} \end{aligned} \tag{6-8}$$

where Q is the mean value of the input sequence. The condition for the filter output to be sensitive to leakage is thus that the term $2Q\Delta p_1$ in Eq (6-8) be greater than one effective LSB. If the decimation filter is designed such that an effective resolution of ENOB-bit is obtained, the condition can be written as

$$2Q\Delta p_1 > \frac{2}{2^{ENOB} - 1}. \tag{6-9}$$

For an ideal decimation filter and an ideal 2nd order single-bit modulator, the theoretical effective ENOB can be calculated as

$$ENOB = \frac{1}{2}\log\left(\frac{5OSR^5}{\pi^2}\right), \tag{6-10}$$

where OSR is the over-sampling ratio. This gives an measure of the minimum integrator leakage that could be detected for a given OSR

$$\Delta p_{min} = \frac{\pi^2}{Q\sqrt{5OSR^5}}. \tag{6-11}$$

Furthermore, the amount of quantization noise that leaks into the baseband for a given leakage can be calculated as

$$\Delta P_{noise}(dB) = 10\log\left(1 + \Delta p^2 \times \frac{OSR^2}{\pi^2} \times \frac{10}{3}\right). \tag{6-12}$$

Hence, the minimum detectable leakage corresponds to a noise degradation of

$$\Delta P_{min}(dB) = 10\log\left(1 + \frac{2}{3} \times \frac{\pi^2}{Q^2 OSR^3}\right). \tag{6-13}$$

According to expressions Eq (6-11) and Eq (6-12), we can say that for larger OSR the resolution of the ΣΔ converter increase. As a result, integrator leakage can be detected with more precision. On the other hand a given pole error results in a greater SNR loss for higher OSR. Eq (6-13) allows us to conclude that the benefits of a large OSR for the leakage test overweigh the major SNR loss for an given pole error. Nevertheless, for a low OSR such as 16, the decimation filter should be sufficient to detect leakage that would cause a 0.03dB SNR loss with an input sequence whose mean value is *Q=0.5*.

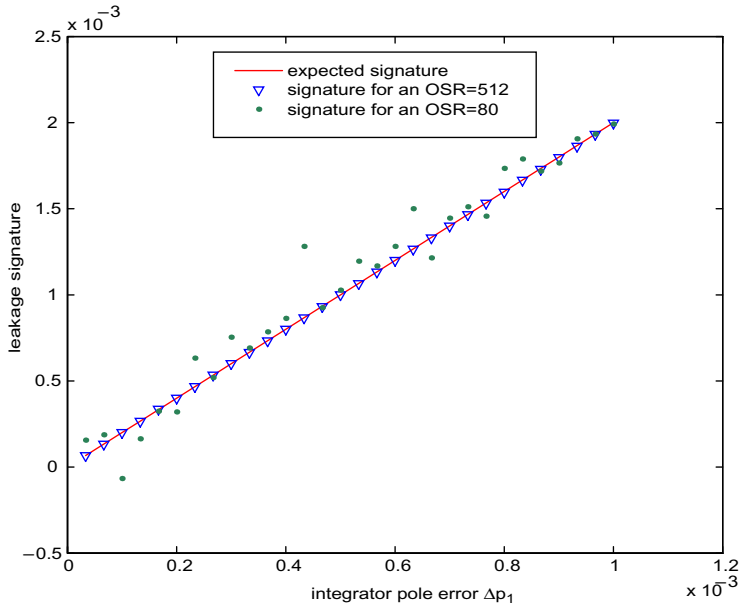


Figure 6-15: Leakage test signature for two OSR values

This was verified by simulation. Figure 6-15 shows the signatures obtained by simulation of a second order modulator as a function of the first integrator pole error, for an OSR of 80 and for an OSR of 512. We see clearly that the results for an OSR of 512 almost perfectly match the expected signature that is represented by the solid curve on the figure. In turn, the results for an OSR of 80 exhibit more dispersion.

Figure 6-16 shows the evolution of this dispersion as a function of the OSR. Note that increasing the OSR drastically reduces the dispersion and thus allows us to detect smaller pole errors.

For a cascaded modulator of order L, with a second order modulator as the first stage, the quantization noise leaking into the baseband due to a pole error in the first integrator can be calculated as

$$\Delta P_{noise}(dB) = 10\log\left(\frac{\Delta_1}{\Delta_n}\left(1+\frac{2\Delta p^2}{\pi^{2L-2}}\times\frac{OSR^{2L-2}}{d^2}\times\frac{2L+1}{3}\right)\right), \qquad \textbf{(6-14)}$$

where Δ_1 and Δ_n are the quantizer step of the first and last stage, respectively; d is a factor greater than unity that depends on the cascaded architecture.

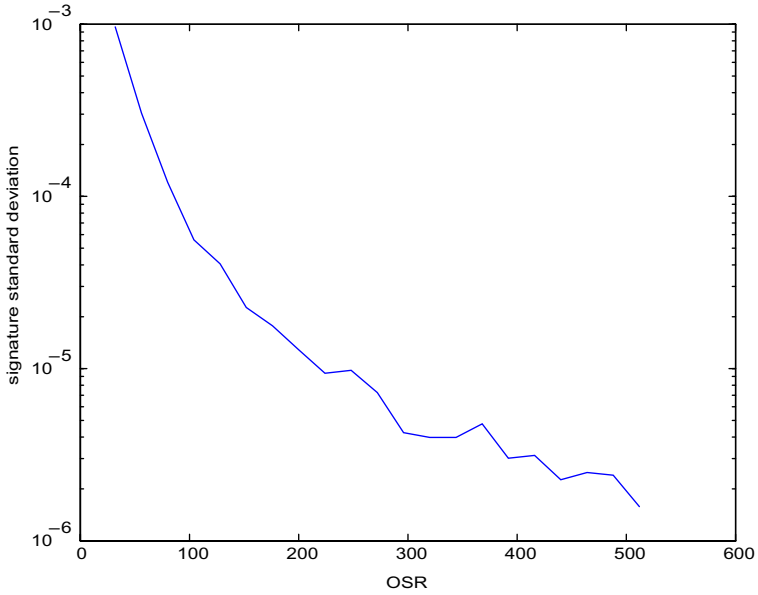


Figure 6-16: Leakage test signature dispersion as a function of the OSR

Hence, in the case of a cascaded modulator, the SNR loss associated with the minimum detectable leakage is

$$\Delta P_{min}(dB) = 10\log\left(\frac{\Delta_1}{\Delta_n}\left(1+\frac{4L+2}{15d^2Q^2}\times OSR^{2L-7}\times\pi^{6-2L}\right)\right). \qquad \textbf{(6-15)}$$

Here, things are different than for a 2nd order modulator alone. Indeed Eq (6-15) shows that the SNR loss associated with the minimum detectable pole error will increase with the OSR if the order of the cascaded modulator is higher than 3.

For instance, taking d=2, Q=0.5 and $\Delta_1 = \Delta_n$= 1, we see that the SNR loss associated with the minimum detectable pole error with the decimation filter at OSR=16 would be 0.25dB for a 3rd order modulator, 4.7dB for a 4th order, and 18dB for a 5th order. Hence, we conclude that the detection of pole errors that have a significant impact on performance in a cascaded modulator of order higher than 4 would require more filtering than the one provided by the decimation filter. This may be done by simply averaging some words at the filter output.

In any case, the interest of re-using the decimation filter not only resides in hardware savings but also in test time reduction, as much fewer samples are necessary to reach a given precision with the decimation filter than by simply averaging the output bit-stream. Let us consider the brief example of a simple 2nd order modulator with a 3rd order comb filter. A comb filter of order n can be seen as a cascade of n moving-average blocks. The length of the window on which the average is performed defines the cut-off frequency. If f_s is the operating frequency of the filter, a running average of k samples corresponds to a cut-off frequency of $f_c=f_s/2k$. In order to properly settle, such a filter requires $n*k$ samples. Indeed, k input samples are needed to perform a running average. Hence, each one of the n stages introduces a latency of k samples. For our example, the comb filter is of 3rd order and has to cut at a frequency of $f_c=f_s/(2OSR)$. It thus requires 3OSR samples to settle properly and to obtain a valid signature.

Equation (6-11) gives the expression of the minimum detectable pole error with the decimation filter. The question is how many samples would be needed to detect such a pole error with a simple counter. If we do not consider quantization noise for the sake of simplicity, the minimum detectable signature would be equal to 2. Hence, the number of acquired samples should be such that

$$2QN_{min}\Delta p_{min} > 2\,. \tag{6-16}$$

Introducing Eq (6-11), we find that the number of samples required to detect Δp_{min} with a counter is

$$N_{min} = \frac{\sqrt{5OSR^5}}{\pi^2}\,. \tag{6-17}$$

It can be verified easily that the test time required using the decimation filter is lower than that of the counter for any OSR above 6 (which means almost in any case). The reader should not conclude, though, that the use of a counter is significantly worse than the decimation filter. Indeed, the settling time of the decimation filter is a fixed quantity while the number of samples averaged by a dedicated counter can be tuned. If the test only requires the detection of a pole error equal to 10 times Δp_{min}, the number of averaged samples can be divided by 10 while the settling time of the filter will remain unchanged.

Concerning the settling error test, it can in principle benefit from the decimation filter in the same way as the leakage test. However two important things have to be taken into account. If the test is carried out using a deterministic sequence with a short period, it is still necessary to implement a counter to acquire the number of occurrence of level 2 (or -2) at the integrator input. Indeed the decimation filter only provides the numerator of Eq (5-13). Another important aspect to take into account is that the decimation filter has to be driven by the same modified clock as the modulator; otherwise the bits at the modulator output that coincides with a level 2 (or -2) at the input of the integrator would be counted twice in the signature. That constraint, though, does not represent much of an issue.

Unlike for integrator leakage, it is difficult to assess if a given decimation filter is sufficient to detect the minimum settling error that would have an impact on performance.

It has been shown in Section 5 • 1 . 1 . 2 that the first integrator settling error can be referred to the modulator input and translates into a distortion term. The expression of the INL as a function of the DC input v is

$$d(v) = \frac{1+v}{2}er(v-1) + \frac{1-v}{2}er(v+1) \qquad \textbf{(6-18)}$$

where *er(x)* is the integrator settling error for an input x. One might expect that the maximum INL should be obtained for the maximum integrator settling error but this is not the case. The settling error for an integrator input of 2 is the highest, but the probability of occurrence of a level 2 at the integrator input tends to zero. Actually, experience says that the INL curve of ΣΔ modulators is usually close to a 3rd order polynomial. The location of its maximum and minimum depend on the modulator but a value of 2/3 of the full-scale is a good example. In this case, the maximum INL could be evaluated as

$$INL_{max} = d\left(\frac{2}{3}\right) = \frac{5}{6}er\left(\frac{-1}{3}\right) + \frac{1}{6}er\left(\frac{5}{3}\right) \approx \frac{1}{6}er\left(\frac{5}{3}\right). \qquad \textbf{(6-19)}$$

To a first approximation, it can be assumed that the integrator settling error associated with a -1/3 integrator input level is order(s) of magnitude smaller than the settling error associated with a 5/3 input level.

For a settling error test performed with a random input sequence, we have seen that the signature was of the form

$$s = \frac{N}{4}er(2) \pm 2\,. \qquad \textbf{(6-20)}$$

If the same test is performed using the decimation filter to sense the DC component deviation in the output bit-stream, the equivalent signature would be

$$s_{filter} = \frac{1}{4}er(2). \tag{6-21}$$

This equivalent signature would be obtained with a precision of 1 effective LSB.

It can be seen that

$$\left(\frac{1}{4}er(2) > \frac{1}{6}er\left(\frac{5}{3}\right)\right) \Leftrightarrow (s_{filter} > INL_{max}). \tag{6-22}$$

If the INL is high enough to impact the ADC, it implies that the maximum INL should be greater than 1 effective LSB. In this case, the decimation filter would be sufficient to perform the settling error test.

6 • 2 . 3 Additional manipulations

In most cases, the best option would probably be to ship the signature counter values off-chip and process the results to make the test decision. The counter values would not have to be shipped at the modulator full-speed and therefore this operation would thus not be demanding at all for a simple data analyzer. Furthermore, such an option allows one to have in hand the signatures that are proportional to the different behavioural parameters and make some kind of “analog” test decision. Indeed, it is not the same to obtain a leakage signature for the third amplifier that is greater than the nominal test limit in 1 count than to obtain a leakage signature that saturates the counter.

If the test decision has to be implemented on-chip, it will require more hardware. If the settling error tests are carried out with a deterministic sequence, it has been seen in Section 5 • 1 . 3 . 1 that a rigorous evaluation requires the division of two counter results (see for instance Eq (5-13)). Implementing a high-speed divider may require an important amount of hardware. However, that is not the case here as the operation is carried out on the counter results after the acquisition. Therefore, it does not have to be realized at full-speed and a sequential implementation is thus much more interesting. For a full-BIST implementation, it is also necessary to store the pass-fail limits for the selected tests in on-chip registers and to compare the resulting signatures in order to generate the corresponding test results.

6 • 3 THE MODULATOR MODIFICATIONS

The proposed digital test set can be contemplated at different level of integration. In a full-BIST approach, both the stimulus generator and the signature analyzer should be implemented on-chip. In a partial BIST approach, only one of the two would be implemented on-chip. Another possibility would be to use a low-cost digital ATE that would perform both operations; in this case it would not be a BIST at all. But in all these cases, some modifications of the ΣΔ modulator would have to be performed to enable the digital tests. These modifications, as explained in chapter 3, should not substantially alter the modulator design flow.

The proper modification of the ΣΔ modulator has to consider three basic points:

- disabling the integrator's nominal input
- enabling a digital test input, and
- modifying integrator branch coefficient if required

We will try to address these points separately but it will quickly appear to the reader that the modifications should be considered as a whole during the design phase, considering the unavoidable trade-off between simplicity and efficiency.

6 • 3 . 1 Modifying the switch control

In order to use a digital input to test the modulator, the regular input has to de disabled during test mode. This can be performed easily with a AND gate and a configuration bit, or even with a simple multiplexer, as shown in Figure 6-17, where ϕ_1 represents the sampling phase and *cfg* is the configuration signal that enables the input.

It could be argued that such a modification is undesirable because clock gating induces an increase of jitter noise. However, this is irrelevant in our case for two reasons. ΣΔ modulators work at a high sampling rate but their input signal bandwidth is usually much lower than this frequency (by the factor OSR). As a result, the jitter associated with the modulator clock is usually small enough when referred to the maximum input signal frequency. Actually, for an input sine-wave of amplitude A and frequency f_b, the power of the jitter noise in the modulator base-band can be written

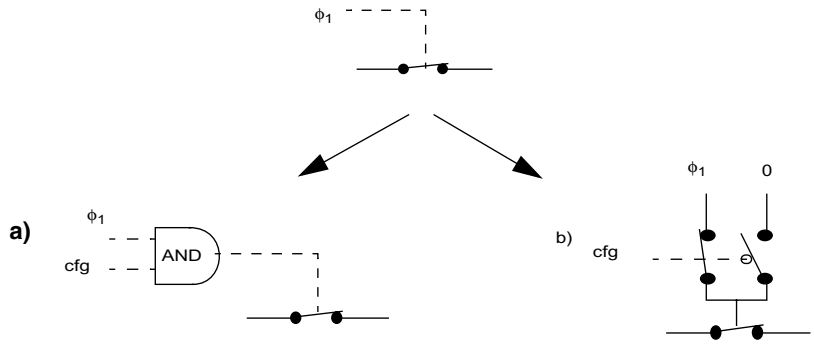


Figure 6-17: Integrator input switch - control modification.
a) implementation with a AND gate
b) implementation with a transmission gate

$$P_{jitter} = \frac{A^2}{2} \times \frac{(2\pi f_b \sigma_t)^2}{OSR}, \quad \textbf{(6-23)}$$

where σ_t is the jitter standard deviation (in s). Considering the worst-case of a full-scale sine-wave of maximum allowable frequency $f_b=f_s/2/OSR$, and expressing the jitter standard deviation as a fraction of the modulator clock period $\sigma_t=\sigma_j/f_s$, we find that

$$P_{jitter}(dB_{FS}) = 20\log\left(\frac{(\pi\sigma_j)^2}{OSR^3}\right). \quad \textbf{(6-24)}$$

It appears clearly that jitter is an issue only for high-speed applications that require the design of a modulator with low OSR and high operating frequency, for which a low σ_j is difficult to obtain.

What is more important is that the input switches that are gated are not those that define the sampling instant. Indeed, a common practice consists of opening the switch that connects the sampling capacitor to the amplifier virtual ground slightly before the input switch, as represented in Figure 6-18. This is done to minimize the effects of charge injection. As a result, the sampled voltage is the input voltage at the falling edge of the virtual ground switch control. In any case, the additional AND gate only adds an extra delay with respect to this falling edge and thus goes in the right direction. The only limitation is to ensure that the delay introduced by the gate is less than the non-overlapping inter-phase.

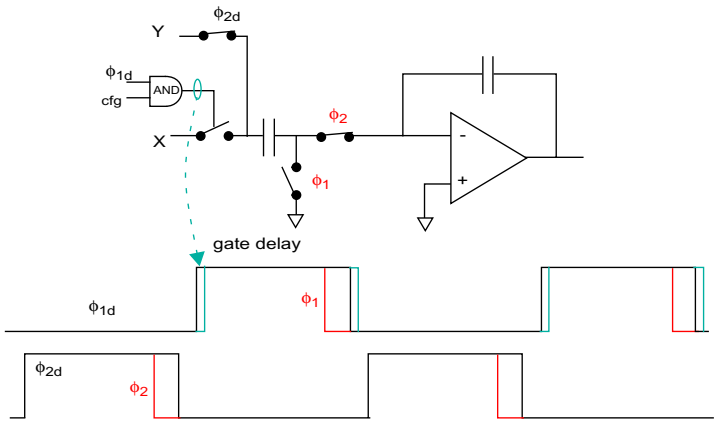


Figure 6-18: Integrator input switch - clock gating effects

When applied to the second integrator in a second order modulator, the modification of the integrator input switch control allows one to reconfigure the second order modulator into a first order modulator. In that way, the second integrator can be tested using the tests developed for first order modulators.

While the study of the proposed test has been limited to 2nd and 1st order modulators (and their combinations in cascaded modulators), the concept may also apply to higher order modulators. The different integrators in the loop may be tested by reconfiguring the modulator in a lower order. However, the reconfiguration and its impact on the test should be studied with care because higher order modulators usually introduce some kind of local feedback or feedforward loops that may not be easily disabled.

6 • 3 . 2 Reusing or replicating the DAC

Once the nominal input of the modulator is disabled, it is necessary to enable the digital test input. In order to input a digital sequence to the ΣΔ modulator, be it periodic or pseudo-random, a single-bit DAC has to be used. Depending on the integrator topology, it is possible to replicate the DAC to substitute the nominal input or to re-use the feedback DAC during the sampling phase.

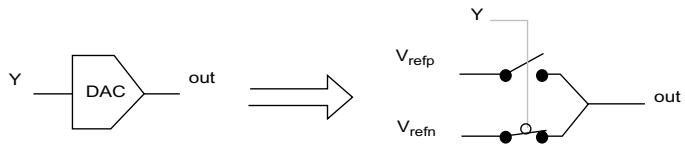


Figure 6-19: Single-bit DAC implementation

6 • 3 . 2 . 1 Peculiarity of the single-bit DAC

As a matter of fact, a single-bit DAC for switched-capacitor circuits is actually a simple multiplexer that connects either a positive reference voltage or a negative reference voltage to the output node, as seen in Figure 6-19. Such a DAC could be connected to any input of the different integrator topologies. However, it appears that the DAC switches and the integrator input switches are connected in series, which is not optimum for passive sampling. It is thus usual practice to combine the multiplexer operation of the DAC with the function of the integrator switch, as illustrated in Figure 6-20 (Notice that the single-ended implementation is represented for the sake of simplicity without loss of generality). We will see how this modification can be further extended for test purposes.

6 • 3 . 2 . 2 Single-branch integrator

For a single-branch integrator, it appears obvious from Figure 6-21 that replicating the DAC to replace the nominal input or re-using the feedback DAC during both phases is functionally equivalent.

During normal operation, the input voltage is sampled on the input capacitor during ϕ_1 while the feedback value is sent to the integrator during the integrating phase ϕ_2. In test mode, the nominal input is disabled so the DAC could be replicated to replace the nominal input, as in Figure 6-21 a), or simply re-used during phase ϕ_1 as seen in Figure 6-21 b). This latter solution implies a modification of the DAC controls so that the DAC is driven by the test sequence during ϕ_1 and by the feedback during ϕ_2. Replicating the DAC is possibly the simplest solution from a design viewpoint but may be slightly more expensive if large switches are required to provide proper settling. On the other hand, re-using the DAC during both phases requires that some care be taken with the timing of switch controls as more

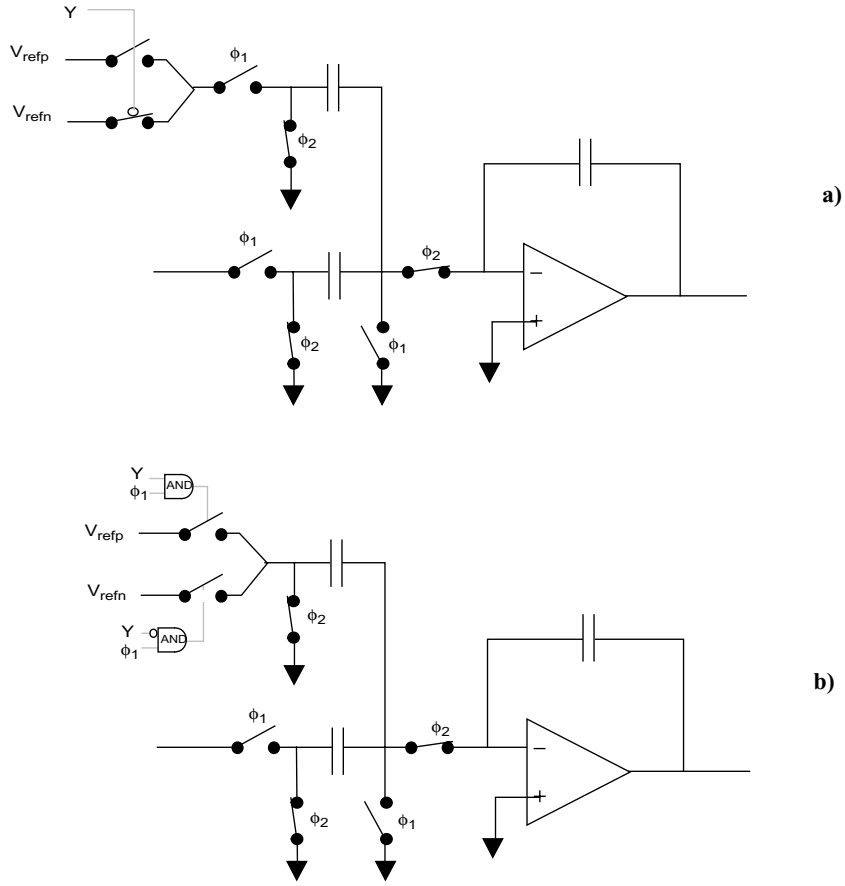


Figure 6-20: a) direct connection of the feedback DAC to the integrator b) combination of the DAC with the integrator input switch

clock gating is required. The observations with respect to clock gating for disabling the nominal input also stand for the DAC modification.

6 • 3 . 2 . 3 Double-branch integrator

Things are different for a double-branch integrator. Indeed, the nominal path is affected by a different coefficient than the feedback path. Even if the two branches are designed with the same capacitor, mismatch will inevitably lead to coefficient differences. If the DAC is replicated to play the role of the nominal input, as in Figure 6-22 a), the gain error between the two branches will lower the precision of leakage tests. Indeed, the gain error would man-

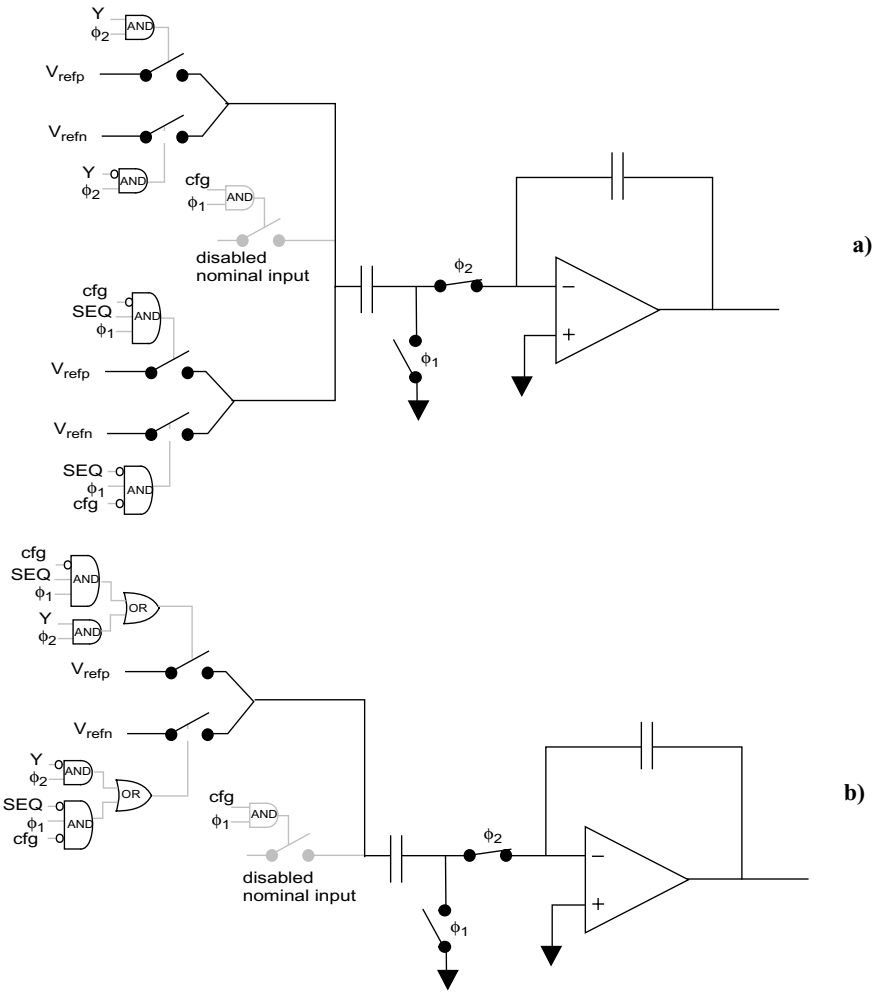


Figure 6-21: Digital sequence input for a single-branch integrator
a) DAC replication
b) DAC re-use

ifest itself in the leakage test signature in the same way as integrator leakage, leading to fault masking. The settling error test would not be significantly affected. Conceptually, the integrator would not see only three levels (-2, 0 and 2) but four, as the multiplicity of level 0 would be suppressed (-a-b -a+b a-b a+b, with a<b). In any case, the settling error associated with levels a-b and b-a could be considered negligible with respect to the other two cases. Hence applying the test without modification would yield the settling error associated with level a+b.

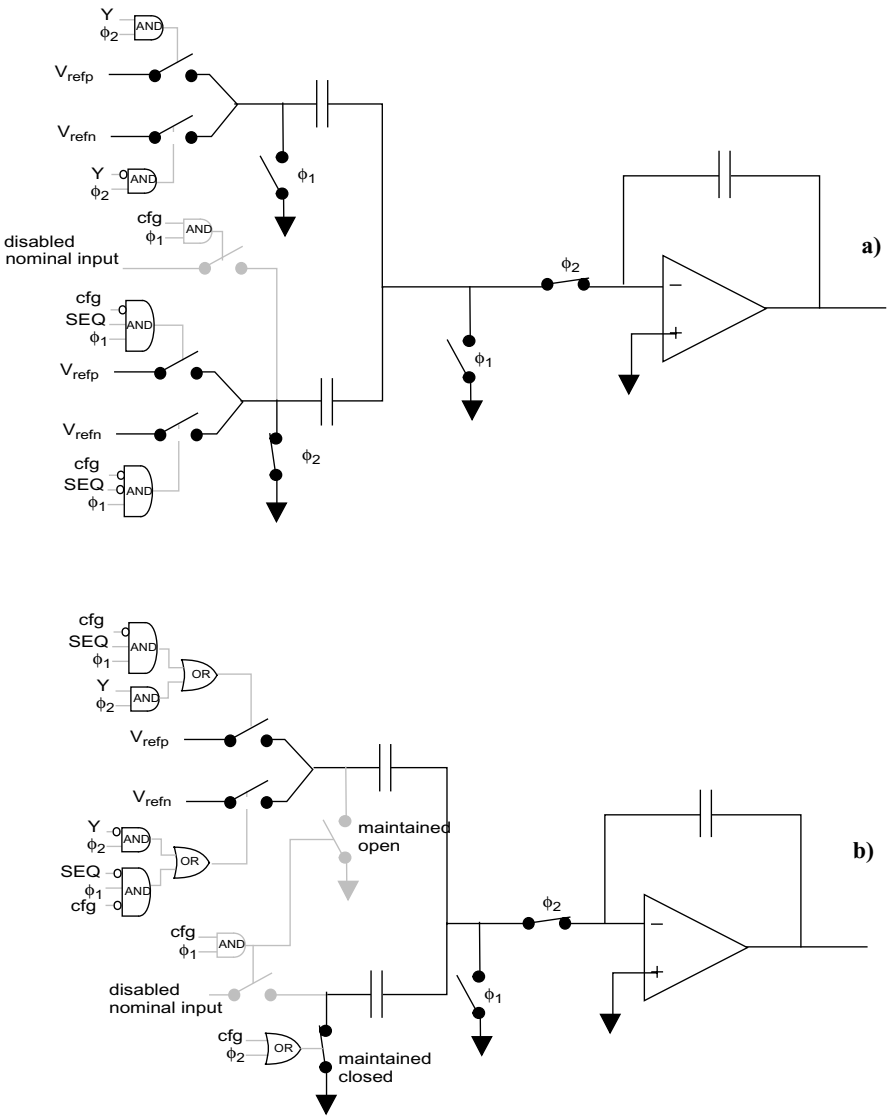


Figure 6-22: Digital sequence input for a double-branch integrator
a) DAC replication at the input branch
b) DAC re-use at the feedback branch

Another solution consists of using only one branch during the test mode and either reusing or replicating the feedback DAC at the feedback capacitor, as seen in case b) of Figure 6-22. In this case, the leakage test could be performed without ther capacitor matching problem.On the other hand, the modified transfer function of the integrator must be taken into account for the signature calculation.

Mixing the two approaches to allow the test sequence to be input in either of the two branches would allow one to test for branch coefficient errors. However, we will let this possibility be studied in future work.

6 • 3 . 2 . 4 Double-sampling integrator

More care has to be taken if the double-branch integrator makes use of double-sampling. Double-sampling is used to relax the capacitor values in fully-differential implementations, as seen in Figure 6-23. As they are used during both phases, their values have to be divided by two to implement the same coefficient as in a single-sampling case.

According to Figure 6-23, the z-domain transfer function of the integrator can be written

$$out = \frac{z^{-1}}{1 - z^{-1}}\left(\frac{2C_1}{C_3}X - \frac{2C_2}{C_3}Y\right). \qquad \textbf{(6-25)}$$

Consider Y in this equation as the DAC output and not as its digital input.

To input the digital test sequence, one solution consists of disabling the double-sampling on the feedback path and driving the DAC with the test sequence during one of the two phases, as seen in Figure 6-24. This may be valid for the leakage test but some care has to be taken as disabling the double-sampling reduces the effective gain of the integrator. During test mode, the transfer function of the integrator of Figure 6-24 becomes

$$out = \frac{C_2}{C_3} \times \frac{z^{-1}}{1 - z^{-1}}(SEQ - Y). \qquad \textbf{(6-26)}$$

The transfer function of the modulator during test mode would thus have to be re-calculated. On the other hand, we have seen that such a modification should be favorable with respect to the integrator output excursion.

In order to avoid the previously commented gain mismatch error between the two branches, an alternative approach consist of using the two branches for both the test

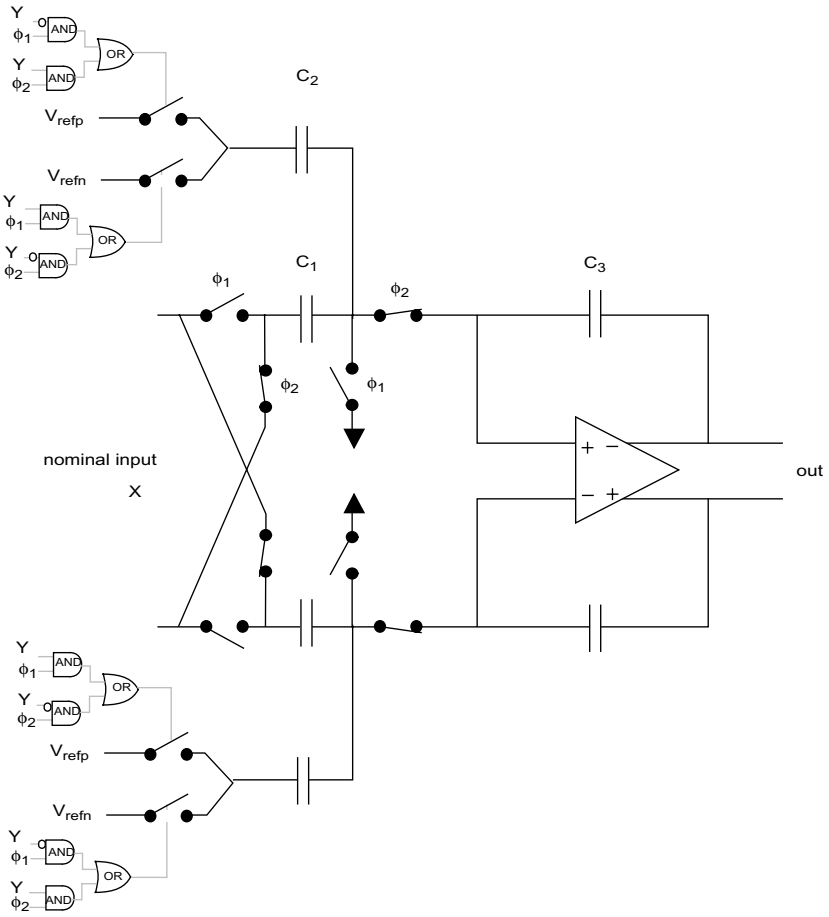


Figure 6-23: Two-branch integrator with double-sampling on both branches

sequence and the feedback, as seen in Figure 6-25. In this figure, this is done by adding an extra signal switch that puts the two capacitors in parallel. In order to avoid switches in series, another solution would consists of replicating the DAC at the nominal input branch and enabling it only during test mode. As a matter of fact, such a modification would also modify the transfer function of the modulator by effectively averaging the two branch coefficients. Indeed, for the integrator of Figure 6-25 and during test mode the transfer function becomes

$$out = \frac{C_1 + C_2}{C_3} \times \frac{z^{-1}}{1 - z^{-1}}(SEQ - Y). \qquad \textbf{(6-27)}$$

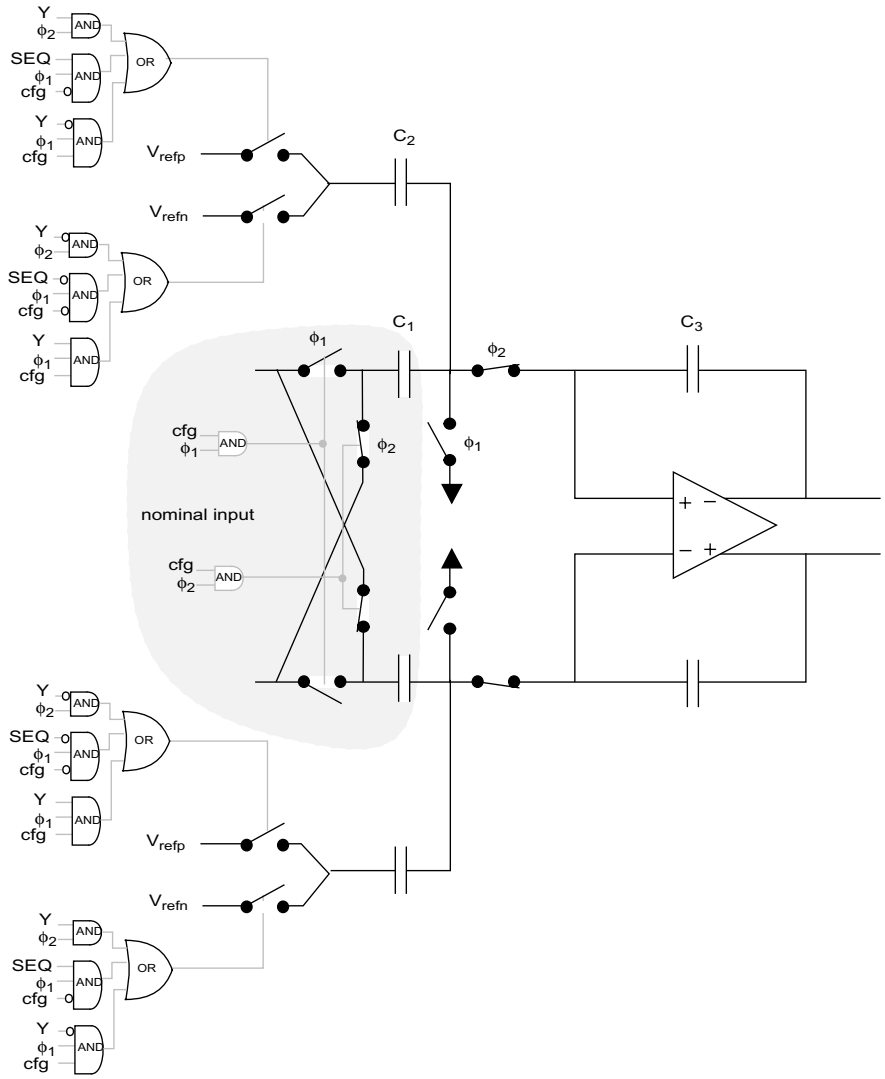


Figure 6-24: Disabling double-sampling to input a digital sequence

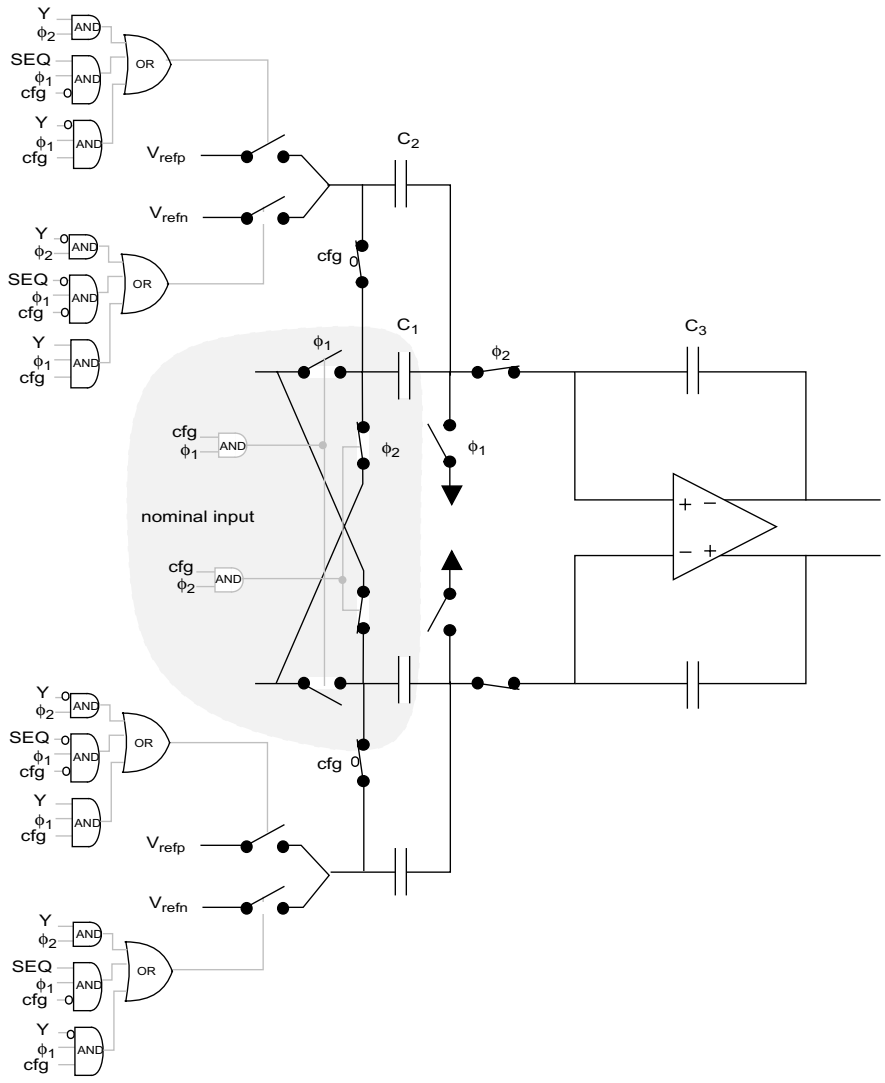


Figure 6-25: Disabling double sampling and connecting both input capacitors.

6 • 3 . 2 . 5 Other architectures

Apart from those already described, there exist other integrator architectures as:

- For instance, an integrator can implement a mix of single/double sampling.
- Dynamic Element Matching is sometimes used either to randomize or modulate unit capacitor mismatch and to provide effective matching when two (or more) different branch coefficients are required.

- The integrator may use a chopped amplifier or correlated double-sampling to avoid an offset. In this case, it would be unnecessary to perform two acquisitions for each test as the offset should be cancelled by design.

Each architecture may require a particular treatment, but the guidelines depicted for the most general cases above should help to find a convenient solution.

6 • 3 . 2 . 6 DAC control implementation

In the previous case studies, DAC switches have been represented as being driven by combinational logic, that involved static configuration signals as well as dynamic signals such as clock phases or digital sequences (the test sequence and the modulator output bit-stream).

In addition to the timing concerns related to clock gating that were discussed in Section 6 • 3 . 1, there are still some points of interest:

- The configuration signal *cfg* is used to select either the nominal configuration, where the DAC is driven only by the modulator output bit-stream, or the test configuration. Hence, it may be interesting to implement such an OR function with transmission gates, that is to say using a multiplexer.
- The clock phases ϕ_1 and ϕ_2 are non-overlapping. This can lead to some simplifications as they will never be at 1 at the same time. For instance, it is possible to implement a wired-OR function.

  These possibilities are illustrated in Figure 6-26 which represents an example of alternative DAC control implemented with transmission gates.

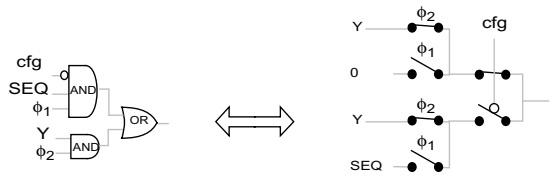


Figure 6-26: Implementation of DAC control with transmission gates

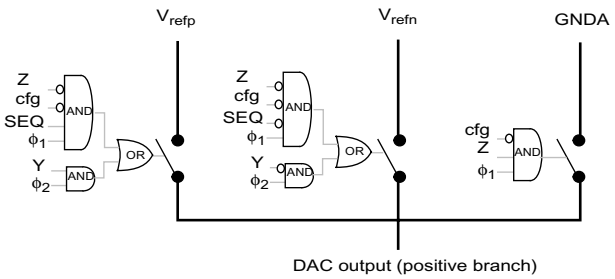


Figure 6-27: Example of implementation of a 3-level test DAC

- The digital sequences have to be properly synchronized. For the modulator output bitstream Y, this is almost straightforward as it usually comes out of a latch that is properly clocked by the modulator phases. However, it must be ensured that the input sequence that drives the DAC does not change in the middle of the active phase (either ϕ_1 or ϕ_2). If the test sequence is generated on-chip, this synchronization may be obtained by design. However, if it is generated by an off-chip pattern generator, the test sequence should be properly sampled and held (by an edge-triggered D-latch for example).

6 • 3 . 2 . 7 Insert zeros in the test sequence

In some test proposals is the previous two chapters, it is necessary to use sequences that introduce an analog zero. Hence a 3-level DAC has to be built instead of a 2-level DAC. Fortunately, most ΣΔ modulator are fully-differential and generating an accurate zero is not a difficult task: the analog ground can simply be sampled by the two branches. The control of the DAC would also have to be modified and the test sequence should be defined with two bits. Figure 6-27 shows an example where the -1/1 sequence is defined by the digital SEQ signal as above and the zero “insertion” is controlled by the digital Z signal. It can easily be seen that the Z signal has priority on the SEQ signal, meaning that when Z is set to 1, the DAC outputs a zero, whatever the value of SEQ.

6 • 3 . 3 Integrator gain scaling

It has been pointed out at the beginning of this chapter that the use of digital sequences as test stimuli may require us to scale down the integrator(s) coefficients in order to avoid integrator clipping. In two-branches integrators with double-sampling, we have seen that disabling double-sampling would effectively divide the integrator gain by two. However, it may be necessary to introduce more flexibility in the choice of the coefficients. A solution also has to be provided for other integrator topologies.

In order to provide good capacitor matching, large capacitors are usually built as an array of identical unit capacitors. Branch coefficient are thus built as fractions of unit capacitors. For instance, if the integrating capacitor is composed of 6 unit capacitors, the sampling capacitor of the first branch of 3 unit capacitors and the sampling capacitor of the second branch of 2 unit capacitor, the first branch coefficient is 1/2 (3/6) and the second branch coefficient is 1/3 (2/6).

A straightforward solution to branch coefficient down-scaling consists of disconnecting part of the sampling capacitors during test mode. For that to be done, an additional switch could be implemented in series with the unit capacitor that has to be disconnected. Another solution would consist of implementing the sampling capacitor as two branches instead of one. These two solutions are represented in Figure 6-28. When the configuration bit (cfg) is set to 0, the gain of the integrator is scaled by a factor 3/4. The first solution (case b) is undoubtedly the simplest. However, the extra switches that are introduced in series with the conventional switches may put additional requirements on the settling during normal operation. In many cases, though, this should not be an issue as the settling bottleneck is much more on the side of the amplifier than on the side of the passive sampling. For demanding cases, the second solution (case c) would give better results as it does not require one to put switches in series. The downside is increased complexity because of the logic gates that have to be introduced and the doubling of the input switches. Notice, though, that the design has to be treated as two-branches. The width of the sampling switches can thus be scaled-down with respect to the original one-branch configuration.

Downscaling branch coefficients may solve the output range issue during the test mode but it appears that, in most cases, it requires one to modify the original design further than

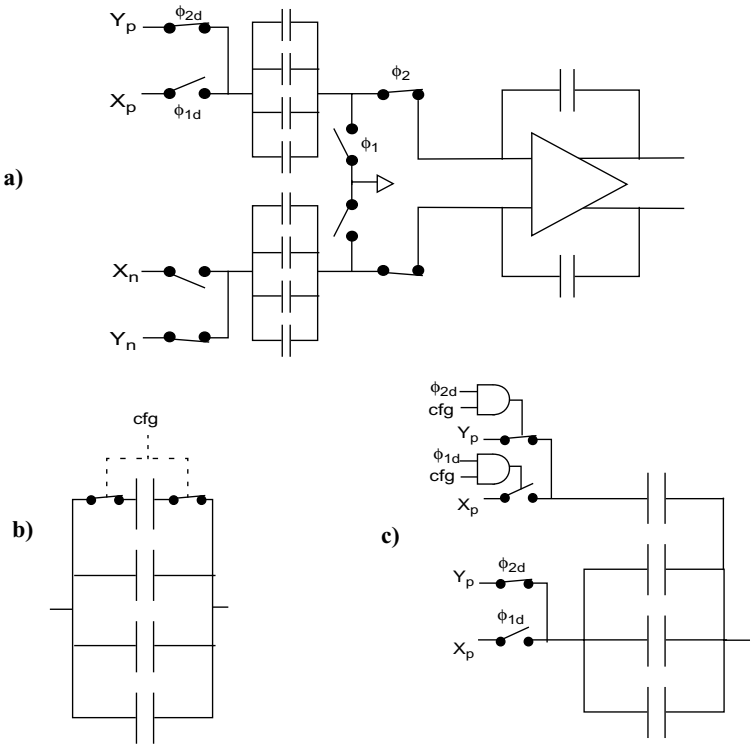


Figure 6-28: a) single-branch integrator;
b) gain scaling by simple capacitor disconnection;
c) gain scaling by reconfiguration into a two-branch integrator.

simple switch control modifications. Furthermore, some capacitors are not used (and thus not tested) during the test. In that sense, branch coefficient downscaling should be considered as the last option unless it relies on a double-sampling reconfiguration.

6 • 3 . 4 Altering the clock phases

For the settling error test that was proposed in Chapter 5, we require that the sampling and integrating phases are modified on a sample basis, as a function of the integrator input. More concretely, the duration of the phases must last twice as much as the nominal for a level 2 (or alternatively -2) at the integrator input.

Level 2 occurs at the integrator input if and only if the input sample is 1 and the feedback sample (i.e. the modulator output sample) is -1. Hence, the modulator clock should be

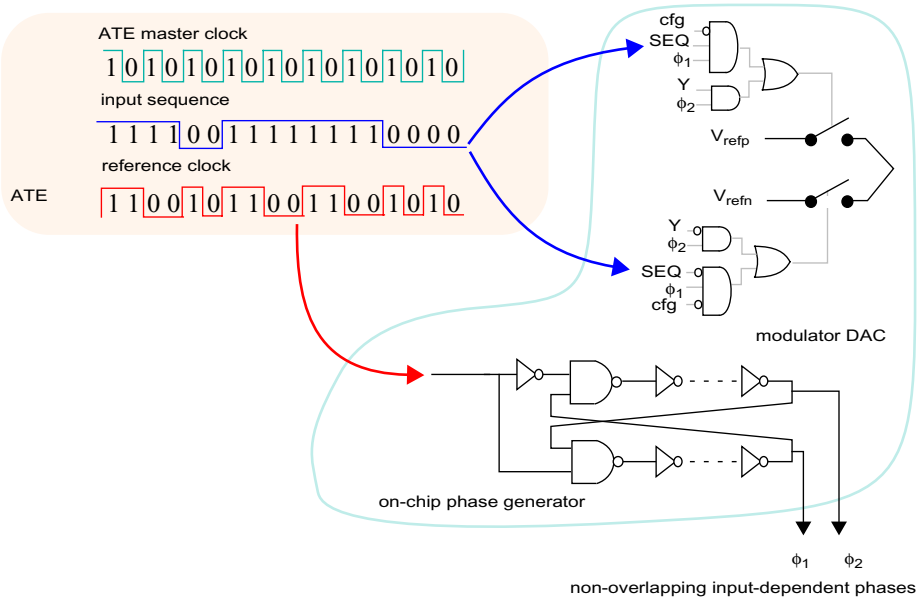


Figure 6-29: Generation of the modulator sampling and integrating phases

modified when such a case is detected. The drawback of this approach is that it requires one to detect the modulator output and generate the correct phases on-the-go. For high operating frequencies this may be troublesome. Fortunately, the scheme can be modified slightly in order to alter the clock phases as a function of the input sequence alone. Indeed, if the phase duration is doubled for all input samples equal to 1, it will necessarily be doubled for a level 2 at the integrator input. It will also be doubled for the level 0 that corresponds to the combination of a 1 input and a 1 feedback. However, the settling error for a level 0 is negligible with respect to the settling error for a level 2, so the doubling of the clock phases for this combination will not have any effect on the signature.

Thanks to this slight correction, the settling error tests can be performed with a simple digital ATE without the need for clocking modifications, as shown in Figure 6-29. ΣΔ modulators necessarily implement a non-overlapping phase generator that ensures the correct synchronization of the different switches. This generator relies on an input reference clock that is provided externally. It is possible to calculate a-priori the modification of the reference clock timing in order to provide the correct phase duration as a function of the digital

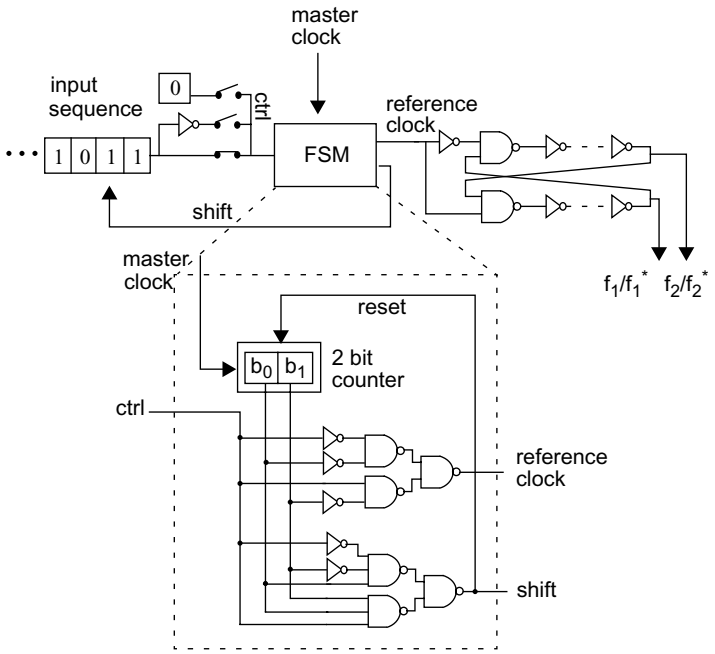


Figure 6-30: Generation of the modulator sampling and integrating phases

input sample. In Figure 6-29, the reference clock and the test sequence are generated for a 1 0 1 1 0 0 sequence. For an 1 input sample the duration of the reference clock period is doubled (and thus equal to two ATE master clock periods) while for a 0 input sample it remains equal to one ATE sequence period.

On the other hand, if the digital tests are to be implemented in a full-BIST scheme, the input sequence, and the sampling and integrating phases ϕ_1* and ϕ_2* have to be generated on-chip. Figure 6-30 shows how they could be generated using a Finite-State-Machine (FSM). A digital multiplexer allows one to select between 3 modes. For the normal operation mode, a zero is sent to the input of the FSM and the phases ϕ_1* and ϕ_2* are independent of the input sequence. For the first test mode, the opposite of the stored sequence is sent to the FSM such that the phases duration is doubled when the input sample is 1. Finally, for the second test mode, the stored sequence is sent to the FSM and the phases duration is doubled when the input sample is a -1 (i.e. a logic 0). As a matter of fact, the FSM presented in Figure 6-30 is nothing other than an input-dependent frequency divider.

This chapter has provided guidelines for the implementation of the test proposal, addressing issues that the designer would meet for its inclusion in a wide variety of cases. The key message of this chapter is that the modifications of the modulator by themselves only concern the control logic for some switches that are not critical for timing. The only extra analog hardware that may be required for test purposes is signal switches (in the case that a three-level DAC had to be introduced, or if the feedback DAC had to be replicated), which will not alter either the performance or the robustness of the modulator. The number of additional logic gates, even including test sequence and signature generation is also insignificant.

7

PROTOTYPE AND EXPERIMENTAL RESULTS

The principal goal of this chapter is to present experimental verification of the proposed test set. For that, a 2-1 cascaded modulator with a sampling clock at 2MHz has been designed and implemented in a AMS 0.35µm CMOS technology for a 3.3V supply.

In the first part of the chapter, the design of the prototype is presented as a particular case of the guidelines provided in previous chapters. Then several experimental results are presented which demonstrate that the proposed test set behaves as expected

7 • 1 PROTOTYPE DESIGN

In order to validate the test proposal, the 2-1 cascaded modulator shown in Figure 7-1 has been chosen. This architecture presents the possibility to re-use the same 0.5 gain integrator. The resulting modulator is not optimized in terms of power because the second and third integrators have less demanding requirements than the first and could be scaled down. On the other hand, re-use of the integrator has no impact on the test strategy and is not required by the test. Apart from the obvious savings in design time, re-using the same integrator also allows us to verify the consistency of the test results for the three integrators. The first stage is thus a single-bit 2^{nd} order modulator like the one proposed by Boser and Wooley in [26]. The second stage is a 1st order single-bit modulator with an integrator gain of 0.5.

In cascaded modulators, the additional stages usually digitize the quantization error of the previous stage. However, this implies that we reconstruct such a quantization error taking into account the quantizer effective gain. Such a reconstruction forces one to use an integrator with at least two branches. As we wanted to re-use the same single-branch integrator as in the first stage, we decided to digitize the input of the first stage quantizer instead of the quantization error. As a result, it can be shown that for the architecture of Figure 7-1 the required reconstruction filter is

$$Y = (z^{-1}Y_1 - 4Y_2)(1 - z^{-1})^2 + z^{-1}Y_1, \qquad \textbf{(7-1)}$$

where Y_1 and Y_2 are the output bit-stream of the first and second stage respectively. With such a filter, the modulator output corresponds to

$$Y = z^{-3}X + 4(1 - z^{-1})^3 E_2. \qquad \textbf{(7-2)}$$

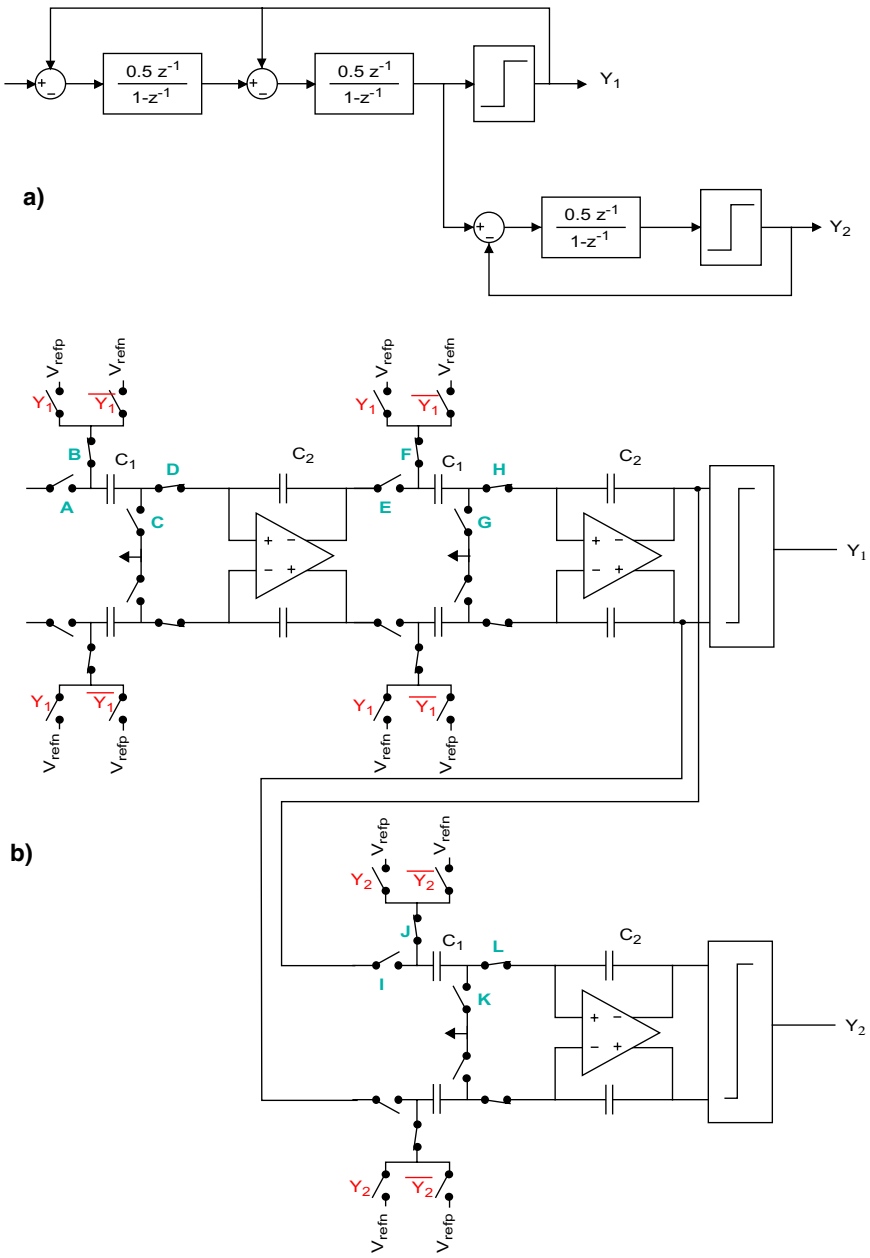


Figure 7-1: 2-1 cascaded ΣΔ modulator
a) z-domain representation
b) switched-capacitor implementation

7 • 1 . 1 Amplifier design: The “fault” injection mechanisms

In order to validate the test and to demonstrate the sensitivity of the proposed signatures to the chosen behavioural parameters, we implement mechanisms that emulate parametric faults.

The proposed tests target parameters that are related to the amplifier. Therefore, we decided to implement an amplifier with tuning inputs that can vary its characteristics. The selected architecture was the folded cascoded amplifier with two tuning inputs shown in Figure 7-2. In this figure the aspect ratios of the different transistors are shown as well as the currents for a balanced input. The first tuning input (V_{tweak1}) controls the bias current of the first stage differential pair through I_1, while the second one (V_{tweak2}) controls the extra current injected in the folded cascoded stage through I_2.

As a fully-differential amplifier, this requires common-mode feedback. For the sake of simplicity, a classical switched-capacitor network was used. In steady-state, the voltage of the common-mode feedback node V_{bias} should match the reference voltage V_{ref}.

Under nominal conditions, that is, when Vtweak1 and Vtweak2 are set to 2.23V, the supply voltage to 3.3V and the temperature to 25ºC, the amplifier performance is as dis-

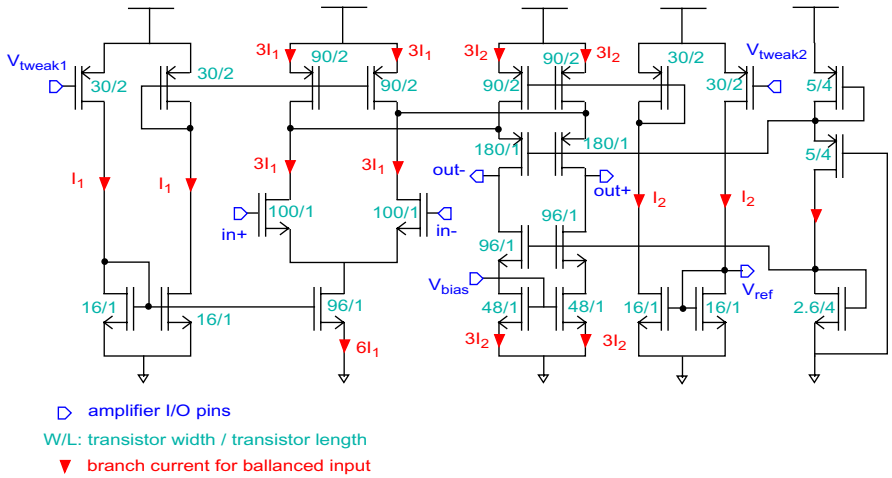


Figure 7-2: Schematics of the amplifier with parametric fault injection mechanism-through V_{tweak1} and V_{tweak2}

played in the second column of Table I. In the same table are also displayed the results obtained in the worst corner cases:

- worst-speed (supply=3V, T=85ºC)
- worst-power (supply=3.6V, T=-20ºC)
- worst-zero (supply=3.3V, T=25ºC)
- worst-one (supply=3.3V, T=25ºC)

Monte-Carlo simulation also showed that the maximum offset should be 5mV.

Table I: amplifier behavioural parameters at the process corners

parameter	nominal	worst-speed	worst-power	worst-zero	worst-one
DC gain	83dB	97dB	58dB	70dB	88dB
Gain-Bandwidth	78MHz	8MHz	210MHz	106MHz	58MHz
Slew-rate	82V/µs	54V/µs	208V/µs	110V/µs	70V/µs
Output range at half DC gain	+/- 1.71V	+/- 1.52V	+/- 1.65V	+/- 1.55V	+/- 1.82V

These performance parameters of the amplifier vary over a broad range with the two tuning voltages, V_{tweak1} and V_{tweak2}. This can be seen in Figure 7-3 which shows the variation of the amplifier DC gain, gain-bandwidth product and slew-rate as functions of the tuning voltages. Roughly speaking, we can say that varying V_{tweak2} mostly influences the amplifier DC gain while varying V_{tweak1} mostly affects the amplifier dynamics (i.e. the GBW and SR). For Figure 7-4 the two tuning inputs were set to the same voltage and that voltage was varied from 1.7V to 2.6V; hence, this corresponds to the parameter values on the diagonals of Figure 7-3.

Although the inclusion of the tuning inputs require 6 additional pads in the prototype (2 for each amplifier), these pads are necessary only to validate the tests but they do not form part of the test hardware requirements.

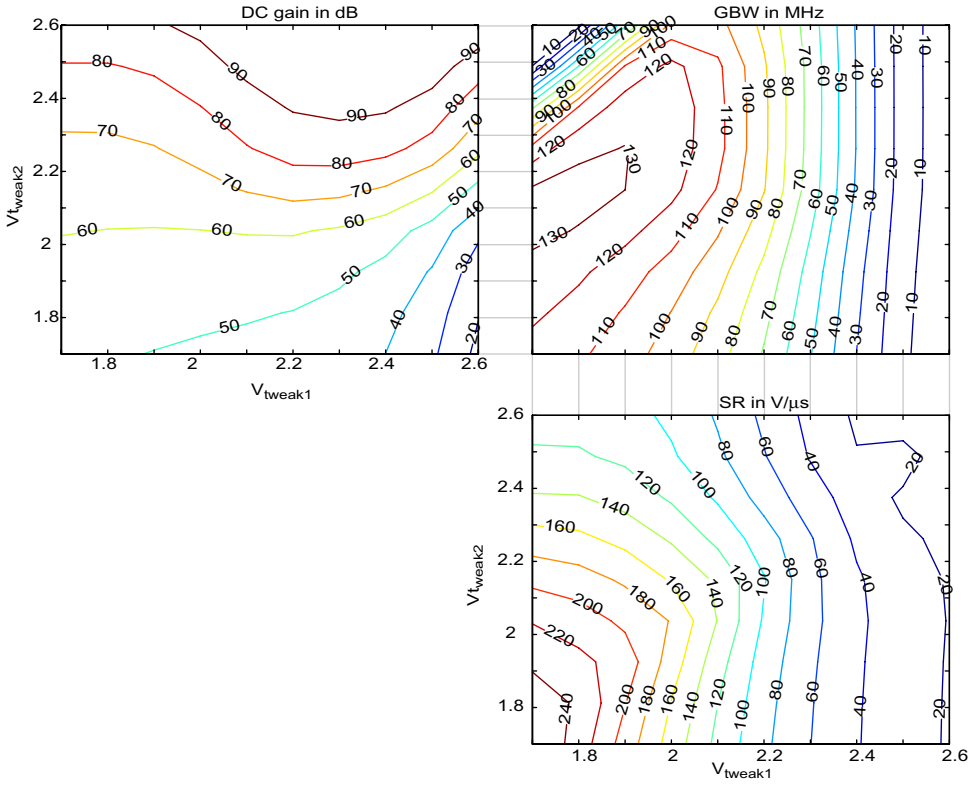


Figure 7-3: **Iso-levels of amplifier parameters when varying the two tuning inputs**

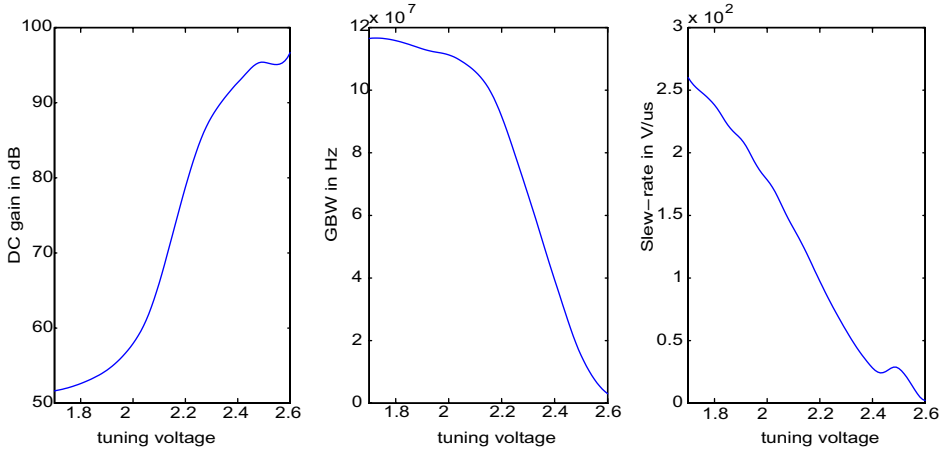


Figure 7-4: **Amplifier characteristics versus tuning voltage for V_{tweak1}=V_{tweak2}**

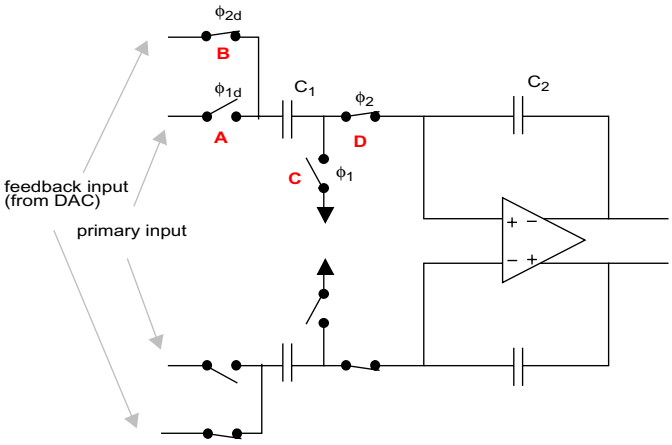


Figure 7-5: Single-branch integrator

7 • 1 . 2 The integrator

The integrator that is re-used across the modulator is depicted in Figure 7-5. It is a single-branch integrator that implements a gain of 0.5. The value of the unit capacitor was 0.4pF. The input capacitors use 2 unit capacitors and the feedback capacitors use 4 unit capacitors. All the switches are CMOS. Their resistance varies in the range 2-8.8kΩ for DC operating points varying between 0.65V and 2.65V, which represents twice the modulator full-scale. In the worst-speed corner, the maximum resistance increases up to 18kΩ. In the worst case, the RC passive sampling time constant, considering two switches in series with the input capacitor, is close to 30ns, which is one eighth of the sampling duration (one half of a period of 2MHz clock).

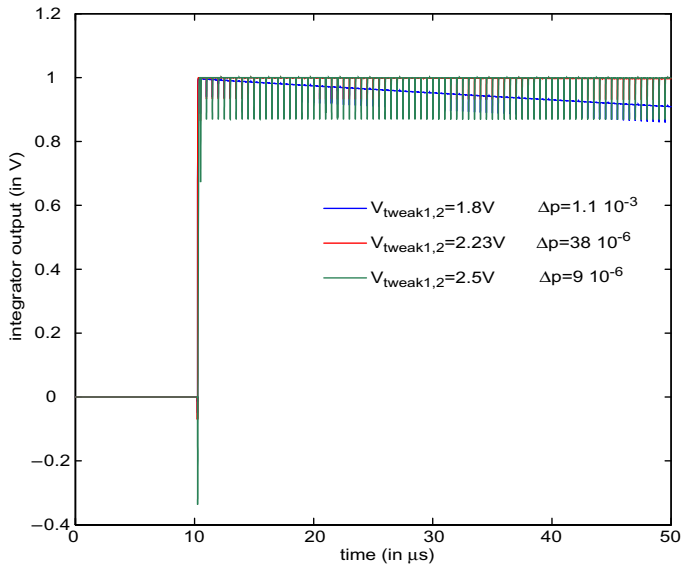
For the single-branch fully differential architecture, the thermal noise contribution related to sampling can be written as

$$P_{th} = \frac{k_B T}{OSR \times C_{in}}. \qquad \textbf{(7-3)}$$

Considering a OSR of 50 and a Full-Scale of +/- 1V, this leads to a maximum SNR slightly greater than 16bits.

If we consider the contributions of the amplifier referred noise, we find that the total input-referred thermal noise would lead to a maximum SNR of about 15bits (for the same OSR and Full-Scale).

a)



b)

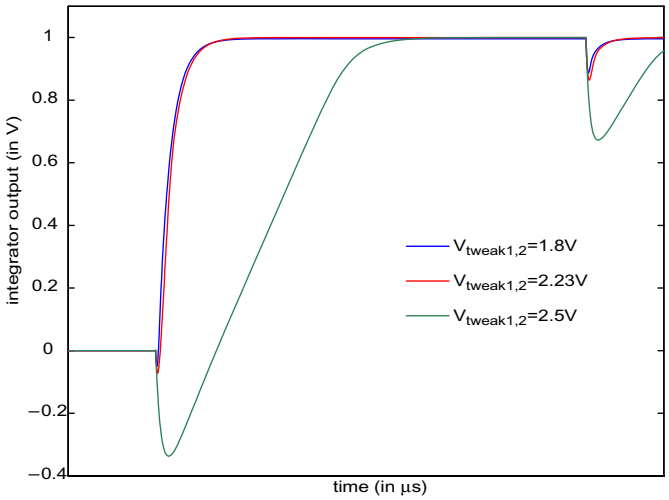


Figure 7-6: Integrator response to an input pulse, for 3 values of the tuning voltages
a) full-scale representation
b) close-up on the step edge

In order to see the effects of the amplifier tuning voltages at the integrator level, Figure 7-6 shows the transient response of the integrator to an impulse. This transient response was obtained from post-layout simulation. For an ideal integrator, the response should be a perfect step, but due to leakage the step exhibits a small decay. The integrator pole error can be measured from the slope of this decay. As could be expected, it can be seen that the decay and the integrator settling vary with the tuning voltage. For the two highest value of the tuning voltages (V_{tweak1}=V_{tweak2}=2.23V or 2.5V), the difference in slope cannot be distinguished on the figure but can be measured. Conversely, the decay for the lowest tuning voltages can easily be appreciated on Figure 7-6 case a). On the other hand, it can be seen on Figure 7-6 case b) that the settling of the integrator is slower for the highest value of the tuning voltages. In particular, it can be seen how the Slew-Rate has decreased. For the two lowest values, only small settling differences can be appreciated in the figure.

7 • 1 . 3 The phase generator

Four phases and their inverses are used to drive the integrators properly. The two main non-overlapping phases ϕ_1 and ϕ_2 define the sampling instants. Two additional phases ϕ_{1d} and ϕ_{2d} are also generated which differ from ϕ_1 and ϕ_2 in having a slightly delayed falling edge. These are used to disconnect the front-end switches slightly after the switches that are connected to the amplifier input. In that way, the latter are the switches that define the effective sampling instants, and signal-dependent charge injection is minimized. The clock generator is represented in Figure 7-7.

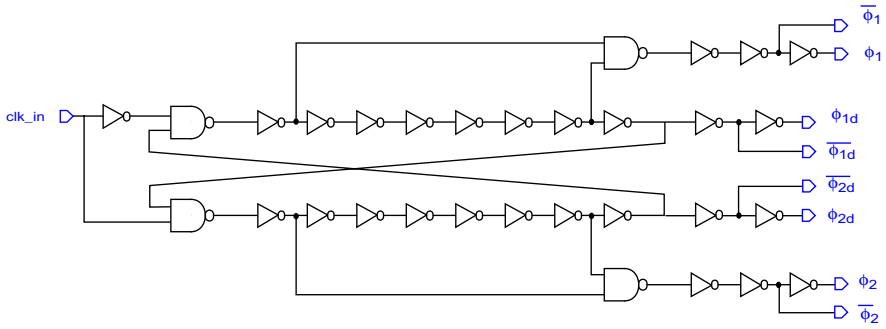


Figure 7-7: Non-overlapping phase generator

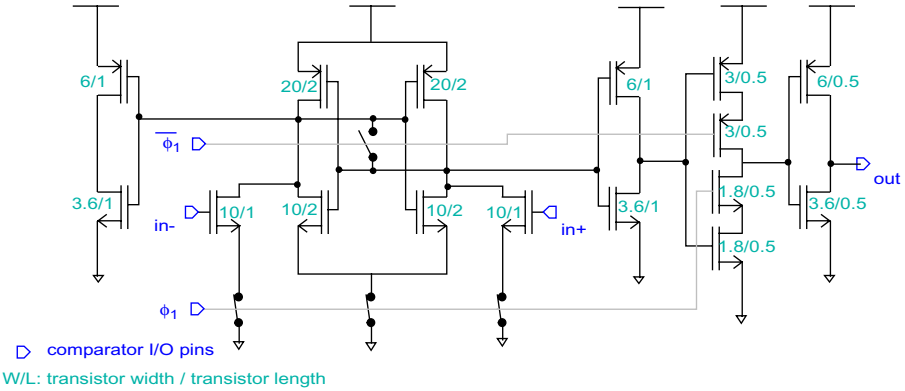


Figure 7-8: Comparator schematics

7 • 1 . 4 The comparator

The comparator is a simple dynamic latch, as represented in Figure 7-8, since its offset is not critical for proper operation of the modulator. Actually, the main consequence of the comparator offset is that it will shift by the same amount the mean value of the preceding integrator output. Taking into account that the variations of the integrator output remain unchanged, the comparator offset can slightly modify the output range requirements. Following the comparator, a D-latch cell samples and holds the data such that the feedback is provided with the correct delay.

Monte-Carlo simulations show that the maximum (3σ) offset is lower than 60mV, which is sufficiently low to be tolerated by the output range of the integrator.

7 • 1 . 5 The DfT modification

For the design of our prototype, it was preferred to generate the test sequences and the signature off-chip. This gives much more flexibility for validation purpose than implementing a limited number of on-chip sequences and fixed-length counters.

The possibility to introduce an analog zero in the test sequence was also added to the prototype and two test pads are thus required to define the sequence. The output bit-streams of the two stages are readily accessible as the reconstruction filter is also implemented in

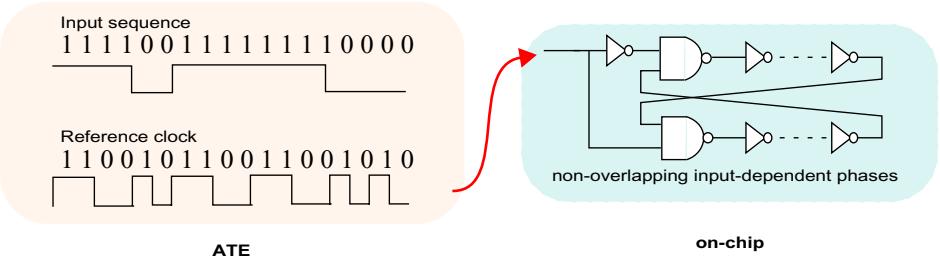


Figure 7-9: Generation of the modulator sampling and integrating phases

software. Hence, the test signatures can also be computed off-chip as both the test sequence and the output bit-stream are available.

Figure 7-9 illustrates how the reference input-dependent clock can be pre-calculated in software, as was commented in the previous chapter. The tests can thus be carried out with simple digital equipment; the only additional requirements are the modulator switching modifications.

7 • 1 . 5 . 1 Disabling nominal input and enabling digital test input

In order to send a sequence to the first integrator, switch A in Figure 7-1 (or Figure 7-5) is kept open and switch B is kept closed. Notice that for our prototype we decided not to implement the sampling function of switch B within the DAC. Hence, the DAC multiplexer will be in series with switch B.

This modification is implemented by simple logic gates:

$$\begin{aligned} A &= \phi_{1d} \cdot en_1 \\ B &= \overline{\overline{\phi_{2d}} \cdot en_1}. \end{aligned} \qquad \textbf{(7-4)}$$

A control signal en_1 is needed to select the operating mode. Similarly, a digital sequence can be sent to the second integrator by maintaining switch E (in Figure 7-1) open and switch F closed (another control signal en_2 is needed). Notice that, by doing so, the first stage is reconfigured as a 1^{st} order modulator for test purposes. The case of the second stage (i.e. the third integrator) is identical and a control signal en_3 is introduced. As the switches used are CMOS, they need the control signal and its inverse so a NAND gate and an inverter are used for both switches, as shown in Figure 7-10.

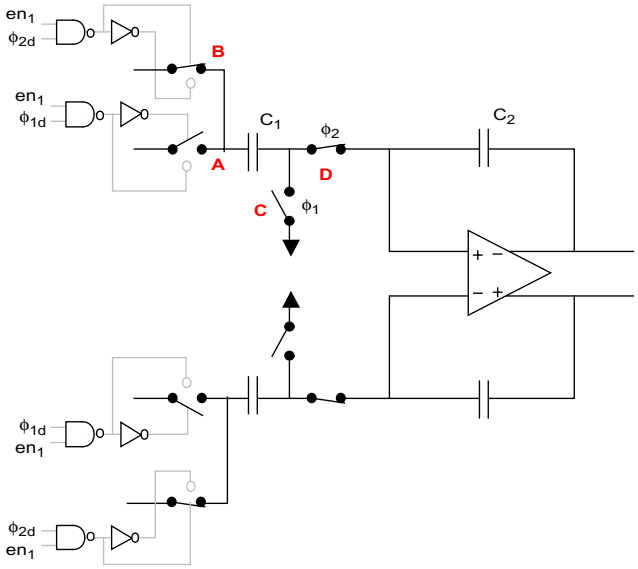


Figure 7-10: Modification of the integrator switch control to enable the test input

7 • 1 . 5 . 2 The Digital-to-Analog converter

The DAC controls also have to be modified. For the modulator without test features, the DAC would be a simple multiplexer driven by the modulator output bit-stream. As it was desired to build a prototype that is as flexible as possible, the DAC was modified to implement a number of possibilities that go beyond those that are strictly required for the proposed test validation. First of all, the DAC has three levels in order to insert zeros in the sequence. During the sampling phase, the DAC is driven by a digital test sequence. During the feedback phase, the DAC is controlled by one of the following:

- the corresponding stage output bit-stream (Y_1 for the first stage and Y_2 for the second stage),
- a delayed version of this output bit-stream (further noted dY_i),
- the other stage output bit-stream (Y_2 for the first stage and Y_3 for the second stage),
- a digital test sequence (that is composed by two bits SEQ and Z)

Two configuration bits ($F_{sel0,1}$) are thus necessary to select the proper feedback mode. Figure 7-11 represents the positive branch of the modified DAC. The modulator is fully dif-

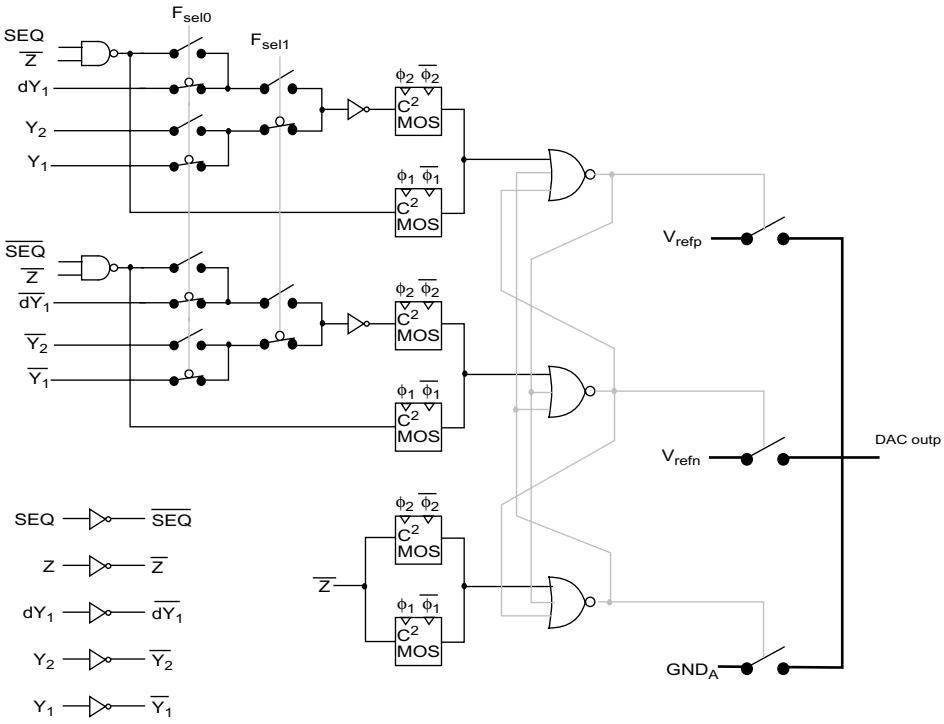


Figure 7-11: Positive branch of the DAC modified for test purpose

ferential and the negative branch is easily deduced from the positive one: only the positive reference voltage V_{refp} and the negative reference voltage V_{refn} have to be inverted. The logic equations that control the switches can be written as,

$$V_{refp} \leftarrow \begin{pmatrix} (SEQ \bullet \overline{Z}) \bullet F_{sel0} \bullet F_{sel1} \\ \ldots + (dY_1) \bullet \overline{F_{sel0}} \bullet F_{sel1} \\ \ldots + (Y_2) \bullet F_{sel0} \bullet \overline{F_{sel1}} \\ \ldots + (Y_1) \bullet \overline{F_{sel0}} \bullet \overline{F_{sel1}} \end{pmatrix} \bullet \phi_2 + (SEQ \bullet \overline{Z}) \bullet \phi_1$$

$$V_{refn} \leftarrow \begin{pmatrix} (\overline{SEQ} \bullet \overline{Z}) \bullet F_{sel0} \bullet F_{sel1} \\ \ldots + (\overline{dY_1}) \bullet \overline{F_{sel0}} \bullet F_{sel1} \\ \ldots + (\overline{Y_2}) \bullet F_{sel0} \bullet \overline{F_{sel1}} \\ \ldots + (\overline{Y_1}) \bullet \overline{F_{sel0}} \bullet \overline{F_{sel1}} \end{pmatrix} \bullet \phi_2 + (\overline{SEQ} \bullet \overline{Z}) \bullet \phi_1 \quad \textbf{(7-5)}$$

$$GND_A \leftarrow Z \bullet \phi_2 + Z \bullet \phi_1$$

A multiplexer driven by two configuration bits is used to select the correct feedback. Transmission gates can be used because the control signals are static. Due to the fact that ϕ_1 and ϕ_2 are non-overlapping phases, the main OR operation in Eq (7-5) could be implemented as a wired-OR thanks to C^2MOS cells that also provide the proper synchronization of the DAC switches. As can be seen in Figure 7-12, the value of the direct signal (i.e. the test sequence) is sampled and held at the rising edge of ϕ_1 while the value of the feedback signal is sampled and held at the rising edge of ϕ_2. In order to make sure that two of the three DAC switches will never be closed at the same time, NOR gates with crossed outputs are used.

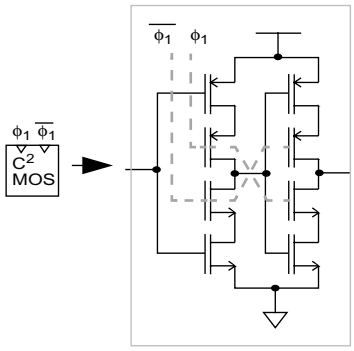


Figure 7-12: C^2MOS cell details

7 • 1 . 5 . 3 The configuration register

In our prototype, nine static controls, one to select a digital input ($en_{1,2,3}$) and two to select the feedback mode for each of the three integrators ($F_{sel0–1,2,3}$, $F_{sel1–1,2,3}$), are thus necessary to control the operating modes. These are stored in a register in order to save test-dedicated pads. Two pads are used for the signal that enables register writing and for the serial register input. This register is represented in Figure 7-13

Actually, the prototype was designed to be as flexible as possible, but only a few configurations are of interest for the validation purpose of this thesis. A summary of configurations is given in Table II.

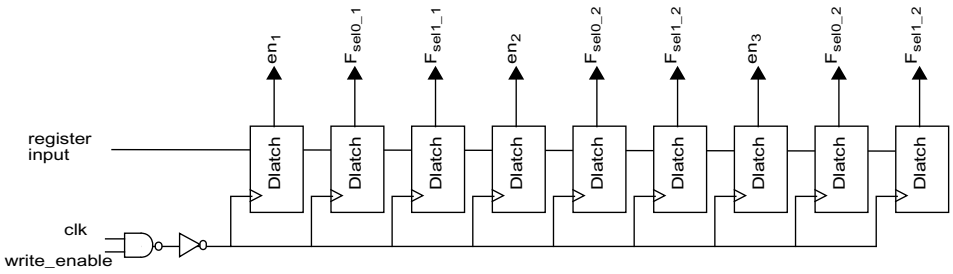


Figure 7-13: Test configuration register

Table II: Useful configuration register combinations

en_1	Fsel0_1	Fsel1_1	en_2	Fsel0_2	Fsel1_2	en_3	Fsel0_3	Fsel1_3	configuration purpose
1	0	0	1	0	0	1	0	0	nominal ΣΔ modulator operation
0	0	0	1	0	0	?	?	?	leakage or settling test for the 1st integrator
?	?	?	1	0	1	?	?	?	leakage or settling test for the 2nd integrator (an extra delay is introduced in the feedback)
?	?	?	?	?	?	0	0	1	leakage or settling test for the 3rd integrator (an extra delay is introduced in the feedback)
?	?	?	0	0	0	?	?	?	settling test for the 2nd integrator, or leakage test using sequences with zeros
?	?	?	?	?	?	0	0	0	settling test for the 3rd integrator, or leakage test using sequences with zeros
?	?	?	0	1	0	0	0	0	reconfigures the 2nd and 3rd integrators into a 2nd order modulator for either leakage or settling test of the 2nd integrator

In this table, the wildcard ? is used to indicate that the value of this configuration bit is not a concern for the purpose that is quoted for that configuration. As can be seen, it is possible to make some test in parallel, such as for instance testing the 3rd integrator (i.e. the second stage) in parallel with the 1st or the 2nd integrator. Figure 7-15 shows how the ΣΔ modulator would be configured to test for integrator leakage in the 1st integrator and the 3rd one. The parts in gray show the paths that are disabled during test mode.

Only the last line in Table II concerns an “odd” configuration. The possibility to select the “other stage” bit-stream for the feedback allows us to reconfigure the 2nd and 3rd integrator into a second-order modulator (for test purpose only). This possibility is illustrated in Figure 7-14.

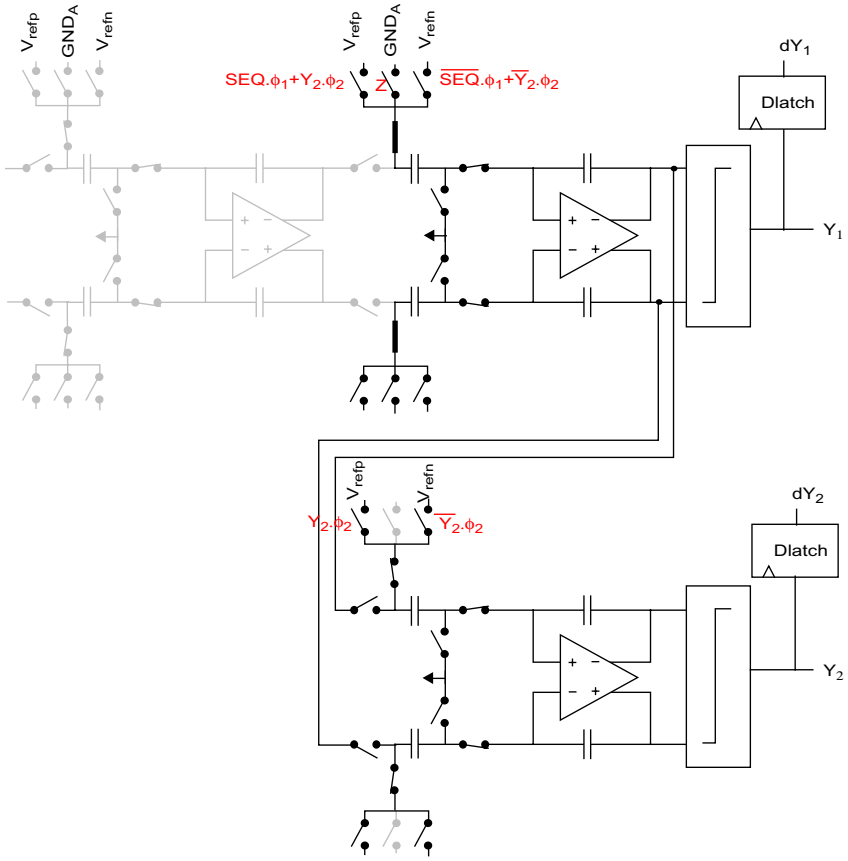


Figure 7-14: The ΣΔ modulator reconfigured such that the 2nd and 3rd integrators form a 2nd order modulator

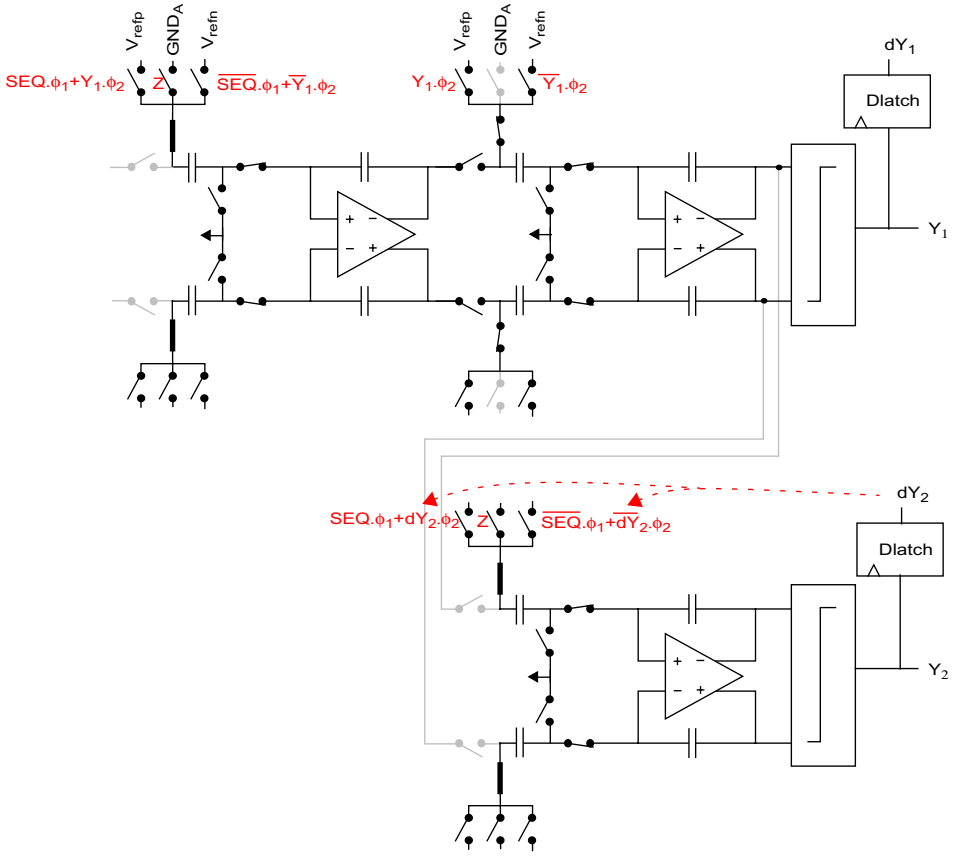


Figure 7-15: The ΣΔ modulator reconfigured to test the leakage of the 1st and 3rd integrators in parallel

7 • 1 . 6 Prototype layout and floor-planning

The prototype has been laid out following the recommended guidelines for mixed-signal circuits. Purely analog parts are separated from mixed-signal and digital parts by the capacitor array. The outer paths in the digital buses were set to the digital ground to provide good shielding and the routing of digital lines was done with care.

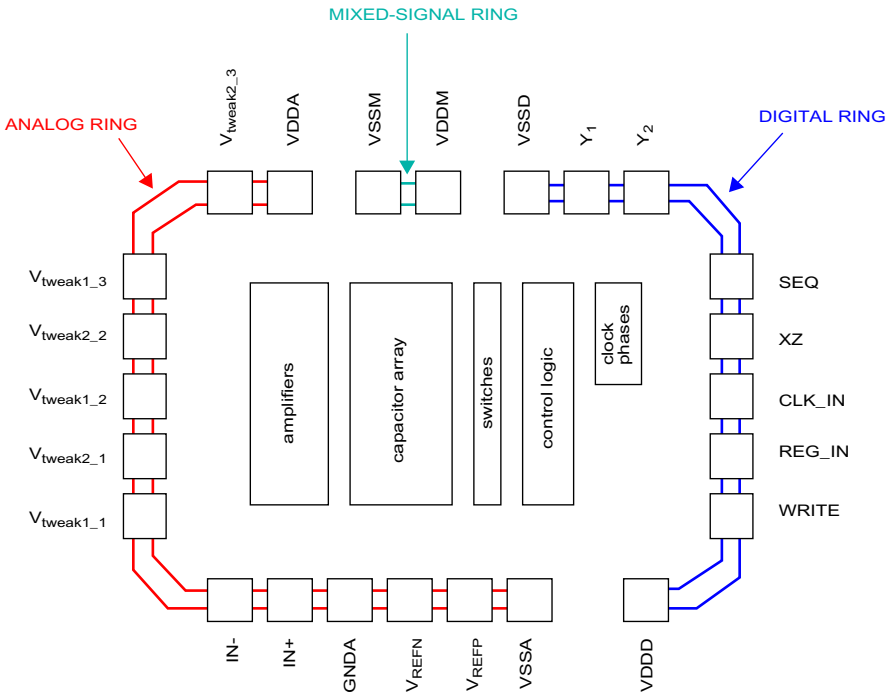


Figure 7-16: Chip floorplanning

Figure 7-16 shows a diagram of the chip floor-planning and Figure 7-17 a microphotography of the chip. The core area is 400µm x 500µm. Notice that three different polarization rings were used to avoid supply noise in critical analog sections.

A description of the different pins can be found in Table III. Notice that the 6 pins that correspond to the tuning voltage are not a requirement of the test method. They are used in our prototype for validation purpose. As we decided to provide the digital input internally, 4 pins are dedicated to test: the configuration register input (REG_IN), the write enable (WRITE), and the two pins that are used to define the test sequence (SEQ and XZ).

Table III: Pin description

Pin name	Description
VSSA	Analog negative power supply (0V)
V_{REFP}	Positive reference voltage for the modulator Full-Scale (2.15V typ.)
V_{REFN}	Negative reference voltage for the modulator Full-Scale (1.15V typ.)
GNDA	Mid-scale (Common-mode) reference voltage (1.65V typ.)
IN+	Modulator conventional input, positive branch
IN-	Modulator conventional input, negative branch
V_{tweak1_1}	1^{st} tuning voltage (V_{tweak1}) for the 1^{st} amplifier
V_{tweak2_1}	2^{nd} tuning voltage (V_{tweak2}) for the 1^{st} amplifier
V_{tweak1_2}	1^{st} tuning voltage (V_{tweak1}) for the 2^{nd} amplifier
V_{tweak2_2}	2^{nd} tuning voltage (V_{tweak2}) for the 2^{nd} amplifier
V_{tweak1_3}	1^{st} tuning voltage (V_{tweak1}) for the 3^{rd} amplifier
V_{tweak2_3}	2^{nd} tuning voltage (V_{tweak2}) for the 3^{rd} amplifier
VDDA	Analog positive power supply (3.3V typ.)
VSSM	Mixed-signal negative power supply (0V typ.)
VDDM	Mixed-signal positive power supply (3.3V typ.)
VSSD	Digital negative power supply (0V typ.)
Y_1	First stage (2^{nd} order section) output bit-stream
Y_2	Second stage (1^{st} order section) output bit-stream
SEQ	Test sequence: a logic 1 sends an analog 1 and a logic 0 sends an analog -1
XZ	Negated of the zero insertion: a logic 1 has no effect, a logic 0 inserts an analog 0 in the sequence, overriding the SEQ signal
CLK_IN	Master clock at 2MHz typ.
REG_IN	Configuration register serial input
WRITE	Register write enable
VDDD	Digital positive power supply (3.3V typ.)

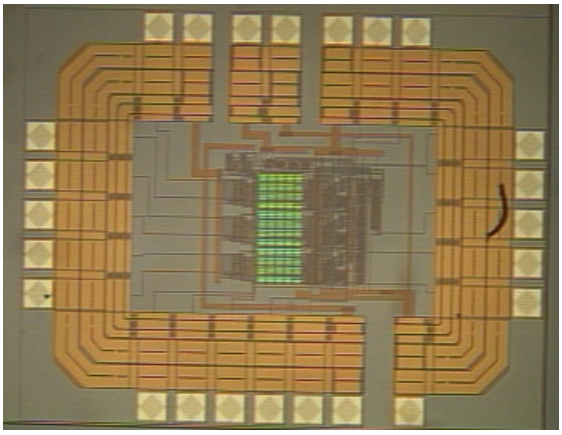


Figure 7-17: Stripped silicon photography

7 • 2 PROTOTYPE TESTING

Due to the modularity of the prototype and the wide range of possibilities offered by the test proposals, it would be an arduous task to make an exhaustive validation varying all the possible parameters:

- which integrator is tested
- which mean value is chosen for the input sequence
- insert zeros or not
- vary the two tuning voltages
- modify the full-scale of the modulator
- modify the operating frequency

Hence, we will try to present the most significant results in order to illustrate the different proposals.

7 • 2 . 1 The test setup

An HP 16500 was used to provide the test sequences, the reference clock and to program the on-chip register that defines the modulator configuration. A LaCroy WaveSurfer 434 digital oscilloscope was used to acquire the output bit-streams of the two stages. The

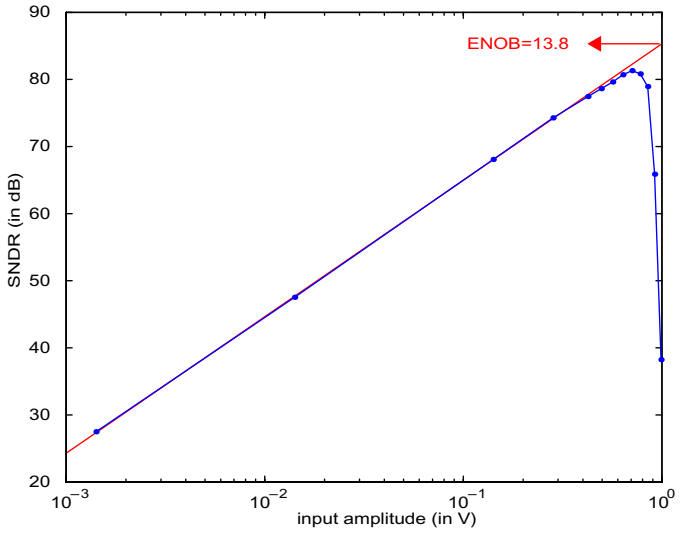


Figure 7-18: SNDR versus input sine-wave amplitude, for an OSR of 50

reconstruction filter was emulated in MATLAB. A Tektronix differential oscillator was used as the regular input of the converter.

7 • 2 . 2 Nominal performance

Figure 7-18 shows the Signal-to-Noise-and-Distortion Ratio (SNDR) of the prototype versus the input sine-wave amplitude, for a tuning voltage set at its nominal value of 2.23V and an Over-Sampling Ratio (OSR) of 50. The prototype reaches 13.8 Effective Number Of Bits (ENOB) for an Over-Sampling Ratio (OSR) of 50. This is approximately 0.4 bits below the ENOB for an ideal modulator. For higher OSR, the resolution improvement is limited by the thermal noise floor of the test setup.

Figures 7-19, 7-20 and 7-21 are examples of the measured output spectra for three different input amplitudes. The gray rectangles in the figures denote the parts of the spectra above the cut-off frequency defined by the OSR that are not considered in the SNDR calculation. For each of these figures, a high performance Rife-Vincent window was used to avoid spectral leakage because coherent sampling was not possible for this test setup. It can be seen how the quantization noise is shaped by the 3^{rd} order function. However, for

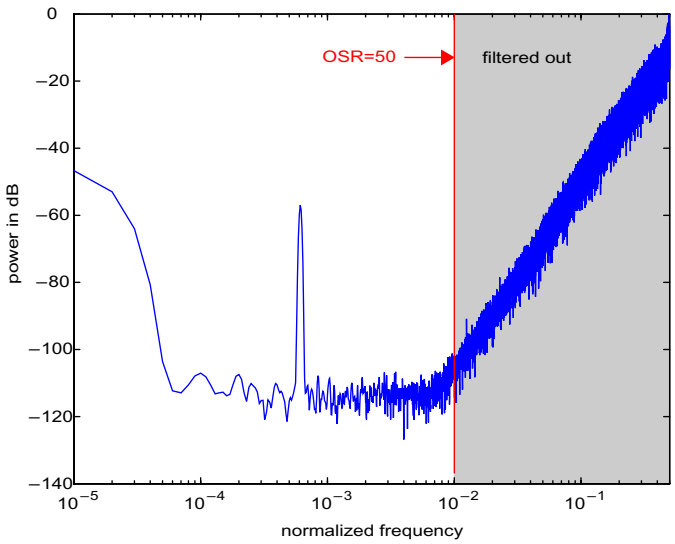


Figure 7-19: Nominal ΣΔ output spectrum for a 1mV$_{rms}$ input sine-wave

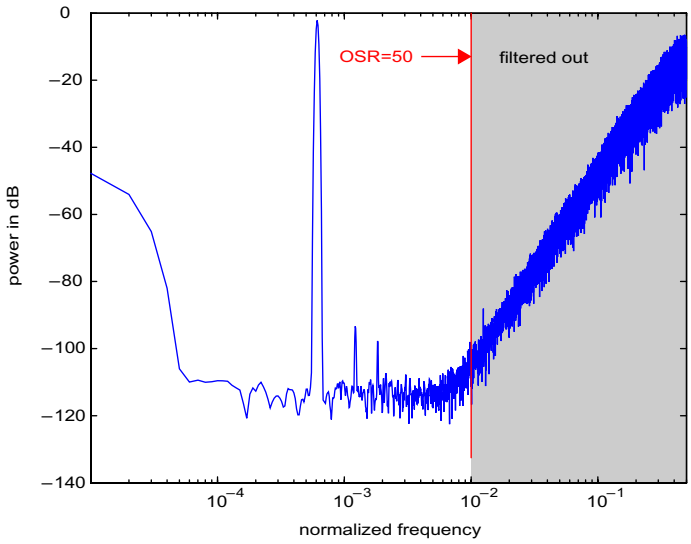


Figure 7-20: Nominal ΣΔ output spectrum for a 550mV$_{rms}$ input sine-wave (i.e. 78% of full-scale)

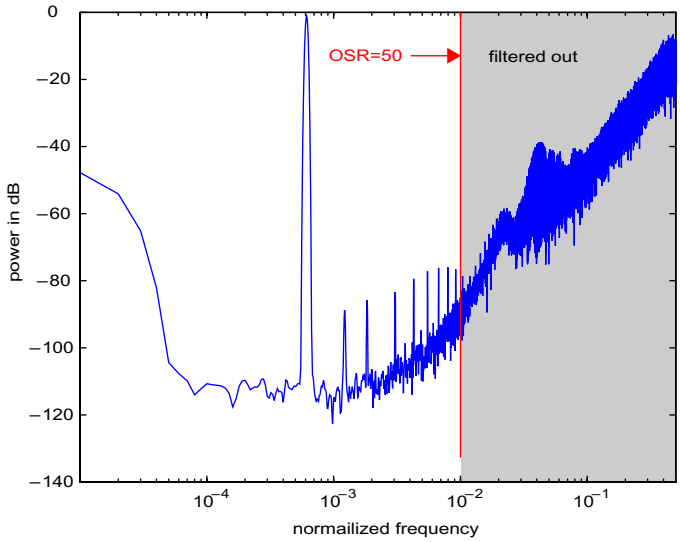


Figure 7-21: Nominal ΣΔ output spectrum for a 650mV$_{rms}$ input sine-wave (i.e. 92% of full-scale)

Figure 7-21 (the 650 mV rms amplitude), note that the modulator overloads, leading to a significant amount of distortion and an alteration of the noise shaping. This is not surprising because the internal states of the 2nd order modulator that composes the first stage begin to increase greatly for inputs above approximately 70% of the full-scale (this could be seen in Figure 6-1 of previous chapter).

7 • 2 . 3 Leakage tests

7 • 2 . 3 . 1 Signature inspection

First of all, let us verify that the test signature behaves as expected, at least in a qualitative manner. For that, a sequence of the form [1 1 1 1 1 1 -1] (and its opposite), with mean value 2/3 (-2/3 respectively), was applied to the modulator. According to Table II, the test configuration register was set at 000100001, which means that the first and third integrators are tested in parallel, as show in Figure 7-15. The tests that are carried out correspond, in the test summary of appendix A, to test 1 for the 1st integrator and test 3 for the 3rd integrator. A

total of 40000 samples of the input sequence and the output bit-streams (from both stages) were acquired for each run (i.e. for the positive sequence and its opposite).

Figure 7-22 a) shows the cumulative sum of the difference between the input sequence and the output bit-stream for the first stage. Note how the deviation between the input and the output accumulates linearly with time as expected. In part b) of the figure, the two acquisitions are combined to separate the contribution of the offset and the leakage.

For the test of the 1^{st} integrator leakage, not much more information than the linearity of the signature with time can be drawn from visual inspection. For the 3^{rd} integrator, in turn, things are different. The same concept of signature linearity can be verified, as seen in Figure 7-23. Moreover, the leakage test for first order modulators relies on a deterministic pattern at the integrator output and by extension at the modulator output. It has been seen in Section 4 • 1 . 3 . 3 that when a 1^{st} order modulator (with an extra delay in the feedback loop) is submitted to a sequence of period L with only one -1 (or alternatively only one 1), the output pattern should be of period 2L with 2(L-1) consecutive 1s (alternatively -1) and 2 consecutive -1s. This can be verified experimentally as illustrated in Figure 7-24 that represents a portion of the output bit-stream for two different input sequences. We verified that this pattern was maintained throughout the acquisition, anywhere between two transitions. It has been seen that integrators'leakage induces a decay in the integrator output patterns that in turn leads to transitions that break the output bit-stream pattern. Such transitions should also follow a given behaviour. Such behaviour was derived in Figure 4-10 where we showed that these transitions introduce a +2 in the cumulative sum of the input/output difference. Actually, Eq (4-72) stated that the leakage signature at the end of the acquisition was equal to 2 multiplied by the number of transitions observed during the acquisition.

Such a transition in the bit-stream is represented in Figure 7-25, and corresponds to experimental data for an input sequence of mean value 2/3. It can be seen that the transition behaviour is not exactly the one that was expected. However, noise was not taken into account during the theoretical analysis, which can explain the observed difference. Furthermore, what is important is that the transition, even if it has a different shape than expected still induces a +2 count in the cumulative sum of the input/output difference. Once again, this could be verified for all the transitions across the acquisition. This can be expected from

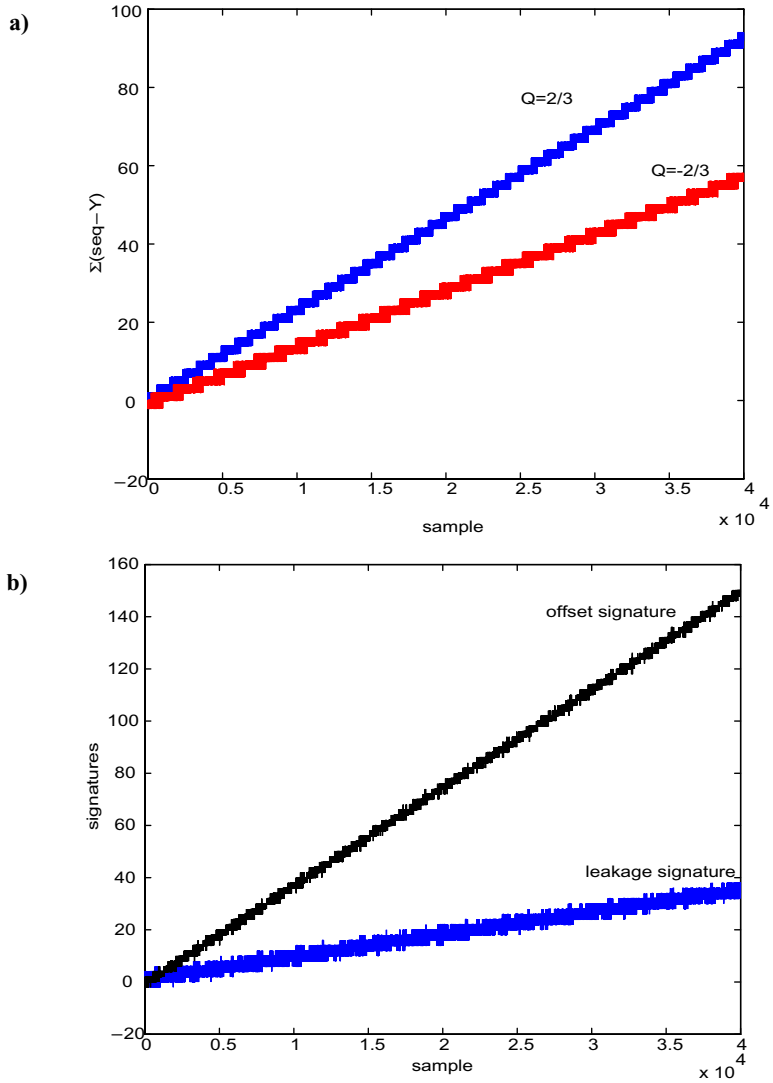


Figure 7-22: Evolution with time for the leakage test of the first integrator
a) cumulative sum of the input/output difference
b) offset and leakage signatures

Figure 7-23 a), as each step in the cumulative sum corresponds to a transition. It appears clearly that the height of the step is always the same: +2.

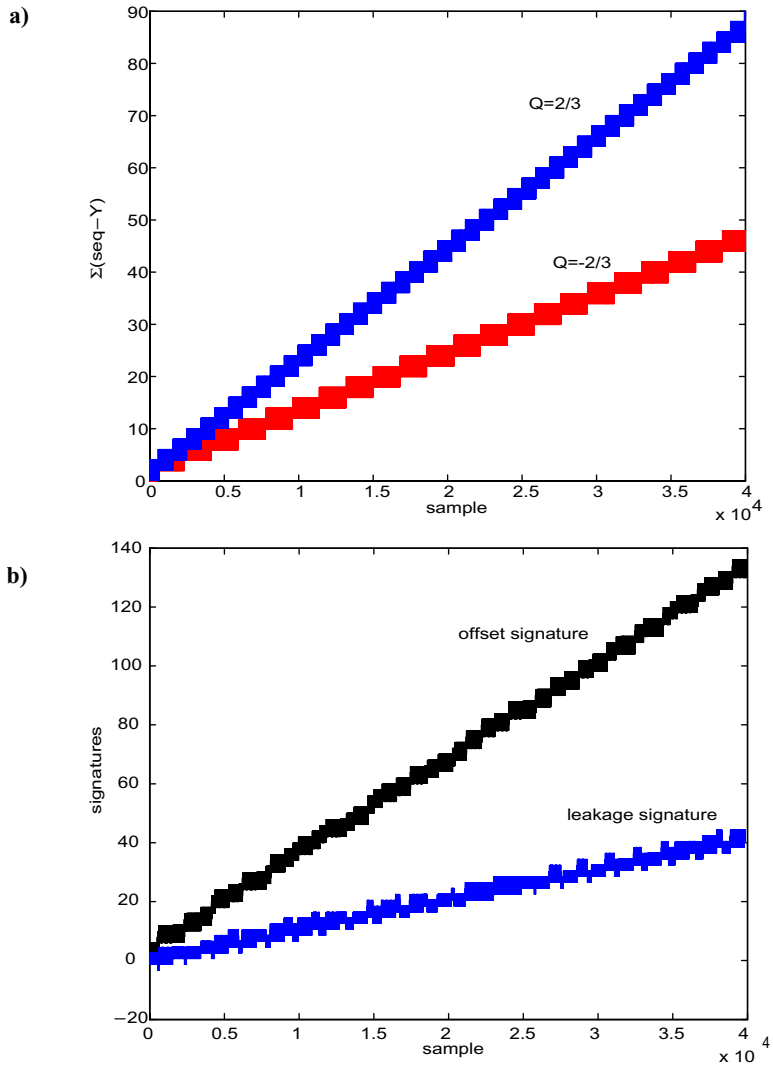


Figure 7-23: Evolution with time for the leakage test of the third integrator
a) cumulative sum of the input/output difference
b) offset and leakage signatures

7 • 2 . 3 . 2 Signature precision

Another thing that can be done to verify if the signatures behave as expected is to check its variability with time. Indeed, the measurement uncertainty for the test of the first integrator leakage in a 2nd order modulator has been derived in Eq (4-20) (and is also quoted for

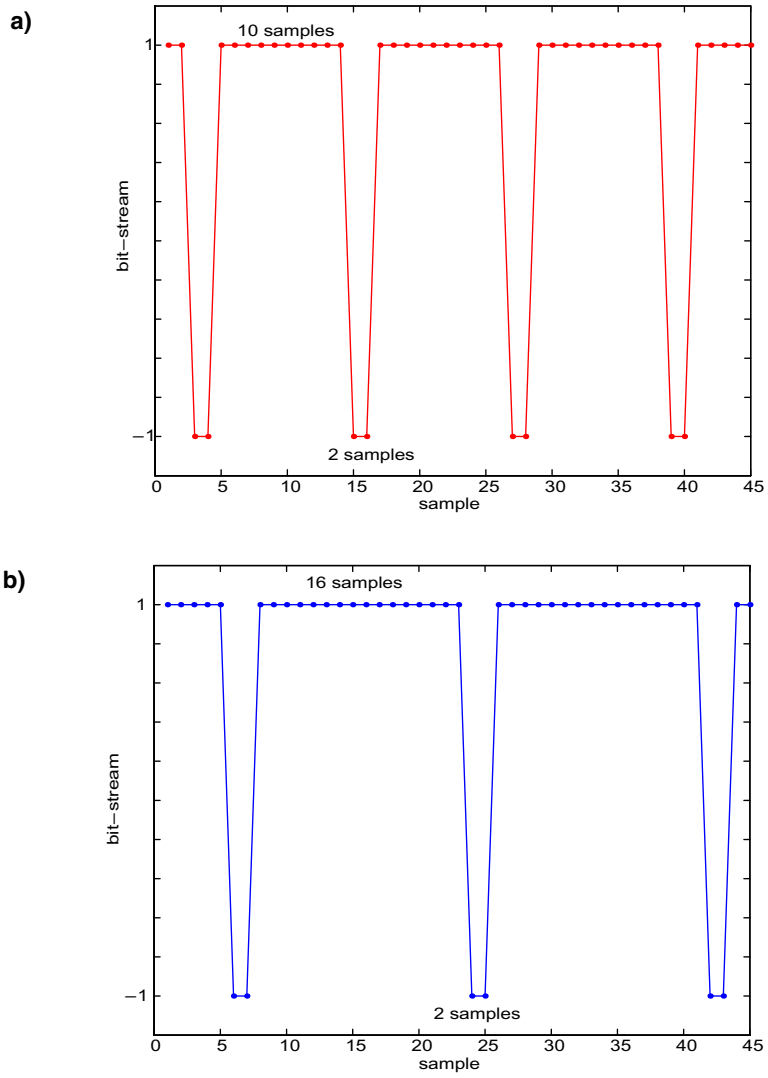


Figure 7-24: Output pattern for the leakage test of the 3rd integrator,
a)for a 2/3 input sequence.
b) for a 7/9 input sequence

test 1 in the test summary of Appendix A). Hence, if we divide the signature by the number of acquired points, we obtain

$$\frac{s}{N} = 4Q\Delta p_1 \pm \frac{6}{N}\sqrt{\frac{2}{3}}. \qquad \textbf{(7-6)}$$

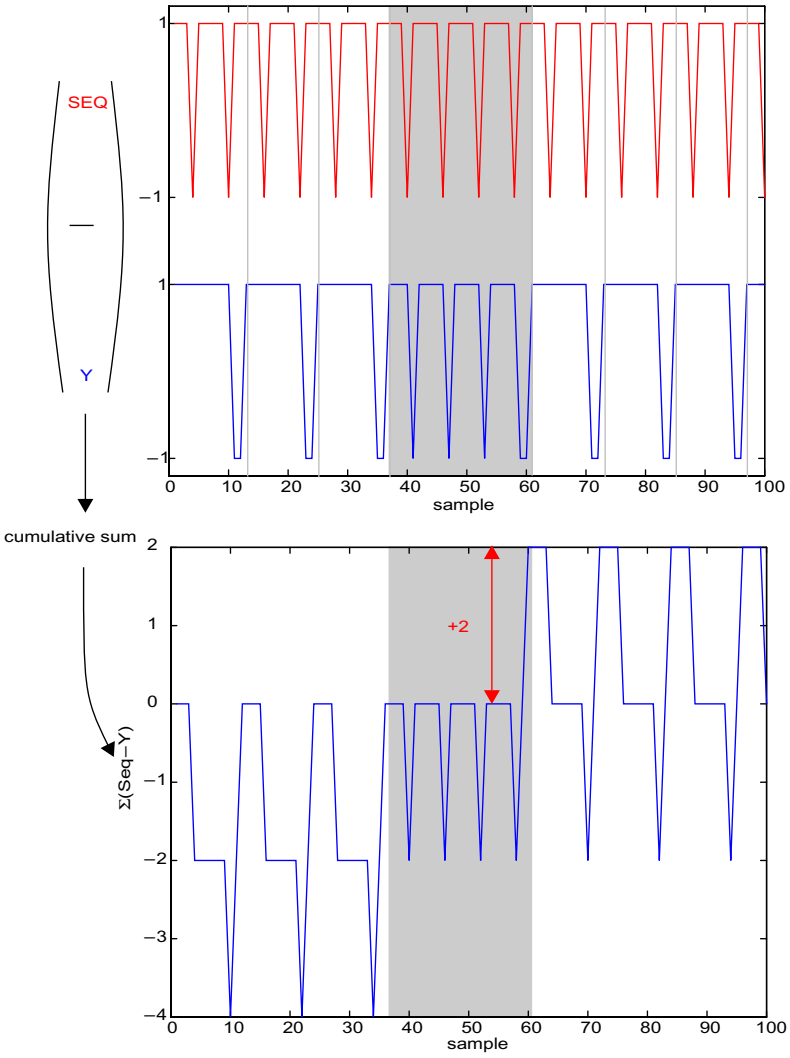


Figure 7-25: Leakage-induced transition in the output bit-stream and its influence on the test signature

The evolution of the measurement uncertainty with the number of samples can easily be verified experimentally. Actually, Figure 7-26 shows the evolution of the leakage signature (divided by the number of samples) with the number of samples. For that, a leakage test was performed for the first integrator, with an input sequence of mean value *Q=1/5*. Two acquisitions were performed (with the 1/5 sequence and its opposite) over 40000 samples. More-

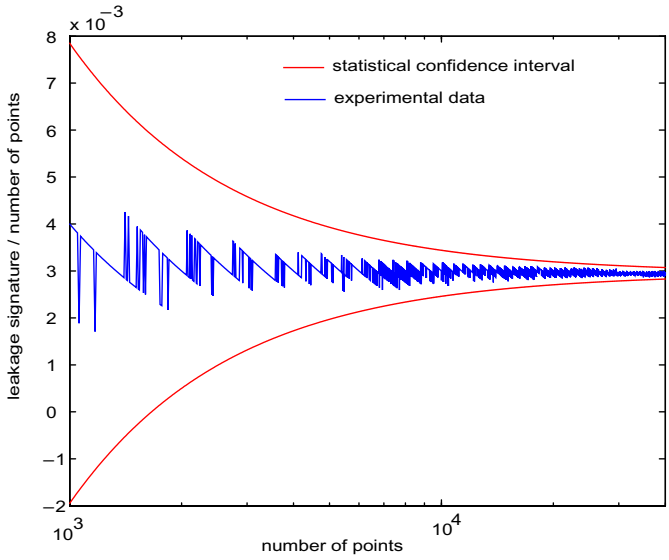


Figure 7-26: Evolution of the 1st integrator leakage signature as function of the number of points

over, the tuning voltage V_{tweak2} in the first amplifier was set to 1.8V in order to induce a higher leakage and to show that the signature precision is valid even for a leakage higher than the nominal value. To construct Figure 7-26, the leakage signature was calculated for the first *N* points and divided by *N*. Then, the confidence interval as calculated in Eq (7-6) is also represented, considering the final value at N=40000 as the reference. Note that the signature fits perfectly within the expected bounds.

Similarly, the same can be obtained for the 2nd and the 3rd integrator (that is to say a leakage test for a 1st order modulator). Dividing the test signature by the number of acquired points we have

$$\frac{s}{N} = \frac{4\Delta p}{\ln\left(\frac{1+5Q}{-3+5Q}\right)} \pm \frac{4}{N}. \qquad \textbf{(7-7)}$$

This evolution is shown in Figure 7-27 for the 2nd integrator using a sequence of mean value Q=2/3 and, as for the first integrator, the obtained signatures fit between the expected bounds.

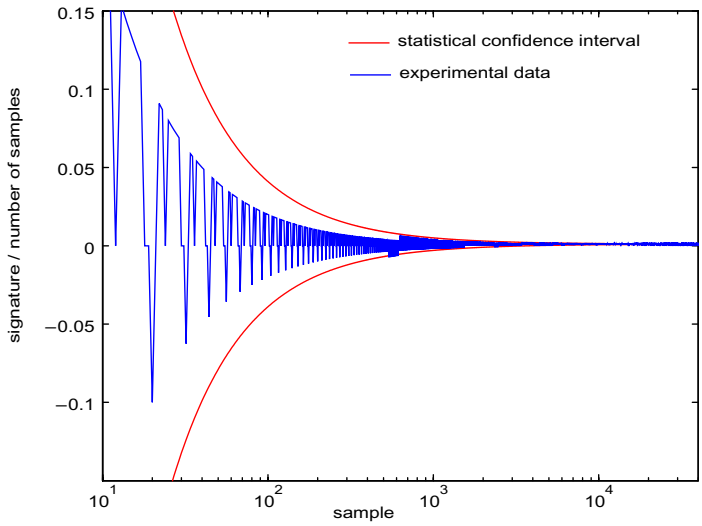


Figure 7-27: Evolution of the 2nd integrator leakage signature as function of the number of points

7 • 2 . 3 . 3 Parametric fault injection

Ideally, it would be better to perform the test by a systematic exploration of the 6-dimensional space defined by the 2 tuning voltages for the three amplifiers. However, this would be a hugely time-consuming task. Hence, in order to emulate parametric drifts, the tuning inputs of the three amplifiers were all set to the same voltage and that voltage was varied. This, in principle, should be sufficient to illustrate the variation of the leakage signatures with the tuning voltage or, in other words, to check the sensitivity of the tests to parametric drifts.

Figure 7-28 shows the integrator pole error as a function of the tuning voltage. The solid curve depicts electrical simulation results for the typical mean process corner (TM). It was obtained by simulating the integrator response to an impulse stimulus. Integrator pole error is extracted form the decaying step output. The results obtained for the other corners are displayed using dashed curves. On the same figure are represented the pole errors extracted from the obtained signatures. Pole errors were calculated from Eq (4-20) for the first integrator (i.e. for the 2nd order modulator leakage test) and from Eq (4-27) for the third amplifier (i.e. for the 1st order modulator leakage test). The tests were performed with an input

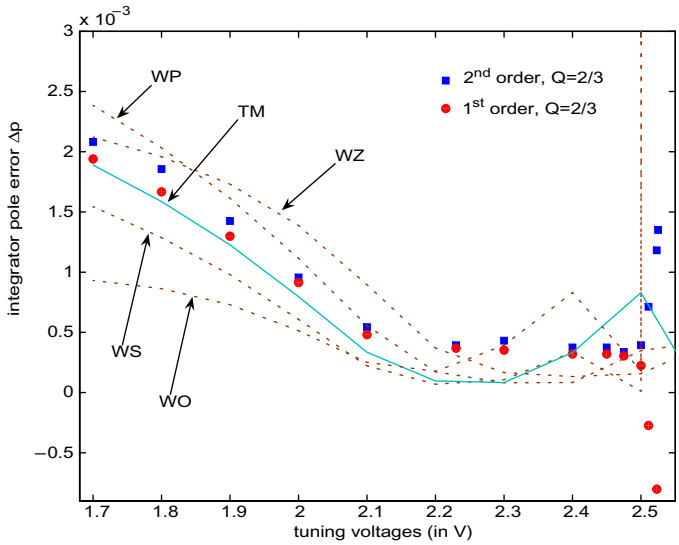


Figure 7-28: Integrator leakage as function of the tuning voltage

sequence of mean value Q=2/3 and its opposite. It was said above that the period M of the test sequence for a 1st order modulator has to be strictly greater than 5. The sequence of mean value Q=2/3 ([1 1 1 1 1 -1]) fulfils this criterion.

Note that the experimental results in the two cases exhibit good matching, which means that the 1st and the 3rd integrators behave in the same manner with respect to the tuning voltage. It also means that the leakage test for the first integrator is not strongly affected by the non-idealities in the 2nd integrator. More importantly, it demonstrates that the test effectively sense a deviation of the integrator pole. Indeed, it is very unlikely that the tests for the second order modulator and the first order modulator would give comparable results if they were failing. From the figure, it can also be seen how experimental measurements slightly overestimate the pole error with respect to simulation results of the typical process corner. Nevertheless, simulations of the integrator in the other process corners show that the experimental results fit within the possible variation range.

What is more important than the exact value of the pole error is that the signature exhibit the same trend as simulations over most of the tuning range. For all corners, it can be seen how the pole error increases significantly for lower values of the tuning voltages. It is also the case for the pole error extracted from experimental data that closely matches the electri-

cal simulation results over the tuning range [1.7 ; 2.2]V. It appears that for tuning voltages in the range [2.2 ; 2.35]V, the leakage measured experimentally is slightly higher than the expected trend. In this range, the DC gain of the amplifier reaches high values, greater than 80dB. A plausible cause is that for such high values of the amplifier DC gain, the integrator pole error is not dominated by the finite DC gain but by other effects such as charge injection.

Finally, we see that the trend of the pole error is predicted correctly up to a tuning voltage of 2.5V approximately. For higher values of the tuning voltage (superior to 2.5V), the results of the 1st and 3rd amplifier do not match with simulations. This is due to the fact that for these tuning voltages, the modulator presents very large settling errors that adversely affect the leakage signatures, as will be seen in Section 7 • 2 . 5.

7 • 2 . 3 . 4 Relation to functional test

In order to relate the test proposal to conventional functional test, the Signal to Noise Ratio (SNR) of the entire 3rd order modulator was also measured for an input sine-wave covering 70% of the full-scale, under the same tuning voltage conditions that were used for the leakage tests.

It can be seen in Figure 7-29 that the SNR does not vary with the tuning voltage, while the leakage signature for the first amplifier exhibits important variations. At first sight, one could be tempted to conclude that the proposed tests are useless because they detect deviations that do not affect performance. Several considerations can be objected to this assertion.

The first one is that leakage does have an impact on the noise present in the modulator output spectrum. It is a well-know effect that cannot be denied. However, in the particular case of our prototype, the result is that the output spectrum presents a relatively high level of thermal noise. This noise can be due to unexpected noise levels within the circuit but also to the test setup. In particular, the test board that is used is a simple through-hole board and not a multi-layer PCB, which would be more desirable. Whatever the reason, the fact is that for an OSR lower than 50, the measured SNR would be dominated by the thermal noise level and the benefits of 3rd order noise shaping would be lost. A leakage in the 1st or 2nd integrator leads to extra noise in the base-band shaped at first order. If there were no thermal noise

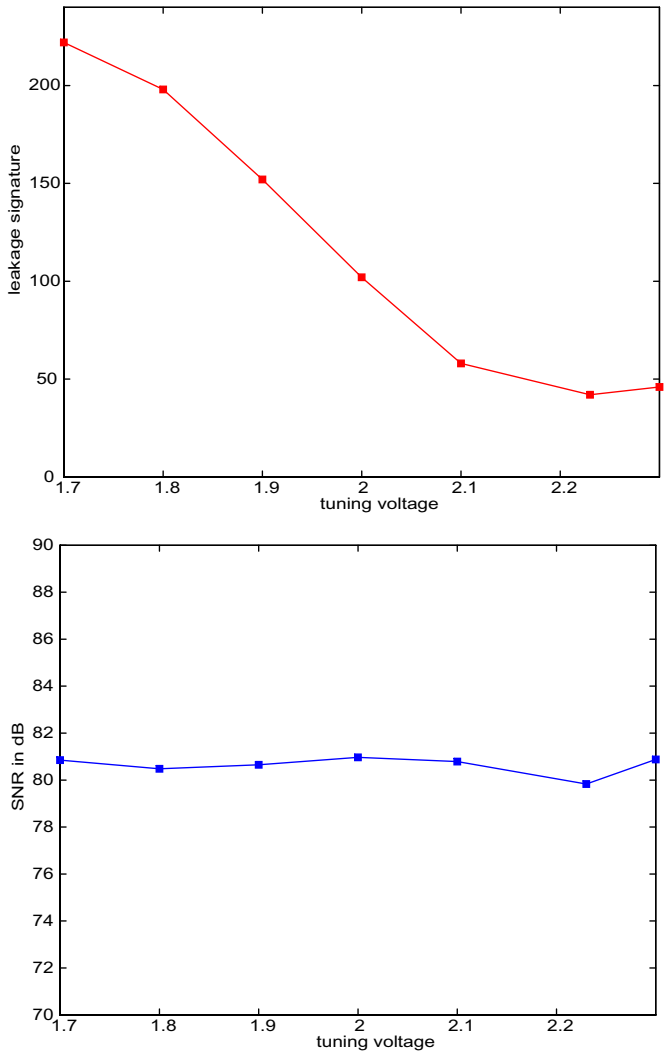


Figure 7-29: Correlation between the first integrator leakage signature and the measured modulator SNR

(or if it were significantly lower), it would be possible simply to increase the OSR until the 1st order leakage noise dominate the 3rd order quantization noise. However, as the thermal noise is not shaped, increasing the OSR even increase its importance with respect to leakage noise. For the effects of the integrator leakage to be noticed as an SNR decreases, the leaking noise has to be greater than that thermal noise. In other words, a pole error is effectively

detected by our tests but the tuning range is not adapted to generate a sufficiently high pole error to observe the leaking noise.

In order to confirm this assumption, let us study the pole error that would be necessary to observe a degradation of the SNR. The SNR can be written as follows

$$SNR = 10\log\left(\frac{A^2/2}{P_Q + P_{th} + P_{leak}}\right), \quad \textbf{(7-8)}$$

where A is the sine-wave amplitude, P_Q the 3rd order quantization noise, P_{th} the thermal noise power and P_{leak} the leakage noise power. Let us consider that the leakage power is negligible when the tuning voltages V_{tweak1} and V_{tweak2} are at their nominal value (2.23V). Hence, by measuring the SNR for the nominal tuning voltages, it is possible to determine P_Q+P_{th}.

Moreover, the power of the 1st order noise leaking into the base-band can be expressed as a function of the pole error as,

$$P_{leak} = \frac{\Delta^2}{12} \times \Delta p \times \frac{\pi^2}{OSR^3}, \quad \textbf{(7-9)}$$

where Δ is the quantizer step, Δp the integrator pole error, and OSR the oversampling ratio.

Figure 7-30 represents the expected SNR for our prototype (taking into account the thermal noise) as a function of the integrator pole error, for a sine wave covering 70% of the full-scale. According to Figure 7-28, the maximum pole error obtained for V_{tweak1}=V_{tweak2}=1.7V is approximately $2x10^{-3}$ (which corresponds to a DC gain of approximately 50dB). For this pole error, it can be verified in Figure 7-30 that almost no SNR degradation is expected. However, if we were able to increase the pole error by a factor 10, we should observe a degradation of about 7dB.

In any case, as was said in Chapter 3 and repeated several times across the thesis, the primary focus of the test proposal is defect-oriented. Hence, we can say that our test can detect a small pole error with a much higher precision than a functional test. Even if the pole error does not impact the performance, if it is higher than what could be expected for normal process variations, it represents the signature of a defect that could be a reliability issue as its effects could increase with temperature or other operating conditions.

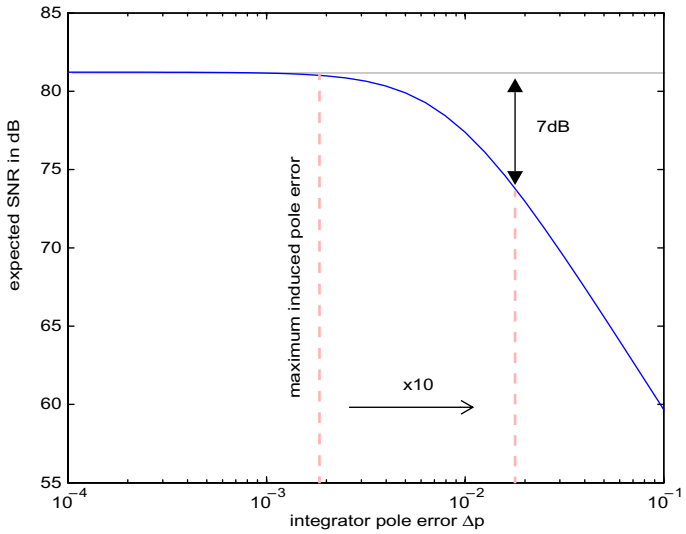


Figure 7-30: Expected SNR variation for the prototype as function of the first integrator pole error

Finally, as was proposed in Section 5 • 4 . 2 . 2, it may be desired to give a more performance-oriented focus to the test. In that sense, the test limit could be set to a value such that the good performers are accepted. For instance, the maximum leakage signature obtained for the 1st integrator for V_{tweak1}=V_{tweak2}=1.7V is 222. Hence, it may be possible to set the leakage test limit to, say, 250. Going even further, it would be possible to perform the acquisitions over only 4000 points instead of 40000 and to set the test limit to 25.

7 • 2 . 4 Non-linear DC gain tests

The leakage signature for the first integrator is expected to be dependent on the DC gain non-linearity of the corresponding amplifier. This is the basis of the test that was proposed in Section 4 • 3. It was said and verified by simulation that for sequences with a high mean value, the effects of the amplifier limited output range would be more significant than for sequences with a lower mean value. This translates into the fact that the leakage signatures should be higher for higher sequence mean values, while for lower sequence mean values the result of the leakage test is not altered and corresponds to the amplifier DC gain.

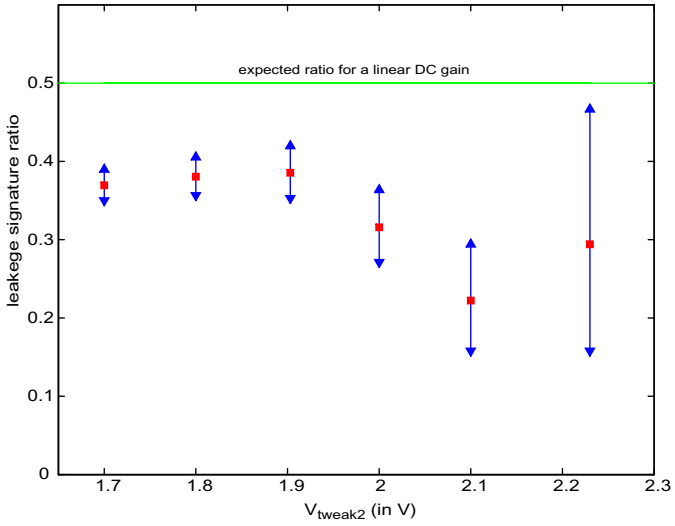


Figure 7-31: Measured 1st integrator DC gain non-linearity signature, as a function of the tuning voltage V_{tweak2}.

The tuning inputs introduced in the amplifier do not allow one to impact directly the amplifier output range in a controllable manner. Hence it is not easy to validate the DC gain non-linearity test by varying the tuning voltages of the amplifier. Nevertheless, the tuning voltage V_{tweak2} does impact the DC gain and hence it will greatly influence the precision of the DC gain non-linearity test. Indeed, the test signature relies on comparing the leakage test results for two different input sequences. For the same number of acquired points, a lower DC gain leads to a higher leakage signature and thus the possible difference between two sequences is more likely to be detected. This is illustrated in Figure 7-31 that plots the results of the DC gain non-linearity test, as specified in Eq (4-114) (and corresponds to test 8 in the test summary of Appendix A). For this test, two sequences of mean values 1/3 and 2/3 were used. Hence, for a perfectly linear DC gain, the expected ratio between the two leakage signatures should be 0.5. Furthermore, the modulator full-scale was set to ±1.4 V in order to amplify the DC gain non-linearity. The figure also displays the confidence interval associated with the signature ratio. It was calculated considering a ±4 error on the individual leakage test signatures. It can be seen that this confidence interval is much smaller for lower

values of V_{tweak2}, which corresponds to lower DC gains. Furthermore, the measured ratio is always below 0.5 which means that a non-linearity has been detected.

As was said above, the tuning voltages of the amplifier do not allow to vary the DC gain non-linearity without varying the DC gain itself. Fortunately, the prototype offer the possibility to set the modulator Full-Scale externally. Obviously this will not change the "real" linearity of the amplifier gain, but the output of the integrators (i.e. the modulator internal states) will effectively depend on the full-scale reference. All the theoretical analysis that has been carried out relies on the fact that everything is normalized to the modulator full-scale, as explained at the end of Chapter 3. Hence, varying the Full-Scale is formally equivalent, from a test viewpoint, to varying all the related parameters in an inverse proportion. For instance, if we change the full-scale by 20% and set it to +/- 1.2V instead of +/-1V, the normalized Slew-Rate is scaled by -20%, as well as the DC gain non-linearity parameter a_{NL}.

Hence, in order to validate experimentally the idea behind the DC gain non-linearity test, we performed leakage tests for several input sequences and for three values of the modulator Full-Scale: +/- 1V, 1.2V and 1.4V. We also set the tuning voltage V_{tweak2} of the first amplifier to 1.8V in order to induce higher leakage and to obtain higher precision on the signature for 40000 points which is our acquisition limit. Figure 7-32 shows the results obtained. It can be seen that for a sequence with a small mean value (1/5), the leakage signature is the same (within the normal measurement uncertainty) for the three values of the modulator Full-Scale. This demonstrates the first point of our test proposal: the non-linearity of the DC gain is not stimulated by small sequences and the leakage result corresponds to the small-signal DC gain. As the small-signal DC gain is independent of the Full-Scale, the results are identical in the three cases. Starting from this observation, the value of the leakage signature for a perfectly linear DC gain has been extrapolated for the rest of the sequences (taking into account that the signature for a zero-mean input sequence has to be zero). This has been done in order to ease comparison. Indeed, it can be seen how, for the three sequences with highest mean values, the leakage signature is above the "linear-DC-gain" line, as expected. Moreover, the higher the Full-Scale, the higher the deviation.

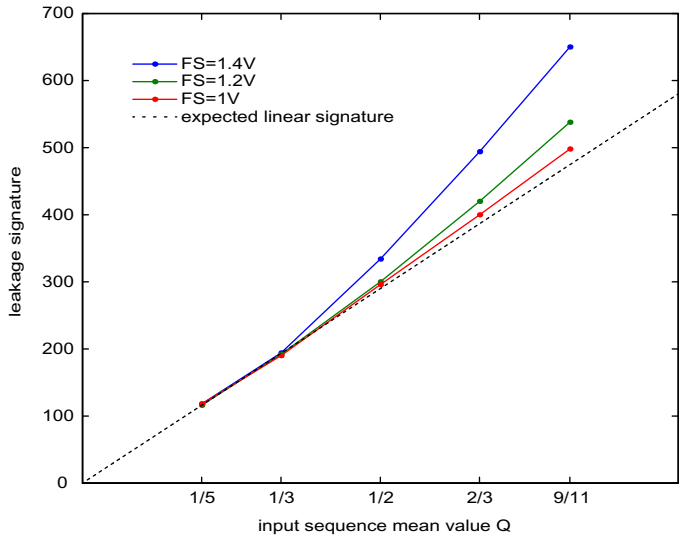


Figure 7-32: 1st integrator leakage signature as function of the input sequence mean value, for 3 values of the modulator Full-Scale (Vtweak2 is set to 1.8V for the 1st amplifier only)

7 • 2 . 5 Settling error tests

7 • 2 . 5 . 1 Comparison of the test signatures

In order to test for settling errors, a digital sequence (ideally of mean value 0 to avoid leakage impact) is sent to the modulator. For the first acquisition the clock period is doubled for a 1 input sample and for the second acquisition it is doubled for a -1 input sample. Using the two acquisitions to get rid of input-referred offsets, the deviation of the output bit-stream (y) from the input (x) mean value accumulated over N samples can be written

$$s = s_1 - s_2 = \sum_{i=1}^{N} (y_i - x_i) - \sum_{i=1}^{N} (y^*_i - x^*_i) = er_2 \times [N_2 + N^*_{-2}]. \qquad \textbf{(7-10)}$$

Two tests were proposed that rely on this principle:

- If a deterministic sequence is used, parameters N_2 and N^*_{-2} have to be measured explicitly because they cannot be known a-priori (this corresponds to test 10 in the test summary of Appendix A).

- If a pseudorandom sequence is used, it has been shown that only a small relative error is committed by taking parameters N_2 and N^*_{-2} equal to *N/4* (this corresponds to test 11 in the test summary of Appendix A).

Let us see how these two proposals behave experimentally. Figure 7-33 displays the evolution of the accumulated input/output deviation (*s* in Eq (7-10)*)* with the number of points obtained for a deterministic sequence of period [1 1 -1 1 -1 -1] and for a pseudorandom sequence. Case a) corresponds to the test of the first integrator (i.e. to a 2nd order modulator) and case b) to the third integrator (i.e. to a 1st order modulator). The acquisitions were performed over 20000 samples and all the tuning voltages were set to 2.5V in order to force a small settling error.

In all cases it can be seen that deviation is clearly sensed. There is also a difference between the slope obtained for the random sequence and for the deterministic sequence, which can be explained by the explicit value of parameters N_2 and N^*_{-2} for each case.

Another thing that is worth noticing is that the signatures obtained for the 1st integrator look more noisy than the signatures obtained for the 3rd integrator. This can be explained by the fact demonstrated in [32] that 1st order ΣΔ modulation is a mapping. Ideally, when the input of a 1st order ΣΔ modulator is a digital sequence, the modulator output strictly follows the input. In the case of Figure 7-33 b), the settling error accumulates at the integrator output. While the accumulated value is two small to change the sign of the modulator output, the mapping is respected and the output follows the test sequence for a deterministic sequence as well as for a pseudo-random sequence. In turn, when the accumulated value is large enough, it introduces a difference in the output bit-stream which corresponds to a step in the signatures depicted in the figure.

Figure 7-34 shows the evaluated settling error in the same cases. For the deterministic sequence, the number of occurrences of level 2 (alternatively -2) at the integrator input was measured. Remember that a level 2 occurs at the integrator input when the modulator input sample is a 1 and the feedback sample (i.e. the modulator output sample) is a -1. The settling error was evaluated as proposed in Eq (5-13). Conversely, for the pseudorandom test sequence, the parameters N_2 and N^*_{-2} equal to N/4=5000 instead of explicitly measuring them. The evaluated settling error is thus the accumulated input/output difference divided by

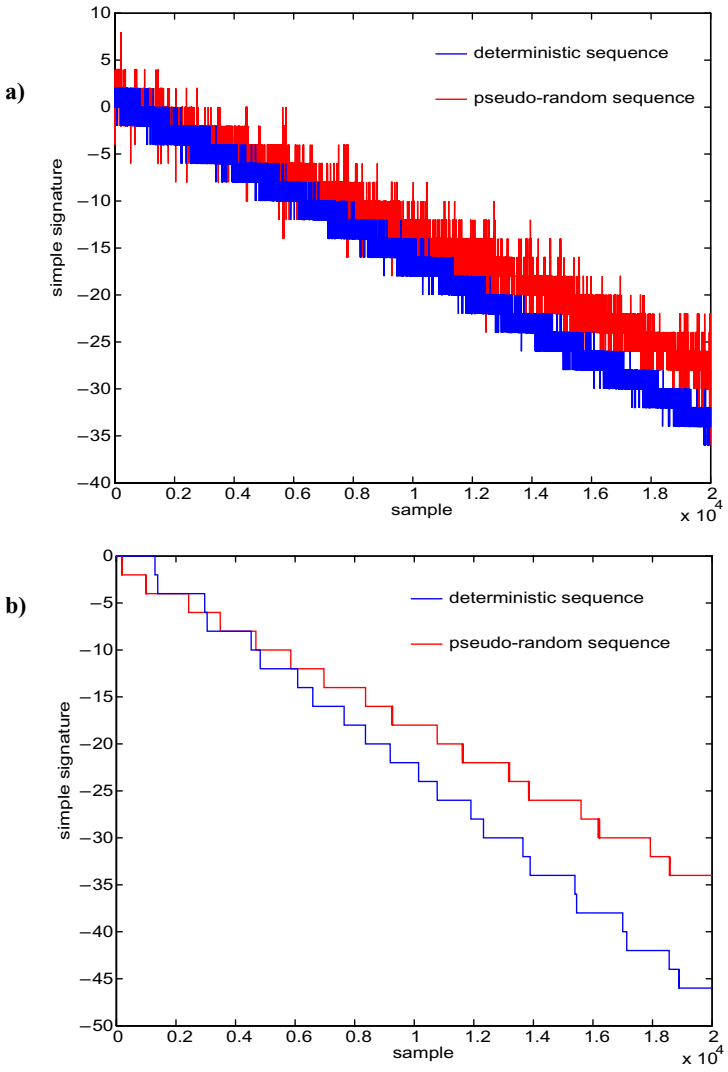


Figure 7-33: **Input/output accumulated difference measured for**
a) the settling error test of the first integrator (i.e. a 2nd order modulator)
b) the settling error test of the third integrator (i.e. a 1st order modulator)

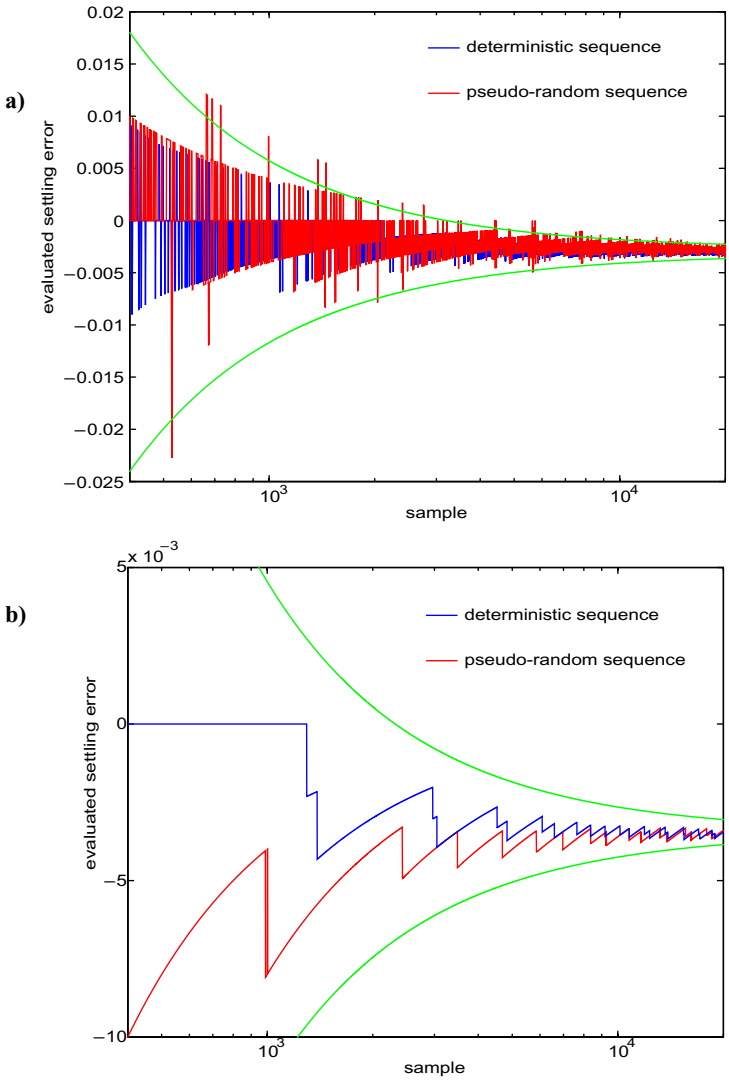


Figure 7-34: Evaluated settling error measured for
a) the settling error test of the first integrator (i.e. a 2nd order modulator)
b) the settling error test of the third integrator (i.e. a 1st order modulator)

N/2=10000. Together with the curves, the confidence interval is also represented. It is calculated for the case of a pseudo-random test sequence, considering Eq (5-42).

It can be seen that the results match perfectly for both tests in both cases (the 1st and 2nd order modulator). Furthermore, the evaluated settling error is of the same order for the different integrators: -0.31% for the first integrators and -0.35% for the third. This is another piece of evidence that everything is working properly as the integrators are identical and their amplifiers are submitted to the same tuning voltages.

7 • 2 . 5 . 2 Parametric fault injection

When the tuning voltage were varied to inject parametric drifts in Section 7 • 2 . 3 . 3, settling error tests were also performed at the same time as leakage tests. The input sequence for these tests was a deterministic sequence of period [1 1 -1 1 -1 -1] and mean value 0. Two acquisitions were performed for each value of the tuning voltage: one doubling the reference clock period for the 1 input samples and the other doubling the reference clock period for the 0 input samples. Hence, the settling error was calculated using Eq (5-13).

Figure 7-35 shows the results obtained. The first thing to notice is that the results obtained for the 1st integrator (with the test for a 2nd order modulator) almost perfectly match those obtained for the 3rd integrator (with the test for a 1st order modulator). It can be seen that the measured settling error is very small on most of the tuning voltage range but abruptly increases for voltages above 2.5V. This coincides perfectly with the value above which the leakage signatures showed important mismatch in Figure 7-28.

The close-up on the range [2.4V ; 2.6V] allows to have a better view of the results. It can be seen that the settling error evaluated through the proposed tests is very close to the typical process corner simulations. Actually the observed difference could simply be explained by either process variation or mismatch.

7 • 2 . 5 . 3 Relation to functional test

In order to relate the proposal to conventional functional test, the Total Harmonic Distortion (THD) of the entire 3rd order modulator was also measured for an input sine-wave covering 70% of the full-scale in the same tuning voltage conditions that were used for the

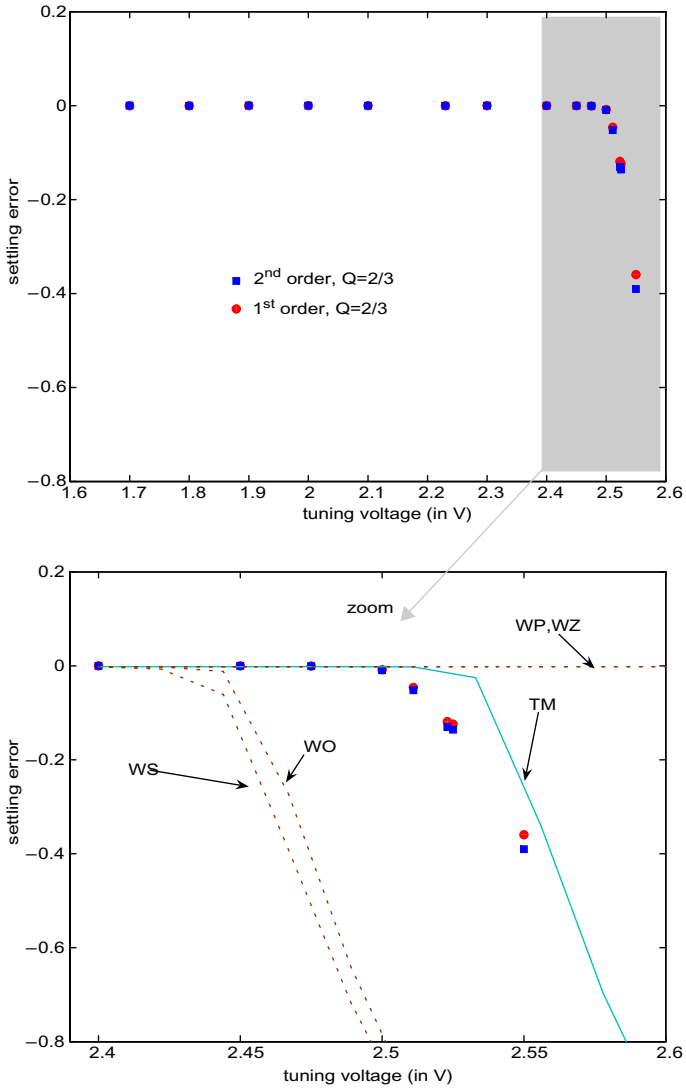


Figure 7-35: Measured (markers) and simulated (solid and dasshed curves) settling errors

settling error tests. Figure 7-36 displays in parallel the value of the measured first integrator settling error and the measured THD. It can be seen that there is a strong correlation between both, as expected. It is well known that the first integrator greatly influences the performance of the overall modulator. We can say that the proposed test is sufficiently sensitive to detect a settling error that produces a THD below 90dB. Indeed, the settling error at the 2.5V tuning

voltage is clearly detected while the THD at the same value is still 90dB. Taking a look at Figure 7-6 b), it can be seen from electrical simulations that the settling of the integrator for a 2.5V tuning voltage is significantly altered with respect to nominal (in particular the slew-rate) but still seems to settle correctly. This consideration is in line with the results observed for the proposed test and the THD.

In our opinion, what is even more important is that the proposed tests maintain the same accuracy for all the integrators. This means that out-of-bounds settling errors can be detected in inner integrators while such defects would be undetectable by conventional functional tests.

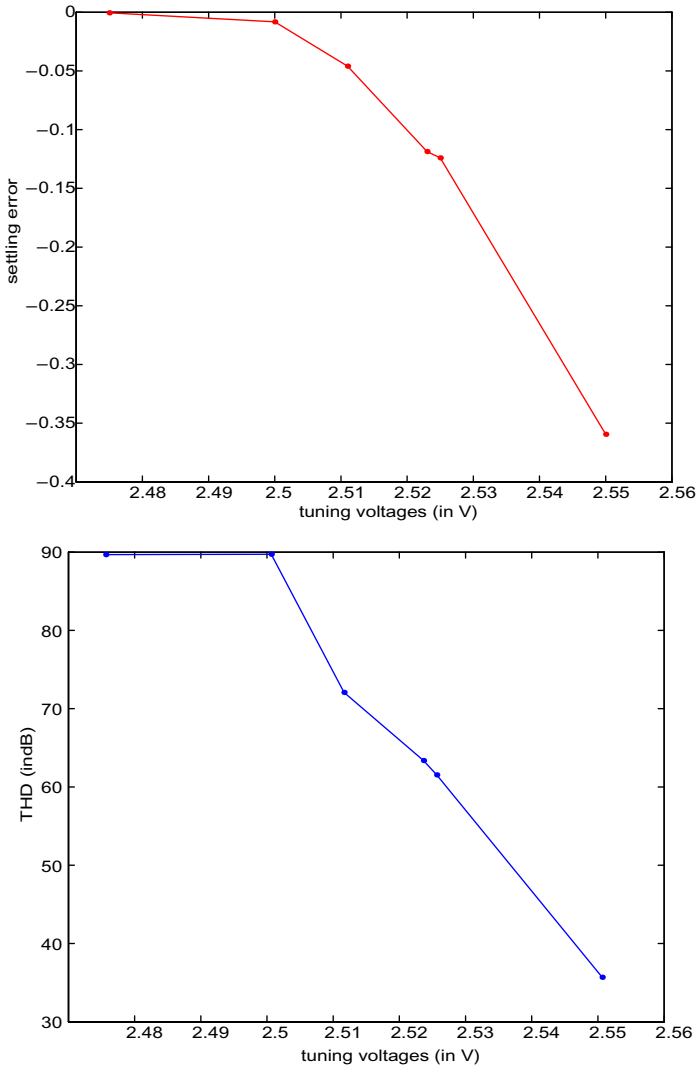


Figure 7-36: Correlation between the measured first integrator settling error and the measured modulator THD

Conclusions

A design-based test approach has been applied to ΣΔ modulators, and a number of tests have been proposed that target important design-parameters of ΣΔ modulators. The approach has been validated through extensive simulation and also experimentally with data obtained from an integrated prototype.

The different tests have been designed to meet low-cost and flexibility requirements. The main characteristics of our approach are:

- All the tests are fully digital. This is an important advantage *per-se*. It allows the use of digital-only test resources (a low-cost digital tester could be used), which may enable massive parallel testing. It also facilitates the test of embedded parts (for instance, in SoCs) as digital signals are much easier to manage than their analog counterparts.

- The stimuli generation and the signature elaboration require little extra hardware, which makes the approach a perfect candidate for BIST. This permits cost-effective in-field test. The proposal can also be used to interface the modulator test with standard board-level test resources such as the IEEE 1149.1 test bus.

- Few modifications are required to the modulator and these mainly affect switch controls. This is a key point as the test-related circuitry is undoubtedly more robust than the circuit under test. This is an advantage for applications where in-field test is mandatory and has to give reliable results. Harsh-environment applications, such as spatial or geothermal applications, are good examples.

From the application of the proposed test set, the following conclusions can be drawn:

- Testing the main characteristics of the device building blocks has been shown to enhance defect coverage with respect to functional testing. Indeed, the test proposal not only allows the detection of parametric drifts that can affect the performance but also the detection of defects that represent a reliability issue but do not translate directly into a performance degradation.

- The approach provides an important degree of freedom in the choice of the test limits. These limits can be chosen to closely match the expected bounds of the nominal variations, leading to a selective defect-oriented test. Alternatively, they can be set much closer to the frontiers of the valid design space so as to minimize the number of good performers rejected. Yield/Test optimization is thus possible, when the test limits are put within the design guard-bands.

- The test is closely linked to the ΣΔ modulator design. As behavioural models are widely used during the design flow, they can be fruitfully used for test purpose.

- Another benefit of this approach is that the test outcome provides valuable information on the building blocks behaviour and represents an added-value for fault-location, fault-diagnosis and silicon-debug in general.

- The tests that have been designed rely on proper ΣΔ modulation and stimulate the entire signal path. We have shown that they are suitable for detecting catastrophic defects even if they affect blocks that are not the test primary target.

- The approach offers the test designer a large degree of flexibilty. Several test alternatives were proposed for various parameters that have different implications in terms of hardware and modulator modifications. This is a valuable degree of freedom for the designer to optimize test costs.

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Appendix A

TEST SUMMARY

In the following table, we summarize the characteristics of all the tests proposed in the thesis. To avoid redundancy in the test comments, we recall to the reader that in the majority of cases, the test sequence is a digital sequence comprising 1s (corresponding to logic 1s) and -1s (corresponding to logic 0s). Some tests use sequences with analog 0s (and must thus use two bits to define the test sequence) but these cases will be specified in the table.

Similarly, most tests use two acquisitions to eliminate the impact of possible input-referred offsets. The test signature for each acquisition is the difference between the test sequence (x) and the modulator output bit-stream (y) accumulated over N samples. The final signature is taken as the difference between the results for the two acquisitions

$$s = s_1 - s_2 = \left(\sum_{i=1}^{N} x_i - y_i \right)_1 - \left(\sum_{i=1}^{N} x_i - y_i \right)_2 . \qquad \textbf{(7-1)}$$

In some cases, a slightly more complex signature has to be generated but these particular cases are also specified in the table.

Table I: Test summary

nº	type	signature	equation ref.
1	leakage test for 2nd order	$s = 4NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}}$	(4-20) p. 123
Stimulus: Any sequence of non-zero mean value Q (-Q). **Comments:** The influence of DC gain non-linearity may be noticed for the highest mean values.			
2	leakage test for 2nd order	$s = 4NQ\Delta p_1 \pm 6\sqrt{\frac{2}{3}}$	(4-20) p. 123
Stimulus: A sequence with analog 0s of mean value Q (-Q). **Comments:** This test has to be run at half the nominal clock frequency to avoid settling errors.			
3	leakage test for 1st order single-bit	$s = \frac{4N\Delta p}{\ln\left(\frac{3L-5}{L-5}\right)} \pm 4$	(4-27) p. 126
Stimulus: A digital sequence of length L with L-1 1s and only one -1, and its opposite. L must be greater than 5. **Comments:** An extra delay has to be introduced in the feedback loop. The offset may cause a strong non-linearity for either the positive or negative sequence, leading to a relative error on the leakage evaluation.			
4	leakage test for 1st order signle-bit	$s = 2N\Delta p\left(\frac{1}{\ln\left(\frac{5-3L_1}{5-L_1}\right)} - \frac{1}{\ln\left(\frac{5-3L_2}{5-L_2}\right)}\right) \pm 4$	(4-87) p. 142
Stimulus: Two digital sequences of length L_1 and L_2, with L-1 1s and only one -1, and their opposites. L_1 and L_2 must be greater than 5. **Signature:** The input/output difference accumulated over N samples. The sign of the offset has to be determined. The results obtained for the two sequences of opposite signs to the offset are combined **Comments:** An extra delay has to be introduced in the feedback loop. The obtained signature has lower sensitivity than the previous test			
5	leakage test for 1st order single-bit	$s = \frac{2N\Delta p}{\ln\left(\frac{3L-2}{L-2}\right)} \pm 2$	(4-28) p. 126

Table I: Test summary

nº	type	signature	equation ref.
Stimulus: A digital sequence of length L with L-1 1s and only one 0, and its opposite. L must be greater than 2. The test must be carried out at half the sampling frequency to avoid settling errors. **Comments:** Analog 0s are used in the sequence. It is the same test as nº 3 but no extra delay has to be introduced in the feedback loop. The offset may cause a strong non-linearity for either the positive or negative sequence, leading to a relative error on the leakage evaluation.			
6	leakage test for 1st order single-bit	$s = N\Delta p\left(\frac{1}{\ln\left(\frac{2-3L_1}{2-L_1}\right)} - \frac{1}{\ln\left(\frac{2-3L_2}{2-L_2}\right)}\right)\pm 2$	(4-93) p. 145
Stimulus: Two digital sequences of length L_1 and L_2, with L-1 1s and only one 0, and their opposites. L_1 and L_2 must be greater than 2. The test must be carried out at half the sampling frequency to avoid settling errors. **Signature:** The input/output difference accumulated over N samples. The sign of the offset has to be determined. The results obtained for the two sequences of opposite signs to the offset are combined **Comments:** The obtained signature has a lower sensitivity than the previous test			
7	leakage test for 1st order multi-bit	$s = 2NQ\Delta p \pm \frac{6}{2^{L_{DAC}-1}}\sqrt{\frac{1}{3}}$	(4-24) p. 124
Stimulus: A sequence of mean value Q superior to half the quantizer step and its opposite. **Comments:** It is recommended to use a mean value significantly greater than half the quantizer step.			
8	DC gain non-linearity test for 2nd order	$s = s_1/s_2 = \frac{Q_1}{Q_2}\times\frac{f(a_{NL},Q_1)}{f(a_{NL},Q_2)} \pm \frac{Q_1}{NQ_2\Delta p}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)$	(4-114) p. 173
Stimulus: Two sequences of non-zero mean value Q_1 and Q_2 and their opposite. **Signature:** It is the ratio of the leakage test signatures **Comments:** The same test as nº 1 is performed with two sequences. For a small mean value the result is proportional to the nominal DC gain while for a high mean value it is sensitive to DC gain non-linearity. The value of the signature is only sensitive to the non-linearity of the DC gain but not its uncertainty.			

Table I: Test summary

nº	type	signature	equation ref.
9	DC gain non-linearity test for 2nd order	$s = s_1 - \frac{Q_2}{Q_2} \times s_2 = 4NQ_1\Delta p[f(a_{NL}, Q_1) - f(a_{NL}, Q_2)] \pm 6\left(1 + \frac{Q_1}{Q_2}\right)\sqrt{\frac{2}{3}}$	(4-115) p. 173
Stimulus: Two sequences of non-zero mean value Q_1 and Q_2 and their opposite. **Signature:** It is the scaled difference between the leakage test signatures. **Comments:** This signature does not requires a division but is a function of the nominal DC gain and not only of its non-linearity..			
10	overall settling error test for any modulator	$er_2 = \frac{s_1 - s_2^* \pm 4}{N_{-2} + N^*_2}$	(5-13) p. 191
Stimulus: A sequence of zero mean value. The period of the clock reference is doubled for a 1 input sample during the 1st acquisition and for a 0 input sample during the 2nd acquisition (*). **Signature:** Apart from the accumulated input/output difference, the number of occurrences of a level -2 (alternatively 2) at the integrator input also has to be acquired.			
11	overall settling error test for any modulator	$s = \frac{N}{2} \times er_2 \pm \left(4 + 3er_2\sqrt{\frac{N}{2}}\right)$	(5-41) p. 197
Stimulus: A pseudorandom sequence of zero mean value. The period of the clock reference is doubled for a 1 input sample during the 1st acquisition and for a 0 input sample during the 2nd acquisition (*). **Comments:** The use of a pseudorandom sequence allows one to estimate as N/4 the number of occurences of a level -2 (alternatively 2) at the integrator input. The signature is thus much simpler but this approximation leads to an additional (small) relative error.			
12	non-linear settling error test for any modulator	$er_{NL} = \frac{(s1_{fs} - s2_{fs}) - (s1_{fs/2} - s2_{fs/2}) \pm 8}{(N_2 + N^*_{-2})}$	(5-58) p. 214
Stimulus: A sequence with only 1s and analog 0s and its opposite. The clocking does not have to be modified as function of the input. Two more acquisitions have to be performed at half the nominal frequency. **Signature:** Apart from the accumulated input/output difference, the number of occurences of a level 2 (alternatively -2) at the integrator input also has to be acquired. **Comments:** As the input sequence is not of zero mean value, the influence of the leakage has to be supressed. For this reason the acquisitions are also performed at half the nominal frequency.			

Table I: Test summary

nº	type	signature	equation ref.
13	non-linear settling error test for any modulator	$s = (s1_{fs} - s2_{fs}) - (s1_{fs/2} - s2_{fs/2}) = \frac{N}{4} \times er_{NL} \pm \left(8 + \frac{3}{4} er_{NL}\sqrt{N}\right)$	(5-59) p. 214
Stimulus: A pseudorandom sequence with only 1s and analog 0s, and its opposite. The clocking does not have to be modified as function of the input. Two more acquisitions have to be performed at half the nominal frequency. **Comments:** The use of a pseudorandom sequence allows one to estimate as N/8 the number of occurences of a level -2 (alternatively 2) at the integrator input. The signature is thus much simpler but this approximation leads to an additional (small) relative error.			