Static Power Consumption in CMOS Gates Using Independent Bodies

D. Guerrero, A. Millan, J. Juan, M.J. Bellido,
P. Ruiz-de-Clavijo, E. Ostua, and J. Viejo

Departamento de Tecnología Electrónica de la Universidad de Sevilla, Escuela Técnica Superior de Ingeniería Informática,
Avda. Reina Mercedes S/N, 41012 Sevilla, Spain*
{guerre,amillan,jjchico,bellido,pruiz,ostua,julian}@dte.us.es
http://www.dte.us.es

Abstract. It has been reported that the use of independent body terminals for series transistors in static bulk-CMOS gates improves their timing and dynamic power characteristics. In this paper, the static power consumption of gates using this approach is addressed. When compared to conventional common body static CMOS, important static power enhancements are obtained. Accurate electrical simulation results reveals improvements up to 35% and 62% in NAND and NOR gates respectively.

1 Introduction

Over the past several years, static CMOS logic design style has played a dominant role in digital VLSI design because of its relative high performance, low static power dissipation, high input impedance, cost effectiveness and many other remarkable qualities [1]. However, static CMOS gates present strong performance degradation as the number of inputs increases, due to the so-called body effect and the internal parasitic capacitance associated to series-connected transistor [1,2]. Also, static power is becoming relevant in CMOS logic as the transistor size decreases, so that reducing leakage current is more and more important [3].

The body effect can be modeled as a dependence of the threshold voltage V_t on V_{sb} as follows [4]:

$$V_t = V_{t0} + \phi_B + \gamma\sqrt{\phi_B + V_{sb}} \tag{1}$$

where V_{t0} is the flat-band voltage, γ is the body effect coefficient and ϕ_B is determined from technological and physical conditions.

In a standard CMOS NAND implementation like the one in Fig. 1a, if the input vector changes from (I_3, I_2, I_1, I_0)=(1, 1, 1, 0) to (I_3, I_2, I_1, I_0)=(1, 1, 1, 1) the series connected NMOS transistors corresponding to inputs I_1, I_2 and I_3 will suffer from a

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reduced conductance due to an increased threshold voltage, lowering the performance of the gate. Additionally, parasitic capacitance associated to nodes A, B and C in Fig. 1a will also affect negatively the delay and power consumption of the gate.

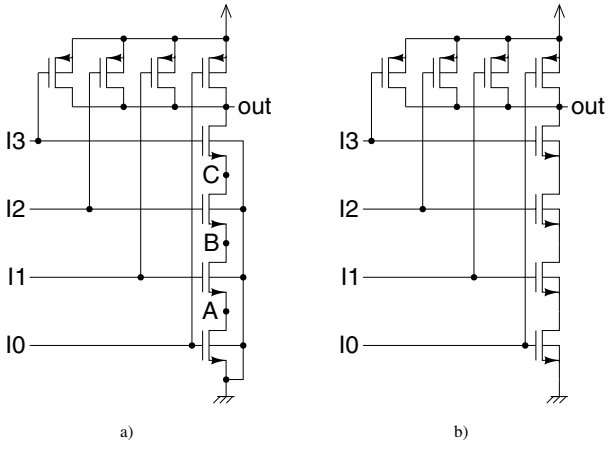

Fig. 1. Schematics of a two implementation of a NAND gate

In order to solve these problems, it has been proposed to make $V_{sb} = 0$ in every series transistor [5]. To do that, the source and body terminals of every NMOS in a NAND gate, and of every PMOS in a NOR gate are connected together using twin-well and triple-well technologies that provide independent bodies for both types of transistors (Fig. 1b). The possibility of using independent bodies for each series transistor has not typically been considered in bulk-CMOS design because of its obvious area penalty. However, this would allow connecting source and body, which has two remarkable consequences:

- The source-to-body junction parasitic capacitance can be neglected. Furthermore, drain-to-body junction capacitances in the series chain are not grounded anymore and are charged at a lower voltage, accumulating less charge. As a consequence, the total parasitic capacitance in the series structure is greatly reduced.
- Since $V_{sb} = 0$ for every transistor, the body effect is avoided and transistor conductance is improved.

Electric simulations of gates implemented using this technique (called INBO, for *Independent Bodies*) and using the conventional common-body design style (called COBO, for *Common Bodies*) have shown remarkable improvements in delay and dynamic power consumption [5] (delay and dynamic power consumption was reduced over 20%). Also, delay and power measurements were more homogeneous across input terminals. This makes the INBO technique adequate for the design of gates with a large number of inputs.

With respect to static power consumption, it has two main causes in CMOS gates [1]:

- Reverse-bias leakage currents
- Subthreshold conduction

The first cause is explained by the existence of parasitic diodes in CMOS gates such as the inverter shown in Fig. 2. Each p-n junction forms a parasitic diode, so there is one for each drain and source terminal and one for the n-well.

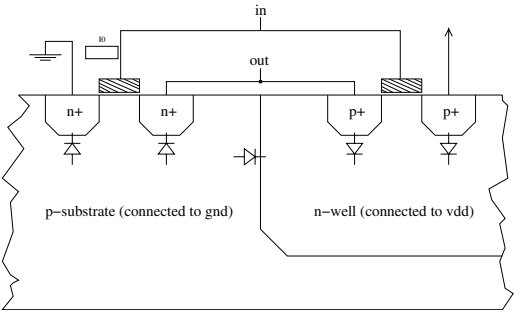

Fig. 2. Parasitic diodes in a CMOS inverter

Depending on the input value, the diodes corresponding to the source and drain terminals can be reverse-biased, driving a little reverse bias leakage current that contributes to the static power consumption.

The second cause of static power consumption is the conductivity of a MOS transistor not being completely equal to zero when the gate voltage does not reach V_t. Hence, inactive transistors allow a little subthreshold current to flow from supply to ground. Since the subthershold conduction decreases with V_t and V_t increases with V_{gs}, in some digital techniques like Variable Threshold CMOS (VTCMOS) [6] V_{gs} is increased when the circuit is in idle state in order to reduce subthreshold currents.

The objective of this paper is to study the static power consumption of gates using the independent body (INBO) approach and to determine that this design style is able to provide important static power savings when compared to the conventional common body (COBO) approach, due to the fact that the independent bodies of the transistors in the series tree provides additional isolation for drain and source diodes.

In section 2 the test set-up is described. Simulation results are presented and analyzed in section 3. Finally, we will summarize some conclusions.

2 Test Set-Up

Four input NAND and NOR gates have been designed using the COBO and INBO styles in order to measure their static power consumptions. The gates have been implemented using a 0.18 µm triple-well CMOS process with transistor sizes wn = 240 nm, wp = 240 nm for NAND (Fig. 3 and 4) and wn = 240 nm, wp = 1440 nm for NOR (Fig. 5 and 6) and minimum lengths.

In a NAND gate, any input with logic value equal to 0 forces the output value to 1 so 0 is typically called the *controlling value* for NAND gates. Analogously, in NOR gates the controlling value is 1. Inputs are named I_0, I_1, I_2 and I_3 with input index increasing for series transistors nearer the output (Fig. 1). The inputs vectors are numbered so that the number associated to the input vector (I_3, I_2, I_1, I_0) is $I_3 2^3 + I_2 2^2 + I_1 2^1$

+ $I_0 2°$. The input vector 5, for example corresponds to (I_3, I_2, I_1, I_0)=(0, 1, 0, 1). Input vector are classified depending on the output value they produce. In a NAND gate, input vectors 0 to 14 contain the controlling value so they produce an output value of 1. In this case, the leakage current is driven by the series NMOS tree. Input vector 15 corresponds to an output value of 0, and makes leakage current to by driven by the parallel PMOS tree. In a NOR gate, input vectors 1 to 15 correspond to leakage current happening in the series PMOS tree, while input vector 0 corresponds to leakage current in the parallel NMOS tree.

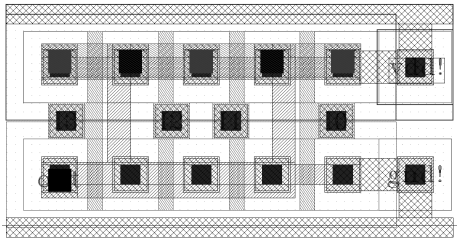

Fig. 3. Layout of a COBO NAND gate

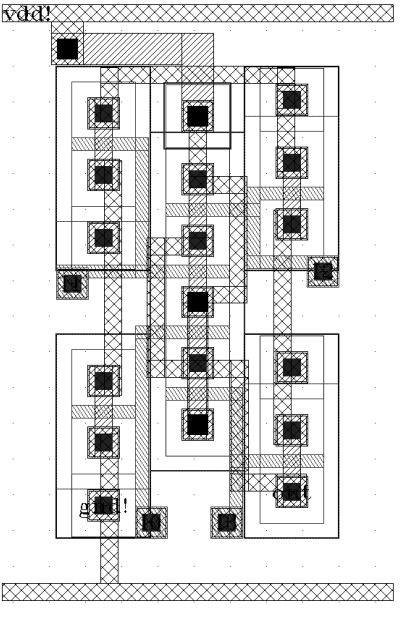

Fig. 4. Layout of an INBO NAND gate

The static power consumption is measured after parasitic extraction using the HSPICE [7] electrical simulator with the model card provided by the foundry and a nominal supply voltage of 1.8V.

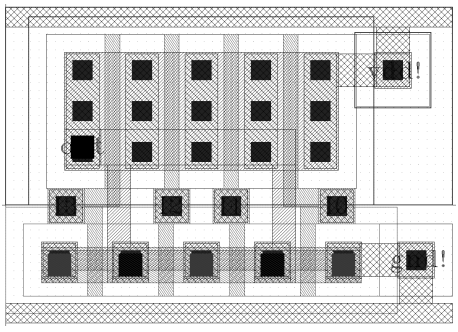

Fig. 5. Layout of a COBO NOR gate

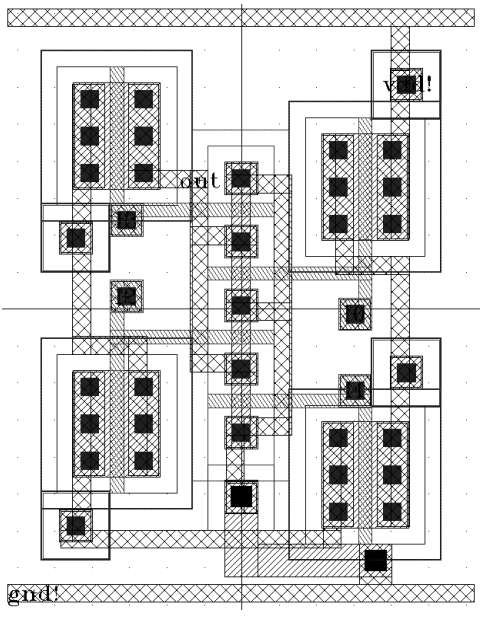

Fig. 6. Layout of an INBO NOR gate

3 Simulation Results

The static power consumption of NAND and NOR gates for all the possible input patterns and both INBO and COBO styles has simulated. Results are analyzed in two cases: patterns containing the controlling value, which correspond to static power dissipated in the series tree, and pattern of all inputs set to the non-controlling value, which corresponds to static power dissipated in the parallel tree. The first case is specially interesting since it is where INBO and COBO styles differ.

3.1 Input Patterns Containing the Controlling Value

The static power consumption for all possible inputs containing the controlling value is shown in Fig. 7 and 8 for NAND and NOR gates respectively. The input vectors have been grouped depending of the number of inputs set to the controlling value. As can be easily seen, the INBO gates have better performance in most of the cases.

From one group of patterns to the other, the major contribution is due to sub-threshold current. From group to group, the number o cut-off transistors increase and the total impedance of the chain increases as well in both types of gates (COBO and INBO). Static power in INBO gates is almost constant inside a group while it varies significantly in COBO gates.

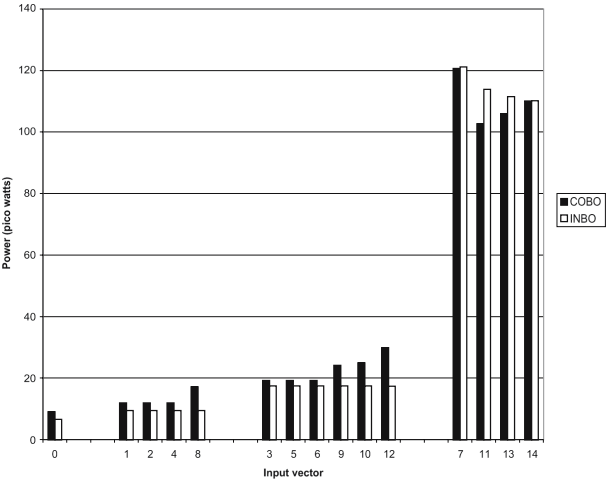

Fig. 7. Static power consumption of NAND gates for input vectors containing the controlling value

In the COBO style, the static consumption within a group will depend on the number of source/drain terminals that are reversed-biased. This is determined by the number of transistors in the series tree connected to the output by an active path. Thus, in the COBO NAND gate the input vector 12 ($I_3I_2I_1I_0$=1100) is more leaky than input vector 10 ($I_3I_2I_1I_0$=1010), since for the first vector there are three reverse-biased diodes while for the second vector there are only two (Fig. 9a). Input vectors 9 and 10 will in turn be leakier than 3, 5 and 6, since in the later ones only the drain diode connected to the output is reverse-biased.

In the INBO NAND gate, on the other hand, the source to body parasitic diodes can be neglected since source and body are connected together, and the drain to body diodes cannot be reverse-biased since the n-wells are not connected to ground (except the one corresponding to input I_0) as shown in Fig. 9b. The lack of reverse leakage currents in the INBO gates make them less leaky than their COBO counterparts in almost all the cases, and is the reason why its static power consumption is almost constant inside each group of patterns.

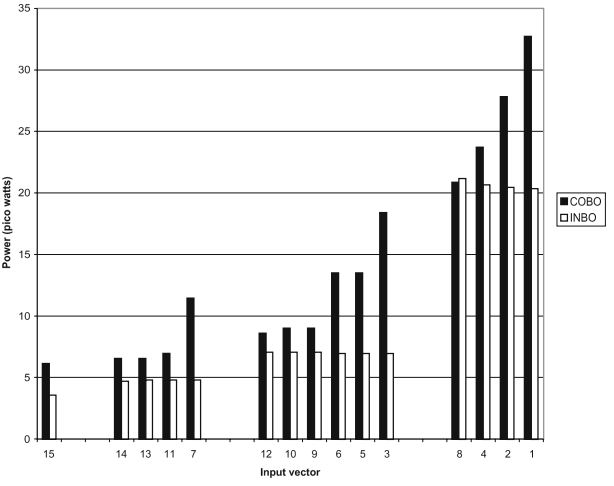

Fig. 8. Static power consumption of NOR gates for input vectors containing the controlling value

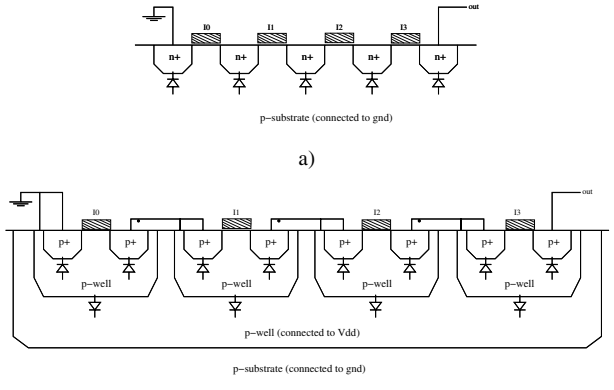

Fig. 9. NMOS tree in a NAND gate. a) COBO implementation b) INBO implementation

As mentioned in section 1, the transistors in the INBO gates present better conductance because they do not suffer from the body effect. This is specially evident when there is only one cut-off transistor in the tree. The transistors between the cut-off one and the output have better conductance in the INBO than in the COBO case. This is the reason why the INBO NAND gate is a bit leakier for input vectors 7, 11, 13 and 14 while the INBO NOR gate is slightly leakier for input vector 8.

Table 1 shows the minimum and maximum enhancements of INBO with respect to COBO for each gate and the overall power consumption assuming equal probabilities for each input vector. Improvements are specially remarkable for the NOR gate (over 30% overall) with particular improvements around 50% in both cases.

Table 1. Minimum, maximum and overall static power consumption enhancements of INBO gates with respect to COBO gates, for input vectors containing the controlling value

	COBO (pW)	INBO (pW)	Enhancement
NAND minimum	9	6.577	27 %
NAND maximum	120.735	121.183	-0.4 %
NAND overall	42.5	40.4	5.1 %
NOR minimum	6.1392	3.58	42 %
NOR maximum	32.742	21.18	35 %
NOR overall	14.325	9.83	31.4 %

3.2 Input Patterns Not Containing the Controlling Value

The static power consumption when all the inputs are set to the non-controlling value is shown in Table 2. In this case, the voltage of the body of the transistors in the serial tree is the same in the COBO and INBO implementations, so their behavior is almost the same. The power consumption comes from the sub-threshold currents of the transistors in the parallel tree, which is identical in both implementations. From Table 2, it is also clear that N-MOS transistors are leakier than P-MOS, as is also deduced from Figs. 7 and 8.

Table 2. Power consumption when all the inputs are set to the non-controlling value

	NAND (pW)	NOR (pW)
COBO	76.1	483
INBO	76.0	483

Table 3. Overall power consumption considering all the input vectors

	NAND (pW)	NOR (pW)
COBO	44.6	43.6
INBO	42.6	39.4
Enhancement	5 %	10 %

To summarize, Table 3 shows the overall power consumption considering the same probability for all the input vectors. The overall INBO enhancements for the NOR gate are reduced with respect to Table 1 due to the large contribution of pattern 0 (Table 2).

4 Conclusions

As triple-well technologies become main-stream, the use of independent bodies (INBO) for each series transistor in static CMOS logic brings remarkable performance improvements in speed, dynamic and static power consumption when compared

to the conventional common body approach (COBO) at the cost of some area penalty. INBO consumes less static power than COBO for almost all the input patterns with improvements up to 45% in NAND gates and up to 62% in NOR gates. This result stimulates further investigation on the application of the INBO style in a general way.

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