A Complete Retargeting Methodology for Mixed-Signal IC Designs

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Abstract - **In this paper, an efficient methodology to retargeting and reuse of embedded mixed-signal blocks is presented. Parametrized layout templates, accurate behavioral modeling of mixed-signal blocks, and appropriate mechanisms for tuning sized circuits to new sets of specs are its key components.**

1 Introduction

From the point of view of economics, and with the increasing ability to implement very complex systems within a silicon die (system on chip - SoC) with each new generation of the technology process, it is vital to shrink the SoC's design effort. A possible solution is a methodology shift based on the retargeting and reuse of previous designs. Design for retargetability and reusability is, clearly, a very effective option. In this context, **retarget** means re-size the required parts of a circuit/system to realize a change in its specifications. In its turn, **reuse** is the process in which the circuit/system is migrated and used in other technologies.

This paper presents a reuse and retargeting methodology applied to a mixed-signal design. In Section 2, the developed methodology is described. The technique used to create fully parameterized and technology portable layouts is introduced in Section 3, whereas Sections 4 and 5 are devoted to illustrate the remaining basic components of the methodology: behavioral models and size tuning. Finally, some experimental results have been included in Section 6.

2 Retargeting Methodology

The design flow to carry out the retargeting of an existing design to new specifications and/or a different technology process is illustrated in Fig. 1. First, the set of specifications are validated by checking that they are within the range of retargetability of the blocks. The design is carried out only if the specifications are validated, meaning that the new set of specifications falls within the range of the retargetability of the block. In principle, it is possible to define the range of retargetability so that the occurrence of unfinished designs is minimal. Nevertheless, by carrying out a tentative retargeting of a block based on assumptions of the validity of the specifications and by progressing through the different levels of the design, it is always possible to determine whether the design cannot be concluded.

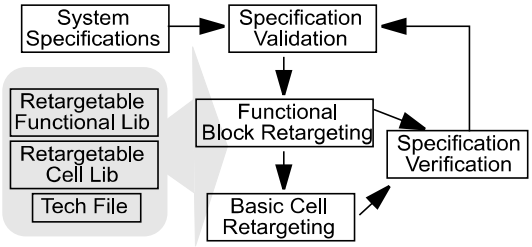

Figure 1: Flow diagram of the retargetable design environment.

The retargeting process proceeds hierarchically by tuning the existing designs to the new specifications. After tuning the functional building blocks, there is a process of tuning the component cells within each functional block. Tuning at any hierarchical level only affects the parts of the circuit components that need to be changed.

The tuning of each block at each hierarchical level is performed by using the iterative mechanism illustrated in Fig. 2. In case the design is being migrated to a different technology the existing layout templates are updated taking into account the layout design rules of the new technology. Layout extraction yields updating of the component block models (transistor-level description at the cell level and behavioral models at all other hierarchical levels). Block behavior is obtained by simulation (electrical simulation for transistor-level descriptions and behavioral simulation for intermediate blocks). According to the simulation results, size corrections are performed. This is the starting point in the retargeting flow in case that a new set of specifications must be met without a change in technology. For intermediate hierarchical levels, the outcomes of the size correction task are appropriate specifications for lower level blocks. At the cell level, size corrections directly provide suitable changes in device sizes. Application of changes to the layout templates allows to close the retargeting cycle.

Obviously, stopping mechanisms break this loop, when either the specifications for the block at that hierarchical level have been achieved or it is impossible to arrive at an appropriate solution. In the latter case, backtracking mechanisms impose additional constraints on the retargeting process at upper hierarchical levels.

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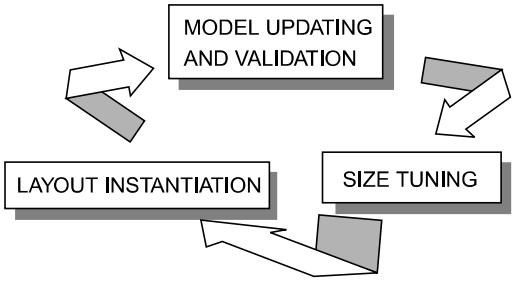

Figure 2: Retargeting cycle at each hierarchical level.

After the tuning of all the functional building blocks and circuit components has been completed, it is necessary to verify the correctness of the new performance characteristics and then proceed to the final processing and verifications.

The operation of the retargeting methodology proposed here will be demonstrated through the design of the CT Filter block in the I/Q DAC transmit interface in Fig. 3 [1].

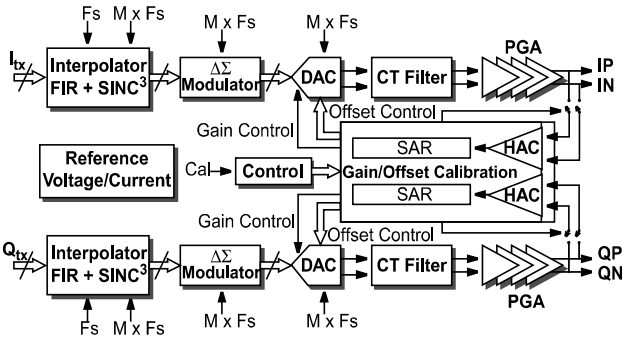

Figure 3: Block diagram of an IQ DAC.

3 Reusing and Retargeting Layouts

Layout corrections have to be provided at the different hierarchical levels. The objective of reusability is not to obtain the optimum design, but to reduce the time-to-market of a system design whose performance accomplishes the required specifications.

To this end, layout corrections are based on the tools, methods and languages available in the Cadence DFWII framework. The use of p-cell technology [2] makes an intensive use of parametrization, hierarchical cells, inheritance through hierarchical cells, and symmetries. The capability of p-cell technology to generate SKILL code, which can be externally modified, enables a full technology portability of the generated layouts [3].

4 Parameterized Behavioral Models

The objective of behavioral modeling is to represent circuit functions using abstract mathematical models that are independent of circuit schematics or architectures. They enable the reduction of the simulation time of the system, a very important feature in this context, since these behavioral models will be used in an iterative cycle of optimization and verification. The high-level description languages for digital circuits are not appropriate for a right behavioral description of analog systems, as long as the analog characterization is composed not only of the function that the circuit has to perform, but also the second-order non-idealities intrinsic to analog operation.

Efficiency/accuracy trade-off of behavioral models of analog blocks is parametrized. When tuning sub-block specifications, efficient, less accurate models are preferred to enable a fast, wide exploration of the design space, whereas for validating block behavior accurate models must be used.

5 The Optimization Stage

Size retargeting, both at the cell level and the functional level, is performed by using both deterministic and statistical optimization methods. Statistical techniques, although more expensive in terms of computation time, are more appropriate at initial stages of the retargeting process, where relatively large regions of the design parameter space should be explored. A statistical optimization technique, inspired on simulated annealing methods, has been developed whose control parameters offer different trade-offs between speed and quality of the retargeting results [4]. Deterministic methods, which are faster, are used for fine tuning circuit sizings.

A modular and flexible structure of the optimization core allows the incorporation of system-specific design rules and constraints, constraints from the existing layout templates for the different blocks, and evaluation procedures of the quality of the retargeted layout cells.

6 Experimental Results

In this section a complete example of the retargeting cycle of one of the blocks in Fig. 3: the continuous-time low-pass filter (CT-LP Filter) is presented. It is a current-driven fully-differential Tow-Thomas second-order low-pass filter, whose schematic is displayed in Fig. 4.

Constraints among the passive elements of the filter can be derived by assuring a maximally-flat transfer of the baseband signal to the filter output. The gain devices

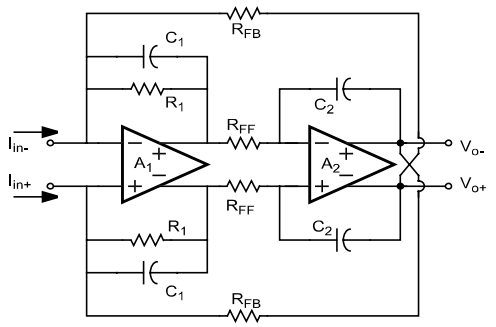

Figure 4: CT-LP Filter schematic

in the filter are fully-differential Miller compensated operational amplifiers.

The starting point in this flow is the validation of the high level specifications for this block, shown in Table 1. These specifications are referred to the GSM communication standard.

HIGH LEVEL SPECIFICATION	VALUE
Minimum Attenuation @13 MHz	20 dB
Group Delay Linearity from DC to 100kHz	<8.3 ns
I/Q Group Delay Mismatch from DC to 100kHz	<12 ns
I/Q Phase Mismatch @ 100kHz	<0.4 deg

Table 1: GSM high level specifications for the CT-LP Filter

Afterwards, it is necessary to tune the building blocks of the CT-LP Filter functional block. In other words, the specifications of these op-amps, such as gain-bandwidth product, dc gain and phase margin have to be found for the CT-LP Filter to achieve the specifications in Table 1. To this goal, behavioral models are used to reduce CPU consumption in each iteration cycle of the optimization process to identify proper op-amp specifications. The minimum specifications obtained from the optimization of the CT-LP Filter are shown in Table 2.

SPECIFICATION	OP-AMP A1	OP-AMP A2
Gain-Bandwidth product	> 26.5 MHz	> 21.2 MHz
DC Gain	> 50.0 dB	> 50.0 dB
Phase Margin	> 72.9 deg	> 46.9 deg
Gain Margin	> 20.3 dB	> 9.4 dB
Output resistance	< 40 kΩ	< 70 kΩ
Output Capacitance	< 0.6 pF	< 0.6 pF

Table 2: Obtained op-amp specifications from high level optimization

The optimization at behavioral level gives us also the correct values for the passive devices: $C_1 \equiv C_2 \equiv 3.8$ pF, $R_{FF} \equiv 427.9$ kΩ, $R_1 \equiv 39.9$ kΩ, $R_{FB} \equiv 7.445$ kΩ, so then the pole quality factor Q_0=0.7069 (the ideal case is Q_0=0.707).

Once the op-amp specifications have been found, the next step in the retargeting flow is the tuning of the op-amps at the electrical level. The targets of this tuning process are the resulting specifications from the behavioral level optimization in Table 2. In this case, the optimization process is composed of two stages, one for the core of the op-amp, in Fig. 5, and another for the tuning of the common-mode feedback circuit.

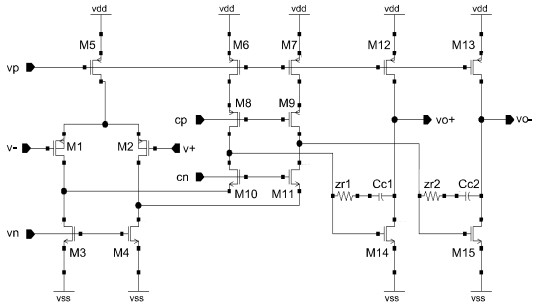

Figure 5: Core of the operational amplifiers of the CT-LP Filter

Table 3 contains the simulated characteristics of both op-amps of the CT-LP Filter, after the transistor level optimization process.

SPECIFICATION	OP-AMP A1	OP-AMP A2
Gain-Bandwidth product	30.4 MHz	55.7 MHz
DC Gain	102.5 dB	94.6 dB
Phase Margin	85.2 deg	62.5 deg
Gain Margin	33.4 dB	12.7 dB
Output resistance	9.9 kΩ	7.5 kΩ
Output Capacitance	0.3 pF	0.2 pF

Table 3: Simulated op-amp specifications from sized schematics

Transistor-level simulation results are displayed in Fig. 6. The figure shows the gain and phase curves of the first amplifier in the CT-LP Filter. In Fig. 7, the filter characteristics obtained from electrical simulation are plotted.

The results of the electrical tuning stage are passed down to the parameterized layout level.

The fully parameterized and technology-portable layout template of the CT-LP Filter can accept each one change in the sizes and values of the blocks and devices

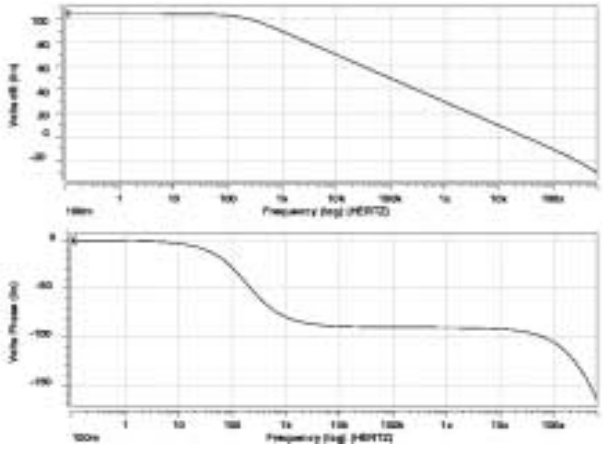

Figure 6: Op-Amp A1 ac behavior

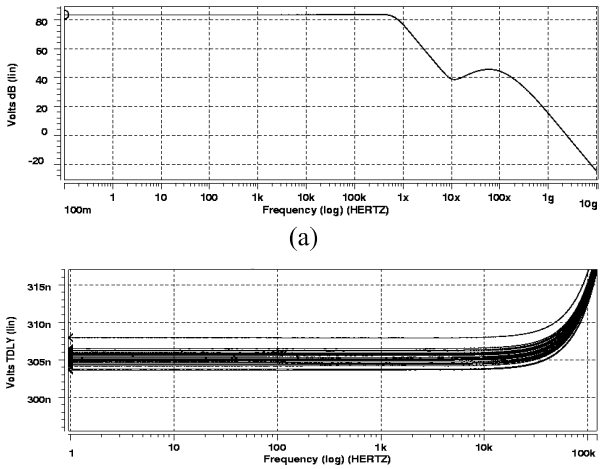

Figure 7: (a) CT-LP Filter ac magnitude and (b) MonteCarlo simulation of group delay between 1 and 100 kHz.

in the filter. The resulting retargeted layout is shown in Fig. 8.

Finally, some results from the electrical simulation of the extracted layout are shown in Table 4. As shown, the specs in Table 1 are met and, therefore, no new iteration of the retargeting methodology is needed.

The CPU time consumption on a workstation UltraSPARC (340 MHz), from the high-level specifications to the retargeted layout is 47.55 minutes.

HIGH LEVEL SPECIFICATION	VALUE
Minimum Attenuation @13MHz	44.8 dB
Group Delay Linearity from DC to 100kHz	6.7 ns
I/Q Group Delay Mismatch from DC to 100kHz	1.5 ns
I/Q Phase Mismatch @ 100kHz	0.06 deg

Table 4: Obtained CT-Filter Performance

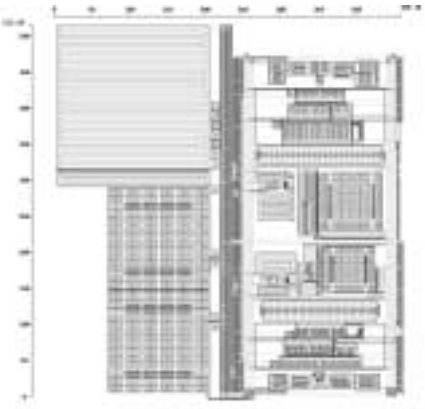

Figure 8: CT-LP Filter Retargeted Layout.

7 Conclusions

A useful methodology to retarget and reuse analog and mixed-signal designs has been presented. Descriptions of the basic components of this method have been included as well as a complete example of its use in practice.

Building reusable components can take up to four or five times the effort spent in building the corresponding non-reusable blocks. But it is important to note that: (1) when the library of reusable components grows up, the effort necessary to create one additional reusable block decreases, and, (2) the repetitive reuse of these components quickly compensates for the previous effort investment.

References

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Acknowledgments

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