EC-RASP: A new Electrical Energy Static Counter based on Random Signal Processing

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Conference Topic: IC's for instrumentation and control

Abstract— **This paper concerns the design and development of electrical energy static counter, based on random pulse stream processing. Measurement proceeding, calibration and hardware implementation are checked in a prototype. As a result, a simple low cost measurement system has been obtained. The resulting measures have been compared with the ones obtained using a poly phase commercial analyzer. A maximum 2% error has been achieved. This measurement proceeding is patent pending.**

I. State of art

Historically the monitoring of electrical energy consumption has been done by various types of induction watt meters. The conventional induction watt meter, with rotating disc and shaft, contains a mechanical register (driven by a gear on the shaft) which continuously displays the total accumulated kilowatt hours consumed. Switch or clutch activable mechanical demand and time of use registers are also used on these meters to display demand and time of use quantities.

Electronic registers are in common use today with induction type watt meter, to accumulate pulse data proportional to power consumption. This pulse data is usually provided to the register from an optical pick up or sensor device which senses meter disc rotation. These registers have the advantage that they can perform calculations on accumulated pulse data and electronically display much more information than is possible with conventional mechanical type registers.

Nowadays, better performances are required and achieved using static counters. In this sense, electric companies have found it desirable to measure, in addition to total kilowatt-hours, power factor, KVA, or reactive volt amperes. The measurement of reactive volt amperes typically has been accomplished by using a second meter in conjunction with the conventional kilowatt-hour meter. From the reactive volt amperes and the real volt amperes, quantities such as power factor and KVA can be calculated. This second meter for measurement of reactive volt amperes is a watt meter connected with phase shifting transformers in the voltage circuits.

It is also interesting to provide the capability to digitally configure the meter to measure electric energy flow in any of the different electrical services. Finally, it is desirable the possibility of connecting to either single phase or poly phase power line systems. All these characteristics should be accomplished by low cost and precise simple devices.

Presently, electronic counters and watt meters use either analog circuits, or an analog to digital conversion, followed by a pure digital processing, based on microprocessor systems, micro controller systems or digital signal processor (DSP).

In the following, several patents are described. European patent No. 94110967.0 [1] describes a static kWh meter that makes use of an analog multiplier. From the pulse-width modulated voltage, a pulse-width / pulse-height modulated signal, proportional to the power, is generated, using analog connectors. A frequency signal is thus obtained, which is passed through a divider circuit to the counter of the kWh meter for determination of the energy that has been consumed. Analog connectors have a detrimental property, because they produce extra voltage and current pulses in the signal to be measured. So, it is necessary to compensate this effect, including an additional electronic to solve the problem. Besides, typical disadvantages of analog electronic devices are present: noise sensitiveness, thermical sensitiveness, manufacturer tolerances . . .

European patent No. 94203283.0 [1] uses a digital signal processor from the analog to digital conversion of voltage and current. High number of performances are achieved at the expenses of a high cost device.

In this paper a new static energy counter is presented. That is, a counter in which both current

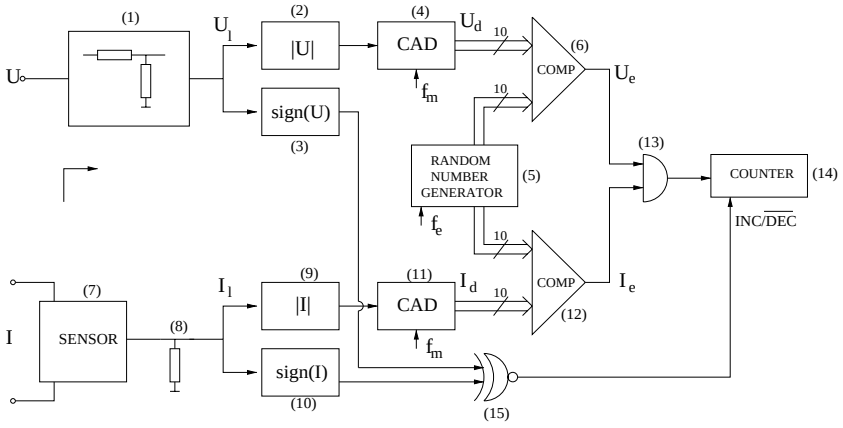

Figure 1: Detailed block diagram

and voltage change properties of solid state electronic devices, generating pulses of frequency proportional to kWh. At first, current and voltage are sensed and digital converted. Stochastic pulse streams are produced by comparing these digital numbers with random numbers. The multiplier is achieved by a simple AND gate. Its output is a random pulse stream that represents instantaneous active power. Time integration is achieved by a digital counter. It should be noticed that stochastic signal processing is entirely digital. In contrast with the last mentioned method our digital circuits are extremely simple and easily implemented in low cost programmable devices or ASICs, preserving all the performances described above.

In the following sections, it will be explained in detail the design and development of the measurement system. First of all, it will be described the mono phase architecture of an active energy counter, that has been implemented. Prototype characteristics, calibration proceeding and illustrative measurements will be shown next. Finally, possible generalizations and several conclusions will be withdrawn.

II. Mono phase architecture

Figure 2 is a simplified block diagram of the electronic meter: Rectified current and voltage signals are digital converted. Stochastic pulse streams are produced by comparing these digital numbers with random numbers. The multiplier is achieved by a simple AND gate. Instantaneous power, coded in the random pulse stream at the output of the AND gate, is time integrated by a counter that increases o decreases its value according to the multiplying signal signs.

Figure 1 is a detailed logic block diagram.

Blocks (1) and (7), connected to the wires of the

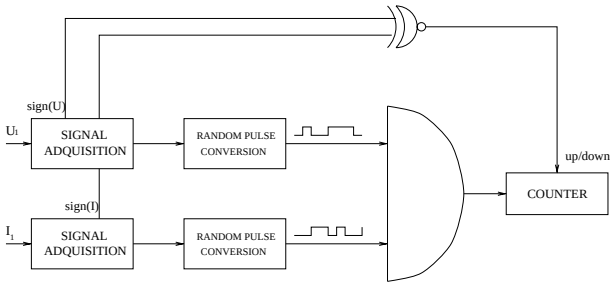

Figure 2: Block diagram

electricity network generates measures U_l and I_l, proportional to voltage (U) and current (I). Blocks (2) and (9) rectify both magnitudes and (3) and (10) calculate the sign. (4) and (11) make analog to digital conversion. (5) generates pairs of random number to get random pulse streams U_e e I_e. AND gate (13) generates the random pulses stream P_e, which codes instantaneous power. This power is integrated by a counter (14), which increases or decreases according to voltage and current signs.

III. Realization

In figure 3 a photograph of the prototype is shown: The prototype is a mono phase static active energy counter. This test board has been developed as a PC expansion board, in order to debug hardware easily. The test board includes a current interface with tariff devices, according to DIN 43864. Every 3600 $W \times s$, it is generated a current pulse greater than 30 ms.

Measurements of both current and voltage are taken from two transducers, according to figure 4. Actually, voltage transducer is not necessary. It could be used a simple resistor voltage divider.

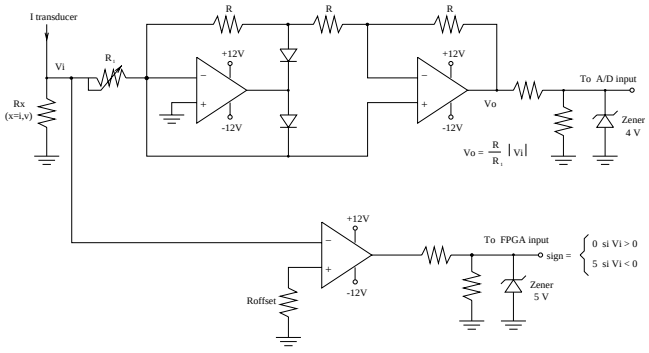

Figure 5: Rectification circuit

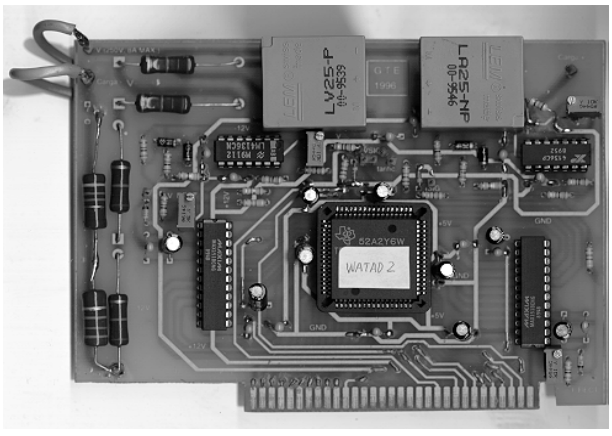

Figure 3: Prototype

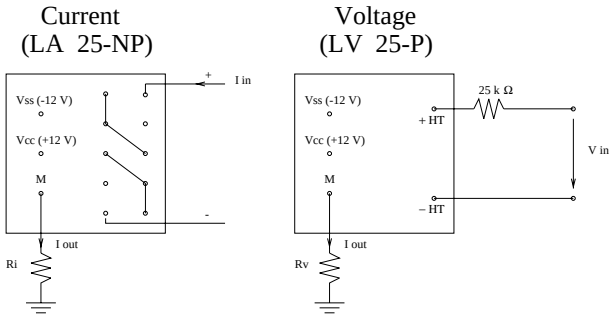

Figure 4: Schematic diagram of transducer connections

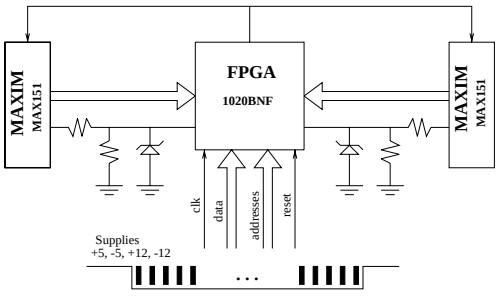

Figure 6: Test board

Rectification circuit is illustrated in figure 5.
Once signal acquisition has been completed and digital converted, data is fed into an Actel FPGA, 1020B, 509 logic blocks of 547 [3] [4] (93 %) (figure 6). The FPGA has been designed with Verilog [5] and synthesized with Cadence. Clock and supplies are taken from PC. Frequency clock is 8 MHz and sampling speed is 250 kHz. So, for each sample, 32 products of random streams are computed. Internally, a random number generator and a 32 bit counter, according to figure 1, is implemented inside the FPGA. This counter can be either increased or decreased, and is readable from the PC. Every time the PC reads the less significant byte of the counter, it resets automatically . This functionality has been included for debugging purposes.

IV. Calibration

It is necessary to define a calibration proceeding of the measurement system according to the scale limits. Maximum voltage value is 380 V, and maximum current value 7 A. That means that the value of a counter unit will be:

$$1pulse = \frac{V \times I}{8 \times 10^6} W \times s = 3.325 \times 10^{-4} W \times s$$

Maximum counting time is:

$$Time = \frac{2^{32}}{8 \times 10^6} = 536.87s = 8.947min$$

In two FPGA's pins, we extract voltage and current random pulse streams, and, with a very simple circuit, we recover analog value. This circuits consists of a low pass filter [6]. Calibration is done by two potentiometers that modify voltage and current gain.

A DC power supply has been used to modify voltage between 0 and 100 V. For 100 V and 3.75 A, analog value of current and voltage has been recovered at the end of the chain, that is, at the output of FPGA. Potentiometers has been calibrated so that we get the equivalent value of 100 V and 3.75 A at the output of the FPGA. Once calibration is finished, inter medium values are taken to check calibration quality. The result is illustrated in figures 7 and 8. Y axis represents in both cases the mean value at the output of the low pass filter, as mentioned above.

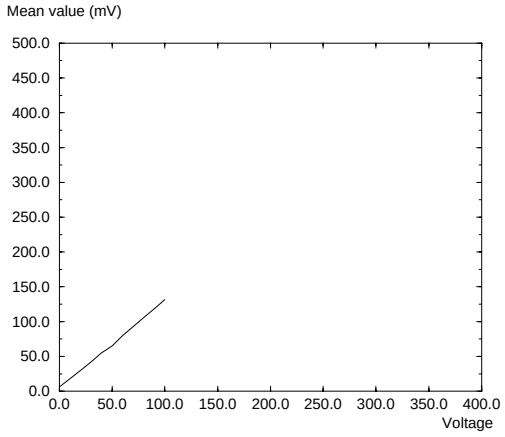

Figure 7: Voltage calibration

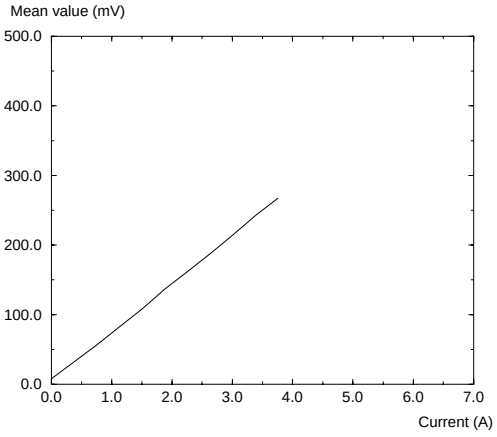

Figure 8: Current calibration

It can be observed that we do not cover the whole voltage and current scale, because our DC power supply is only up to 100V. Besides, there is an offset in current and voltage calibration that corresponds with one bit of the analog to digital converter.

Continuous power measurement error, for 2s time intervals, is detailed in figure 9. It has been represented real power and experimental power against voltage.

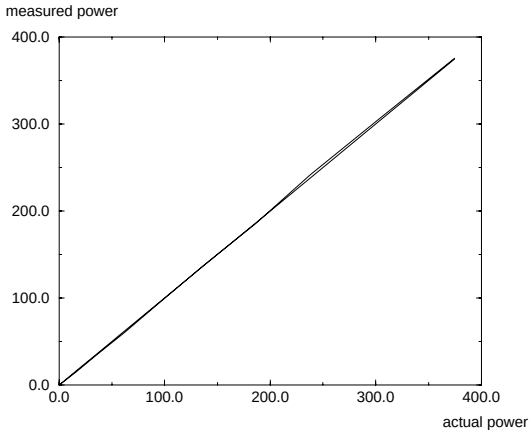

Figure 9: Continuous power measurement error

V. MEASUREMENTS

Measurements have been done using a poly phase analyzer Equa, based on a DSP technique, as a reference device [8]. Internally, Equa has a 0.2 % error in measurement of voltage and current. All other magnitudes are computed from these ones. Reference device uses the following equation to compute magnitudes:

- RMS voltage: $V_{L_{iN}} = \sqrt{\frac{\sum_{k=1}^{P} \nu_{L_{iN}k}^2}{P}}$
- RMS current: $I_{L_i} = \sqrt{\frac{\sum_{k=1}^{P} i_{L_ik}^2}{P}}$
- Active power: $W_{L_i} = \frac{\sum_{k=1}^{P} \nu_{L_{iN}k} \times i_{L_ik}}{P}$
- Reactive power: $Q_{L_i} = \frac{\sum_{k=1}^{P} \nu_{L_{iN}k} \times i_{L_i(k-\Delta)}}{P}$
- Power factor: $PF_{L_i} = \frac{W_{L_i}}{\sqrt{W_{L_i}^2 + Q_{L_i}^2}}$

where P=128, i=1,2,3 y Δ=P / 4. It can be noticed reactive power is computed using old current values instead of shifting instantaneous current value. Experimental results are separated from load:

- Resistive power factor:

PF	EC-RPS	Equa	Error
1	553.6	557	0.6 %
1	569.4	573.8	0.76 %
1	1088	1104	1.45 %

- Capacitive power factor:

PF	EC-RPS	Equa	Error
0.888	439.4	443	0.81 %
0.885	447.5	451	0.77 %
0.693	537	546	1.64 %

- Inductive power factor:

PF	EC-RPS	Equa	Error
0.994	536	538.7	0.50 %
0.994	556.8	560.6	0.67 %
0.979	1032	1045	1.24 %
0.979	513.5	519	1.05 %
0.979	524.8	530.6	1.09 %
0.923	900	916.3	1.7 %
0.910	86.81	86.13	0.78 %
0.834	81.88	82.3	0.51 %

Measures under 2% error are achieved. According to [7], this device would be a *class 2* static counter. In futures improvements, lower error values are expected. We can mention, although we have not included such results, the stability of measurements. The standard deviation of results is very low.

VI. Generalizations

From the mono phase description, its poly phase version can be easily deduced. According to figure 2, its generalization is drawn in figure 10:
A multiplexor is utilized to combine the power signal streams for each phase. Each phase is sequentially selected, increasing o decreasing the counter according to signs. The final result is a random codification of n-th part of instantaneous poly phase power at the multiplexor output, integrated in time by the counter.
Reactive power measurement is done by integration of reactive power. In the mono phase architecture, current is the same of the mono phase circuit, but voltage shifts 90 degrees respect voltage of mono phase circuit (figure 12).

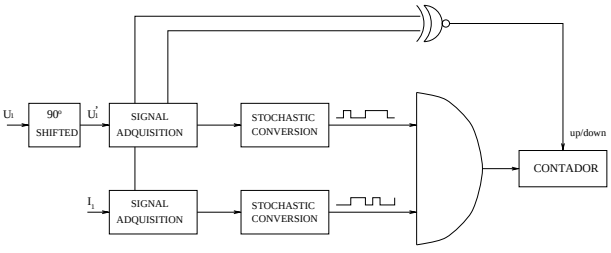

Figure 12: Reactive energy computation: mono phase architecture

Reactive poly phase energy will be the sum of reactive mono phase reactive energy. Again, the same multiplexor strategy is applied (figure 11).

VII. Conclusions

This paper describes the complete proceeding of design, development and calibration of an electrical energy counter based on random signal processing. It has been developed a FPGA prototype with satisfactory results. Above, it has been explained all the generalizations over this simple prototype, so we can achieve similar utilities given by moderns measurement equipments, based on DSP. But, as a great difference with these equipments, we have improved a low cost measurement system. One of these equipments have been used as a reference device. A maximum 2 % error has been obtained under any load condition.
As a future improve, we can think in an ASIC implementation. It would be positive a mixed technology ASIC, including analog to digital converters. This way, it would be only necessary a previous stage of signal acquisition before ASIC, reducing manufacturing cost. This measurement proceeding is patent pending [9].

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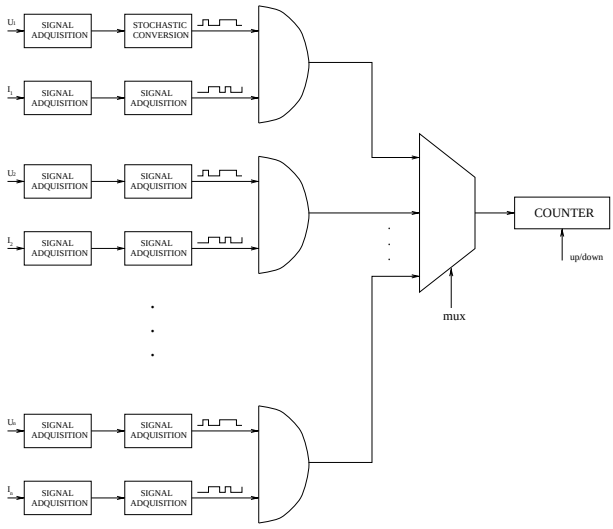

Figure 10: poly phase system generalization

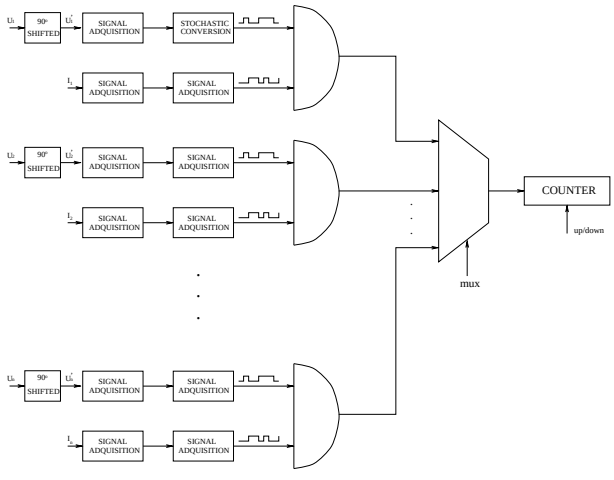

Figure 11: Reactive energy computation: poly phase architecture