# CMOS Fuzzifier Using Mixed-Signal Techniques with Emphasis in Power Consumption.

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***Abstract*— A novel mixed-signal CMOS membership function generator (MFG) is presented. It is based on an enhanced version of a linear tunable transconductor proposed in [1] and implements trapezoidal/triangular functions with all parameters (slope, position, width and height) independently and continuously adjustable. It is suitable to be used in analog and mixed-signal fuzzy circuits working in current mode. The computer simulations that verify the characteristics and performances of this circuit are given, showing high speed operation (up to 10 MHz input signals, working in continuous time) with low power consumption (about 80 $\mu A$ per MFG). The MIN-MAX rule of composition has been selected for the inference process. An innovative method for limiting power consumption has been devised for this kind of MFG. To this purpose, the winner-take-all circuit that makes the MIN operator, periodically deactivates its non-winning inputs. For non–fast varying input signals, considerable power saving can be achieved.**

## I. Introduction

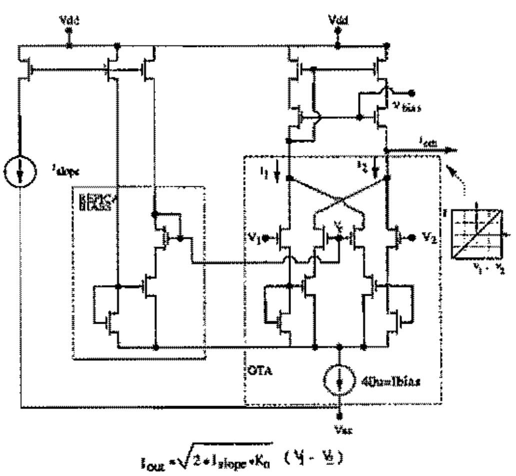


Fig. 1. Basic OTA circuit

In the last few years several implementations of analog fuzzy controllers have been proposed using either, a voltage-mode [2], [3] or a current–mode approach [3], [4], [5], [6]. The advantages of the current-mode approach are a great and flexible range of values and high speed. Most of the CMOS current-mode circuits proposed to build a MFG are based on the differential pair. This circuit produces sigmoidal type shapes and has good programming properties. But triangular/trapezoidal are the most used shapes in fuzzy literature.

Some of the circuits proposed in the literature have been used in the design of mixed–signal fuzzy controllers [6], [14], [13] to reduce the complexity of the controller. In this paper a novel mixed-signal CMOS MFG is presented. It is based on an enhanced version of a linear tunable transconductor proposed in [1] and the piecewise–linear approximation to function synthesis proposed in [7]. This OTA has excellent properties in terms of linearity and tunability. Furthermore, with the help of MAX-MIN circuits, it is possible to generate any type of piecewise linear (PWL) function. The MFGs obtained with this method are fully and continuously programmable. The MAX-MIN circuits can also be used to reduce the power consumption of the MFG. The bias current of the membership function generators, which are the most power demanding part in our fuzzy controllers, can be periodically switched off depending on the result of the inference process, achieving considerable power saving for non–fast varying input signals.

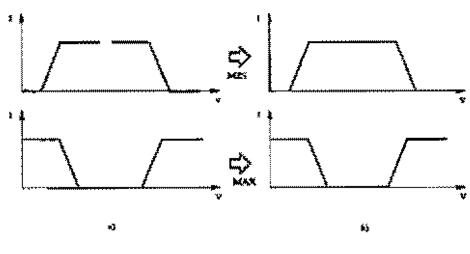


Fig. 3. Membership function shapes

This paper is organized as follows. Section II describes the architecture of the MFG and the way to generate triangular, trapezoidal and PWL shapes. The mixed-signal scheme is detailed in Section III. Section IV presents some results and advances future research.

## II. Architecture of the MFG

Figure 1 shows the OTA circuit used to build the MFG. Compared to the OTA proposed in [1], this circuit presents two differences that enhance the performances obtained in a previous implementation [8]:

• Power consumption is limited by means of the current source $I_{bias}$. In its absence, power consumption would increase with the common mode input voltage.

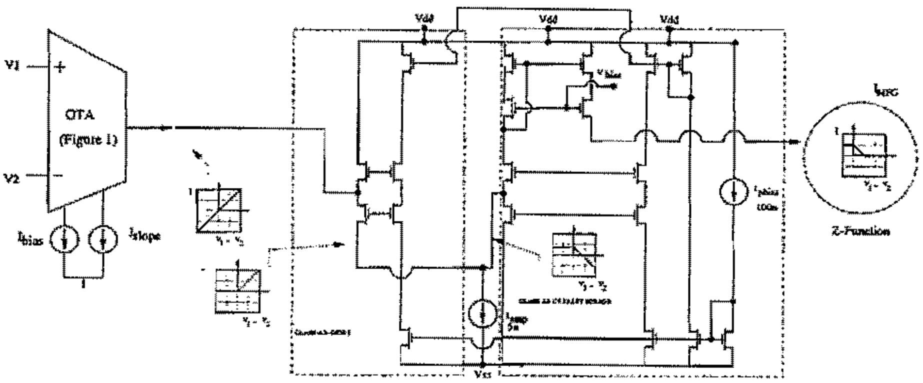

Fig. 2. Z-function generator

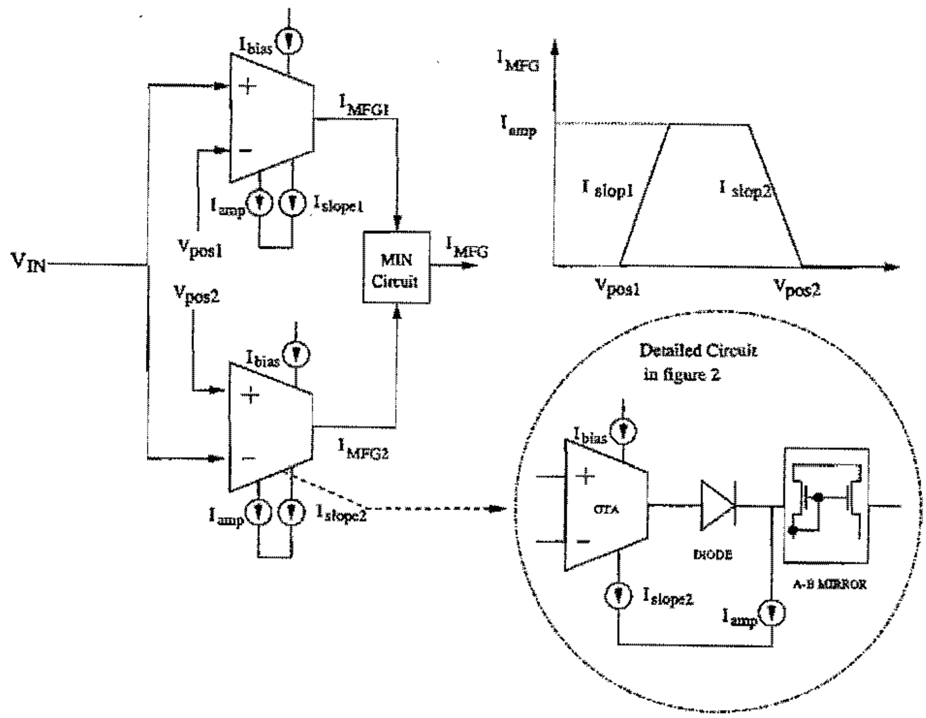


Fig. 4. Membership Function Generator (MFG)

• The bias voltage $V_c$ is generated by means of a replica biasing circuit, making the current output independent on the threshold voltages of MOS transistors. In figure 1, the output current $I_{out}$ is given by:

$$I_{out} = \sqrt{2I_{slope}k_n}(V_1 - V_2) \quad (1)$$

Note that the output transconductance only depends on technological parameter $k_n$. Even this dependence can be canceled using two OTA's and a multiplier/divider block, as proposed in [9].

To build a Z-function it is necessary to saturate the OTA response. This operation is carried out by means of a current rectifier and current mirrors as shown in figure 2. Note that class AB current mirrors have been used to achieve high speed of operation. The fuzzy controller input directly drives one OTA input, while the other defines the position of the Z-function on the X-axis. The amplitude of the Z-function can be programmed by the $I_{amp}$ current source, while $I_{slope}$ changes the slope.

### A. Use of the Z-function

The functions shown in figure 3a (Z-functions) can be generated with the circuit in figure 2. Note that if the position and slope of the Z-functions can are selected , any type of triangular/trapezoidal shapes can be constructed with the help of one MIN(MAX) operator (see figure 3b, and figure 4 for its hardware implementation).

However, as MIN operators are also required to perform the inference process, this type of MFG only duplicates the number of inputs of the MIN circuits that perform the inference process. This is not a high price to be paid, because each additional input to a MIN circuit only requires two transistors.

The MIN operator can be built by means of a MAX function using complementary logic and the De Morgan's Law:

$$I_{MFG} = MIN(I_{MFG1}, I_{MFG2}) \Rightarrow \quad (2)$$
$$\hat{I}_{MFG} = MAX(\hat{I}_{MFG1}, \hat{I}_{MFG2}) \quad (3)$$

where $\hat{I}$ is the complement of I, i.e., $\hat{I} = I_{amp} - I$

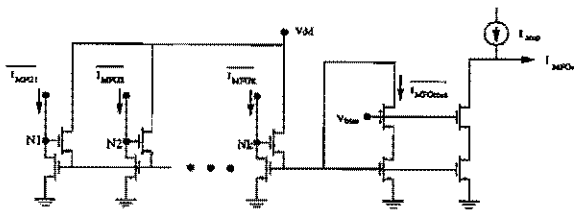

Fig. 5. Max Circuit

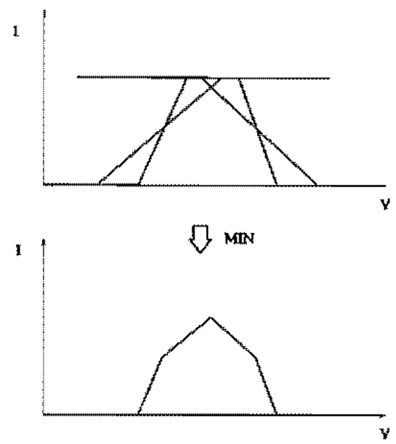


Fig. 6. An example of PWL function generation

The MAX circuit proposed in [10] and later improved in [11] for fuzzy hardware applications, is shown in figure 5.

Changing the MIN circuit of figure 4 by a MAX circuit, the complementary shape can be produced. Furthermore, it is easy to see that we can construct any PWL function by combining several Z-functions with MAX/MIN circuits (figure 6).

## III. Mixed-Signal Scheme

In this section a novel scheme to reduce power consumption of the fuzzifier previously defined is presented. This scheme is also suitable to be used with MFGs implemented with diferent transconductors.

In the previous section we used Lazzaro's circuit to perform inference process (min-max operator). This circuit is a mixed-signal circuit as all nodes $N_i$ in figure 5 have a low voltage value except in the node with the winning current. The information stored in those nodes can be sampled to periodically turn off the loosing MFGs that are not adding information to the circuit output.

In our mixed-signal fuzzifier (figure 7) we need to turn off the bias current of the non-winning MFG circuits that form a rule. It is obvious that this process slows down the operation of the fuzzifier and the resulting fuzzy controller has a lower bandwidth. If a higher bandwidth is needed it is possible to partially turn off the current sources making the turn on process faster. The achieved power saving will depend the sampling frequency. For example, if a sample frecuency of $100kHz$ is selected, the measured power consumption is the 15% of the fuzzifier's power consumption working in continuous time. This important power saving (around 85%) can be programmable if low sample frequency is selected.

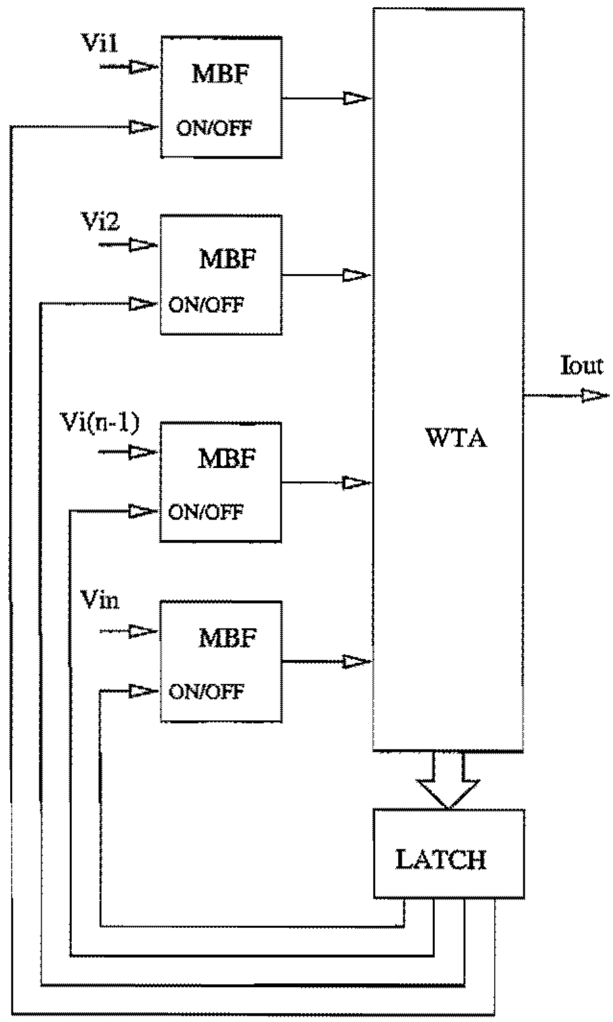


Fig. 7. Mixed-Signal Fuzzifier Scheme.

Lazzaro's circuit needs to be redefined for mixed-signal operation (figure 8) as the output signal doesn't need to be copied from the winning (maximum) current. Using analog switches and simple digital circuit it is possible

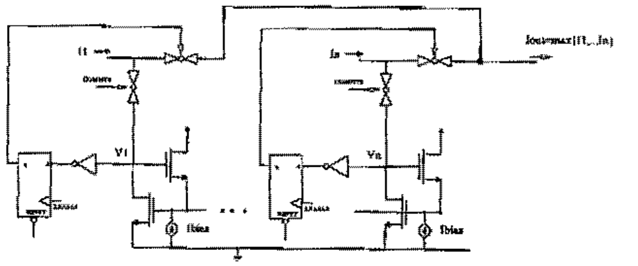

Fig. 8. Mixed-Signal MAX circuit.

to take the winning current to the output. This novel technique reduces noise and offset as only one MFG is adding signal to the output. Also there is no copy error as the winning value is directly passed to the output. This scheme can be also used in neural networks with winner-take all circuits to reduce power consumption.

## IV. Simulation Results

The membership function generator depicted in figure 4 has been designed using a 0.8 $\mu m$ CMOS technology. The area of the complete MFG is 0.07 $mm^2$, and the static power consumption is 80 $\mu A$. Figures 9 to 13 show postlayout simulation of the MFG.

In figures 9 and 10 the position and width tunability of the MFG is shown. Note that the position of the Z-functions is controlled by means of $V_{pos1}$ and $V_{pos2}$ OTA inputs.

Figure 11 shows the gain tunability of the OTA circuit. This figure has been obtained changing the $I_{slope}$ current source.

The transient response of the MFG circuit is shown in Figure 12. In this figure, the MFG input is a voltage ramp. Note that the maximum delay is less than 100ns (about 70ns).

Finally, figure 13 shows an example of a PWL function generated using OTA's and MAX/MIN circuits.

Presently, the mixed-signal version of the MFG circuit is being sent to fabrication and experimental results will be provided in the final version of the manuscript.

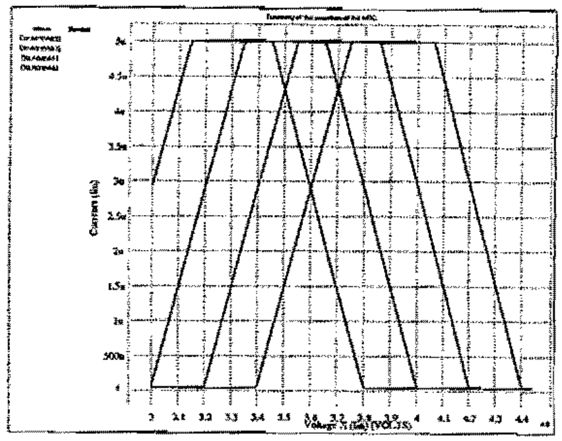

Fig. 9. MFG position tunability

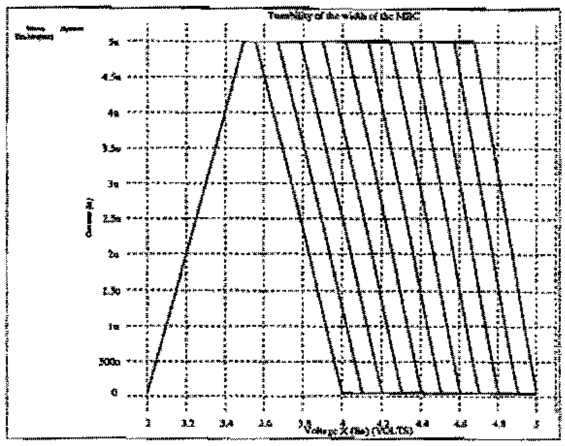

Fig. 10. MFG width tunability

## V. Acknowledgments

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## References


[1] S. C. Huang and M. Ismail, "Linear tunable COMFET transconductors", *Electronics Letters*, vol 29, pp. 459-461, March 1993.

[2] Shuwei Guo, Liliane Peters and Hartmut Surmann, "Design and Application of an Analog Fuzzy Logic Controller". *IEEE Transactions on Fuzzy Systems* vol. 4, no. 4, November 1996.

[3] J. Ramírez-Angulo, K. Treece, P. Andrews and T. Choi. "Current-Mode and Volage-Mode VLSI fuzzy processor architecture". *Proc. Int. Conf. on Circuits and Systems, ISCAS'95*, pp 1156–1159, Seattle 1995.

[4] L. Lemaitre, M. J. Patyra and D. Mlynek "Analysis and design of CMOS fuzzy logic controller in current mode". *IEEE Journal of Solid-State Circuits*, vol. 29, pp 317–322, March 1994.

[5] Kyoto Tsukano and Takahiro Inoue, "Synthesis of Operational Transconductance
Amplifier–Based Analog Fuzzy Functional Blocks and Its Application".*IEEE Transactions on Fuzzy Systems*, vol. 3 no.1, February 1995.

[6] I. Baturone, S. Sánchez-Solano, A. Barriga and J.L. Huertas, "Implementation of CMOS Fuzzy Controllers as Mixed-Signal Integrated Circuits". *IEEE Transactions on Fuzzy Systems*, vol, 5, no 1, February 1997.

[7] E. Sánchez-Sinencio, J. Ramírez Angulo, B. Linares-Barranco and A. Rodríguez Vázquez, "Operational Transconductance Amplifiers for nonlinear function syntheses". *IEEE Journal of Solid-State Circuits*, pp 1576-1585, Dec. 1989.

[8] R.Carvajal, A.Torralba, F.Colodro and L.G.Franquelo. "An Analog CMOS Universal membership Function Circuit with fully independent, adjustable parameters", in *Proc. of the 12th Design of Circuits and Integrated Systems Conf.*, pp. 407–411. Sevilla, Nov. 1997.

[9] P.Saavedra, A.López, J.Zrilic, J.Ramírez Angulo. "New analog current-mode/voltage mode fuzzifier with continuously adjustable parameters", in *Proc. of the 40th Midwest Symp. on Circ. and Syst.*, Aug. 3-6, 1997, Sacramento, CA.

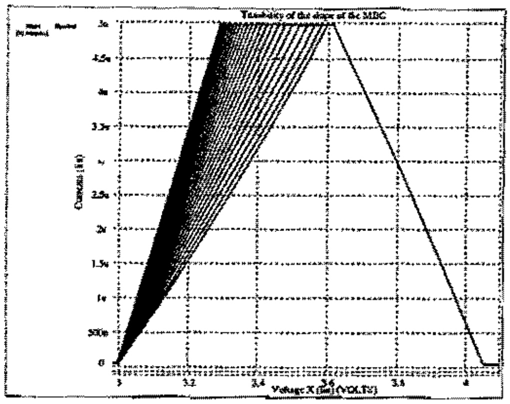

Fig. 11. MFG slope tunability

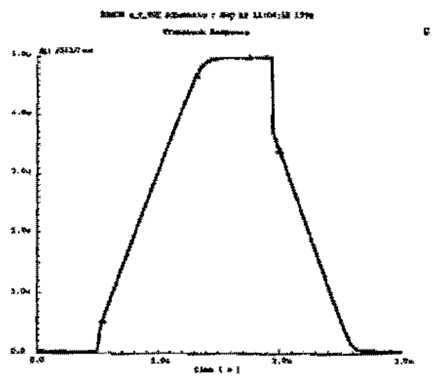

Fig. 12. Transient response of the MFG circuit

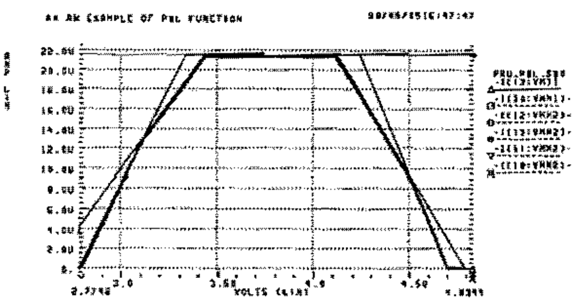

Fig. 13. PWL function generated with OTA's and one MIN circuit


[10] J. Lazzaro, S. Ryckebusch, M. A. Mahowald and C. A. Mead. "Winner-Take-All Networks of O(n) Complexity". *Advances in Neural Information Processing Systems*, vol. 1, D.S. Toureztky, ed. Morgan Hauffmann, 1989.

[11] Bin-Da Liu and Chun-Yueh Huang. "Array Based Fuzzy Inference Mechanism Implemented with Current-Mode CMOS Circuits". *Proc. Int. Conf. on Circuits and Systems, ISCAS'94* vol. 5, London, June 1994.

[12] M. Sasaki, T. Inoue, Y. Shirai and F. Ueno. "Fuzzy Multiple-Input Maximum and Minimum Circuits in Current Mode and Their Analyses Using Bounded-Difference Equations". *IEEE Transactions on Computers*, vol. 39, no. 6, June 1990.

[13] J. Tombs, A. Torralba and L.G. Franquelo. "A PWM fuzzy logic controller". *IEEE MICRO*, pp 68–71, October 1996.

[14] U. Çilingiroglu, B. Pamir, Z.S. Günay and F. DÜlger. "Sampled-Analog Implementation of Application-Specific Fuzzy Controllers". *IEEE Transactions on Fuzzy Systems*. vol. 5, 1997