A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge

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***Abstract*—In this paper, a new three-phase, five-level inverter topology with a single-dc source is presented. The proposed topology is obtained by cascading a three-level flying capacitor inverter with a flying H-bridge power cell in each phase. This topology has redundant switching states for generating different pole voltages. By selecting appropriate switching states, the capacitor voltages can be balanced instantaneously (as compared to the fundamental) in any direction of the current, irrespective of the load power factor. Another important feature of this topology is that if any H-bridge fails, it can be bypassed and the configuration can still operate as a three-level inverter at its full power rating. This feature improves the reliability of the circuit. A 3-kW induction motor is run with the proposed topology for the full modulation range. The effectiveness of the capacitor balancing algorithm is tested for the full range of speed and during the sudden acceleration of the motor.**

***Index Terms*—Flying capacitor (FC), H-bridge, induction motor drive, multilevel inverter.**

I. Introduction

MULTILEVEL inverters have changed the face of medium- and high-voltage drives [1], [2]. The most popular topologies of multilevel converters are the neutral-point-clamped inverter (NPC) [3], the flyin capacitor inverter (FC) [4], and the cascaded H-bridge (CHB) inverter [5]. Each one of these inverters has its own merits and demerits [1]. In the NPC inverter [3], multiple dc sources are generated by splitting a single-dc bus voltage using capacitor banks. This configuratio has large number of clamping diodes and presents the problem of dc bus capacitor unbalance especially with high number of voltage levels [6], [7]. An interesting work for balancing capacitors in NPC inverter that can be operated in limited modulation range has been presented in [8]. A pulse-width modulation (PWM) control scheme to balance the dc link capacitor voltages of the NPC inverter, connected in cascade with a two-level inverter to realize a fi e level inverter structure for an open-end winding induction motor, is proposed in [9].

The concept of FC inverter was introduced firs in 1992 [4]. In this configuration multiple capacitors of different voltage magnitudes are used to generate multiple voltage levels. The advantages include modularity, lack of clamping diodes, lack of problems like unbalance in the split dc -link capacitors, etc. Also, as in the NPC case, single supply can be used to generate multiple pole voltage levels. Many strategies for balancing the capacitor voltages have evolved over time [10], [11]. However, generating more voltage levels in a FC inverter requires larger number of capacitors. Interesting derivatives of this configura tion have been presented in [12] and [13], where more levels have been achieved by cross connecting the capacitors using additional switches. Operation of FC inverter with improved reliability has been presented in [18], where additional circuitry is provided to bypass the faulty cell. However, in this scheme, the devices have to be sufficientl overrated to operate at full power level when the faulty cell is bypassed. The operation of FC inverter with asymmetrical capacitor voltages to generate more voltage levels has been presented in [15]. In this configuration the number of voltage levels that can be achieved depends on the modulation index and the power factor.

The multilevel CHB inverter with isolated supplies presented in [5] has many advantages compared to the NPC and FC topologies. The CHB configuratio does not require clamping diodes and the input power is distributed among different input sources that makes it more suitable for certain applications [16]. One additional advantage of the CHB converter is that if any device fails in the H-bridges, the inverter can still be operated at reduced power level and, hence, this configuratio is fault tolerant to some extent [17], [18]. The concept of using CHBs with capacitors and their voltage balancing has been introduced in [19] and [20]. The advantages include more redundant states, better voltage balancing, lack of clamping diodes, and fault tolerant operational ability by bypassing the faulty H-bridge cells. This configuratio is especially suitable for applications like STATCOM. DC-voltage ratio control strategy for a CHB converter fed with a single-dc source is presented in [21]. With this control strategy, a higher number of levels in output voltage waveform can be achieved with capacitor voltage balancing in a limited range of load power factor. This scheme is very much suitable for grid-connected applications. A multilevel config uration with improved reliability has been presented in [22] and [23].

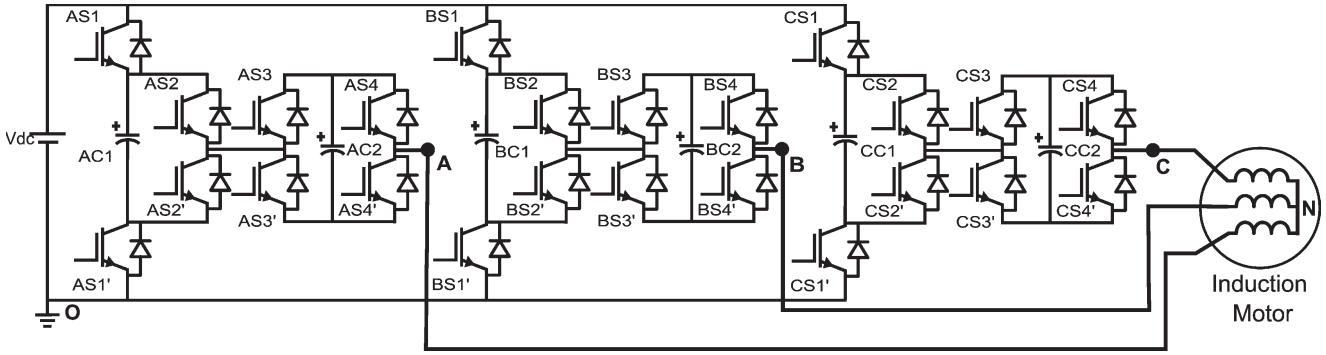

Fig. 1. Proposed three-phase power circuit formed by the connection of a three-phase flyin capacitor inverter with H-bridges in series.

Many other multilevel inverter configuration have been developed based on the three conventional (NPC, FC, and CHB) topologies. A configuratio in which two-level inverter is cascaded with multiple H-bridges has been presented in [24], where more voltage levels can be generated. New multilevel inverter configuration for open-end winding induction motors, formed by cascading two-level inverters and capacitor-fed H-bridges are given in [25] and [26].

Five-level active neutral point clamped (ANPC) inverter topology [27] is another configuration which is a hybrid of FC topology and NPC configuration This fi e-level ANPC converter is being commercialized by ABB as the ACS2000 (up to 1.6 MW). The configuratio presented in [28] introduces the concept of integrating the cross-connected intermediate level [29] and the ANPC configuratio to form a hybrid configuration A hybrid derivative of the ANPC configuratio and CHB has been presented in [30]. Derivatives of CHB where different devices [Integrated Gate-Commutated Thyristor (IGCT) and insulated gate bipolar transistor (IGBT)] are used in such a way that the IGCT would switch at fundamental frequency and IGBT would switch at carrier frequency has been presented in [31]. The concept of a hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells has been presented in [32]. The hybrid clamped multilevel inverter topology [33] is a hybrid of NPC topology and FC topology, which does not have neutral point fluctuation

The multilevel inverter proposed in this paper is a cascaded topology consisting of three-level FC inverters and capacitor-fed H-bridges, in which balancing of the capacitor voltages are possible independently of the load power factor.

II. Proposed Power Circuit

As shown in Fig. 1, the proposed topology has a three-level FC inverter with dc bus voltage of $V_{\rm DC}$ and FC voltage equal to $V_{\rm DC}/2$, which can generate voltages of 0, $V_{\rm DC}/2$, and $V_{\rm DC}$ with respect to point 0. A capacitor-fed H-bridge is cascaded to each phase of the inverter. The voltage across the H-bridge capacitor has to be maintained at $V_{\rm DC}/4$. This combination can produce voltage levels of 0, $V_{\rm DC}/4$, $V_{\rm DC}/2$, $3V_{\rm DC}/4$, $V_{\rm DC}$, $-V_{\rm DC}/4$, and $5V_{\rm DC}/4$. Out of these, the voltages $-V_{\rm DC}/4$ and $5V_{\rm DC}/4$ are not used in the proposed inverter as they do not have redundant switching states to balance the capacitor voltages. The switching states of the useful voltage levels and their effects on the capacitor voltages based on the current direction are given in Table I.

The capacitor voltages remain unaffected while producing the voltages $V_{\rm DC}$ and 0. The capacitors can either be charged or discharged in any direction of the current for the voltages $V_{\rm DC}/4$, $V_{\rm DC}/2$, and $3V_{\rm DC}/4$ as shown in Figs. 2–4, respectively. In each phase, the switches S1, S2, S3, S4 and S1′, S2′, S3′, S4′ are operated in complementary manner. The output voltage is based on the switching states that decide the path of the current fl w.

For voltage levels of $V_{\rm DC}/4$ and $3V_{\rm DC}/4$, there are three redundant states. By switching between these three states the capacitors C1 and C2 can be charged or discharged for any direction of the current. The voltage level of $V_{\rm DC}/2$ has two redundant states. By switching between them, C1 can be charged or discharged based on the current direction. When $V_{\rm DC}/2$ is applied, the C2 is not affected. As the capacitors can be either charged or discharged by switching between the redundant states, based on the current direction, quick capacitor voltage balancing is possible, irrespective of the load power factor. To maintain the capacitor voltages at a f xed value, the capacitor voltages are sampled at regular intervals and a hysteresis controller is used to switch between the redundant states based on the current direction to balance the capacitor voltages.

Each pole can generate one of the f ve voltage levels 0, $V_{\rm DC}/4$, $V_{\rm DC}/2$, $3V_{\rm DC}/4$, and $V_{\rm DC}$. The effective voltage space vector formed based on the three-phase pole voltages is given by

$$V_{\rm SV} = V_{\rm AO} + V_{\rm BO}\angle 120^\circ - V_{\rm CO}\angle 120^\circ \qquad (1)$$

where $V_{\rm SV}$ is the voltage space vector and $V_{\rm AO}$, $V_{\rm BO}$, and $V_{\rm CO}$ are the pole voltages in the three phases A, B, and C, respectively.

The f ve-level space vector diagram obtained for the combinations of the pole voltages of the three phases is shown in Fig. 5. There are 61 voltage vector locations possible for the fi e-level space vector structure. Many of the voltage vector locations have redundant switching state combinations of the pole voltages of three phases. The switching state combinations for a space vector sector of 60° interval (as shown shaded in Fig. 5) are presented in Table II. The space vector locations 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, and 60 are located on the outermost hexagon and these vectors can be obtained with only one pole-voltage

TABLE I
VARIOUS VOLTAGE LEVELS AND CAPACITOR STATES BASED ON THE SWITCHING STATES

S.No	Switch State (S1,S2,S3,S4)[b]	V_{AO}	I_A[a]	Cap C1 (V_{DC}/2)	Cap C2 (V_{DC}/4)
1	(0,0,1,0)	-V_{DC}/4	+	No effect	Charge
2	(0,0,0,0)	0	+	No effect	No effect
3	(0,0,1,1)	0	+	No effect	No effect
4	(0,0,0,1)	V_{DC}/4	+	No effect	Discharge
5	(0,1,1,0)	V_{DC}/4	+	Discharge	Charge
6	(1,0,1,0)	V_{DC}/4	+	Charge	Charge
7	(1,0,0,0)	V_{DC}/2	+	Charge	No effect
8	(0,1,0,0)	V_{DC}/2	+	Discharge	No effect
9	(0,1,1,1)	V_{DC}/2	+	Discharge	No effect
10	(1,0,1,1)	V_{DC}/2	+	Charge	No effect
11	(0,1,0,1)	3V_{DC}/4	+	Discharge	Discharge
12	(1,0,0,1)	3V_{DC}/4	+	Charge	Discharge
13	(1,1,1,0)	3V_{DC}/4	+	No effect	Charge
14	(1,1,1,1)	V_{DC}	+	No effect	No effect
15	(1,1,0,0)	V_{DC}	+	No effect	No effect
16	(1,1,0,1)	5V_{DC}/4	+	No effect	Discharge
17	(0,0,1,0)	-V_{DC}/4	-	No effect	Discharge
18	(0,0,0,0)	0	-	No effect	No effect
19	(0,0,1,1)	0	-	No effect	No effect
20	(0,0,0,1)	V_{DC}/4	-	No effect	Charge
21	(0,1,1,0)	V_{DC}/4	-	Charge	Discharge
22	(1,0,1,0)	V_{DC}/4	-	Discharge	Discharge
23	(1,0,0,0)	V_{DC}/2	-	Discharge	No effect
24	(0,1,0,0)	V_{DC}/2	-	Charge	No effect
25	(0,1,1,1)	V_{DC}/2	-	Charge	No effect
26	(1,0,1,1)	V_{DC}/2	-	Discharge	No effect
27	(0,1,0,1)	3V_{DC}/4	-	Charge	Charge
28	(1,0,0,1)	3V_{DC}/4	-	Discharge	Charge
29	(1,1,1,0)	3V_{DC}/4	-	No effect	Discharge
30	(1,1,1,1)	V_{DC}	-	No effect	No effect
31	(1,1,0,0)	V_{DC}	-	No effect	No effect
32	(1,1,0,1)	5V_{DC}/4	-	No effect	Charge

[a] (+) indicates the current direction from A to O of the load.
[b] (1) indicates ON state and (0) indicates OFF state of the switch.

combination. The locations 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, and 36 are located in the third largest hexagon and have two redundant states. The locations 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are located in the second largest hexagon and have three redundant states. The space vector locations 1, 2, 3, 4, 5, and 6 are located in smallest hexagon and have four redundant states. The zero vector location 0 has fi e redundant states in total. The redundancies in the switching state combination for realizing a particular voltage space vector location can be effectively used for PWM control to minimize the inverter switching transitions.

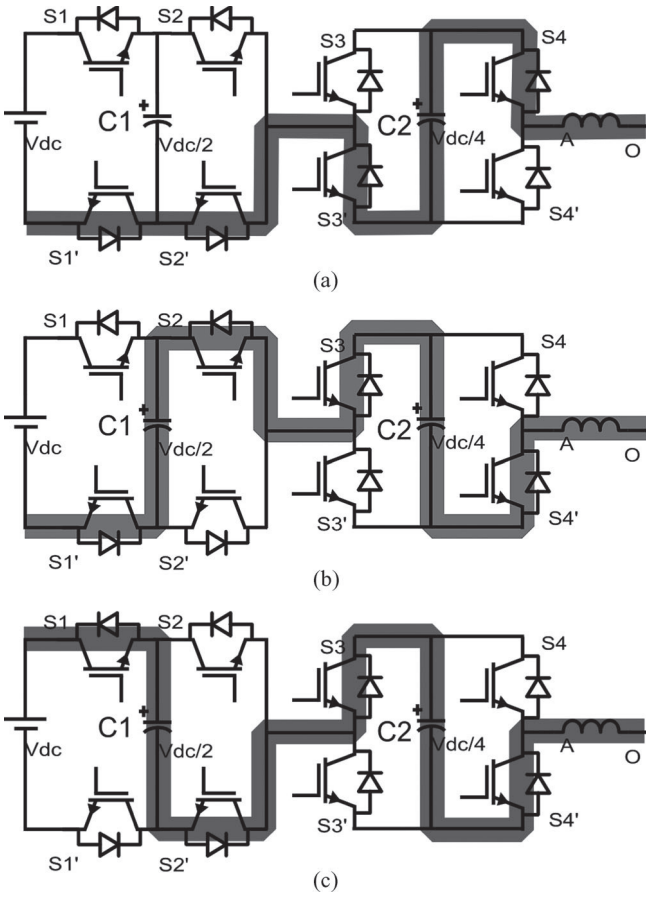

Fig. 2. Switch transitions and current path for the redundant states of $V_{\mathrm{DC}}/4$ for a phase. (a) Current path for switch state of (0,0,0,1), (b) Current path for switch state of (0,1,1,0). (c) Current path for switch state of (1,0,1,0).

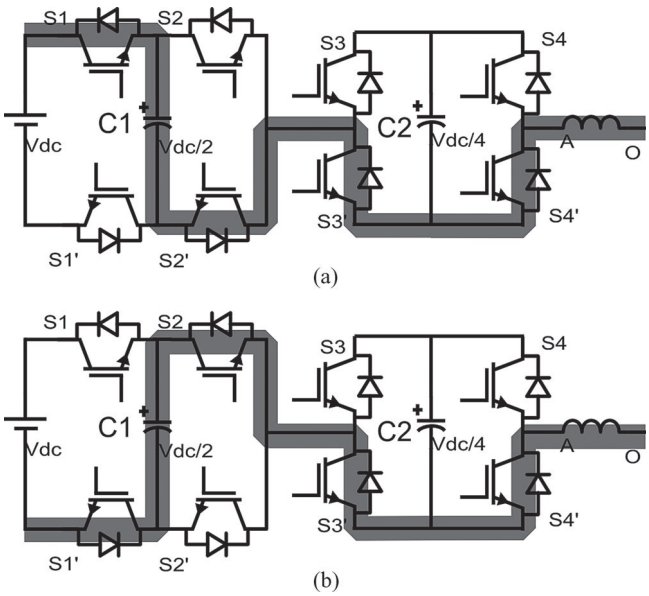

Fig. 3. Switch transitions and current path for the redundant states of $V_{\mathrm{DC}}/2$ for a phase. (a) Current path for switch state of (1,0,0,0). (b) Current path for switch state of (0,1,0,0).

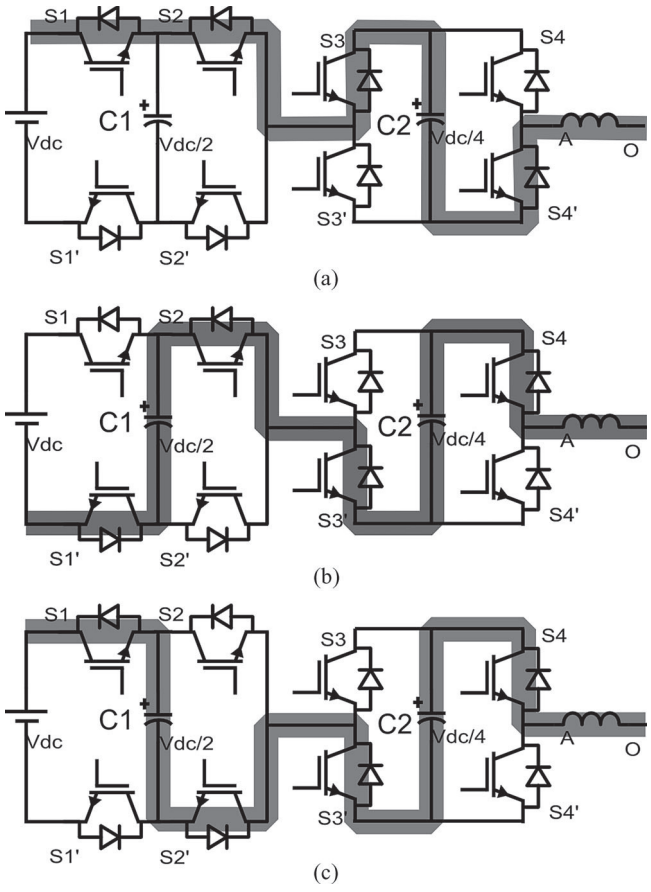

Fig. 4. Switch transitions and current path for the redundant states of $3V_{\mathrm{DC}}/4$ for a phase. (a) Current path for switch state of (1,1,1,0). (b) Current path for switch state of (0,1,0,1). (c) Current path for switch state of (1,0,0,1).

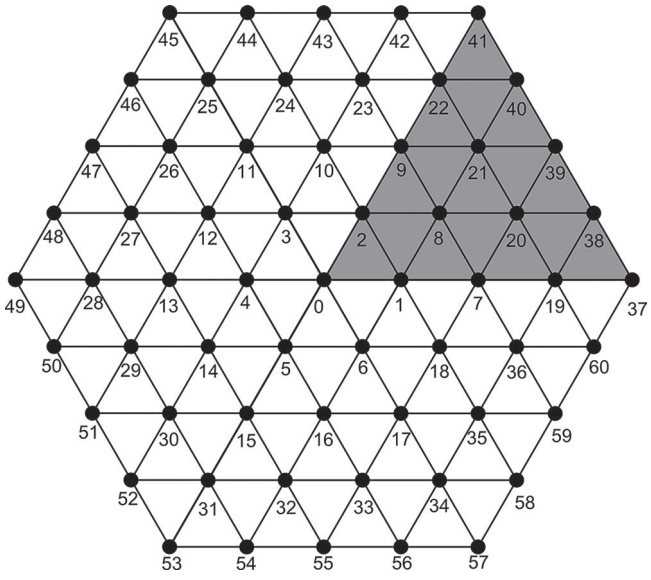

Fig. 5. Space Vector polygon formed with the proposed fi e-level inverter.

III. Salient Features

The proposed three-phase topology uses 12 switches of voltage rating $V_{\mathrm{DC}}/2$ and 12 switches of voltage rating $V_{\mathrm{DC}}/4$ (total 24 switches), where V_{DC} is the dc bus voltage. It has two capacitors per phase, one is rated at $V_{\mathrm{DC}}/2$ and the other is rated at $V_{\mathrm{DC}}/4$. So in total, the proposed three-phase configuratio requires only six capacitors, while the conventional fi e-level FC inverter requires nine capacitors. The asymmetrical FC configuratio shown in [15] requires 12 switches of rating $V_{\mathrm{DC}}/4$, six switches of rating $V_{\mathrm{DC}}/2$, three capacitors of rating $V_{\mathrm{DC}}/4$, and three capacitors of rating $V_{\mathrm{DC}}/2$ for a three-phase inverter. However, this configuratio has limited range of power factor for fi e-level operation. The conventional fi e-level CHB configu ration uses six isolated power supplies of voltage rating $V_{\mathrm{DC}}/4$ and 24 switches of voltage rating $V_{\mathrm{DC}}/4$. However, the proposed configuratio uses just one dc source of magnitude V_{DC}. The fi e-level NPC inverter requires four capacitors of rating $V_{\mathrm{DC}}/4$, 36 clamping diodes of voltage rating $V_{\mathrm{DC}}/4$ and 24 switches of rating $V_{\mathrm{DC}}/4$. However, the proposed topology does not require any clamping diode.

The f ve-level ANPC topology [27] requires three capacitors of voltage rating $V_{\mathrm{DC}}/4$ for three phases and two capacitors of voltage rating $V_{\mathrm{DC}}/2$. However, this configuratio has neutral point fluctuation The proposed configuratio does not have any such problem as it has FC front end. The hybrid clamped multilevel topology requires more number of switches and clamping diodes as compared to the proposed configuration A comparison of the proposed topology with the other fi e-level inverter topologies can be found in the Table III. Another important advantage of the proposed scheme is that if one of the devices in the H bridge fails, the H-bridge can be bypassed through a fast bypass switch or by routing the current through the devices in the complementary path and the inverter can work in three-level mode at the full power rating. For example, if S3 or S4 fails then the current can be routed through S3′ and S4′ by switching them ON and removing the gating signals to S3 and S4 or vice versa.

TABLE II
Voltages Formed as a Result of the Three Phases for 60° Interval

State No	Combinations of three phases[a]	Combinations
0	(0,0,0) (1,1,1) (2,2,2) (3,3,3) (4,4,4)	5
1	(1,0,0) (2,1,1) (3,2,2) (4,3,3)	4
2	(1,1,0) (2,2,1) (3,3,2) (4,4,3)	4
7	(2,0,0) (3,1,1) (4,2,2)	3
8	(2,1,0) (3,2,1) (4,3,2)	3
9	(2,2,0) (3,3,1) (4,4,2)	3
19	(3,0,0) (4,1,1)	2
20	(3,1,0) (4,2,1)	2
21	(3,2,0) (4,3,1)	2
22	(3,3,0) (4,4,1)	2
37	(4,0,0)	1
38	(4,1,0)	1
39	(4,2,0)	1
40	(4,3,0)	1
41	(4,4,0)	1

[a](a,b,c) where a,b,c values of 0,1,2,3, and 4 implies pole voltages of 0,$V_{\mathrm{DC}}/4$, $V_{\mathrm{DC}}/2$,3$V_{\mathrm{DC}}/4$, and V_{DC}, respectively.

TABLE III
COMPARISON BETWEEN NPC,FC,CHB, AND PROPOSED CONFIGURATION

Component	NPC[a]	FC[b]	CHB[c]	ANPC[d]	HCMLI[e]	PI[f]
Capacitor(V_{DC}/4)	4	3	0	3	13	3
Capacitor(V_{DC}/2)	0	3	0	2	0	3
Capacitor(3V_{DC}/4)	4	3	0	0	0	3
Switches(V_{DC}/4)	24	24	24	12	42	12
Switches(V_{DC}/2)	0	0	0	12	0	12
Clamping diodes(V_{DC}/4)	36	0	0	0	18	0
Power Supplies(V_{DC}/4)	0	0	6	0	0	0
Power Supplies(V_{DC}/2)	0	0	0	0	0	0
Power Supplies(V_{DC})	1	1	0	1	1	1

[a]NPC inverter.
[b]FC inverter.
[c]CHB inverter.
[d]Simplified active NPC inverter [27].
[e]Hybrid clamped multilevel inverter [33].
[f]Proposed inverter configuration.

IV. EXPERIMENTAL RESULTS

The proposed fi e-level inverter circuit has been tested on a 400 V, 3 kW, 50 Hz, Y-connected, induction motor drive with *V*/*f* control scheme at a switching frequency of 1 kHz. The hardware setup for the controller consists of a TMS320F2812 digital signal processing (DSP) platform and a Digilent SPARTAN-3 XC3S200 field-programmabl gate arrays (FPGA). The capacitor voltages of all the three phases are sampled at every switching cycle and compared with the reference values ($V_{\rm DC}$/2 for C1 and $V_{\rm DC}$/4 for C2). Level-shifted carrier-based space-vector pulse-width modulation algorithm given in [34] has been used to generate the PWM signals. The PWM output along with the carrier level data for all the three phases, hysteresis controller outputs for all the capacitors, and current direction data for all the three phases are sent out to the FPGA by the DSP. FPGA generates the gating signals to the inverter switches based on the inputs from the DSP. The logic for generating a dead time of 3 s has been implemented in FPGA itself. The inverter dc-link voltage is set to 200 V. The hysteresis limit for the capacitors is set at 5% of the respective capacitor voltage. The capacitors are sized suitably so that the voltage of the capacitors would not cross the hysteresis limits in two switching cycles at full load current.

The capacitance *C* is determined by

$$C = \frac{2(i_L T_S)}{\Delta V_C} \tag{2}$$

where ΔV_C is the capacitor voltage ripple, T_S is the sampling time, and i_L is the peak load current. The capacitor voltages are sampled every switching cycle (1 ms in this case). A capacitance value of 4400 μF has been used for C1 and C2 for all the three phases. The motor is run at various modulation indexes and frequencies at no load.

The motor is run at modulation indexes ($V_{\rm SV}$ /$V_{\rm DC}$) of 0.2, 0.4, 0.6, and 0.8 at frequencies of 10, 20, 30, and 40 Hz, respectively, at no load. The phase voltage waveform along with the phase current and the voltage ripple of the capacitors C1 and C2 for frequencies of 10, 20, 30, and 40 Hz are shown in Fig. 6(a)–(d), respectively. The pole voltage waveform along with the phase current at no load operation and the voltage ripple of capacitors C1 and C2 at frequencies of 10, 20, 30, and 40 Hz are shown in Fig. 7(a)–(d), respectively. The capacitor voltage ripple is less than 2.5 V for both C1 and C2. This validates the capacitor voltage balancing algorithm.

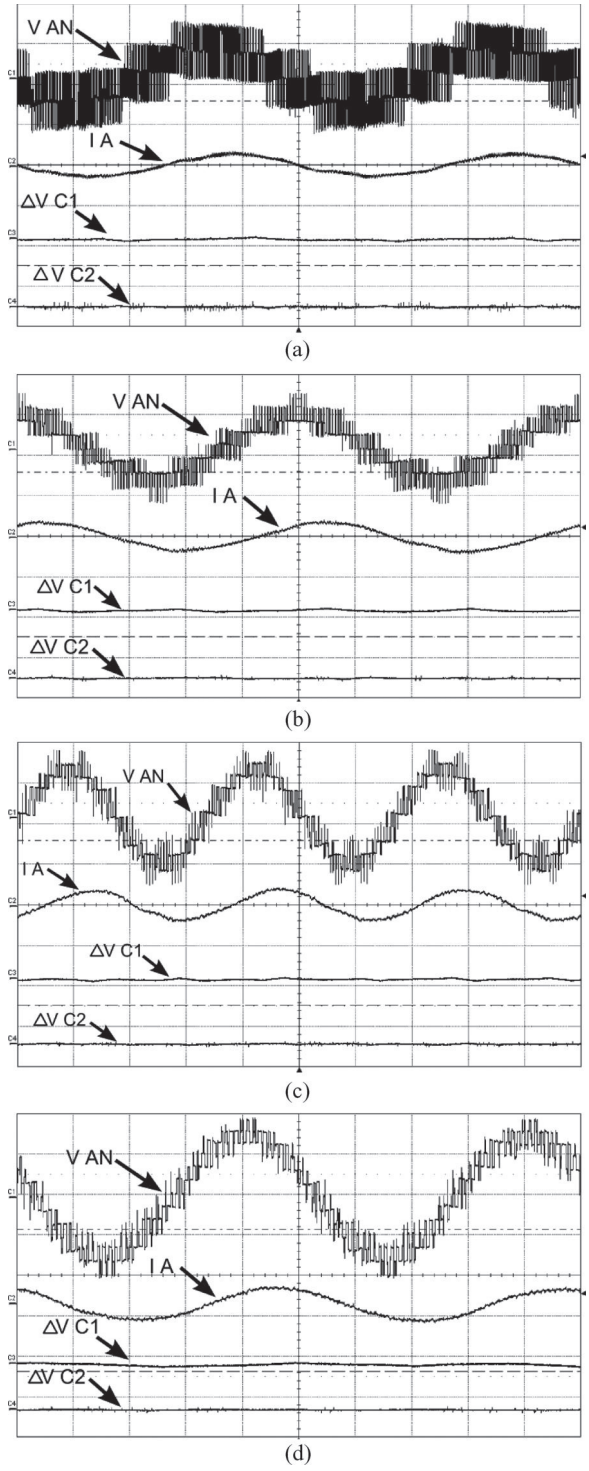

Fig. 6. Phase voltage $V_{\rm AN}$, phase current I_A and capacitor voltage ripple for different modulation indexes for phase A: $\Delta V_{\rm C1} = 5$ V/div; $\Delta V_{\rm C2} = 10$ V/div; $I_A = 2$ A/div. (a) 10 Hz with modulation index of 0.2 ($V_{\rm AN} = 50$ V/div, time = 20 ms/div). (b) 20 Hz with modulation index of 0.4 ($V_{\rm AN} = 100$ V/div, time = 10 ms/div). (c) 30 Hz with modulation index of 0.6 ($V_{\rm AN} = 100$ V/div, time = 10 ms/div). (d) 40 Hz with modulation index of 0.8 ($V_{\rm AN} = 100$ V/div, time = 5 ms/div).

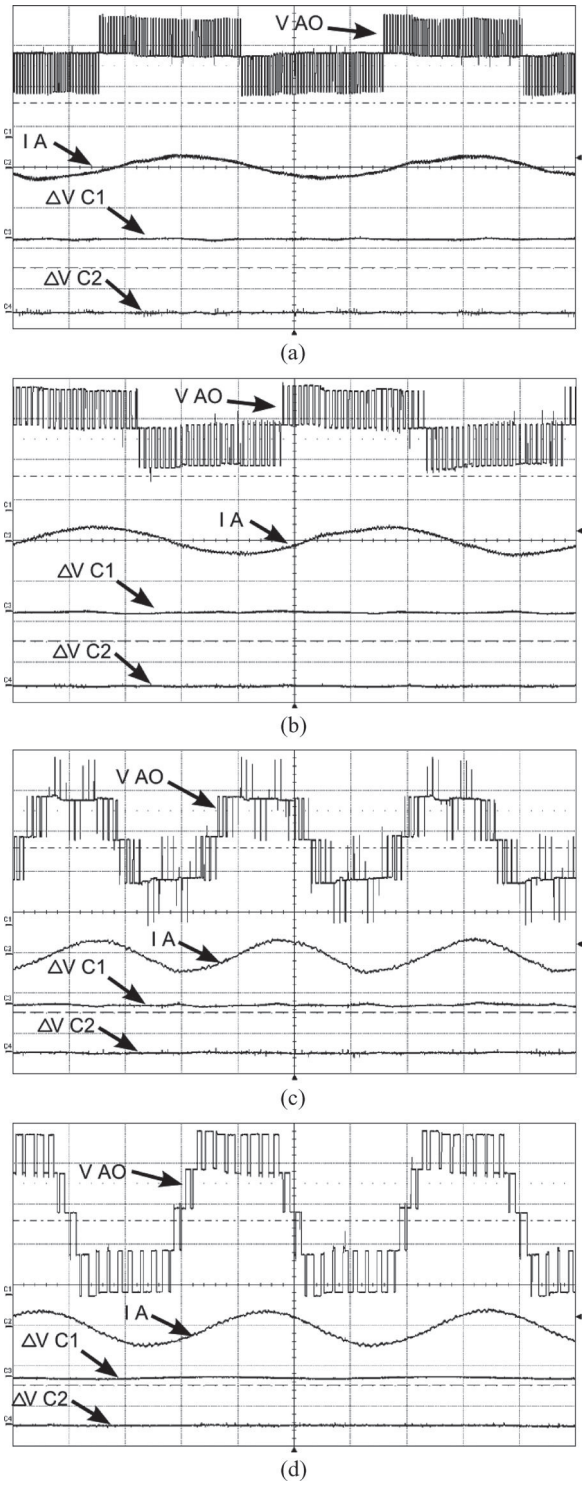

Fig. 7. Pole voltage V_{AO}, phase current I_A and capacitor voltage ripple for different modulation indexes for phase A: $\Delta V_{\mathrm{C1}} = 5$ V/div; $\Delta V_{\mathrm{C2}} = 10$ V/div; $I_A = 2$ A/div. (a) 10 Hz with modulation index of 0.2 ($\mathrm{V_{AO}} = 50$ V/div, time = 20 ms/div). (b) 20 Hz with modulation index of 0.4 ($V_{\mathrm{AO}} = 100$ V/div, time = 10 ms/div). (c) 30 Hz with modulation index of 0.6 ($V_{\mathrm{AO}} = 100$ V/div, and time = 10 ms/div). (d) 40 Hz with modulation index of 0.8 ($V_{\mathrm{AO}} = 100$ V/div, time = 5 ms/div).

The motor is accelerated from 10–40 Hz in 5 s at no load. The phase voltage, phase current, and the capacitor voltages are shown in Fig. 8. It can be observed that the dc voltages of the

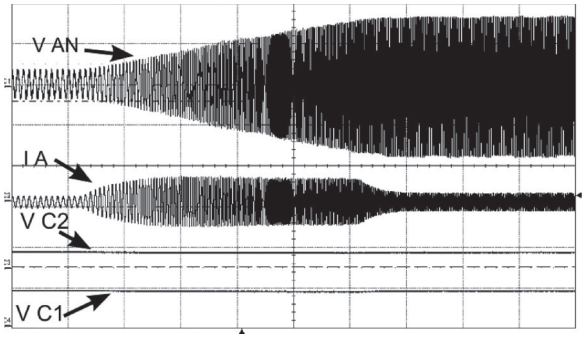

Fig. 8. Rapid acceleration of motor from 10 to 40 Hz in 5.5 s. Capacitor voltage remains constant. V_{AN} (phase voltage): 200 V/div, I_A (phase current): 2 A/div, V_{C1} (V_{DC}/2 capacitor DC voltage): 100 V/div, V_{C2} (V_{DC}/4 capacitor DC voltage): 100 V/div, and time scale: 1 s/div.

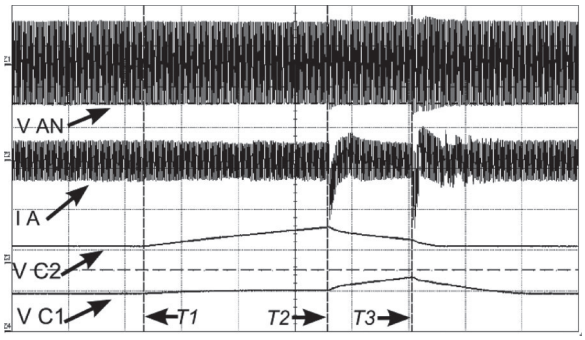

Fig. 9. Capacitor balancing operation. The balancing logic has been disabled at T1. C1 balancing has been enabled at T2 and C2 balancing has been enabled at T3. V_{AN} (phase voltage): 200 V/div, I_A (phase current): 2 A/div, V_{C1} (V_{DC}/2 capacitor DC voltage): 100 V/div, V_{C2} (V_{DC}/4 capacitor DC voltage): 100 V/div, and time scale: 2 s/div.

capacitors remain balanced even during sudden acceleration. In Fig. 9, the effect of disabling the capacitor voltage balancing algorithm is shown. The capacitor voltage balancing algorithm has been disabled at T1 and enabled for C1 at T2 and C3 at T3. It can be observed that the capacitor voltages are restored to preset values once the capacitor voltage balancing algorithm has been enabled. These experimental results verify the performance of the proposed fi e-level inverter topology.

V. Conclusion

In this paper, a new three-phase f ve-level inverter topology with a single-dc source has been proposed. This configuratio is formed by cascading a three-level FC inverter and capacitor-fed H-bridges. The key advantages of this topology compared to the conventional topologies include reduced number of devices and simple control. An important feature of this inverter is the ability to balance the capacitor voltages irrespective of load power factor. Another advantage of this inverter is that if one of the H-bridge fails, it can operate as a three-level inverter at full power rating by bypassing the H-bridge. This feature of the inverter improves the reliability of the system.

The proposed configuratio has been analyzed and experimentally verifie for various modulation indexes and frequencies by running a 3-kW squirrel cage induction motor in *V/f*

control mode, at no load. The working of the capacitor balancing algorithm has been tested. The stable operation of the inverter for various modulation indexes and stability of the inverter voltage levels during rapid acceleration have been validated experimentally.

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