ELectronics EXpress

IEICE Electronics Express, Vol.1, No.12, 339–345

Biasing CMOS amplifiers using MOS transistors in subthreshold region

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Abstract: The implementation of large-valued floating resistive elements using MOS transistors in subthreshold region is addressed. The application of these elements to bias wideband AC coupled amplifiers is discussed. Simple schemes to generate the gate control voltages for the MOS transistors implementing large resistors so that they remain in high resistive state with large signal variations are discussed. Experimental results of a test chip prototype in 0.5-μm CMOS technology are presented that verify the proposed technique.

Keywords: analog CMOS integrated circuits, wideband amplifiers, AC coupled amplifiers

Classification: Integrated Circuits

References

[1] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw Hill, Boston 2001, Chapter 12.

[2] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, and F. Munoz, "Very Low Voltage Analog Signal Processing Based on Quasi-Floating Gate Transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 434–442, March 2004.

[3] F. Krummenacher, "Micropower Switched Capacitor Biquadratic Cell," *IEEE J. Solid-State Circuits*, vol. 17, no. 3, pp. 507–512, March 1982.

[4] R. G. Benson and D. Kerns, "UV-Activated Conductances Allow for Multiple Scale Learning," *IEEE Trans. Neural Networks*, vol. 4, no. 3, pp. 434–440, May 1993.

[5] M. Hovin, D. Wisland, Y. Berg, and T. S. Lande, "A Low-Voltage Sinc2 Decimator Implemented by A New Circuit Technique Using Floating-Gate Transistors," *Proc. of the 2002 IEEE International Symposium on Circuits and Systems*, Phoenix, AZ, USA, Paper ID: 0-7803-7448-7/02, pp. V-397–V-400, May 2002.

[6] Carver Mead, *Analog VLSI and neural systems*, Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA, 1989.

DOI: 10.1587/elex.1.339
Received July 27, 2004
Accepted August 09, 2004
Published September 25, 2004

[7] R. R. Harrison and C. Charles, "A Low Power Low Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, June 2003.
[8] R. H. Olsson III, M. N. Gulari, and K. D. Wise, "Silicon Neural Recording Arrays with on-Chip Electronics for *In-Vivo* Data Acquisition," 2nd Annual International *IEEE-EMBS Special Topic Conference on Microtechnologies in Medicine and Biology*, Madison, Wi, pp. 237–240, May 2–4 2002.
[9] P. Mohseni and K. Najafi, "A Fully Integrated Neural Recording Amplifier with DC Input Stabilization," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 5, pp. 832–837, May 2004.

1 Introduction

CMOS inverters can be used as compact high-gain amplifiers and comparators in many applications like in flash A-to-D converters and as output stages of class AB operational amplifiers. This is commonly done using dynamic biasing techniques where MOS switches periodically connect the input and output terminals of the CMOS inverter to develop a biasing voltage V_{bias} during the sampling (connection) phase. The voltage V_{bias} biases the inverter in its linear (high gain) region and it is stored in the input parasitic capacitance C_{in} during the evaluation (disconnection) phase where the CMOS inverter is used as a high-gain amplifier. Some of the problems associated to dynamic biasing include: clock injection, clock feed through, change of V_{bias} due to switch leakage and most importantly, severe limitation of the effective amplifier's bandwidth [1]. This is due to the fact that the maximum frequency of the input signal is typically limited to a factor 20 to 50 below the clock frequency f_{clk}. The maximum frequency f_{clk} is determined (among other factors) by the inverter's settling time. In this Letter we describe a simple method to bias the inverter and other amplifier structures in continuous-time in order to overcome limitations associated to switching in dynamic biasing schemes. This method is based on very large valued floating resistive elements implemented with MOS transistors operating in subthreshold region.

2 AC coupled wideband CMOS amplifiers

Large-valued floating resistive elements are denoted R_{large} in what follows. They allow continuous-time operation of CMOS inverters as wideband high gain AC coupled amplifiers. Two CMOS inverter biasing schemes using large-valued floating resistors R_{large} are shown in Figs. 1 a and 1 b. In Fig. 1 a R_{large} is connected between the input and output terminals of the CMOS inverter formed by transistors M1–M2. In Fig. 1 b a biasing voltage V_{bias} is generated using a reference inverter with diode-connected transistors M1B, M2B that have the same dimension as M1, M2. In this case the biasing voltage V_{bias} is transferred to the amplifier's input terminal X through R_{large}. In both cases the input signal is coupled capacitively through capacitor C. Biasing resistors require to have very large values due to the following reasons: a) The input

DOI: 10.1587/elex.1.339
Received July 27, 2004
Accepted August 09, 2004
Published September 25, 2004

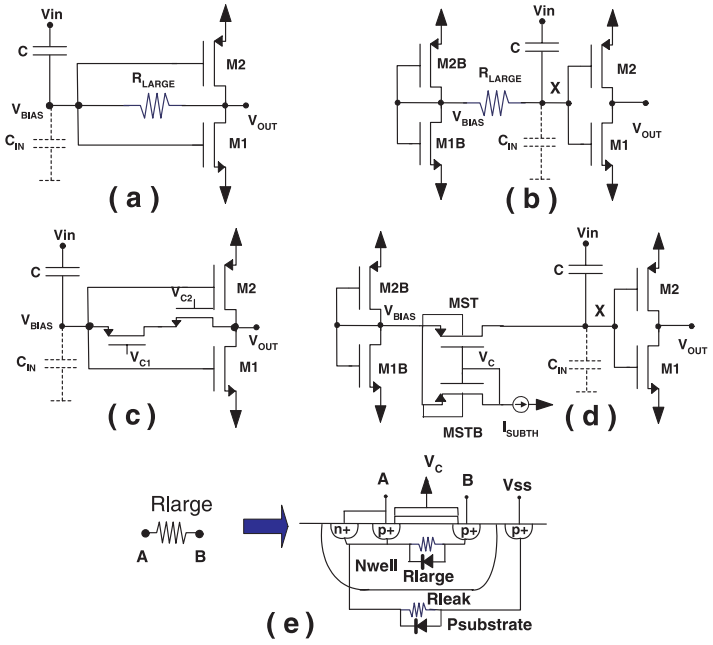

Fig. 1. Biasing CMOS inverters using large resistive elements (a) Using feedback resistor (b) Using reference CMOS inverter (c) R_{large} implementation with NMOS and PMOS transistors in subthreshold region (d) R_{large} implementation with PMOS transistor (e) Cross sectional view of PMOS transistor and associated PN junctions

resistance in Fig. 1 a is given approximately by the Miller reflected resistance $R_{in} = R_{large}/A_v$ and by $R_{in} \approx R_{large}$ in Fig. 1 b (A_v is the voltage gain of the CMOS inverter). In order to prevent gain and input impedance degradation of the CMOS amplifier R_{large} should have very large values, b) the AC coupling capacitor C and the input resistance R_{in} form a high pass circuit with a corner frequency $f_{3dBLOW} = 1/(2\pi R_{large}C)$. This frequency defines the lower 3 dB frequency of the wideband amplifier. For typical values of integrated capacitors C (in the pF range), R_{large} should have extremely large values ($R_{large} > 1\,G\Omega$). This is required in order to set the lower 3 dB frequency of the amplifier as low as possible (e.g. $f_{3dBLOW} < 100\,Hz$). Due to the relatively low sheet resistances of layers available integrated resistors R_{large} with such large values would have very large area and parasitic capacitances that would limit seriously the bandwidth of the amplifier.

3 Implementation of large-valued floating resistive elements

Efficient implementation of large-valued resistors with one of their terminals connected to a power rail using reverse-biased PN junctions has been reported (for example in the quasi-floating gate technique presented in [2]). Floating PN junctions available within a transistor's well have been also proposed for this purpose [3]. This is illustrated in Fig. 1 e that implements R_{large} with the reverse-biased drain-well junction of a PMOS transistor in cutoff with $V_C = V_{DD}$. The main problem is that these junctions have relatively limited

DOI: 10.1587/elex.1.339
Received July 27, 2004
Accepted August 09, 2004
Published September 25, 2004

swing ($V_{swing} < 0.3\,V$), this in order to prevent them from becoming forward biased and reducing their resistance. Another problem is that there are other reverse biased junctions like the nwell to p-substrate junction (R_{leak} in Fig. 1 e). This junction is connected to a power rail (V_{SS} in Fig. 1 e) and its resistance R_{leak} forms a voltage divider with the floating junction implementing R_{large}. This divider leads to errors and drift in the input DC operating point of the amplifier which causes the voltage at node X to differ from the value V_{bias}. Another problem is that if the junction implementing R_{large} becomes forward biased a PNP substrate bipolar transistor is activated. Ultraviolet (UV) activated conductances [4, 5] in conjunction with floating-gate transistors can also be used to implement large-valued floating resistive elements. These elements can be implemented with MOS transistors in cutoff. During the programming phase they are activated into (very slight) conduction from gate to source/drain using UV light exposure and with the circuit powered on. This generates amplifier biasing voltages that remain stored at the input of a CMOS inverter (or other amplifier structure) with floating gate transistors. The main disadvantage of this approach is that the biasing voltages are fixed and can not adjust to subsequent temperature or supply voltage variations. During normal operation these variations can bring the amplifier to leave the linear region. Large-valued floating resistors implemented using MOS transistors in subthreshold region have been used in diffusive networks [6] and in wideband AC coupled amplifiers with op-amps [7, 8] similar to the circuits shown in Fig. 3 c and 3 d (to be discussed later). In [7], R_{large} was implemented using the series combination of two PMOS diode-connected transistors which under quiescent conditions (with $V_{out} = V_{in}$) operate in subthreshold region. Both implementations are characterized by relatively limited swing since large voltage variations ($V_{swing} > 2V_{TH}$ in [7] and $V_{swing} > V_{TH}$ in [6, 8]) drive transistors into saturated mode and/or turn on their associated reverse-biased junctions reducing dramatically their resistance. [9] addresses the utilization of transistors in subthreshold region to clamp the input of a noninverting amplifier to ground and to implement a high pass circuit with a very low 3 dB corner frequency.

Next we address two simple schemes for implementation of large-valued floating resistive elements using MOS transistors in subthreshold region:

3.1 Large swing implementation

The first proposed implementation for R_{large} is shown in Fig. 1 c. It consists of the series combination of a minimum-size PMOS and an NMOS transistor. In this scheme the effective resistance of the series combination always remains very large in spite of large variations in the output voltage V_{out}. This is due to the fact that variations either in the positive or negative direction tend to turn on one transistor but at the same time they turn off the other transistor, so that under dynamic conditions the effective resistance of the series combination remains very large. Under quiescent conditions with $V_{out} = V_{Bias}$ the control voltages V_{cn} and V_{cp} keep MRN and MRP in subthreshold region with a very large effective resistance.

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Received July 27, 2004
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3.2 Limited swing implementation

In the second case a minimum-sized PMOS transistor MST is biased by means of a control voltage V_C generated by a diode-connected transistors MSTB. This transistor is fed by a very small bias current I_{subt} that keeps both MST and MSTB in weak inversion as shown in Fig. 1 d. In this case and in order to keep MST in subthreshold region the signal variations across R_{large} must be limited to maintain the voltage across R_{large} to values below V_{THP}. This is not a problem in the structure of Fig. 1 b (and in other similar structures) since R_{large} is not subject to large signal variations given that it is connected to the input node X of the amplifier where relatively small signal variations are available.

In both schemes PMOS transistors in subthreshold region are implemented with minimum-size transistors as shown in Fig. 1 e but with the gate of the MOS transistor connected to a control voltage V_C (or V_{CP}) that bias the transistors in subthreshold rather than connecting the gate to V_{DD} In this case R_{large} is the subthreshold resistance of the MOS transistor which is at least on the order of GΩ but much lower than the leak resistance of both junctions.

4 Experimental and simulation results

Both schemes of Figs. 1 c and 1 d have been experimentally verified. The circuit of Fig. 1 d was fabricated in 0.5-μm CMOS (AMI-MOSIS) technology using transistors M1, M1B and M2, M2B with sizes 90/1.8 and 30/1.8 (in μm). Transistor MST had dimensions 0.9/0.6. Values C = 0.5 pF, V_{DD} = 2 V and a control voltage Vc = 0.55 V were used for measurements. Experimental values for the voltage gain were Av = −8.85V/V, the lower and upper 3 dB frequencies f_{3dBlow} = 10 Hz and $f_{3dBhigh}$ = 100 kHz, respectively. These values show good agreement with simulations using an off chip load capacitance C_L = 50 pF. The measured value for V_{bias} was 0.95 V and remained stable over several hours. The gain was close to the theoretical value for an AC coupled amplifier. This is given approximately by the ratio Av = $-C_F/C$. In this case $C_F = C_{GDM1} + C_{GDM2} \approx 0.04$ pF for the selected transistor sizes.

The circuit of Fig. 1 c was breadboarded using integrated PMOS and

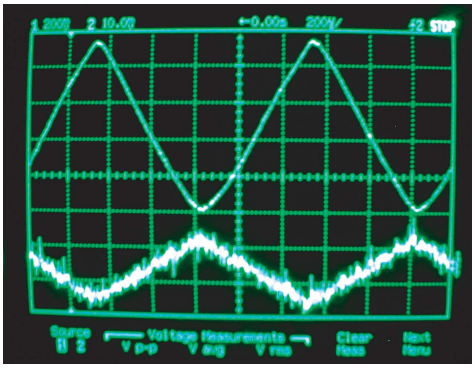

Fig. 2. Measured output (upper waveform) for a 1 kHz triangular input (lower waveform).

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NMOS arrays ALD1106 and ALD1107 from Advanced Linear Devices. These transistors have nominal threshold voltages $V_{TH} = 0.75\,V$ and approximately equal gain factors $\beta = 1.3\,mA/V^2$. A supply voltage $V_{DD} = 1.8\,V$ and control voltages $V_{CP} = 1.5\,V$ and $V_{CN} = 0.2\,V$ were used for measurements with $C = 100\,pF$. Values $V_{bias} = 0.9\,V$ and $f_{3dBHIGH} = 60\,KHz$ and voltage gain $A_v = -46V/V$ were measured. Figure 2 shows the measured input and output waveforms. Simulations with a typical on-chip load capacitance $C_L = 0.5\,pF$, W/L = 25/0.6 and 10/0.6 for M1, M2 M1B and M2B and W/L = 2/0.6 for transistors implementation R_{large} lead to a voltage gain Av = −40V/V with $f_{3dBlow} = 10\,Hz$ and a bandwidth BW = 128 MHz. This corresponds approximately to a gain bandwidth product GBW = 5 GHz.

5 Low-voltage and op-amp based architectures

Currently technology and power dissipation constraints require topologies that can operate with sub-volt supplies $V_{DD} < 1\,V$. The minimum supply requirements of the circuits of Fig. 1 correspond to two gate-source drops $V_{DD}{}^{MIN} = V_{GSN} + V_{SGP}$. Figures 3 a and 3 b show the schemes of a class A and class AB inverters with lower supply requirements $V_{DD}{}^{MIN} = V_{GSN} + V_{DSsat}$ where V_{DSsat} is the drain source saturation voltage. These circuits can operate with sub-volt supplies in 0.18-μm CMOS technology with typical threshold voltages $V_{TH} \approx 0.45\,V$ and $V_{DSsat} \approx 0.2\,V$. Many other AC coupled circuits can be derived from the basic schemes discussed here. As example Figs. 3 c and 3 d show inverting and summing amplifiers using op-amps biased with large valued resistive elements.

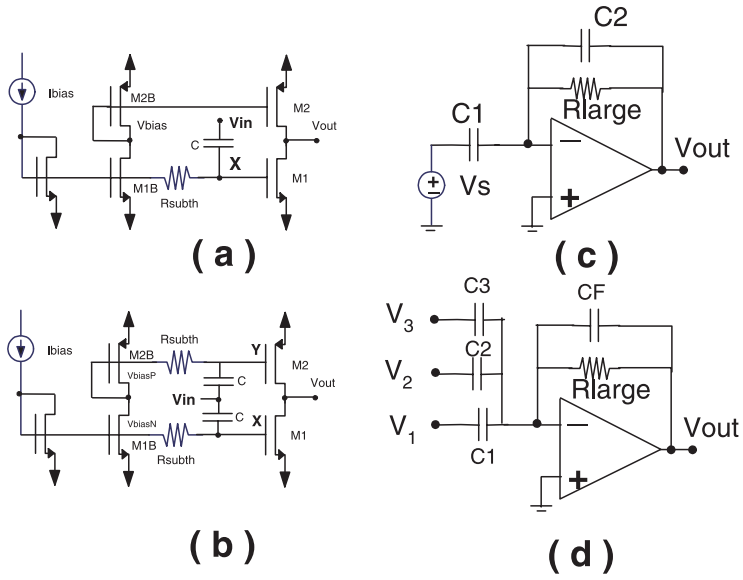

Fig. 3. Applications of R_{large} to bias AC coupled wideband amplifiers (a) Low-voltage class A CMOS inverter amplifier (b) Low voltage class AB CMOS inverter amplifier (c) Inverting op-amp amplifier (d) Summing op-amp amplifier.

DOI: 10.1587/elex.1.339
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Accepted August 09, 2004
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6 Conclusion

The practical implementation of very large-valued floating resistive elements with MOS transistors in subthreshold region has been discussed and demonstrated experimentally Applications for biasing CMOS inverters for their utilization as AC coupled wideband amplifiers were discussed. Other possible applications include low-voltage circuits, biasing of op-amp circuits, linear, nonlinear and auto-zeroing circuits.

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