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Low-voltage wide gm adjustable range highly linear BiCMOS OTA

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Abstract: A low distortion low-voltage BiCMOS OTA with wide g_m adjustment range and constant input range is presented. It is based on a highly linear voltage-to-current converter input stage merged with translinear loops that implement linear electronically programmable current mirrors. Experimental results are provided that confirm the characteristics of the proposed OTA with a single 1.7 V supply, 1.2 V input range, two decades gain adjustment range, and 0.3% THD.

Keywords: analog CMOS integrated circuits, programmable current mirrors, Operational Transconductance Amplifiers (OTA)

Classification: Integrated circuits

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1 Introduction

Due to its versatility, the Operational Transconductance Amplifier (OTA) is a very important building block of analog VLSI circuits. It is used to implement continuous-time linear and nonlinear VLSI circuits with electronically programmable characteristics [1, 2]. Some key features for many OTA applications are: 1) a wide range of transconductance gain adjustment, 2) a highly linear transconductance characteristic, and 3) constant input range independent of gain adjustment.

Traditionally, OTA linearization has taken place in the input Differential Pair (DP) so that either a linear difference $I_A - I_B$ (I_A and I_B being the DP transistor currents) or both linear I_A and I_B are generated. The difference $I_A - I_B$ is delivered as the OTA output current using a current mirror differencing network. In this approach, adjustment of the transconductance gain takes place usually by adjustment of the DP gain (g_{md}). Drawbacks of this approach, where both linearization and g_m control take place on the DP are: 1) most of the OTA performance characteristics (input range, BW, noise, offset, distortion) change significantly with adjustment of g_{md}, 2) in CMOS structures the gain adjustment range is very limited (practically to only 2 octaves), and 3) most of the proposed approaches are not appropriate for operation with low supply voltages. Bipolar differential pairs allow g_m to be adjusted over a very wide range of values (several decades) but their input range is very small (a few mV). The use of emitter (or source) degeneration to achieve linear transconductance gain and to increase the DP input range leads to fixed (non programmable) transconductance gain $g_{md} = 2g_m/(2 + g_mR)$ where R is the source degeneration resistor and g_m the transconductance gain of the DP transistors. Gain programmability can be achieved by replacing the gain degeneration resistor R by MOS transistors operating in ohmic mode [3]. This leads to very limited gain adjustment range imposed by the condition to keep MOS transistors in ohmic mode of operation. In this scheme the input range is also very limited and changes with gain adjustment. The condition to achieve high linearity in resistive degenerated DPs is $R \gg 2/g_m$. Current variations over the input range cause g_m to decrease leading to large distortion for small currents in the DP. In MOS DPs large drain current changes yield non equal gate-source voltage changes that introduce additional distortion. Other approaches for wide gain adjustment have been based on a fixed gain linear V to I conversion bipolar input stage followed by current scaling using gain programmable current mirrors [4].

In this Letter we report a low-voltage, highly linear OTA that uses a BiCMOS input stage in combination with gain programmable current mirrors to provide the OTA with very wide range gain programmability and constant

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input range. The input stage is merged with the translinear loop serving as wide range linear gain programmable mirrors. Besides gain programmability the proposed circuit has high input impedance, low supply requirements and wide and independently adjustable input range. This remains approximately constant with gain adjustment.

2 Wide g_m adjustable range BiCMOS OTA architecture

Input stage: Figure 1 shows the scheme of the proposed OTA. The linear voltage to current conversion input stage uses two BiCMOS gain enhanced voltage followers (or buffers) and a resistor R. The input buffers are formed by M_1, Q_2 & Q_3 and M_{1P}, Q_{2P} & Q_{3P}. Negative feedback leads to a very low impedance at the source of the input transistors M_1 and M_{1P}: $R_x = 1/(g_{m1}g_{m2}r_o)$ on the order of a few Ohms. These buffers are a modified version of a circuit that some of the authors have denoted "super voltage follower" or "flipped voltage follower" [5] which has low supply requirements. A bipolar version of this circuit was reported in [6]. The supply requirements of the input buffers of the circuit of Fig. 1 are given by $V_{DD}^{MIN} = 2V_{BE} + V_{DSsat}$ (V_{BE} is a base-emitter voltage drop; V_{DSsat} is the MOS drain-source saturation voltage). V_{DD}^{MIN} can be as low as 1.5 V. The buffers are used to transfer the differential input voltage $V_d = (V_{i+}) - (V_{i-})$ to the terminals of R. This generates a signal current $I_{in} = V_d/R$. The voltage to current transformation is highly linear given that V_d is transferred with very low distortion to R. This is due to the fact that the current and the gate-source drop in M_1, M_{1P} is constant and the impedance R_x at the sources of M_1, M_{1P} is very low as indicated above.

Current Gain Stage: Transistors $Q_2 - Q_5$ and $Q_{2P} - Q_{5P}$ form translinear loops. They implement linear programmable current mirrors with current gain $A = I_{dir}/I_{inv}$. This gain has two degrees of freedom for adjustment: the DC bias currents I_{dir} and I_{inv}. Straightforward analysis using the translinear

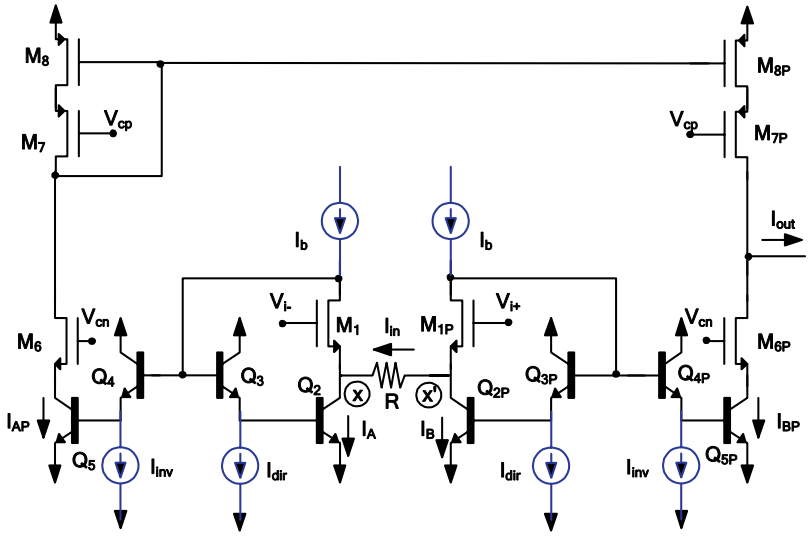

Fig. 1. Wide g_m adjustable BiCMOS OTA.

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principle [7] shows that currents I_{AP} and I_{BP} in Fig. 1 can be expressed by $I_{AP} = I_A(I_{dir}/I_{inv})$ and $I_{BP} = I_B(I_{dir}/I_{inv})$ respectively (currents I_A and I_B are given by: $I_A = I_b + I_{in}$ and $I_B = I_b - I_{in}$ with $I_{in} = V_d/R$). Transistors $M_7 - M_8$ (and $M_{7P} - M_{8P}$) form a conventional MOS current mirror which generates an output current $I_{out} = I_{AP} - I_{BP} = A(I_A - I_B) = 2I_{in}(I_{dir}/I_{inv})$. This can be expressed by

$$I_{out} = G_m V_d$$

where $G_m = 2(I_{dir}/I_{inv})/R$.

3 Characteristics of the proposed OTA

1). Currents I_A and I_B are linear and complementary. This is as opposed to most CMOS linearization schemes where individual currents in the input stage have large nonlinear and signal dependent common mode components which need to be cancelled and are for this reason current inefficient.

2). The transconductance gain $G_m = 2(I_{dir}/I_{inv})/R$ has linear and reciprocal control in terms of the bias currents I_{dir} and I_{inv}. It has very wide range programmability and it is approximately temperature independent (this assumes that R has a low temperature coefficient).

3). The input range of the circuit of Fig. 1 is $V_d^{MAX} = min\{I_bR,\ 2V_{BE} - V_{DSsat} - V_{CEsat}\}$ where V_{DSsat} and V_{CEsat} are the drain source and collector emitter saturation voltages of M_1 and Q_{2P} respectively, and *min* denotes the minimum operator. This range remains constant with gain adjustment. It can be adjusted independent of the gain via I_b.

4). Given that there are two degrees of freedom (I_{dir} and I_{inv}) for adjustment of the transconductance gain, the proposed OTA has additional flexibility and versatility for many applications.

5). A folded version of the circuit of Fig. 1 with PMOS transistors at the input stage allows the interconnection of source and substrate terminals in order to avoid the body effect.

4 Experimental results

The circuit of Fig. 1 has been verified experimentally using commercial MOS transistor arrays ALD1106/1107 and bipolar transistor arrays CA3046 on a breadboard. Figure 2 shows the experimental DC transconductance characteristics with $I_b = 30\,\mu A$, $R = 33\,k\Omega$, $R_L = 9\,k\Omega$, $V_{DD} = 1.7\,V$, $I_{inv} = 100\,\mu A$ and I_{dir} stepped from $1\,\mu A$ to $106\,\mu A$ in $15\,\mu A$ steps. Complementary input voltage signals (V_{i+} and V_{i-}) with a 1.4 V common mode voltage were applied. It can be seen that the input range is close to 1.2 V and the gain remains linear over a very wide adjustment range (in practice gain can be adjusted experimentally over two decades). Measured Total Harmonic Distortion (THD) for a 100 kHz input signal is shown in Fig. 3. Simulated THD

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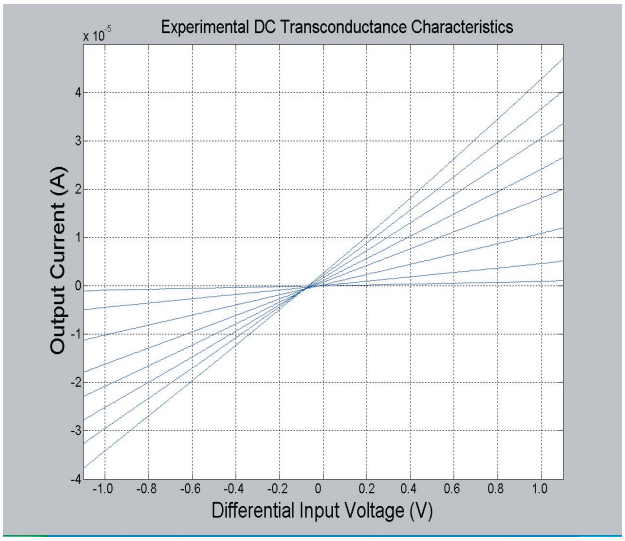

Fig. 2. Measured DC transconductance characteristics for different gain settings.

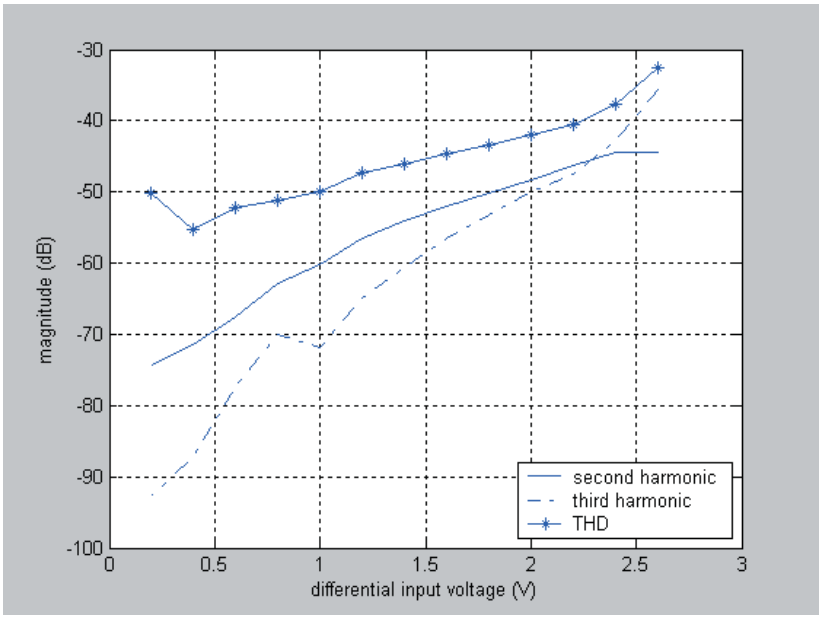

Fig. 3. Measured distortion vs. input voltage *Vertical axis*: distortion *Horizontal axis*: peak-to-peak differential input voltage.

using the same test conditions and using 0.5 μm CMOS SPICE models with W/L = 50/1.2 μm was under 0.03%. The higher experimental THD values shown in Fig. 3 are attributed to the discrete implementation. The experimental transconductance gain adjustment range was 2 decades. Simulated bandwidth was 30 MHz. Experimental high frequency characterization was not possible due to large parasitic capacitances associated to the discrete implementation.

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5 Conclusion

A highly linear OTA structure with very wide g_m adjustment, wide input range and both linear and reciprocal linear g_m control was introduced and experimentally verified. It is based on gain programmable current mirrors which are linear and continuously adjustable. The proposed circuit is believed to overcome some of the practical limitations of other reported low voltage linear OTA structures and to provide increased versatility to the OTA as a building block for analog VLSI systems.

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