Operation Limits for RTD-based MOBILE Circuits

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***Abstract*—RTD-based MOBILE circuits operate properly in a certain frequency range. They exhibit both a minimum operating frequency and a maximum one. From a design point of view, it should be desirable to have gates with a correct operation from DC up to the maximum operating frequency (*i.e.*, without the minimum bound). This paper undertakes this problem by analysing how transistors and RTDs interact in RTD-based circuits. Two malfunctions have been identified: the incorrect evaluation of inputs, and the lack of self-latching operation. The difficulty to study these problems in an analytical way has been overcome by resorting to series expansions for both the RTD and the HFET *I-V* characteristics in the points of interest. We have obtained analytical expression linking representative device parameters and technological setup, for a MOBILE-based circuit to operate correctly.**

***Index Terms*— Resonant Tunnelling Diodes (RTDs), MOBILE circuits, Linear Threshold Gates, Nanoelectronics.**

I. Introduction

RESONANT tunnelling diodes (RTDs) are very fast non linear circuit elements which have been integrated with transistors to create novel quantum devices and circuits. This incorporation of tunnel diodes into transistor technologies has shown improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption [1], [2], [3], [4], [5]. Thus, RTD based circuits have been receiving a great amount of interest in the last years. Most of the reported working circuits have been made in III/V materials while Si-based tunnelling diodes compatible to standard CMOS fabs are currently an area of active research [6]. In fact, it has been claimed that augmenting CMOS with RTDs could be the way to extend the lifetime of CMOS and fully exploit its huge economical investments [7]. Recent advances in the development of those Si-based RTDs have risen a renewed interest on circuit design using RTDs and transistors.

Efficient RTD complex logic gates are designed on the basis of the MOnostable-BIstable Logic Element (MOBILE) [8], [9], [10], [11], [12], [13]. The MOBILE is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage. The addition of transistors in parallel to the RTDs allows implementing logic functionality. These MOBILE gates exhibit self-latching and can be cascaded and operated in a pipelined fashion.

Several works have been dedicated to the performance modelling of MOBILE gates. In particular, basic aspects of their DC operation have been studied [14]. Their maximum operating speed has been investigated through circuit simulations [15], [16], and, in some cases, following an analytical approach, [17], [18]. In addition, their self-latching capabilities have been also studied [19]. In one of these works [16], it is shown that these gates operate properly in a certain frequency range. That is, they exhibit both a minimum operating frequency and a maximum one. The frequency range depends on the gate fan-out. From the design point of view it should be desirable to have gates without the minimum limit (correct operation from DC up to a maximum frequency). Through extensive simulations, a relationship between RTD areas and transistor size that must be satisfied for a given MOBILE gate, in a specific technology, to operate properly at very low frequencies, is derived in the above referenced work. However, this design constraint has not been analytically studied, which will allow technology independence and reuse. In addition, the obtained constraint does not guarantee the self-latching behaviour of the gate. It should be interesting to have expressions for design constraints which guarantee both the lack of a minimum operating frequency and the self latching capability (DC correct behaviour) as functions of technological parameters. For this purpose, we have carried out an in-depth analysis of the DC operation of MOBILE circuits.

We have selected two basic MOBILE circuits, a follower and an inverter, and we show that a correct DC behaviour is not inherent to the practical circuit topologies employed to implement RTD-based MOBILE circuits. We have analyzed their operation limits and derived analytical models of required relationships among design parameters (RTDs‘and transistor sizes) and technological parameters to guarantee correct DC operation. The analytical results have been then validated by simulation experiments performed with HSPICE. Finally, the models are used to investigate the effects of different figures of merit which describe the electrical characteristics of RTDs and transistors on MOBILE design and they have been generalized to more complex gates. The difficulty of an analytical study has been overcome by resorting to simple algebraic approximations for the *I–V* characteristics of both the RTD and the transistor.

The paper is organized as follows: Firstly, the DC operation of MOBILE circuits is described, and stated the equation ruling their behaviour. Next, the relations between sizing devices, technological setup and an incorrect DC operation are analyzed. Two malfunctions giving an incorrect DC operation are identified and described. Algebraic methods to get bounds for a correct

behaviour are developed in Section IV and Section V. In Section VI, simulation results validating our analysis are provided, and expressions giving the bounds for a correct behaviour are used to explore the capabilities a technology presents to efficiently implement MOBILE-based circuits. Section VII extends the techniques used in the previous analysis to analyze more complex logic blocks. Finally, some conclusions are given

II. DC Operation of MOBILE Circuits

Resonant tunnelling devices are today considered the most mature type of quantum-effect devices, already operating at room temperature. Resonant tunnelling diodes (RTDs) exhibit a negative differential resistance (NDR) region in their current-voltage characteristics, which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies [12], [20], [21]. The basic RTD device configuration (Figure 1a) is a sandwiched structure composed of two contacts (called the emitter and the collector, although the device is symmetric) made from a semiconductor with a small bandgap (e.g. GaAs), and a double tunnel barrier structure made from a semiconductor with a larger bandgap (e.g. AlGaAs or InGaAs). This contains a narrow quantum well (about 5 nm) made from the smaller bandgap semiconductor [20], [22], which allows electrons to travel through only at the resonant energy levels. The quantum well uses to be so narrow that it can only contain a single energy level. The characteristic of this device is similar to the Esaki tunnel diode, and exhibits a region of negative resistance, as shown in Figure 1b. This figure depicts the driving point characteristic of an RTD showing the typical three regions of positive (I), negative (II), and positive (III) differential resistance, as well as key parameters for circuit design: peak current and voltage, I_p and V_p, and valley current and voltage, I_v and V_v, and peak current is proportional to RTD area. Circuit applications of RTDs are mainly based on the MOnostable- BIstable Logic Element (MOBILE) [8], [9], [10], [13]. The MOBILE is a rising edge triggered current controlled gate which consists of two RTDs connected in series (the load and the driver RTDs) and driven by a switching bias voltage (V_{bias}), as shown in Figure 2a. When V_{bias} is low both RTDs are in the on-state (or low resistance state) and the circuit is monostable. During the critical period when V_{bias} exceeds twice the peak voltage of the RTD, the monostable to bistable transition occurs, and results in two self-stabilizing digital output states (on- and off-states). Consequently, the voltage at the output node V_{bias} goes to one of the two stable states (low and high corresponding to "0" and "1" in binary logic), depending on which NRD has the smaller peak current. The device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state) when V_{bias} increases. Output is high if the driver RTD is the one which switches, and it is low if the load switches.

The RTD is a two terminal device without input-output capabilities. Logic functionality is achieved by embedding an input stage which modifies, according to the applied input signal, the peak current of one of the RTDs, as shown in Figure 2b; for example, a Heterojunction Field-Effect Transistor (HFET) in parallel to the load (or driver) being the peak current of RTD_L (RTD_D) modulated by an external input V_{in} [8], [13].

Because of the two stable states in the load curve representation, the output node maintains its value for V_{bias} high even if the input changes. That is, this circuit structure is self-latching allowing the implementation of pipelining at the gate level without any area overhead associated to the addition of the latches [8], [11], [20]. The self-latching feature has been claimed to be a very attractive feature of MOBILE-based circuits, and this nanopipelined architecture allows very high through-output.

In the simulations and numerical analysis performed, models for RTDs and transistors from LOCOM [23] have been used, where the mathematical model for the non-linear *I–V* characteristic of the RTD uses exponential and Gaussian functions. For this RTD, V_p is 0.21V, the peak current density 21KA/cm^2, and the peak to valley current ratio is about 6.25 at room temperature. The transistor is a depletion HFET with threshold voltage –0.2*V*.

Two basic RTD-based MOBILE circuits have been considered in order to analyze their DC operation: the follower and the inverter. Figure 3a shows a follower based on MOBILE which consists of two serially connected RTDs (RTD_L and RTD_D) and an input stage composed of an HFET (TT_1). The transistor connected in parallel with RTD_L works as a current modulator and can

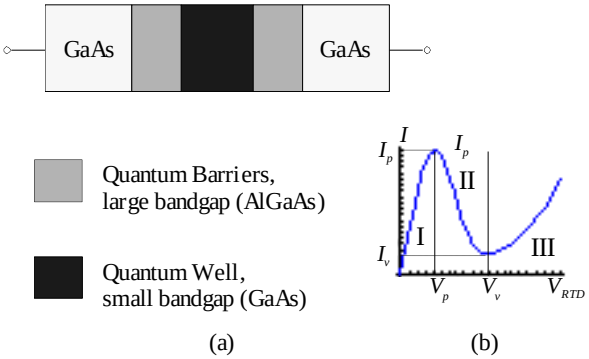


Figure 1. (a) Typical structure for a resonant tunneling diode
(b) *I–V* characteristics for a typical RTD.

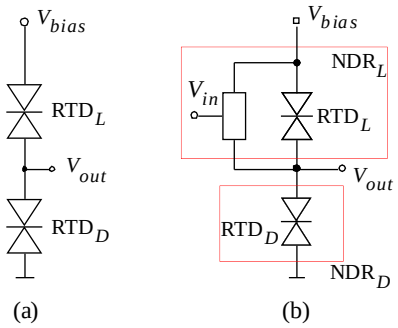


Figure 2. (a) Basic MOBILE circuit, (b) generic MOBILE follower cir cuit.

change the effective peak current of RTD$_L$. The circuit is driven by a clocked bias voltage, V_{bias}. The behaviour of a well designed follower is as follows: when V_{bias} is low the circuit is monostable and the output is in a low state. When V_{bias} is high, the output must follow the input V_{in}. The MOBILE is in the bistable state, *i.e.*, the output is "high" or "low" depending on the relationship in the peak currents between NDR$_L$ and RTD$_D$ at the rising edge of V_{bias}. If the peak current of NDR$_L$ is larger than that of RTD$_D$, the output is "high". If it is RTD$_D$ that is larger than that of NDR$_L$, then the output is "low". Once the output has been determined, it is maintained while V_{bias} is high. Figure 3b shows this behaviour for the low and high input values, respectively. Output V_{out} always traces the thick black line with the change in V_{bias}. As it can be easily verified, this follower presents a correct static operation.

Figure 3c shows an RTD-based MOBILE inverter. The transistor is now connected in parallel with RTD$_D$ and changes its effective peak current. The circuit is driven by a clocked bias voltage, V_{bias} and its behaviour is similar to the one shown in Figure 3b for the follower, but now interchanging the low and high input values. The behaviour of a well designed inverter is as follows: when V_{bias} is low the circuit is monostable and the output is in a low state. When V_{bias} goes high, the output must invert the input V_{in}. The MOBILE is in the bistable state, *i.e.*, the output is "high" or "low" depending on the relationship in the peak currents between NDR$_L$ and NDR$_D$ at the rising edge of V_{bias}. If the peak current of NDR$_L$ is larger than that of NDR$_D$, the output is "high". If it is NDR$_D$ that is larger than that of NDR$_L$, then the output is "low". Once the output has been determined, it is maintained while V_{bias} is high.

DC operation of the MOBILE follower is obtained by applying the Kirchoff's Law to the circuit in Figure 3a, *i.e.*, current through NDR$_L$ must be equal to current through NDR$_D$. Thus,

$$G_L\left[V_{bias}-V_{out}\right]+I_{DS}\left[V_{in}-V_{out},V_{bias}-V_{out}\right]=G_D\left[V_{out}\right] \quad (1)$$

where $G_i[v_{RTD}]$ and $I_{DS}[v_{GS}, v_{DS}]$ are the mathematical representation of the RTD$_i$ and HFET currents. Assuming equal current densities for all the RTDs, peak currents are proportional to RTD areas and thus, $G_i[v_{RTD}] = f_i\, g[v_{RTD}]$, where f_i is the area factor[1] of RTD$_i$, and $g[v_{RTD}]$ the mathematical representation of the current corresponding to an RTD of area factor equal to the unity. Thus, Eq. (1) transforms in:

$$f_L\, g\left[V_{bias}-V_{out}\right]+FF\, i_{DS}\left[V_{in}-V_{out},V_{bias}-V_{out}\right]=f_D\, g\left[V_{out}\right] \quad (2)$$

where $I_{DS}[\cdot,\cdot] = FF\, i_{DS}[\cdot,\cdot]$, and FF is the form factor ($FF = W / L$) for the transistor.

For the case of the MOBILE inverter in Figure 3c, the DC operation is given by

$$f_D\, g\left[V_{out}\right]+FF\, i_{DS}\left[V_{in},V_{out}\right]=f_L\, g\left[V_{bias}-V_{out}\right] \quad (3)$$

III. Sizing of MOBILE Circuits

Sizing the RTDs and the transistor has critical effects on the correct operation of the MOBILE follower or inverter. Two different problems can be pointed out, and both of them are related to the modulation of the effective peak current by transistor TT$_1$.

The first one claims that this modulation may not be enough for the output (V_{out}) to follow V_{in} when V_{bias} is high ("incorrect evaluation" fault). Figure 4 depicts plots of the solutions to Eq. (2) in the plane V_{out}–V_{bias} for both the low value $V_{in}^{low} = 0V$ and the high value $V_{in}^{high} = 0.65V$, and two FF values for a MOBILE follower. These profiles are determined by the I–V characteristics of the RTDs and the transistor. With static (or an slow enough transient) operation, V_{out} always traces the thick black line with the change in V_{bias} from 0 to $V_{bias}^{high} = 0.8V$. The extensive and experimentally validated RTD and HFET models developed within the LOCOM European Project [23] have been used to solve Eq. (2). Area factors employed are: $f_D = 1$ in the

[1] An area factor of 1 corresponds to an RTD of area 10μm^2

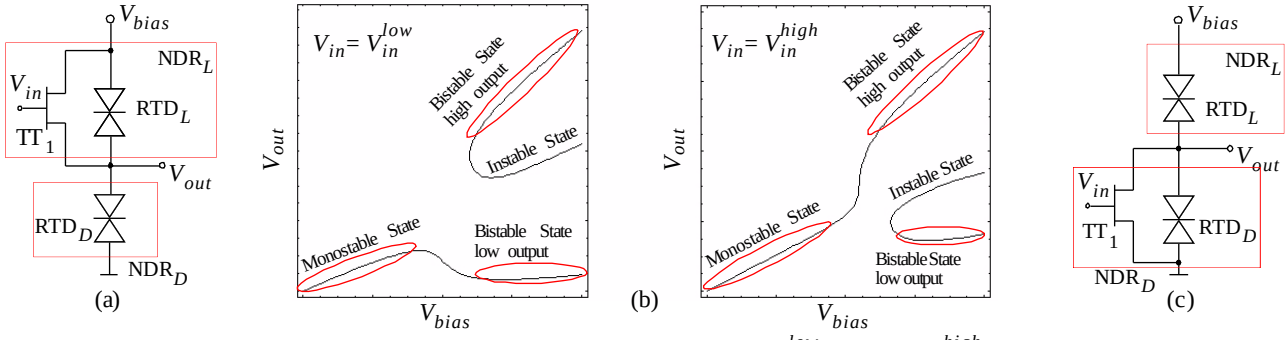


Figure 3. (a) MOBILE follower circuit. (b) DC solutions in a MOBILE follower for $V_{in}= V_{in}^{low}$, and $V_{in}= V_{in}^{high}$, (c) MOBILE inverter circuit.

RTD$_D$, and $f_L = 0.7$ in the RTD$_L$. Figure 4a has been obtained with a transistor form factor of 6, and 8 has been used to obtain Figure 4b. As it can be easily verified, there is a correct static operation in the case of Figure 4b, *i.e.*, solutions to Eq. (2) in the plane V_{out}–V_{bias} constitute a 'continuum' beginning in $V_{out}= 0V$ for $V_{bias}= 0V$, and finishing in a low voltage value for the high value of V_{bias} if $V_{in}= 0V$, or in a high voltage value if $V_{in}= 0.65V$. However, in Figure 4a an incorrect behaviour can be observed because the output is a low voltage even for a high value in the input, instead of the correct high value. The only difference between the circuits is the transistor sizing. In a similar way, it is possible to consider an incorrect behaviour for the low input. It would produce a high output voltage for the high value of V_{bias}. However, this behaviour is not possible with the LOCOM technology we are considering.

The second problem, the "self-latching disappearance" fault, is related to the disappearance of the MOBILE self- latching capability. In a well-designed MOBILE follower (Figure 3), if the input value is a low voltage when the bias rises, the output is a low voltage value. A change in the input value from low to high when V_{bias} is a high value has no effect on the output which maintains its low voltage value, as it is shown in the simulation results of Figure 5a for a follower with RTD area factors given by $f_D = 1$ (RTD$_D$) and $f_L = 0.7$ (RTD$_L$), and a transistor form factor of $FF = 8$. The final output is a correct low value.

Let us consider another follower with the same RTD area factors but with a transistor form factor of $FF = 12$. Figure 5b depicts the simulation results for this follower and its final output state in an incorrect high voltage value. The output node can not maintain its value for V_{bias} high with an input rise; the self-latching capability has disappeared. Figure 5c depicts the DC solutions for this MOBILE ($f_D = 1$, $f_L = 0.7$, and $FF = 12$), when $V_{in} = 0V$, and $V_{in} = 0.65V$. The disappearance of one of the two stable states in the DC solution representation for the V_{bias} high value when $V_{in} = V_{in}^{high}$ motivates this malfunction. In general, when the high or the low "lobe" in the V_{out}–V_{bias} graphs (Figure 3), disappear, there is a "self-latching disappearance" fault. Qualitatively, this means that there is only one cut between load and driver NDR characteristics for $V_{bias} = V_{bias}^{high}$.

Concerning the inverter, the same problems of incorrect evaluation and self-latching disappearance can be pointed out. Figure 6 depicts plots of the solutions to Eq. (3) in the plane V_{out}–V_{bias} for both the low and high value of V_{in} in a MOBILE inverter with area factors $f_D = 0.7$ and $f_L = 1$, and three different FF values. Figure 6a has been obtained with a transistor form factor of 4, $FF = 5$ has been used to obtain Figure 6b, and $FF = 30$ in order to get Figure 6c. As it can be easily verified, there is a correct static operation only in the case of Figure 6b, *i.e.*, solutions to Eq. (3) in the plane V_{out}–V_{bias} constitute a 'continuum' beginning in $V_{out} = 0V$ for $V_{bias} = 0V$, and finishing in a high voltage value for the high value of V_{bias} if $V_{in} = 0V$, or in a low voltage value if $V_{in} = 0.65V$. In Figure 6a an incorrect behaviour can be observed because the output is a high voltage even for a high value in the input, instead of the correct low value. In Figure 6c the output is a low voltage even for a low value in the input.

Figure 7 depicts plots of the solutions to Eq. (3) in the plane V_{out}–V_{bias} for $V_{in} = 0V$ and $V_{in} = 0.65V$, for a MOBILE inverter with RTD area factors of $f_D = 0.7$ and $f_L = 1$, but now with a transistor size of $FF = 8$. This MOBILE inverter does not present an incorrect evaluation, *i.e.*, if the input value is a low voltage when the bias rises, the output is a high voltage value. After this, however, in a well designed inverter (as the one in Figure 6b), a change in the input value from low to high (when V_{bias} is a high value) has no effect on the output, which maintains its high voltage value (Figure 8a). For the MOBILE inverter with $FF = 8$, the same sequence of changes in V_{in} and V_{bias} forces the output to be a low voltage value, as shown in Figure 8b, and the output node can not maintain its value for V_{bias} high with an input rise.

IV. Critical Dependencies in a MOBILE Follower

In the previous section we have discussed how the shape of the set of solutions to Eq. (2) or Eq. (3) is critical to design an RTD-based MOBILE follower with a correct DC operation. In this Section, we will develop simple algebraic methods to obtain bounds for such correct behaviour. A more elaborate analysis has been performed in the Appendix.

A. Incorrect Evaluation

When area factors for both RTDs in a MOBILE configuration are extremely close, the decision on what output the MOBILE will give [11] is taken for $V_{bias} = 2V_p$, being the voltage drops approximately equal in the upper and lower RTDs ($V_{RTD_L}^{crit} = V_{RTD_D}^{crit} = V_p$). Voltage V_p is the peak voltage where the current peak I_p is reached (Figure 1b). In the case of a MOBILE follower, a good approach to obtain the critical dimension for the HFET which avoids the malfunction can be derived by maintaining the analogy with the behaviour above described.

Initially, for V_{bias} rising from a low value, both RTDs are in their first region of positive resistance, and the value for V_{out} increases as V_{bias} does. For a given value of V_{bias}, V_{bias}^{crit}, close to $2V_p$, the voltage through RTD$_D$, V_{out}, reaches its peak voltage V_p, as well as the voltage through NDR$_L$. Two types of incorrect evaluation can appear: incorrect evaluation for the low or the high input voltages. Thus, two evaluation conditions must be verified,

$$\begin{aligned} f_L\, g\left[V_{bias}^{crit} - V_{out}\right] + FF\, i_{DS}\left[V_{in}^{low} - V_{out}, V_{bias}^{crit} - V_{out}\right] &< f_D\, g\left[V_{out}\right] \\ f_L\, g\left[V_{bias}^{crit} - V_{out}\right] + FF\, i_{DS}\left[V_{in}^{high} - V_{out}, V_{bias}^{crit} - V_{out}\right] &> f_D\, g\left[V_{out}\right] \end{aligned} \quad (4)$$

which, taking into account that $V_{out} = V_p$ for $V_{bias}^{crit} = 2V_p$ and $g\left[V_p\right] = I_p$, provide two critical values for the transistor form factor *FF*,

$$\frac{\left(f_D - f_L\right) I_p}{i_{DS}\left[V_{in}^{high} - V_p, V_p\right]} \le FF \le \frac{\left(f_D - f_L\right) I_p}{i_{DS}\left[V_{in}^{low} - V_p, V_p\right]} \quad (5)$$

i.e., values FF^{min} and FF^{max} are given by,

$$FF^{min} = \left(f_D - f_L\right) I_p \Big/ i_{DS}\left[V_{in}^{high} - V_p, V_p\right] \quad (6)$$

$$FF^{max} = \left(f_D - f_L\right) I_p \Big/ i_{DS}\left[V_{in}^{low} - V_p, V_p\right] \quad (7)$$

Usually $i_{DS}\left[V_{in}^{low} - V_p, V_p\right] \cong 0$, and in order to obtain a correct evaluation, Eq. (4) provides $f_L < f_D$, and a constraint on *FF* which only involves the minimum value, FF^{min}. This situation is true for the LOCOM technology, for which $V_{in}^{high} = 0.65V$, and $V_{in}^{low} = 0V$. For it, current $i_{DS}\left[V_{in}^{high} - V_p, V_p\right]$ (i_{DS1}) is 98.43μA, and the relation $I_p / i_{DS1} = 21.3$. Thus, the minimum size for the transistor in LOCOM technology is about 20 times the difference between RTD area factors. For the RTDs in Figure 9, ($f_D = 1$, $f_L = 0.7$) the minimum transistor size would be approximately $FF^{min} \cong 20 \times 0.3 = 6$. The follower in Figure 9a (*FF* = 6) does

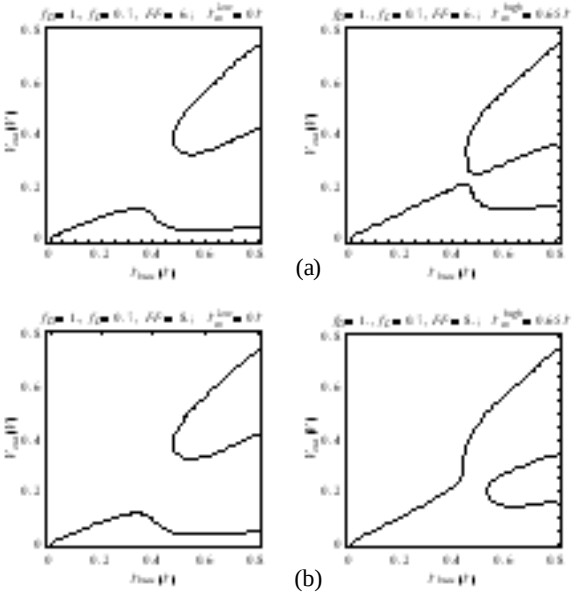


Figure 4. DC solutions for $f_D = 1$, $f_L = 0.7$, $V_{in} = 0V$, and $V_{in} = 0.65V$, (a) *FF* = 6, (b) *FF* = 8.

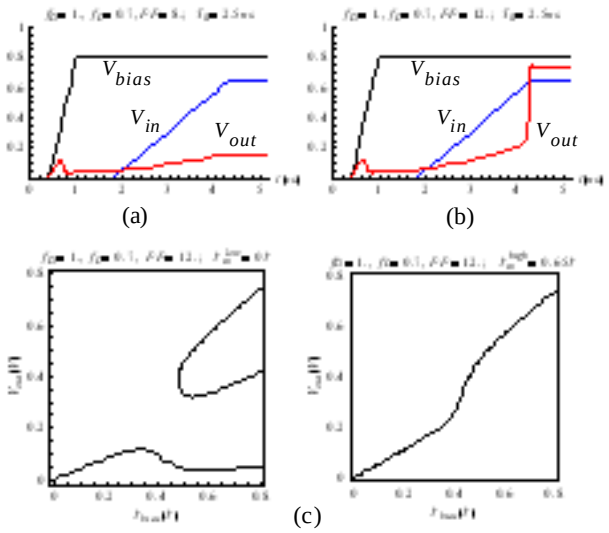


Figure 5. Waveforms for a MOBILE follower with $f_D = 1$, $f_L = 0.7$, (a) for $FF = 8$, (b) $FF = 12$,
(c) DC solutions for the MOBILE follower with $f_D = 1$, $f_L = 0.7$, and $FF = 12$, when $V_{in} = 0V$, and $V_{in} = 0.65V$.

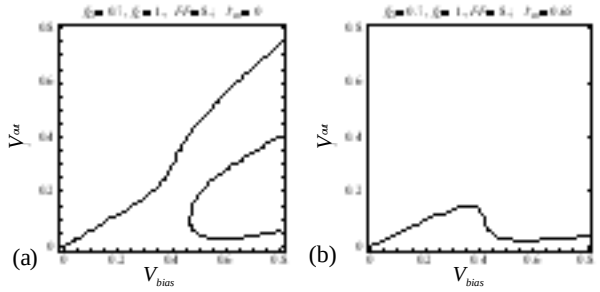


Figure 7. DC solutions for a MOBILE inverter in the plane V_{out} –V_{bias} for $f_D = 0.7$, $f_L = 1$, $FF = 8$, (a) $V_{in} = 0V$ and (b) $V_{in} = 0.65V$.

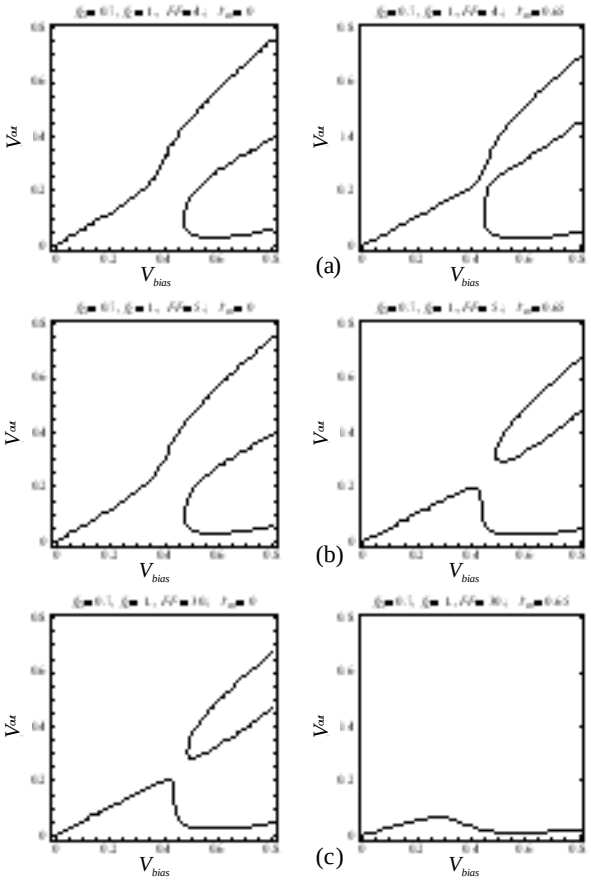


Figure 6. DC solutions for $f_D = 0.7$, $f_L = 1$. (a) $FF = 4$, (b) $FF = 5$, and (c) $FF = 30$.

present malfunction, but the one in Figure 9b ($FF = 7$) operates correctly.
More elaborate calculations to obtain more precise FF bounds can be found in the Appendix.

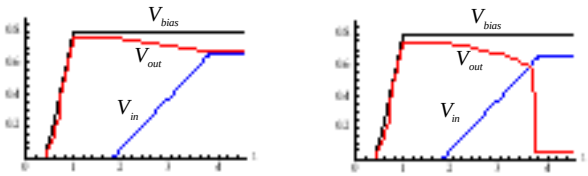
B. Self-latching Disappearance

The second problem is the disappearance of the self- latching capability. This problem is related to the disappearance of one of the two stable states in the DC solution representation for the V_{bias} high value, what means that the high or the low "lobe" in the V_{out}–V_{bias} graphs (Figure 3), disappear. Qualitatively, there is only one cut between load and driver NDR characteristics for $V_{bias} = V_{bias}^{high}$. Two situations must be considered depending on the value, low or high, of the applied input V_{in}.

Let us consider the MOBILE follower with $f_D = 1$, $f_L = 0.7$, and $FF = 12$ which lobe lacking DC solutions for $V_{in} = V_{in}^{high}$ are in Figure 5c. A change in the input value from low to high when V_{bias} is the high voltage value forces the output to be a high voltage value. To analyze this problem it is interesting to consider plots of the solutions to Eq. (2) in the plane V_{out}–V_{in} for the high voltage value of the bias voltage. Figure 10a depicts such a plot for this MOBILE follower when $V_{bias}^{high} = 0.8V$. The red discontinuous line corresponds to the evolution of the follower output for the input change above described (simulation data taken from Figure 5b), and the red point (at $V_{in} = 0.65V$) the final output value.

The analysis of the behaviour for the MOBILE follower in Figure 4b ($f_D = 1$, $f_L = 0.7$, $FF = 8$) shows a very different result. Figure 10b shows the solutions to Eq. (2) in the plane V_{out}–V_{in} and the red discontinuous line is also the output evolution for the same input change (simulation data taken from Figure 5a). The final output is a correct low voltage value, and the output does not modify its value.

The previous results suggest that a good criterion for foreseeing the problem of self-latching disappearance is to determine



(a) (b)

Figure 8. Simulation results for a MOBILE inverter with $f_D = 0.7$, $f_L = 1$, (a) $FF = 5$, (b) $FF = 8$.

whether there are one or three solutions to Eq. (2) for the high voltage value of V_{in}. Let us consider the situation in Figure 10b. There are three solutions for $V_{in}^{high} = 0.65V$ marked as ①, ②, and ③. For the first solution, (marked as ①), RTD$_D$ is in its first positive region (region I in Figure 1b), and RTD$_L$ is in its second positive region (region III in Figure 1b). The second solution (marked as ②) has both RTD$_D$ and RTD$_L$ in the NDR region (region II). Finally, for the third solution (marked as ③), RTD$_D$ is in its second positive region (region III), and RTD$_L$ is in its first positive region (region I). A critical point to malfunction will appear if solutions marked as ① and ② collapse. Next, we will derive a method to obtain an analytical solution for this situation.

For the critical situation, RTD$_D$ is biased close to its peak voltage, V_p, and RTD$_L$ is biased close to $V_{bias}^{high} - V_p$. A first analysis of this problem can be performed by approximating voltages through RTD$_D$ and RTD$_L$ as V_p and $V_{bias}^{high} - V_p$, respectively, Thus,

$$f_L\, g\left[V_{bias}^{high} - V_p\right] + FF\, i_{DS}\left[V_{in}^{high} - V_p, V_{bias}^{high} - V_p\right] = f_D\, g\left[V_p\right] \quad (8)$$

i.e., there is a self-latching disappearance problem for $V_{in} = V_{in}^{high}$ if the transistor form factor is,

$$FF \geq FF^{max} = \frac{f_D\, I_p - f_L\, g\left[V_{bias}^{high} - V_p\right]}{i_{DS}\left[V_{in}^{high} - V_p, V_{bias}^{high} - V_p\right]} = k_1\, f_L\left(k_2 \frac{f_D}{f_L} - 1\right) \quad (9)$$

where constants k_1 and k_2 are given by $k_1 = g\left[V_{bias}^{high} - V_p\right] / i_{DS}\left[V_{in}^{high} - V_p, V_{bias}^{high} - V_p\right]$ and $k_2 = I_p / g\left[V_{bias}^{high} - V_p\right]$, respectively. For the LOCOM technology these values are 1.95 and 6, respectively.

A similar analysis can be done to study the conditions for the lack of solutions when $V_{in} = V_{in}^{low}$. In the critical situation RTD$_D$ is biased close to $V_{bias}^{high} - V_p$, and RTD$_L$ is biased close to its peak voltage, V_p. If both voltages are approximated by $V_{bias}^{high} - V_p$ and V_p, respectively, then,

$$f_L\, g\left[V_p\right] + FF\, i_{DS}\left[V_{in}^{low} - \left(V_{bias}^{high} - V_p\right), V_p\right] = f_D\, g\left[V_{bias}^{high} - V_p\right] \quad (10)$$

Usually, $i_{DS}\left[V_{in}^{low} - \left(V_{bias}^{high} - V_p\right), V_p\right] = 0$, and there is a self-latching disappearance problem for the low input voltage when the relation f_D/f_L is greater than $I_p / g\left[V_{bias}^{high} - V_p\right]$. This value is the same k_2 in Eq. (9). If the current through the transistor is not zero, then, the critical value for the transistor form factor is given by,

$$FF^{crit} = \frac{f_D\, g\left[V_{bias}^{high} - V_p\right] - f_L\, I_p}{i_{DS}\left[V_{in}^{low} - \left(V_{bias}^{high} - V_p\right), V_p\right]} \quad (11)$$

and the transistor form factor must be greater than it to obtain a correct operation.

As in the case of the incorrect evaluation, a more precise analysis can be found in the Appendix.

C. *Existence of solutions*

At this point we are able to know whether a specific MOBILE follower has or not a DC correct operation. For this, we will suppose $i_{DS}\left[V_{in}^{low} - V_p, V_p\right] = 0$, which forces $f_L < f_D$. A correct DC operation is obtained if the form factor of the transistor is into the interval given by FF^{min} (from the evaluation) and FF^{max} (from the self-latching). The quotient between these values depends on f_D/f_L as well as on technological parameters, both if we use the equation pair Eq. (6) and Eq. (9) or the more precise expressions from the Appendix (Eq. (30) and Eq. (36)).

The limit condition for the quotient FF^{min}/FF^{max} (which depends on f_D/f_L) gives the maximum possible ratio between driver and load area factors, which allows a MOBILE follower to have DC correct operation. We call it the technological factor for a follower (TF_f). For the LOCOM technology and using the expressions for FF^{min} and FF^{max} from the Appendix, TF_f is $TF_f \cong 2.6$, which joined with the more basic $f_L < f_D$ results in the relation $1 < f_D/f_L < 2.6$. Additionally, $I_p / g\left[V_{bias}^{high} - V_p\right] \cong 6$, and the self-

latching disappearance problem for the low input voltage does not introduce any modification on these limits. That is, a MOBILE follower in the LOCOM technology is only possible if the relation between area factors is comprised between 1 and 2.6.

V. Critical dependencies in a MOBILE Inverter

In this section we will perform a similar analysis to the one we have just carried out in the previous Section for the MOBILE follower, and bounds for a correct DC behaviour will be given. These bounds can be also refined as it was done in the Appendix for the follower.

A. Incorrect Evaluation

A correct behaviour forces the voltage through the driver NDR_D to be in its peak voltage, V_p^*, which now depends on the input voltage applied to the transistor. Thus, this peak voltage is different from the RTD peak voltage, but close to it. A first evaluation for this parameter and a generic input voltage V_{in}= VIN follows. Current through NDR_D, $I_{NDR_D}[v]$, is given by,

$$I_{NDR_D}\left[v_{NDR_D}\right] = f_D\, g\left[v_{NDR_D}\right] + FF\, i_{DS}\left[VIN, v_{NDR_D}\right] \tag{12}$$

where v_{NDR_D} is the voltage between NDR_D terminals. Eq. (12) can be approximated by

$$I_{NDR_D}\left[v_{NDR_D}\right] \cong f_D\left(g\left[V_p\right] + g''\left[V_p\right]\left(v - V_p\right)^2\right) + FF\left(i_{DS}\left[VIN, V_p\right] + i'_{DS}\left[VIN, V_p\right]\left(v - V_p\right)\right) \tag{13}$$

By deriving this expression, and equating the result to zero, we have

$$V_p^* = V_p - \frac{FF}{2 f_D}\frac{i'_{DS}\left[VIN, V_p\right]}{g''\left[V_p\right]} \tag{14}$$

i.e., the NDR_D peak voltage depends on both, geometric (RTD area factor and the transistor form factor) and technological parameters, as well as on the transistor gate voltage. For the LOCOM technology, the term $i'_{DS}\left[VIN, V_p\right] / g''\left[V_p\right]$ is approximately $-1.2\cdot10^{-3}V$ for V_{in}= $0V$, and $-7.5\cdot10^{-3}V$ for V_{in}= $0.65V$.

Given the low difference between the V_p and V_p^* values, we can consider that decision about the output is taken for $V_{bias} = 2V_p$, in a similar way to the follower. Two evaluation conditions must be verified,

$$\begin{cases} f_L\, g\left[V_p\right] > FF\, i_{DS}\left[V_{in}^{low}, V_p\right] + f_D\, g\left[V_p\right] \\ f_L\, g\left[V_p\right] < FF\, i_{DS}\left[V_{in}^{high}, V_p\right] + f_D\, g\left[V_p\right] \end{cases} \tag{15}$$

which allow us to obtain a double constraint for the FF values,

$$\frac{\left(f_L - f_D\right) I_p}{i_{DS}\left[V_{in}^{high}, V_p\right]} \le FF \le \frac{\left(f_L - f_D\right) I_p}{i_{DS}\left[V_{in}^{low}, V_p\right]} \tag{16}$$

i.e., values FF^{min} and FF^{max} for the correct evaluation are given by,

$$FF^{min} = \left(f_L - f_D\right) I_p \,/\, i_{DS}\left[V_{in}^{high}, V_p\right] \tag{17}$$

$$FF^{max} = \left(f_L - f_D\right) I_p \,/\, i_{DS}\left[V_{in}^{low}, V_p\right] \tag{18}$$

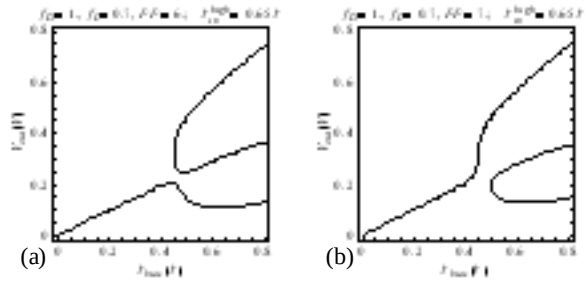


Figure 9. DC solutions for a type-I follower $f_D = 1$, $f_L = 0.7$, (a) for $FF = 7$, (b) for $FF = 6$.

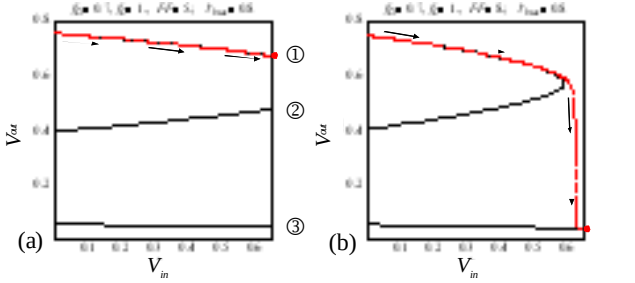


Figure 11. DC solutions in the plane $V_{out} - V_{in}$ for $V_{bias} = 0.8V$ $f_D = 0.7$, $f_L = 1$, (a) $FF = 5$, (b) $FF = 8$.

For the LOCOM technology, $i_{DS}\left[V_{in}^{low}, V_p\right]$ and $i_{DS}\left[V_{in}^{high}, V_p\right]$ are 22.62μA, and 139.22μA, respectively. Thus, transistor size limits are about 15 times and 90 times the difference between RTD area factors. For an RTDs with $f_D = 0.7$, $f_L = 1$ these bounds are 4.5 and 27, *i.e.*, there is a correct evaluation if $4.5 \le FF \le 27$. Only the inverter in Figure 6b ($FF = 5$) evaluates correctly. The one in Figure 6a ($FF = 4$) or in Figure 6c ($FF = 30$) does present malfunction.

B. Self-latching disappearance

The disappearance of one of the two stable states in the DC solution representation for a high value of V_{bias} can be observed in Figure 7 (for V_{in}^{high}). Let us consider the situation in Figure 11a. There are three solutions for $V_{in}^{high} = 0.65V$, shown as ①, ②, and ③. A malfunction will appear after solutions marked as ① and ② collapse.

For the critical situation RTD_L is biased close to V_p, and RTD_D is biased close to $V_{bias}^{high} - V_p$. Thus,

$$f_L\, g\left[V_p\right] = f_D\, g\left[V_{bias}^{high} - V_p\right] + FF\, i_{DS}\left[V_{in}^{high}, V_{bias}^{high} - V_p\right] \qquad (19)$$

i.e., there is a self-latching disappearance problem for $V_{in} = V_{in}^{high}$ if the transistor form factor is,

$$FF \ge FF^{max} = \frac{f_L\, I_p - f_D\, g\left[V_{bias}^{high} - V_p\right]}{i_{DS}\left[V_{in}^{high}, V_{bias}^{high} - V_p\right]} = k_1\, f_D\left(k_2\, \frac{f_L}{f_D} - 1\right) \qquad (20)$$

where constants k_1 and k_2 are now given by $g\left[V_{bias}^{high} - V_p\right] / i_{DS}\left[V_{in}^{high}, V_{bias}^{high} - V_p\right]$ and $I_p / g\left[V_{bias}^{high} - V_p\right]$, respectively. For the LOCOM technology these values are 1.38 and 6, respectively.

A self-latching bistability problem for the low input value is produced when RTD_L is biased close to $V_{bias}^{high} - V_p$, and RTD_D is biased close to V_p. Graphically, there is another lobe (similar to the one in Figure 11b), but noe it is closed at the left side. Thus,

$$f_L\, g\left[V_{bias}^{high} - V_p\right] = f_D\, g\left[V_p\right] + FF\, i_{DS}\left[V_{in}^{low}, V_p\right] \qquad (21)$$

i.e., there is a self-latching disappearance problem for $V_{in} = V_{in}^{low}$ if the transistor form factor is,

$$FF \le FF^{min} = \frac{f_L\, g\left[V_{bias}^{high} - V_p\right] - f_D\, I_p}{i_{DS}\left[V_{in}^{low}, V_p\right]} = k_1\, f_D\left(\frac{f_L}{f_D} - k_2\right) \qquad (22)$$

where constants k_1 and k_2 are now given by $g\left[V_{bias}^{high} - V_p\right] / i_{DS}\left[V_{in}^{low}, V_p\right]$ and $I_p / g\left[V_{bias}^{high} - V_p\right]$, respectively. For the LOCOM technology these values are 8.48 and 6, respectively.

C. Existence of solutions

There are four limits for the inverter: two minimum bounds, those given by a correct evaluation of the logic one, and by the correct self-latching operation for the logic zero; and two maximum bounds, the corresponding ones to the correct evaluation of the logic zero, and to the correct self-latching operation for the logic one. Let us call FF^{MIN} to the maximum of these two minimum bounds and FF^{MAX} to the minimum of the maximum bounds. A correct operation is obtained if the transistor is seized between FF^{MIN} and FF^{MAX}. The quotient between these values depends on f_L/f_D as well as on technological parameters; both if we use the simpler previously derived equations or more precise expressions (as in the follower)

The limit condition for the quotient FF^{MIN}/FF^{MAX} gives the maximum possible ratio between driver and load area factors for a MOBILE inverter with DC correct operation. We call it the technological factor for an inverter (TF_i). For the LOCOM

technology, and using more precise expressions for FF^{MIN} and FF^{MAX}, TF_i results in 2.36. Thus, a MOBILE inverter in the LOCOM technology is only possible if the relation between form factors in load and driver is comprised between 1 and 2.36.

VI. Simulation Results

Expressions previously derived can be used to explore the capabilities of a technology to efficiently implement MOBILE-based circuits. In order to check the approach, this has been tested on a real technology: the LOCOM technology. Figure 12a shows the feasible operation regions for three different followers each one with a fixed value for the driver RTD area, f_D (f_D = 1, 2, and 3). For each possible value of the load RTD area factor, f_L, there exists a minimum and a maximum allowable values for the transistor form factor (it has been employed the most precise expressions given by Eq. (30) and Eq. (36) in the Appendix), and thus a closed area (like a "triangle") is obtained. Permissible values for f_L are limited by f_D (the vertical line), and they begin in the f_L value corresponding to f_D/TF_f (from Eq. (38)). This figure also includes extreme points from HSPICE simulations. As it can be easily observed, the agreement between simulation and model is very good.

Figure 12b shows the triangular feasible operation regions for three different inverters each one with a fixed value for the load RTD area factor, f_L (f_L = 1, 2, and 3). For each f_L, the minimum and maximum allowable values for the transistor form factor have been obtained. Permissible values for f_D are limited by vertical lines at f_L, and they begin in the f_D value corresponding to f_L/TF_i. The figure also includes points from HSPICE simulations. As it can be easily observed, the agreement between simulation and model is also very good.

Additionally, we have tested our approach by using a different modelling for the RTDs: the Schulman-Broekaert formula fit [24]. The RTD we have used has a peak current density of $10KA/cm^2$, a peak voltage of $0.16V$, and the peak to valley current ratio is about 9.5 at room temperature (we call it TECH2). Figure 13 shows the feasible operation regions for three different followers obtained with our approach as well as the HSPICE simulation points. The agreement is very good. Calculated triangular feasible regions and simulation points also show the same excellent agreement for the inverter.

Once the model has been adequately tested, we can exploit it by exploring the capabilities of an arbitrary RTD/HFET process to implement MOBILE circuits. Firstly, we have modified the RTD valley current from the model in LOCOM. Figure 14 shows the technological factor for the follower, TF_f, depending on the peak to valley current ratio, PVCR. In the curve we have obtained, the point corresponding to RTDs produced by LOCOM has been marked. The same experiment has been performed on the technology producing the RTDs we called TECH2. The corresponding TF_f curve is also shown in Figure 14, and the point corresponding to TECH2 has been also marked.

From these results, two conclusions are clear. First, there is a limit value for the PVCR below of which there is no operation as MOBILE follower (approximately 1.6 for the curve based on LOCOM; 1.3 for the one based on TECH2), and second, the f_D/f_L ratio does not significantly increment above a point. For example, in LOCOM technology, the PVCR is equal to 6.24, and its TF_f results in 2.67. A technological process reducing the valley current ten times (which is linked, for example, to a lowering in the power consumption) until a PVCR about 60 is reached, only improves TF_f from 2.67 until 2.85 (*i.e.*, it does not improve the circuit robustness).

Related to these considerations, it is interesting to see how the feasible operation regions are modified with the PVCR. Figure 15 shows how the feasible operation regions for a MOBILE follower depend on the PVCR. As it has been previously explained, the main difference is between results from a PVCR of 2.5 and a PVCR of 6.4. After this, the difference in the feasible regions for increasing PVCR is very little.

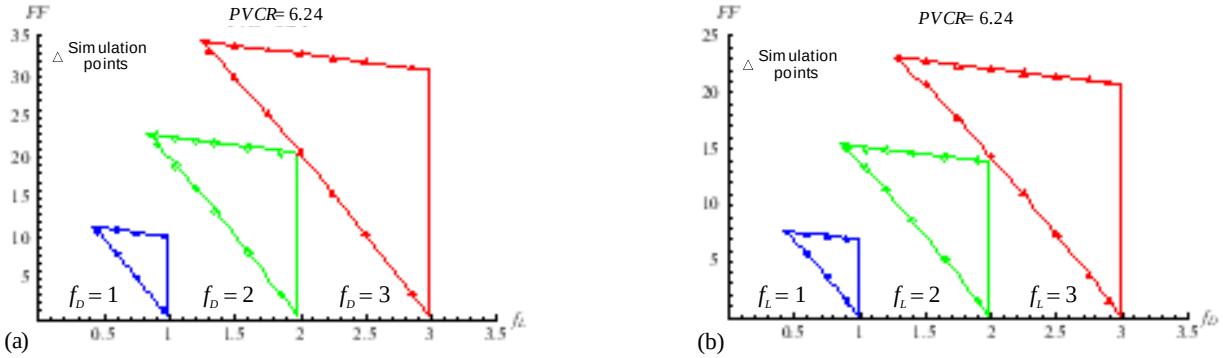


Figure 12. Feasible operation regions for LOCOM technology. (a) MOBILE followers depending on driver area factor, f_D. (b) MOBILE inverters depending on load area factor, f_L.

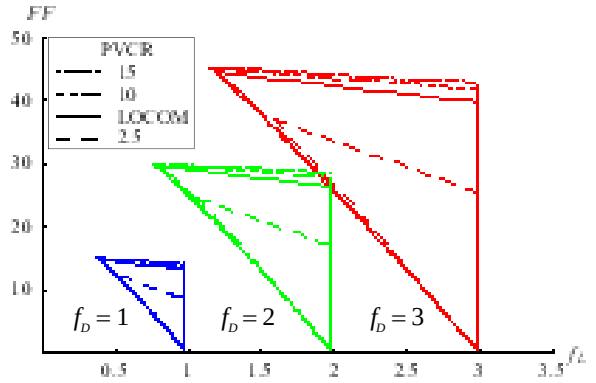


Figure 17. Feasible operation regions for a MOBILE follower depending on driver area factor, f_D, and different PVCR. Threshold voltage for the HFET = $-0.1V$.

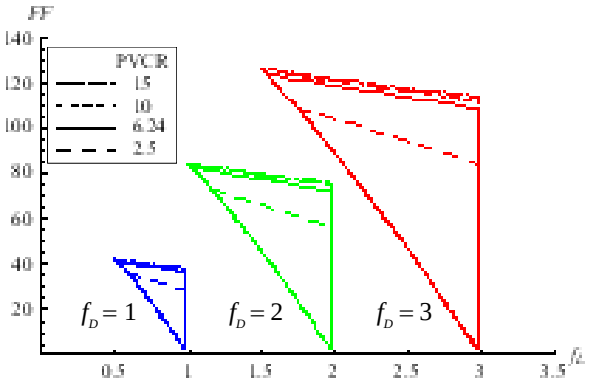


Figure 18. Feasible operation regions for a MOBILE follower depend ing on driver area factor, f_D, and different PVCR. Technology based on TECH3.

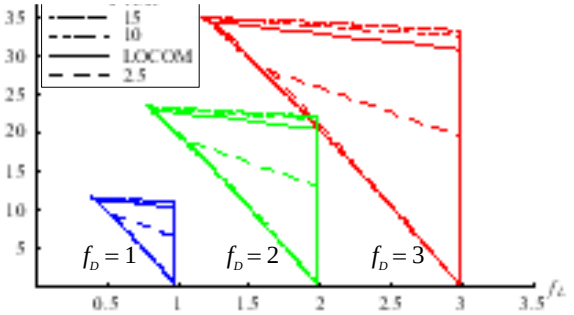


Figure 15. Feasible operation regions for a MOBILE follower depending on driver area factor, f_D, and different PVCR. Technology based on LOCOM.

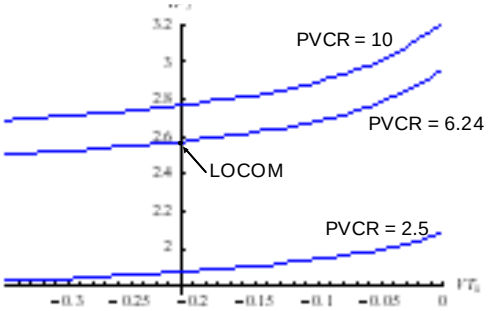


Figure 16. Technological factor for a MOBILE follower depending on the threshold voltage of the transistor.

Additionally, we have explored how differences in the transistor threshold voltage modify the technological factor in a MOBILE follower. As it can be easily seen in Figure 16, this technological factor is approximately constant for a wide variation of the threshold voltage, even if different PVCR values are considered. Figure 17 shows the feasible operation regions for a MOBILE follower depending on driver area factor, f_L, and different PVCR, but now the HFET has a threshold voltage of –0.1V. The main difference with Figure 15 is the wider range of *FF* values.

Previous results are mainly based on modifications of the LOCOM modelling (valley current, threshold voltage). It is interesting to analyze what happens when a deeper modification is performed. For that, we have considered a hypothetical technology (we call it TECH3) producing an RTD with a peak voltage in $0.1V$, a valley voltage of $0.3V$, a peak current about a 50% greater than the corresponding to LOCOM, and a PVCR of 12. Bias voltage is now $0.4V$, and a high input voltage for the transistor of $0.35V$ has been selected for input-output compatibility. Threshold voltage for the transistor has been maintained to $-0.21V$, and its beta, raised. Figure 14 shows the technological factor for the follower, obtained by modifying the PVCR. The corresponding curve shows a point for RTDs produced by TECH3. Previous considerations on the existence of a PVCR limiting value, or the quick increment of TF_f in a small region of PVCR, or the quasi-null increment of TF_f above a critical point can be also observed. Figure 18 shows the dependence on the PCVR of the feasible operation regions for a MOBILE follower. As it can be observed, it follows the same pattern than the one in Figure 15.

VII. Extension to Complex Logic Blocks

Techniques used in the previous analysis can be extended to examine more complex logic blocks. The case of a linear threshold gate (LTG) with n positive input variables x_1, ..., x_n, and threshold T is developed in this Section. This gate can be implemented by placing n input stages in parallel to RTD_L. Even more complex logic functions can be treated in a similar way.

The output of such an n-input LTG takes the logic value 1 if $\sum_{i=1}^{n} w_i x_i \geq T$, where w_i is the weight associated to the input x_i and T is the threshold, otherwise, it is 0. It can be shown that weights w_i and the threshold are integer positive numbers. Input

combinations satisfying $\sum_{i=1}^{n} w_i x_i = T$ define the minimum current contribution of input stages needed to obtain a high value in the output, and $\sum_{i=1}^{n} w_i x_i = (T-1)$, the maximum current contribution of input stages required to obtain a low value in the output. Thus, Eq. (4) can be rewritten as,

$$\begin{cases} f_L I_p + (T-1) FF\, i_{DS}\left[V_{in}^{high} - V_p, V_p\right] < f_D I_p \\ f_L I_p + T\, FF\, i_{DS}\left[V_{in}^{high} - V_p, V_p\right] > f_D I_p \end{cases} \qquad (23)$$

where $V_{out} = V_p$, $V_{bias}^{crit} = 2V_p$ and $g\left[V_p\right] = I_p$. Thus, Eq. (23) provides a double inequality,

$$\frac{\left(f_D - f_L\right) I_p}{T \cdot i_{DS}\left[V_{in}^{high} - V_p, V_p\right]} \le FF \le \frac{\left(f_D - f_L\right) I_p}{(T-1) \cdot i_{DS}\left[V_{in}^{high} - V_p, V_p\right]} \qquad (24)$$

i.e., we have an FF^{max} coming from the evaluation, even if $i_{DS}\left[V_{in}^{low} - V_p, V_p\right] \cong 0$. The new FF^{min} is the one calculated for a correct DC evaluation of logic 1 for the follower divided by the threshold *T*. The worst scenario which must be considered to avoid the self-latching disappearance problem is the situation with all the inputs at a logic "1". Thus, the FF^{max} calculated for the follower must be divided by $\sum_{i=1}^{n} w_i$. In consequence, there are two values for the upper *FF* bound. As a result, to obtain a correct DC operation in the implementation of the LTG we are considering, the form factor of the transistor must satisfy,

$$\frac{FF^{min}}{T} \le FF \le Min\left[\frac{FF^{min}}{T-1}, \frac{FF^{max}}{\sum_{i=1}^{n} w_i}\right] \qquad (25)$$

where FF^{min} and FF^{max} are the ones calculated for the follower.

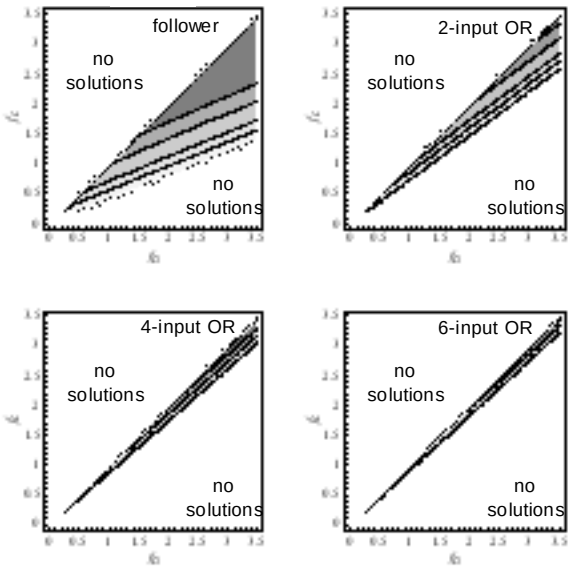


Figure 19. Feasible region set of (f_D, f_L)-pairs for *n*-input OR gates.

Well known logic functions are LTGs. For example, an *n*-input OR gate is a LTG defined by *n* weights all of them equal to 1 and a threshold of 1; an *n*-input AND gate is a LTG defined by *n* weights all of them equal to 1 and a threshold of *n*; or an *n*-input MAJ (majority) gate (*n* odd) is a LTG defined by *n* weights all of them equal to 1 and a threshold of (*n*+1)/2. To implement an *n*-input OR gate, the form factor of the transistor must be in the interval {FF^{min}, FF^{max}/n}; *FF* must be in {FF^{min}/n, Min[$FF^{min}/(n-1)$, FF^{max}/n]} for an *n*- input AND gate, and in the interval given by {$2FF^{min}/(n+1)$, Min[$2FF^{min}/(n-1)$, FF^{max}/n]} for an *n*-input MAJ gate (*n* odd).

For example, for LOCOM technology, a configuration with $f_D = 1$, $f_L = 0.8$ is useful for implementing a follower ($4.17 \le FF \le 10.7$), and a 2-input OR gate ($4.17 \le FF \le 5.35$), but it fails to implement a 3-input OR-gate. However, it allows an implementation of a 3-MAJ ($2.09 \le FF \le 3.56$) or a 3-AND gate ($0.70 \le FF \le 1.05$).

Figure 19 shows (f_D, f_L)-pairs for which there exist some *FF* value that allows a correct DC operation of four OR gates, the corresponding to *n* = 1 (the follower), 2, 4, and 6. The grey scale indicates how large the valid *FF* range is (contour lines for 0,

2.5, 5, 10, and 15 have been represented). Comparing the cases for $n = 2$, 4, and 6 with the region for the follower, it can be observed the drastic reduction in the number of solutions.

There are n different LTGs for an n-input LTG with weights are all of them equal to 1: those corresponding to $T = 1$ (n-input OR gate), 2, ..., n (n-input AND gate). Figure 20 shows the transistor form factor regions for different n- input LTGs and three specific $\{f_D, f_L\}$ configurations for the MOBILE circuit: {1, 0.8}, {1, 0.9}, and {2, 1.9}. *FF* regions are shown for LTGs until $n = 7$. For example, when $f_D = 1$ and $f_L = 0.8$, it is possible to implement a 2-input OR gate, but it is not possible to build a 3-input OR gate. This limit is raised until $n = 4$ if f_L increases until 0.9. For $f_D = 2$ and $f_L = 1.9$, there is no problem to implement OR gates until $n = 7$. The implementation of AND gates is more difficult because as it is shown on the figure (for each n, $T = n$), *FF* regions become narrower as n increases. For example, if $f_D = 2$ and $f_L = 1.9$, $FF \in \{0.53, 0.70\}$ to implement a 4-input AND gate.

Finally, LTGs with weights different to 1 can easily be treated because a weight of w can be considered as w weights of value unity. Figure 21a shows the feasible operation regions for the logic function $f(x, y, z) = x+yz$, depending on driver area factor f_D. This function is a LTG defined by a weight set of {2, 1, 1} and a threshold of 2. In Figure 21b the feasible operating region, depending on the difference, $\delta = f_D - f_L$. has been represented. Note that $\sum_{i=1}^{n} w_i$ is now 4.

VIII. Conclusions

DC operation in basic MOBILE circuits has been analyzed. Two problems able to produce an erroneous behaviour have been pointed out. The first one is related to the incorrect evaluation of inputs, at the rising edge of the bias voltage, and the second one, to the self-latching operation. An algebraic method to obtain relations between circuit and technological parameters in order to get correct operating circuits has been derived. Simulation results using complex models for the RTDs and transistors show an excellent agreement with the algebraic results. These results allow the exploration of the capabilities of an arbitrary RTD/HFET process to implement MOBILE circuits.

Appendix

In this appendix, we will perform a more precise calculation of the critical form factors in Section IV. The same considerations can be applied to develop more precise expressions to the bounds for both the MOBILE inverter and the complex logic gates.

A. *Incorrect Evaluation in the MOBILE follower*

Bound for the minimum *FF* can be refined taking into account that decision about a correct behaviour is taken for a critical bias voltage V_{bias}^{crit}, close to $2V_p$, and a V_{out} close to V_p,

$$f_L\, g\left[V_{bias}^{crit} - V_{out}\right] + FF^{min} i_{DS}\left[V_{in}^{high} - V_{out}, V_{bias}^{crit} - V_{out}\right] = f_D\, g\left[V_{out}\right] \qquad (26)$$

which must have a solution for $V_{bias}^{crit} - V_p \cong V_p$, and $V_{out} \cong V_p$. The mathematical model for the non-linear *I–V* characteristic of the RTD generally uses exponential and/or Gaussian functions. To obtain algebraic expressions, it is necessary to approximate the current of both, the load RTD and the transistor, by two-variable power series expansions. This solution is the correct one but it is not efficient because the high degree of the resulting expressions. We have solved the problem by fixing V_{out} to V_p, and performing second-order power series expansions about $V_{bias}^{crit} \cong 2V_p$ for the current through the load RTD and the transistor. Thus, the current $g[v]$ through the load RTD is

$$g[v] = g_0 + g_1\left(v - V_p\right) + g_2\left(v - V_p\right)^2 \qquad \text{for } v \cong V_p \qquad (27)$$

Given the bias voltage for the MOBILE circuits, the transistor is in its linear operating region (which ends approximately at $v_{DS} = 1V$ for the LOCOM technology). Transistor current can be approached by a first-order series expansion about $V_{bias}^{crit} \cong 2V_p$, and thus, Eq. (26) transforms in

$$f_L\left(I_p + g_1\left(V_{bias}^{crit} - 2V_p\right) + g_2\left(V_{bias}^{crit} - 2V_p\right)^2\right) + FF\left(i_0 + i_1\left(V_{bias}^{crit} - 2V_p\right) + i_2\left(V_{bias}^{crit} - 2V_p\right)^2\right) = f_D\, I_p \qquad (28)$$

which must have a solution for $V_{bias}^{crit} \cong 2V_p$. Parameters $g_0 = g\left[V_p\right] = I_p$, $g_1 = g'\left[V_p\right]$, and $g_2 = g''\left[V_p\right]$, are the series expansion coefficients of $g\left[v_{RTD}\right]$ around the peak voltage. Parameter i_0 is the previously calculated i_{DS1}, $i_1 = i_{DS}{}'\left[V_{in}^{high} - V_p, V_p\right]$, and i_2 is given by $i_2 = i_{DS}{}''\left[V_{in}^{high} - V_p, V_p\right]$. Eq. (28) is a second-order equation in $\left(V_{bias}^{crit} - 2V_p\right)$, which has a solution if the discriminant, Δ_{eval}, is greater than or equal to zero; that is,

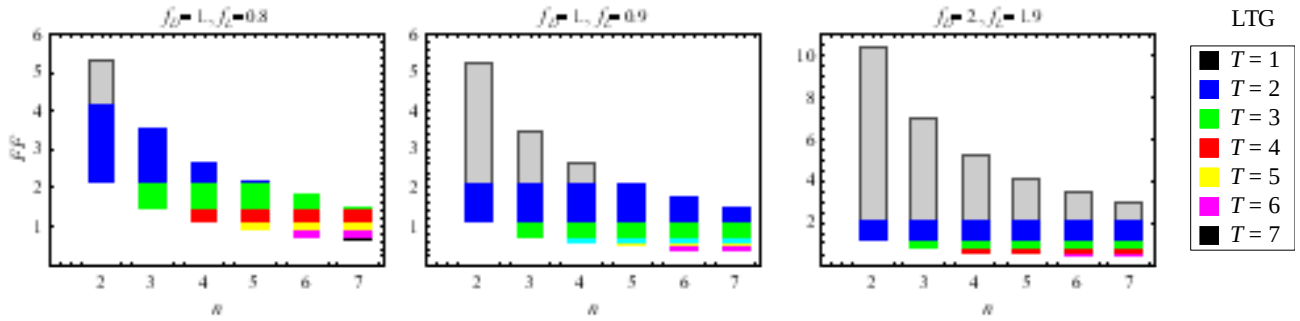


Figure 20. Feasible transistor form factor for *n*-input LTGs with different thresholds .

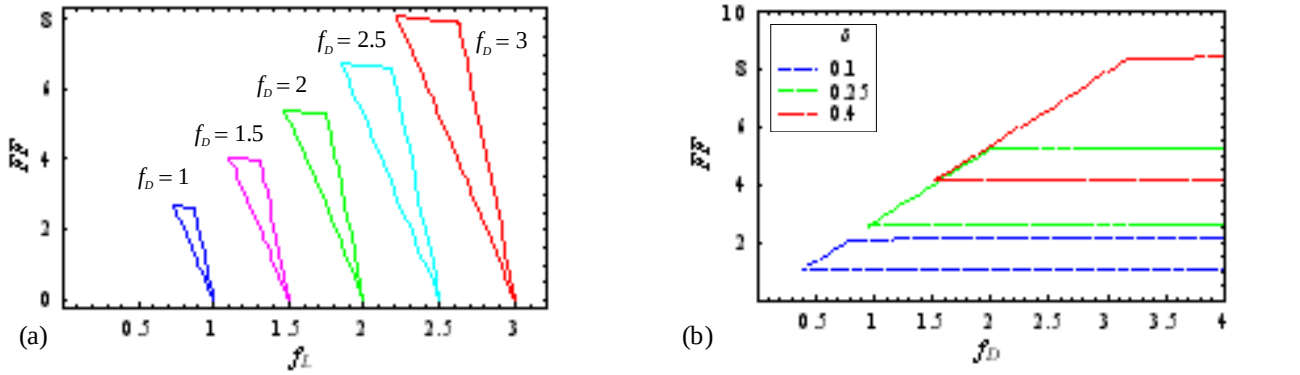


Figure 21. Feasible operation regions for the logic function $f(x, y, z) = x+yz$, (a) depending on driver area factor, f_D, (b) depending on difference $\delta = f_D - f_L$.

$$\left(FFi_1 + f_L g_1\right)^2 + 4\left(f_L g_2 + FFi_2\right)\left(I_p\left(f_D - f_L\right) - FFi_0\right) \geq 0 \quad (29)$$

Thus, an expression for the minimum value of *FF*, depending on area factors in the driver and load RTDs, can be obtained by equating Eq. (29) to 0,

$$FF^{min} = 2\left(f_L g_2 i_0 + \sqrt{f_L g_2\left(f_L g_2 i_0^2 - I_p\left(f_D - f_L\right) i_1^2\right)}\right) \Big/ i_1^2 \quad (30)$$

where $g_1 \cong 0$ has been supposed because we are close to the peak voltage, and i_2 has been eliminated because it does not introduce appreciable differences to obtain FF^{min}.

When $i_{DS}\left[V_{in}^{low} - V_p, V_p\right] \neq 0$, another incorrect operation is observed: a high voltage output is obtained when V_{in}^{low} is applied at the input. For this FF^{max}, a more refined analysis could be also performed following the previous considerations (Eq. (26) –Eq. (30)).

In the case of the MOBILE follower with $f_D = 1$ and $f_L = 0.7$, Eq. (6) provides $FF^{min} = 6.38$, Eq. (30) provides $FF^{min} = 6.13$, and through simulations, with the non linear and very complex expressions for the RTD *I*–*V* characteristics, $FF^{min} = 6.19$ has been obtained.

B. Self-latching disappearance in the MOBILE follower

More accurate solutions are obtained when current $g[v]$ is approached by second-order power series expansions about the peak voltage (Eq. (27)) and the $V_{bias}^{high} - V_p$ voltage, respectively. Thus,

$$g\left[v\right] = h_0 + h_1\left(v - \left(V_{bias}^{high} - V_p\right)\right) + h_2\left(v - \left(V_{bias}^{high} - V_p\right)\right)^2 \quad (31)$$

for $v \cong V_{bias}^{high} - V_p$, where parameters h_0, h_1, and h_2, are given by $g\left[V_{bias}^{high} - V_p\right]$, $g'\left[V_{bias}^{high} - V_p\right]$, and $g''\left[V_{bias}^{high} - V_p\right]$, respectively.

Modelling of the linear region for the real *I*–*V* characteristics of the LOCOM depletion HFET has been also approached by a first-order power series expansion of the expression for the real device about the point $V_{out} = V_p$. That is because both the bias and the input voltages have fixed values, $V_{bias} = V_{bias}^{high}$, and $V_{in} = V_{in}^{high}$, and the output value when solutions marked as ① and ②

collapse is approximately the peak voltage value. We have found no appreciable differences between the results with a first- and a second-order power series expansion for the transistor current. Thus, we have selected the easiest one,

$$i_{DS}\left[V_{in}^{high}-V_{out},V_{bias}^{high}-V_{out}\right]=j_0+j_1\left(V_{out}-V_p\right) \quad \text{for } V_{out}\cong V_p \tag{32}$$

where V_{out} is the source voltage in the transistor and parameters j_0 and j_1 are given by $i_{DS}\left[V_{in}^{high}-V_p,V_{bias}^{high}-V_p\right]$, and $i_{DS}'\left[V_{in}^{high}-V_p,V_{bias}^{high}-V_p\right]$, respectively.

Eq. (2) transforms in,

$$f_D\left(I_p+g_2\left(V_{out}-V_p\right)^2\right)=FF\left(j_0+j_1\left(V_{out}-V_p\right)\right)+ f_L\left(h_0+h_1\left(-V_{out}+V_p\right)+h_2\left(-V_{out}+V_p\right)^2\right) \tag{33}$$

which is a second-order equation in $\left(V_{out}-V_p\right)$. If the discriminant (Δ) of the solution is greater than zero, we have solutions marked as ① and ②. If it is equal to zero, both solutions collapse, and if the value is less than zero, we are in the situation of Figure 10a. Thus, the critical condition for the self-latching disappearance is obtained by equating this discriminant, Δ_{bist_I}, to zero,

$$\Delta_{bist_I}=-4\left(f_D g_2-f_L h_2\right)\left(f_D I_p-f_L h_0-FF\, j_0\right)+\left(f_L h_1-FF\, j_1\right)^2=0 \tag{34}$$

and an expression for the maximum value of *FF* depending on RTD area factors can be obtained from it as,

$$FF^{max}=\left(-2f_D g_2 j_0+f_L\left(2h_2 j_0+h_1 j_1\right)-2\sqrt{\left(f_D g_2-f_L h_2\right)\left(f_D p_1-f_L p_2\right)}\right)\Big/ j_1^2 \tag{35}$$

where constant p_1 and p_2 are given by $p_1=g_2 j_0^2+I_p j_1^2$ and $p_2=h_2 j_0^2+h_0 j_0 j_1+h_0 j_1^2$.

An additional simplification comes from considering that the contribution of h_2 parameter is negligible. So,

$$FF^{max}=\left(-2f_D g_2 j_0+f_L h_1 j_1-2\sqrt{f_D g_2\left(f_D p_1-f_L p_2\right)}\right)\Big/ j_1^2 \tag{36}$$

where p_2 is now $p_2=h_0 j_0 j_1+h_0 j_1^2$.

For the devices in LOCOM technology, the values for g_0, g_2, h_0, h_1, h_2, j_0, and j_1 are: 2095.69μ*A* (I_p), – 66403.1μ*A*/*V*^{2}, 349.16μ*A*, 716.06μ*A*/*V*, 8159.72μ*A*/*V*^{2}, 179.069μ*A*, and –447.081μ*A*/*V*, for a bias voltage of $V_{bias}^{high}=0.8V$ and an input voltage of $V_{in}^{high}=0.65V$.

In the case of the MOBILE follower in Figure 10, with $f_D=1$ and $f_L=0.7$, Eq. (35) gives a bound for the transistor size of $FF^{max}=10.90$. This bound is evaluated as $FF^{max}=10.34$ when Eq. (9), is employed. Through the DC solution from Eq. (2), a $FF^{max}=10.89$ is obtained.

C. Existence of solutions in the MOBILE follower

DC correct operation is possible if (Eq. (30) and Eq. (36)),

$$2\left(f_L g_2 i_0+\sqrt{f_L g_2\left(f_L g_2 i_0^2-I_p\left(f_D-f_L\right)i_1^2\right)}\right)\Big/ i_1^2 \le FF \le \left(-2f_D g_2 j_0+f_L h_1 j_1-2\sqrt{f_D g_2\left(f_D p_1-f_L p_2\right)}\right)\Big/ j_1^2 \tag{37}$$

i.e., if the ratio of area factors (f_D/f_L) verifies:

$$\frac{FF^{min}}{FF^{max}}=\frac{2j_1^2}{i_1^2}\frac{g_2 i_0+\sqrt{g_2\left(g_2 i_0^2-I_p\left(\frac{f_D}{f_L}-1\right)i_1^2\right)}}{h_1 j_1-2\frac{f_D}{f_L}g_2 j_0-2\sqrt{\frac{f_D}{f_L}g_2\left(\frac{f_D}{f_L}p_1-p_2\right)}}<1 \tag{38}$$

Additionally, we can consider if a self-latching disappearance problem for the low input voltage introduces some modification to this calculations. From Section IV.B, we obtained that such a problem appears when $f_D/f_L>I_p/g\left[V_{bias}^{high}-V_p\right]$. This number uses to be greater than the limit given by Eq. (38). Thus, before this problem appears, the MOBILE follower does not present a correct operation.

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