Dedicated Hardware IP Module for Fingerprint Recognition

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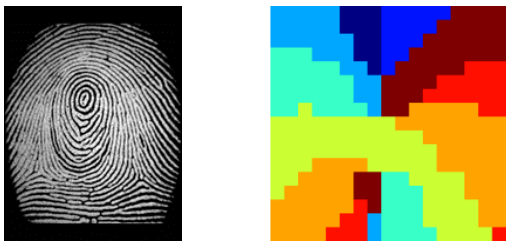
***Abstract*—This work presents a dedicated hardware IP module for fingerprints recognition based on a feature, named QFingerMap, which is very suitable for VLSI design. FPGA implementation results of the IP module are given. A demonstrator has been developed to evaluate the IP module behavior in a real scenario.**

Keywords— Biometrics; Fingerprint recognition; IP module; FPGAs

I. INTRODUCTION

Biometric solutions are widely employed for individual recognition. In particular, fingerprint recognition is widely accepted for its distinctiveness and ease of use. Most of fingerprint recognition systems carry out complex algorithms that have to be implemented in hardware platforms with high computational resources to offer real-time performance. To include fingerprint recognition in small devices such as wearable devices, car keys, etc., dedicated hardware solutions are demanded. Complexity of the algorithms should be reduced to offer real-time response with small size and power consumption.

Fingerprint features can be classified into three levels [1]. The feature is more local, and the algorithm to extract it is more complex, as higher the level is. Minutiae, which are level-2 features, are typically employed in recognition systems. Level-1 features, which are more global, are usually extracted previously to aid the extraction of level-2 features. The use of level-1 features allows reducing considerably the algorithm complexity. Distinctiveness can be maintained if the user collaborates to be recognized and multi-biometrics is employed (for example several samples of several fingers are provided to the system).



(a) (b)

Fig. 1. (a) Fingerprint image from the public database FVC2002 DB1 and (b) its associated QFingerMap.

Recently, a new level-1 feature called QFingerMap (QFM) has been presented [2]. Since it offers a good trade-off between ease of VLSI design and capability of recognition, an IP module has been designed to extract it from a fingerprint image. To evaluate its performance in a real scenario, a FPGA-based demonstrator has been developed.

The paper is organized as follows. The IP module architecture and FPGA implementation results are described briefly in Section II. Section III summarizes the features of a demonstrator that uses the designed module. Finally, conclusions are given in Section IV.

II. IP MODULE DESCRIPTION

The module extracts a QFM from a fingerprint image. The QFM is extracted from a window centered at the convex core (a singular point) of the fingerprint. The IP module is formed by several blocks connected in cascade which process serially the fingerprint image until the QFM is extracted. These blocks are the following [2]-[3]:

- Directional image extractor: extracts a directional image from the fingerprint by assigning a symbol to each pixel. The symbol represents the one out of 8 representative direction intervals which the ridges at that pixel belong to. It is calculated by applying two Sobel masks to obtain horizontal and vertical gradient values around the pixel and evaluating the relation between both gradient values (Fig. 1b illustrates each symbol with a color).
- Smoothing process: maintains the symbol with the highest number of occurrences within a 27 x 27 window centered at the current pixel. The result is a segmented directional image with homogeneous direction regions (as illustrated in Fig. 1b).
- Singular points extraction: identifies possible convex cores using several 9 x 9 pattern masks.
- Singular point post-processing: detects the convex core, eliminating false cores.

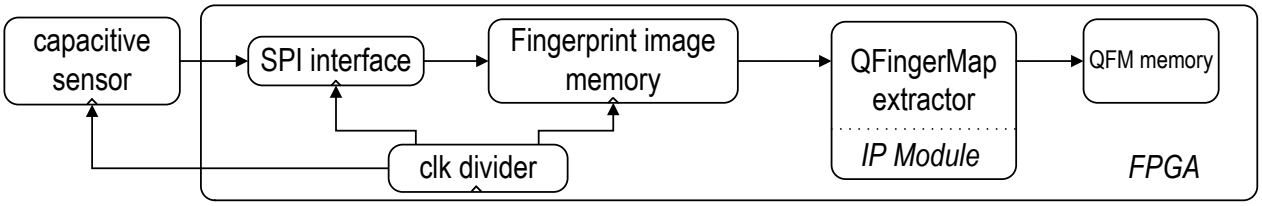


Fig. 3. Scheme of the demonstrator.

- Singular window extraction: extracts a 129 x 129 window centered at the convex core detected.
- QFM extraction: down-samples the singular window to 17 x 17 symbols, represented by 867 bits.

All the blocks were described in Verilog hardware description language. The IP module employs a generic architecture that can be implemented in both a digital integrated circuit and a FPGA. The implementation results of the module in a 45-nm FPGA are shown in Table I. The IP module can reach a maximum frequency of 116.41MHz. For a whole image of 152 x 200 pixels the time needed to extract the QFM is 0.26ms. The total power consumption estimated is 75mW. The operation frequency can be smaller maintaining real-time response, which would reduce power consumption.

TABLE I. IMPLEMENTATION RESULTS IN A 45-NM FPGA

	Resources			
	Occupied slices	***Slice registers***	***Slice LUTs***	***RAM Kbits***
IP module	744	1945	2158	270.4

III. DEMONSTRATOR

A demonstrator has been developed using a commercial fingerprint sensor and a general-purpose FPGA board. A photograph of the demonstrator is shown in Fig. 2. The module is employed in the registration and recognition stages to extract one or several QFMs. Fig. 3 shows a schematic of the demonstrator.

The sensor is a compact capacitive CMOS area sensor with a size of 10.64mm x 14mm and an ergonomic guidance frame for improving the placement of the finger. It captures an 8-bit greyscale image with a resolution of 152 x 200 pixels and transmits it by a SPI interface at up to 32MHz. It admits supply voltage from 2.5V to 3.3V and includes a 30kV ESD protection. The FPGA board contains general-purpose input-outputs (GPIOs) to which the sensor was connected. The architecture described in Section II was implemented in the FPGA together with the SPI protocol and a dedicated SRAM memory where the fingerprint image is stored. The image is then read pixel by pixel from the memory and each 8-bit pixel is the input to the module that extracts the QFM. The FPGA board can work at a maximum frequency of 48MHz but a block fixes it to 24MHz to adapt the operation frequency of both the FPGA and the sensor.

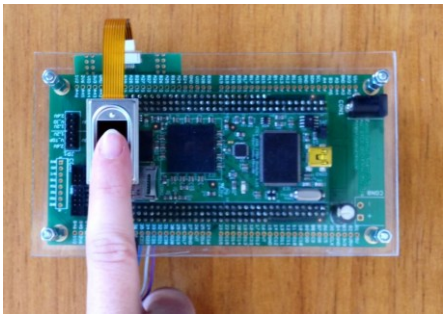


Fig. 2. Photograph of the demonstrator.

The FPGA board also includes an USB microcontroller so that the demonstrator can be connected via USB to a PC. The PC is used to download the program files in the FPGA and to visualize results from the demonstrator.

IV. CONCLUSIONS

A dedicated hardware IP module for fingerprint recognition has been designed in Verilog. It employs simple logic and arithmetic operations so that allows very low power consumption and rapid extraction of the fingerprint feature. The module has been implemented in a FPGA board connected to a fingerprint sensor and to a PC, so that the IP module can be tested in a real scenario.

ACKNOWLEDGMENT

This work was partially supported by TEC2014-57971-R, TEC2011-24319, IPT-2012-0695 and RTC-2014-2932-8 projects from the Spanish Government (with support from FEDER). M.C. Martínez-Rodríguez is supported by FPI fellowship program for Ph.D. Students from Spanish Government. The work of R. Arjona has been supported by a Post-Doc Fellowship from the Regional Government of Andalusia. P. Brox is supported by 'V Plan Propio de Investigación' from the University of Seville.

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