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Achieving Energy Efficiency in Analogue and Mixed Signal Integrated Circuit Design

E. López-Morillo, F. Márquez,
T. Sánchez-Rodríguez, C.I. Luján-Martínez and F. Munoz
Electronics Engineering Department, Universidad de Sevilla
Spain

1. Introduction

Wireless communications are one of the major successes of the engineering over the past two decades. The progress made in this area has not only produced a huge technological growth, but also a great impact at social and economical level. In fact, the possibility of being connected anywhere at any time has radically changed people habits.

The evolution of wireless communications is obviously linked to the power consumption of devices, which also continues increasing due to the growing amount of data and transmission speed required by the new communication standards. In contrast, the energy available in portable batteries does not grow at the same rate, improving only their capacity in a 10% every two years (Shahab, 2010). This leads to an increasingly gap between power needs and battery capacity. Therefore, energy efficiency of electronics systems has become a crucial factor to maximize the lifetime of the available batteries and one of the most important research topics in integrated circuits design in recent years.

The increase in power consumption is less dramatic for the digital domain, since it is partially compensated, as the technology scales-down, by the reduction of the supply voltage and the geometrical dimensions of a single device. The main reason for decreasing the supply voltage in modern CMOS technology is to avoid the possible breakdown of the transistors due to the extremely thin oxide. For a CMOS logic gate, e.g. an inverter, the simplest logic cell, the power consumption can be expressed as:

$$P = C_L \cdot V_{dd}^2 \cdot f \tag{1}$$

where C_L is the load capacitor at the output of the inverter, V_{dd} is the supply voltage and f is the operating frequency. Despite of the ever-increasing working speed, the power consumption in CMOS logic circuits is reduced as the supply voltage and geometry sizes scale down. For instance, the power consumption of microprocessors is reduced in a 50% for each technology generation if the supply voltage scales down in a 30% (Bokar, 1999) and according to Gene's law, the power dissipation in embedded DSP processors will be decreased by a half every 18 months. As it will be explained later, this relative "low cost" of digital computation in terms of power dissipation, supports the idea of maximizing the

digitization level of an electronic system not only to dismiss the fabrication costs but also as a way of reducing its power consumption.

The System-On-Chip (SoC) trend is the main cause for the analogue and mixed-signal and digital integrated circuits (ICs) to be fabricated on the same wafer. This fact eventually requires the analogue and mixed-signal ICs to be fabricated in modern CMOS technologies to save cost. However, several challenges are encountered in the scaling-down of the CMOS technologies for analogue designs with not much clear advantages (Yao et al. 2006). The threshold voltage is not scaled as aggressively as the supply voltage to avoid leakage current in transistors. As a consequence, the available signal swing is lower and a reduction of the noise of the circuit to maintain the same dynamic range is required. Reducing thermal noise increases the power consumption of analogue and mixed-signal circuitry. Particularly, in discrete time applications, reducing circuit noise means increasing the capacitances which results in higher power consumption in order to maintain the same operation speed. Additionally, as technologies are scaled down, the output resistance of the MOS transistors decreases resulting in lower op-amp gain. In order to increase the gain, it is required to use either cascode transistors or cascade amplifiers, increasing the complexity of the circuits. These solutions worsen the swing problems and increase the power consumption.

The analogue-to-digital (A/D) converter is one of the most important and power consuming building blocks in modern electronics systems. Moreover, A/D converter (ADC) requirements tend to be more stringent as the analogue functionality is moved to the digital domain. In recent years, the demand of more and more performance (speed and/or resolution) within a limited energy budget has pushed the IC research community to put a huge effort into increasing the energy efficiency of the ADCs. For instance, data collected from the literature over the last years indicate that the power efficiency of ADCs has improved by a factor of two every two years (Murmann, 2008), allowing some designs to become portable, such as those for biomedical applications. Due to this fact, a special attention to ADC architectures will be taken in some sections of this chapter, as they are the most limiting blocks in recent systems.

In portable bio-signals acquisition micro-systems, the power consumption requirements are taken to the extreme. For instance, medical implant devices, such as modern pacemakers, require extremely low power consumption (about 10-40 μW) in order to operate up to 10 years or more using a small non-rechargeable battery (Yeknami et al., 2010).

In wearable electronics for biomedical monitoring applications, extreme miniaturization is required and this will limit the battery size and power draw. Wearable electroencephalography (EEG) is a good example of such a power-limited system. EEG records the voltage between electrodes placed on the scalp and provides a non-invasive interface to the brain. Discrete, lightweight and comfortable devices are essential for user acceptance in applications such as epilepsy diagnosis (Casson & Rodriguez-Villegas, 2011). Long-term EEG monitoring of patients in their daily environment is generally required for epilepsy diagnosis. As these types of medical tests can take long periods of time, ultra-low power and miniaturized electronics systems need to be developed.

Another interesting arising application is the Energy Autonomous Sensors (EAS) which will represent a revolution in the use of wireless technologies, such as wireless sensor networks, in the ambient intelligence paradigms. Exploiting this continuously improving energy

efficiency and advances in energy harvesting, miniaturized battery-less sensors that do not need to be recharged for their whole operational life are becoming possible nowadays (Belleville et al. 2010).

In the second section of the chapter, we give a summary on the most common techniques that have been used by the IC research community in the last years to reduce the power consumption in analogue and mixed signal circuits. Several references to relevant works where each technique is detailed are provided. The following four general categories have been considered to classify the presented techniques:

- Biasing point optimization.
- Digitally assisted techniques.
- Analogue circuitry simplification.
- Efficient use of biasing.

The authors' main contribution in this chapter is described in the third section. Some of the techniques commented on section two will be illustrated with some actual designs, a micropower channel filter for an Ultra Low Power Bluetooth (ULPBT) receiver and a compact continuous time (CT) Sigma Delta (ΣΔ) modulator for a sensor interface powered by a passive Radio Frequency Identification (RFID) front-end.

2. Power reduction techniques in analogue integrated circuit design

2.1 Biasing point optimization

CMOS technology is used in most of the electronic devices because of its high density of integration. Traditional analysis of MOS circuits is often based on the assumption that every transistor is operating in the strong inversion region, although signal amplification can be done in any of the three inversion regions. The better knowledge of the strong inversion models and equations is one of the main reasons for its use.

Although simple MOS amplifier stages have much higher bandwidths in the strong inversion region, parameters like voltage gain, power dissipation, white noise, and distortion can be optimized by operating in the weak or moderate inversion regions (Binkley et al., 2003; D. J. Comer & D. T. Comer, 2004a, 2004b; Vittoz, 1994). Most often operation in weak inversion is synonymous to minimum power operation (Markovic et al., 2010).

There are several advantages that make operating in weak inversion an interesting issue:

1. It is possible to achieve higher gains (Allen & Holberg, 2002; D. J. Comer & D. T. Comer, 2004; Gray et al., 2001; Tsividis, 2002).
2. Low power consumption can be achieved as the quiescent drain current needed for this level of inversion is quite low.
3. Lower distortion compared to the strong inversion region (D. J. Comer & D. T. Comer, 2004a, 2004b).
4. Higher output resistance of the devices of the input stage due to the low drain currents of transistors operating in weak inversion region.

But there are also some disadvantages when designing in weak inversion region. The most important is the reduction in circuit bandwidth and therefore in frequency operation,

although, they can be maximized if some issues are taken into account. In a single transistor, the maximum operating frequency is determined by the gate capacitances, C_{GS} and C_{GD}. In order to maximize the device bandwidth, these capacitors need to be kept as small as possible which is achieved with minimum transistor width and length.

In order to improve MOS modelling techniques, a large amount of research has been done until this moment regarding transistor MOS operation at the three levels of inversion (Binkley et al., 2003; Vittoz, 2009). All this research has been quite useful to define accurate equations for the weak inversion region, as for instance the EKV model (Enz et al., 1995).

Many analogue circuits have been designed using weak inversion region, such as operational transconductance amplifiers (Chanapromma et al., 2010), filters (Corbishley& Rodríguez-Villegas, 2007; Omeni, 2005), ADCs (Farshidi&Alaei-sheini, 2009; Ou et al., 2006), etc., all of them performing very low power consumption.

2.2 Digitally assisted techniques

Recent CMOS technologies open an interesting possibility for ADC design by translating analogue precision problems to the digital domain, where higher frequency signals can be processed at much lower energy cost. The additional complexity of digital processing circuits can be compensated by relaxing the analogue requirements and, as a consequence, lowering the total required energy per conversion.

Digitally assisted techniques have become a major concern in ADC design nowadays. Some traditional A/D conversion architectures (such as Successive-Approximation-Register-based -SAR- and ΣΔ ADCs) can be considered digitally assisted architectures since they make extensive use of CMOS digital logic. On the one hand, oversampling is a widely implemented technique in ΣΔ converters with high energy efficiency. As modern technologies allow a more efficient digital data processing, there are trends to extend these techniques to other Nyquist ADC architectures to decrease the required energy per conversion. On the other hand, there are a great number of approaches based on compensating errors generated in the analogue parts (such as mismatch and offset of the comparators) by means of implementing redundancy-based architectures and digital calibration methods instead of very power-demanding analogue compensation techniques.

In next sections, some of the most interesting trends involving digitally assisted techniques will be explained.

2.2.1 Digital calibration and redundancy

As it was commented before, the analogue circuits suffer some difficulties due to the MOSFET size reduction. One of the most applied techniques to compensate these errors is to introduce some digital calibration schemes, usually employing redundancy-based ADC architectures.

As an example, a widely employed architecture in wireless communication systems to reach fast operation at very high frequencies is the Flash ADC. Traditionally, these schemes have been characterized by using very power-demanding topologies with multiple gain stages for offset compensation. Actually, there are different design trends, mainly based on “relaxed precision” comparators redundancy combined with digital error compensation of mismatch

and offset deviations. A first approach is illustrated in (Flynn et al., 2003), where a bank of comparators with a factor-four redundancy is implemented with no special care about their offset or mismatch properties, drastically decreasing the consumption in the analogue blocks. In an initial calibration phase, the most suitable comparator for every input range is selected and the rest are powered down, with no contribution to power consumption of the system. Another example is a Flash ADC using process variations to generate the input references from random comparators offsets (Sundström & Alvandpour, 2009), whose resolution and input signal range are optimized by means of digital calibration.

A great variety of similar approaches combining redundancy and digital error correction methods can be implemented in a similar way. For instance, there are redundancy-based ADC with a current trimming DAC for error compensation to minimize the input-referred offset of the comparators (Park et al., 2007) or partially redundant schemes -with only some additional comparators- with background calibration implemented during conversion, as shown in (Kijima et al., 2009).

2.2.2 Time-Interleaving

Time-Interleaving (TI) technique is a method based on the concept of running a system with M parallel channels by taking just one sample alternatively from each one. As a consequence, the ADC as a block would operate at an M times higher frequency than each individual channel. This allows reaching higher operation frequencies at no additional cost of analogue power consumption. However, mismatch between channels (usually the most limiting factors are offset and gain mismatch and clock skew errors) will reduce the resolution of the system. It is possible to compensate these errors using digital calibration or post processing.

An example of this technique can be found on (Cao et al., 2009), where a 6-bit Time-interleaving ADC working at 1.25 GS/s without any off-line calibration, error correction or post processing has been designed. The proposed architecture has been implemented using a two time-interleaved SAR ADCs topology combined with flash ADC sub-conversion processes, allowing a reduction from 65 to 6 comparators and lowering its power consumption well below typical values for state-of-art flash ADCs without digital calibration techniques. Another example of a Time-interleaving 7-bit SAR ADC working at 2.5 GHz is described on (Alpman et al., 2009). The proposed scheme is based on 16 parallel ADC running at 1.25GS/s with two additional ADC to allow background calibration to compensate offset and mismatch errors. Timing calibration can be done by means of adjusting a programmable delay line, which can be done during the packet header of the communication standard used for data transmission.

2.2.3 Time-domain processing

With the evolution of CMOS fabrication processes, higher bandwidth is available for analogue designers. Therefore, systems that process signals in the time domain can benefit of the improved speeds to achieve larger resolutions. Traditional time-based architectures, such as dual-slope converters, can achieve very high resolution at the cost of large conversion times. Nowadays, as technology scales down, such time-based architectures are not only limited to low speed applications.

A good example of achieving high-energy efficiency using time-domain processing and an extensive use of digital logic is the ADC architecture presented in (Yang & Sharpeshkar, 2005, 2006). They propose a current-mode ADC that works like a pipelined converter which performs the residue amplification and subtraction in time domain, without the use of conventional amplifiers. The ADC is made of only two matched capacitors, a comparator and a switched reference current source controlled by a digital state machine. Since only a single comparator and one reference current source are used for the entire conversion process, the ADC consumes minimal power and avoids inaccuracies due to gain errors and offsets.

In (Jimenez-Irastorza et al. 2011) an interesting Time-to-Digital converter (TDC) achieving high energy efficiency is presented. It implements a recursive successive approximation algorithm in the time domain to perform the conversion with a low-voltage fully digital circuitry and very low power consumption.

Another example of a simplified scheme lowering power consumption in a ΣΔ ADC is presented in (Colodro & Torralba, 2008). This paper presents a CT ΣΔ modulator where the N-bit Flash quantizer is replaced by an asynchronous comparator. As a result, the feedback signal is coded in the time-domain as a PWM signal.

2.3 Analogue circuitry simplification

In previous sections, the way of successfully translating most of the analogue complexity to the digital domain by applying some techniques has been discussed. Another complementary approach to improve power efficiency could be based on the design of simplified analogue sub-circuits, allowing higher speed operation and power consumption decrease in basic building blocks. These techniques would include not only system level designs strategies but also analogue basic topologies that can be applied to many different architectures. In this way, higher energy efficiency can be obtained also at SoC level.

In the next sections, a review of some of the most interesting approaches for circuitry simplification will be provided.

2.3.1 Switched Op-amp and Op-amp sharing

Op-amps are usually one the most power-consuming basic analogue blocks; therefore, a feasible option to reduce power consumption is to minimize their number in designs. Many switched-capacitor circuits need an active op-amp only during one clock phase, the amplification phase. As a consequence, there are two widely used techniques to reduce the number of active op-amps (Kim et al, 2006); one shares op-amps between successive stages and the other switches them off during the sampling phase.

Op-amp sharing is a technique based on using the op-amp for two adjacent stages in successive alternative phases. This technique is widely implemented in pipelined ADCs (Hashemi & Shoaei, 2007; Sasidhar, 2009), but can be applied to any op-amp based topology.

Two-stage Class-A switched-op-amp (SO) is the most popular solution for low power switched capacitor (SC) sigma-delta modulators with ultra low supply voltage conditions. The SO saves about 30%-40% of the total power since its output stage is just turned off at the integrating phase. For instance, an application to implement a 4th order band-pass ΣΔ

modulator using switched op-amps is presented in (Kuo & Liu, 2004). While a classic op-amp topology would require four integrators working in two phases, in the proposed architecture the ΣΔ modulator is implemented only with two switched op-amps, drastically reducing the power consumption. To further increase efficiency, class AB output and input stages can be used in the op-amp implementation. In (Wang et al., 2009) by turning off the entire SO together, instead of only the output stage, with its common mode feedback (CMFB) circuit, the power consumption of the SO can be reduced about 50%.

2.3.2 Op-amp less

The traditional way of designing analogue circuits relies on high gain op-amps in negative feedback loops. As it was stated before, the op-amp power consumption directly impacts in the overall system. Recently, there is the trend of replacing the op-amps by more power efficient blocks such as comparators, inverters or simple structures based on local feedback. In this section, some of these approaches are described to illustrate this trend.

CBSC (Comparator Based Switched Capacitors) and zero-crossing detector based circuits

The CBSC technique was firstly proposed in (Fiorenza et al., 2006) and is applicable to any traditional op-amp based SC circuit. This technique consists in replacing the op-amp by a comparator and one or more switched current sources. As the author explains, the power reduction relies in the fact that a CBSC circuit senses the virtual ground while in traditional op-amp based SC circuit the virtual ground is forced which is less energy efficient.

Several ADC prototypes have demonstrated the practical application of CBSS and its potential high energy efficiency. In (Shin et al. 2008), a 10 bits pipelined ADC based in zero-crossing detector fabricated using 65nm CMOS technology is reported.

Another pipelined zero-crossing detector based is presented in (Brooks & Lee, 2009). It achieves 12 bits of ENOB sampling at 50MS/s with high power efficiency indicated by a FOM of 88fJ/step.

Inverter based ΔΣ modulators

This technique is another approach in which the op-amp is replaced by a simple inverter, which can be considered as a very simplified amplifier architecture. In the past, inverters had been applied to SC circuits as low-performance amplifiers for micropower consumption (Hosticka, 1979). In spite of the limited performance of inverters compared with op-amps, inverters attract attention again to be used in deep submicron technologies. This is because of their ability to operate with very low supply voltages. Recent works have demonstrated that inverter-based design techniques can be applicable to high-performance SC circuits in aggressively scaled CMOS technologies.

For example, (van Veldhoven et al., 2008) present a hybrid ΣΔ modulator fabricated in 65nm CMOS technology. It uses a highly digitized architecture with a five bits quantizer and a digital filter in order to reduce the complexity of the feedback DAC. A first order analogue loop filter (implemented using inverters) reduces the analogue parts to the minimum, so the area and power consumption are drastically reduced.

In (Chae & Han, 2009) the inverter behaviour used as an extremely simple amplifier is explained in detail. Three discrete time (DT) ΔΣ modulators of second and third order

completely implemented by means of inverters are presented in this work. All of them achieve high dynamic range under low voltage supply conditions with a power consumption that places the best of them in the state-of-the-art nowadays.

Simple analogue cells based in local feedback

Simple local feedback can lead to substantial enhancement of the performance with low cost in terms of noise, area and power consumption as it is usually implemented by a simple structure.

One good example is the structure called the Flipped Voltage Follower (FVF), a popular building block that relies on the local feedback idea. It was proposed in (Carvajal et al., 2005) to improve the performance of the classical voltage follower by means of local feedback.

A very commonly implemented basic cell in analogue microelectronics is the voltage follower (Fig. 1a). However, the gate-to-source voltage (v_{GS}) of the transistor acting as the follower (M1) depends on the output current, which leads to a high distortion for large output current variations. Some solutions have been proposed to address this problem (Sánchez-Sinencio & Silva-Martínez, 2000), (Barthélemy & Kussener, 2001), (Carvajal et al., 2005). The FVF is the basic cell made up by transistors M_1 and M_2 and the current source I_B shown in Fig. 1b. The local feedback implemented by transistor M_2 keeps constant the current through transistor M_1; this decreases the output impedance increasing the linearity of the current copy and in spite of output current variations.

A modified version of the FVF was proposed in (Luján et al., 2011) showing a better performance for large excursions of the input signal up to 10MHz and allowing a reduction in the quiescent power consumption of about 15 times when comparing with the classical solution, for the same linearity performances.

The idea of using local feedback to maintain the linearity requirements, while the power consumption is decreased, can be extended to more complex systems such as ADCs. One example of this is the CT ΣΔ modulator described in the section 3.2 of this chapter. A low power extremely low area CT ΣΔ modulator implementation based on the FVF is explained.

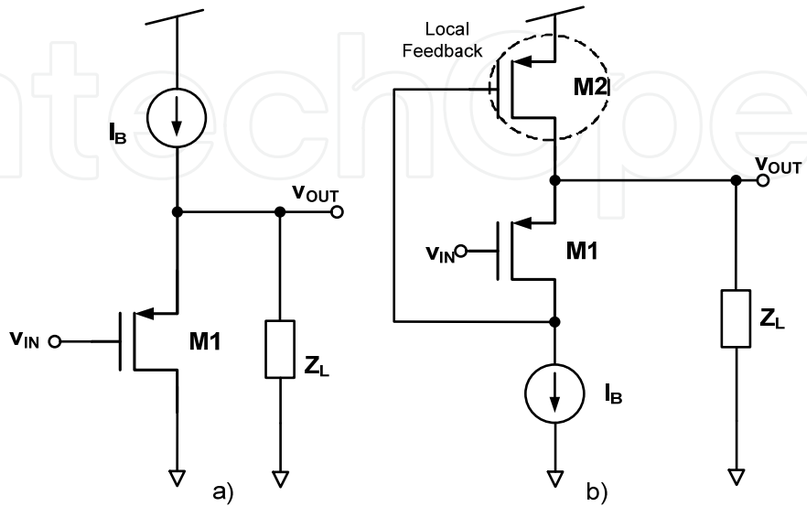


Fig. 1. Voltage followers: a) classical solution and b) FVF.

Other op-amp-less approaches

Another example of a simplified op-amp-less architecture is the ADC array (Draxelmayr, 2004). Using parallelism to exploit the power efficiency of simple structures, a 6-bit ADC working at 600 MS/s based on eight SAR ADCs using a charge redistribution architecture is proposed. A power consumption of only 10 mW is obtained with very simple analogue circuitry (capacitors, switches and a comparator are sufficient) and no need for "precision" analogue blocks, like high gain op-amps.

In (Van der Plas, 2006) a 4-bit flash scheme with a comparator based simplified structure is proposed to design a high speed low-power ADC. Its structure is reduced to save power by removing all the non essential blocks: Track &Hold, preamplifiers, reference ladder and bubble error correction. A comparator circuit combining sampling, amplification and reference level generation is used to implement the ADC obtaining a power consumption of only 2.5 mW.

2.4 Efficient use of biasing

Charge transfer in class-A op-amp circuitry is inherently inefficient; the amplifier is biased with a constant current, while delivering on average only a small fraction of this current to the load. In this section, a more efficient use of biasing is discussed and various approaches adopted to solve this problem are commented.

2.4.1 Dynamic and adaptive biasing

In the last decades, several approaches have been proposed to optimize the efficient use of biasing towards the challenge of minimizing the power consumption-performance ratio. Most of them can be classified according to the concepts of dynamic and adaptive biasing. The term *dynamic biasing* was first coined in (Copeland & Rabaey, 1979), where a method to reduce the power consumption by taking advantage of having several clock phases in a SC integrator was proposed. This method is valid for all those circuits where there is a capacitive feedback between the output and a virtual ground.

Since then, the concept of dynamic biasing has been extended, in general, to those approaches in which a block or part of it is connected or disconnected according to the received input power. An example of this technique is proposed in (Ozun et al., 2006) where a parallel combination of transconductors is used, increasing the power consumption only if very low noise is required.

At the same time, the term of *adaptive biasing* (Degrauwe et al., 1981) has also become popular. It is usually referred to a continuous time change in the biasing according to the input. One of the most important adaptive biasing techniques is the class AB operation. In this technique, the slew rate limitation is tackled by boosting automatically dynamic tail currents for large inputs, keeping a well-controlled low quiescent current (Degrauwe et al., 1981) , (Callewaert & Sansen, 1990), (Castello & Gray, 1985), (Tan & Chen, 2007), (Klinke et al., 1989), (Harjani et al., 1999).

Several schemes can be found in the literature for class AB operation amplifiers. Most of them require of additional circuitry, which increases both power consumption and active area. Often they also imply additional parasitic capacitances to the internal nodes

(Degrauwe et al., 1981), degrading the small signal performance of the circuit which is already poor due to the low quiescent current. In some cases, the stability issues get worse due to the use of positive feedback or structures that are sensitive to variations in process and environmental parameters (Callewaert & Sansen, 1990), (Klinke et al., 1989). Although other contributions consider negative feedback (Harjani et al., 1999), the required additional amplifiers to implement the feedback loops lead to complex designs. Another weakness of the tail current boosting topologies is that usually are not suitable for low voltage applications as in (Castello & Gray, 1985) due to the stacking of gate to source voltages.

Recently, some topologies based in the FVF (López-Martín et al., 2009) or using "Quasi" Floating Gate (QFG) techniques have been proposed (Ramírez-Angulo et al., 2006), while the first one offers simplicity of design and suitability for low-voltage operation simultaneously to high efficiency; the second one also minimizes the additional circuitry required just substituting a normal MOS transistor by a QFG MOS.

Class AB operation can be applied to the input, to the output or both. This last option is known as superclass AB operation (López-Martín et al., 2005). The concept of class AB operation is so spread that today we can talk, for instance, about Class AB DACs (Seo et al., 2009), Sample & Holds (Sawigun & Serdjin, 2011) and multipliers (Sawigun & Serdijn, 2009) among others.

2.4.2 Assisted op-amp and helper techniques

Instead of removing op-amps, as it has been explained in section 2.3.2, a less aggressive technique consists in keeping the op-amp but adding helper circuits that increase the energy efficiency by relaxing the requirements for the op-amp gain or bandwidth.

For instance, in (Musah et al. 2007) the concept of correlated level shifting (CLS) is introduced. Correlated double sampling (CDS) technique can be used to reduce the error caused by finite open-loop gain, but it limits the maximum speed and its performance is poor near the rails. This makes it unsuitable for low voltage conditions, since the voltage swing is reduced too much. CLS is a SC technique similar to CDS, which also decreases the errors due to finite open-loop gain and allows rail-to-rail operation increasing the "distortion-free" swing. A third clock phase is needed but the settling time is about the same, so it does not have impact on the circuit speed. Open-loop gain requirements can be relaxed for a given resolution, leading to power consumption saving.

Another approach of op-amp helper is the assisted op-amp technique proposed in (Pavan et al. 2010). It is well known that the op-amp in the first integrator of high resolution single-bit CT ΣΔ modulators has stringent slew rate requirements, increasing power dissipation. In CT single bit ΣΔ modulators the feedback DAC injects a very high frequency current signal at the virtual ground node of the op-amp which the first integrator is implemented with. If the op-amp is not fast enough, this high frequency signal produces strong variations at the virtual ground node which result in distortion. The conventional way of addressing this issue is to bias the op-amps with large currents, so that the bandwidth and slew rate of the op-amp are enhanced. This work introduces the "assisted op-amp" integrator, which offers a way of relaxing the speed specifications of the op-amp in the first integrator, achieving low distortion operation with low power consumption.

3. Applications examples

In this section, two examples of design which make use of some of the previous power reduction techniques are presented. Firstly, the design of an active-RC channel filter for ULPBT applications is explained. It achieves micro-power consumption by using an efficient class-AB op-amp biased in the weak inversion region. Then, the design of an efficient op-amp less implementation for CT ΣΔ modulators is described. In the proposed implementation, the op-amp is replaced by the compact local feedback structure explained in section 2.3.2.

3.1 Micropower active-RC channel filter for a Zero-IF Ultra Low Power Bluetooth receiver

In the case of the low-power RC filter and in order to reduce the power consumption, an adaptive biasing technique has been used. Specifically, a new topology of class-AB op-amp has been used so that the current consumption is adapted to the output requirements. The designed filter will be used in the ULPBT receiver based on a Zero-IF architecture like the one shown in Fig. 2. The main challenge of this design is the implementation of an efficient low-pass channel filter meeting the stringent demands of the receiver.

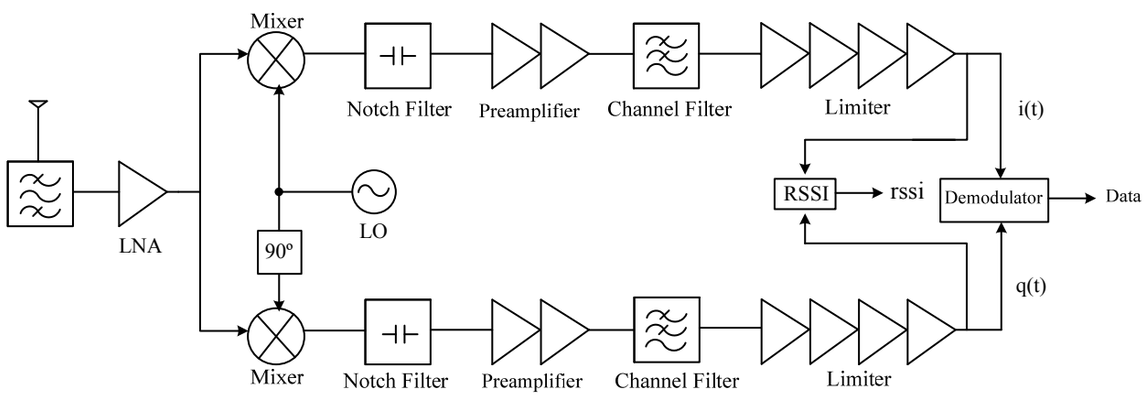


Fig. 2. Zero-IF receiver architecture for Ultra Low Power Bluetooth Standard.

An active RC topology has been chosen to implement the filter. Sallen-Key (SK) and multifeedback (MFB) topologies are usually employed in this kind of filters. Both architectures are attractive for low power design, since they comprise an active element per biquad performing at the same time low noise and high linearity. The main drawback of active RC filters for low power design is the high op-amp bandwidth required. The power consumption is optimized by using class-AB two-stage op-amp with enhanced gain and rail-to-rail output swing.

Based on the overall receiver planning, the low pass filter should provide a gain of 10 dB with a cut-off frequency of 1 MHz and a noise figure of less than 50 dB. According to the required stop-band attenuation of 45 dB at 3 MHz, a fourth-order Butterworth filter meets the requirements.

The topology of the active RC filter is shown in Fig. 3. It has been implemented by two biquadratic sections in cascade. Several combinations of second-order sections connected in cascade have been studied to fulfil the requirements for noise and op-amp bandwidth.

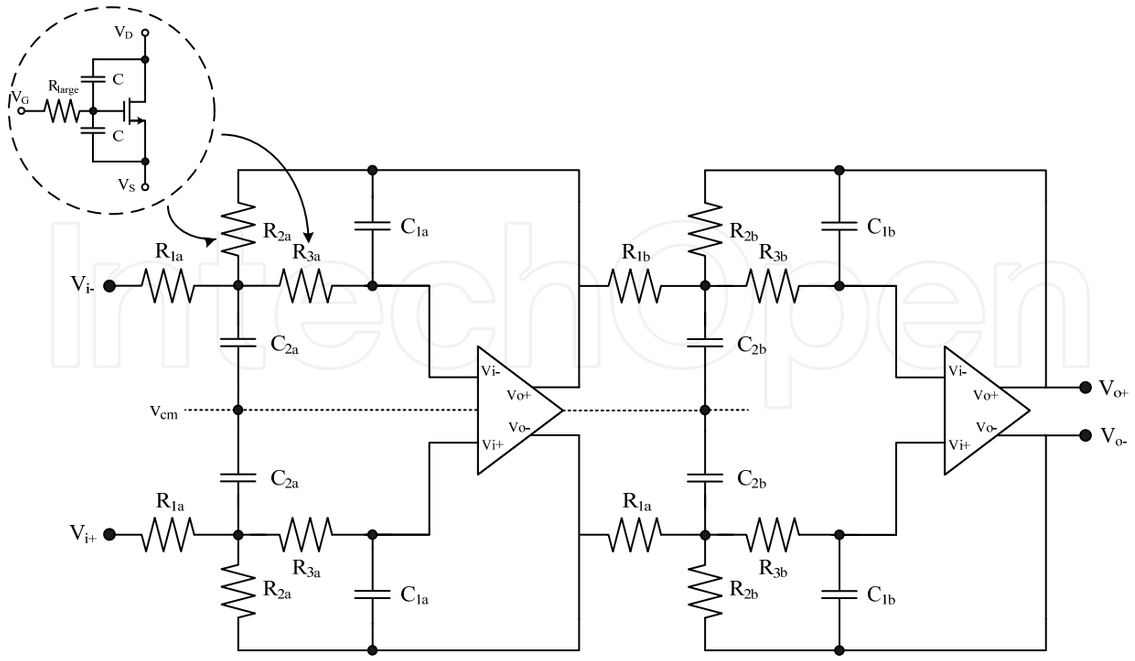


Fig. 3. Fourth-order low pass Butterworth filter with MFB topology.

The low voltage environment of this work (1.2 V power supply) leads to an amplifier topology that should provide rail-to-rail output swing. This fact precludes the use of cascode transistors to increase the voltage gain. In this context, two-stage op-amps are the natural choice, since they have rail-to-rail output swing and can drive both resistive and capacitive loads. In active RC topologies, the high op-amp bandwidth required (the op-amp unity-gain bandwidth has to be much larger than the filter pole) leads easily to high power consumption.

The fully balanced two-stage amplifier is shown in Fig. 4. This topology can provide rail-to-rail operation with better power efficiency than a Miller amplifier since the conventional two-stage amplifier needs a compensation capacitor to ensure the stability, and additional current to drive this capacitance. The main drawback is the low voltage gain. The operational amplifier often consumes large power to obtain a high gain. However, in this case, the gain is increased by placing two current sources M_{4a} and M_{4b} in parallel with the diode-connected transistors. In this design, the current of transistors M_{4a} and M_{4b} has been set at $k(I_{bias}/2)$ where the k factor is 0.8, boosting the gain $1/(1 - k)$ times (Steyaert et al., 1991; Yao et al., 2004).

For minimum power consumption and large current drive capability, one of the techniques explained in this chapter, the class-AB operation is used. Class AB output stages generate output currents larger than the output stage quiescent current. The class-AB performance of the output stage is achieved, without additional current, including a large resistive element implemented using a minimum size diode connected PMOS transistor M_{Rlarge} and a small capacitor C_{bat} (Ramírez-Angulo et al., 2006). The value of C_{bat} can be small, as transistor M_{Rlarge} is intended to operate as a very large resistive element. Under quiescent conditions and given that no DC current flows through M_{Rlarge} the voltage at the gate of M_{6b} is the same as at the gate of M_{bias} so that the quiescent current in M_{bias} and M_{6b} has the same value I_{bias}. During dynamic operation, when the output of the op-amp is slewing, the voltage at node X

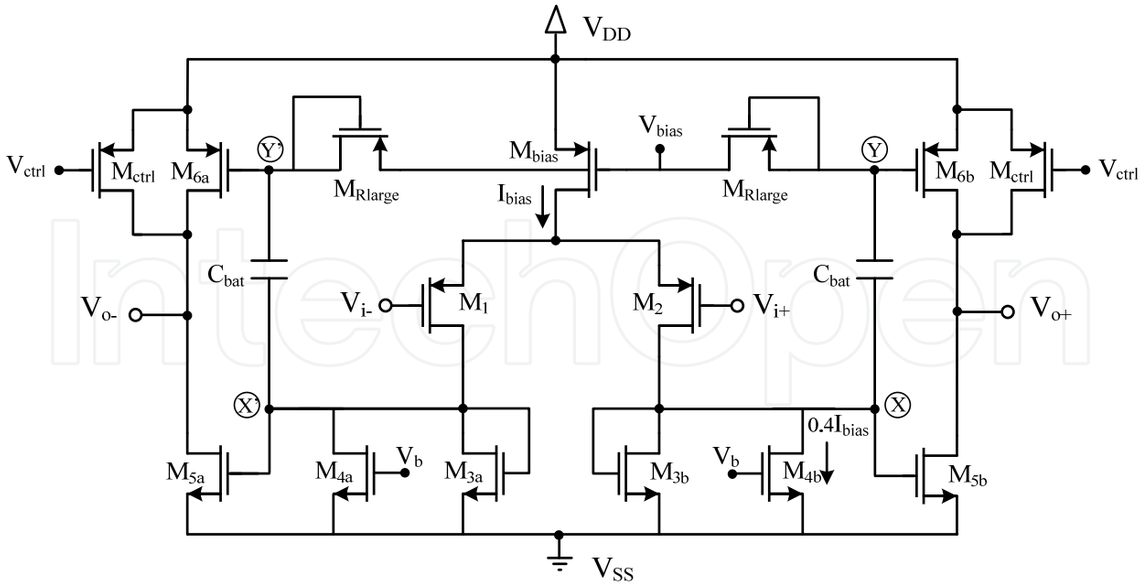


Fig. 4. Fully differential single-stage amplifier with class-AB output.

is subject to a large change. Given that capacitor C_{bat} cannot charge or discharge rapidly through M_{Rlarge}, it acts as a floating battery and transfers the voltage variations at node X to node Y. This provides class AB (push–pull) operation to the output stage. No additional circuitry to control the desired value of the quiescent output current is necessary due to the large resistor.

A conventional CMFB circuit is incorporated to control the output voltage. The output stage has low supply requirements since it can operate with a voltage close to the threshold voltage of a transistor: $V_{DD}^{\min} = V_{GS,5b} + V_{SDsat,2} + V_{SDsat,bias}$.

The biasing current of the op-amp is 20 μA. The current through transistors M_4 is adjusted at $0.4I_{bias}$ and M_5 size is ten times larger than M_3 size. The CMFB consumes 20 μA. Thus the total supply current is 80 μA.

Due to process variations, integrated components can differ significantly from their nominal values. In order to compensate for these variations, RC-opamp filters must be tuneable. A switched array of passive resistors and/or capacitors and MOSFET-C technique are usually employed. The latter is the simplest way and features continuous programmability. Passive resistors are replaced by MOSFET operated in triode region and the gate voltage is tuned to make the filter parameters programmable.

In this work, the device coined as ''quasi'' floating gate MOS (Ramírez-Angulo et al., 2003) is used to replace the passive resistors. A QFG MOS transistor consists of a MOS transistor with capacitive gate voltage averaging biased using a large resistive element R_{large} (Ramírez-Angulo et al., 2004), as shown in Fig. 3. for resistances R_{2a} and R_{3a}. The large resistance R_{large} for QFG MOS resistors has been implemented using MOS transistors operating in subthreshold region (Bikumandla et al., 2004), since the resistance of a transistor operating in this region is very large (tens of GΩ). Transistors operate in subthreshold region with a bias current I_{subth} of 10 nA. This method to implement programmable linear resistors

improves the linearity at the cost of increasing the area, mainly due to the use of two capacitors (C in Fig. 3). In order to save area, resistors R_1 are implemented by polysilicon ensuring a linear V–I conversion. Resistors R_2 and R_3 will be tuned to control the main parameters of the filter: gain, quality factor and cut-off frequency.

The proposed fourth-order Butterworth filter has been fabricated in a 0.18 µm CMOS technology. Figure 5 shows the chip microphotograph. The active area of the chip is 0.45 mm x 0.27 mm = 0.12 mm^2 and it is dominated by the capacitors. The filter operates with a single 1.2 V supply voltage.

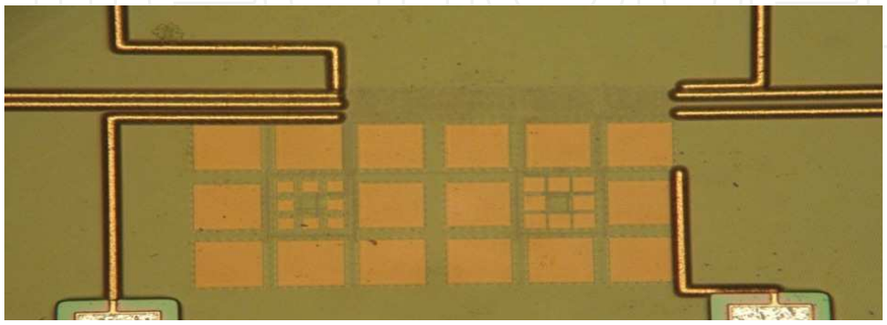
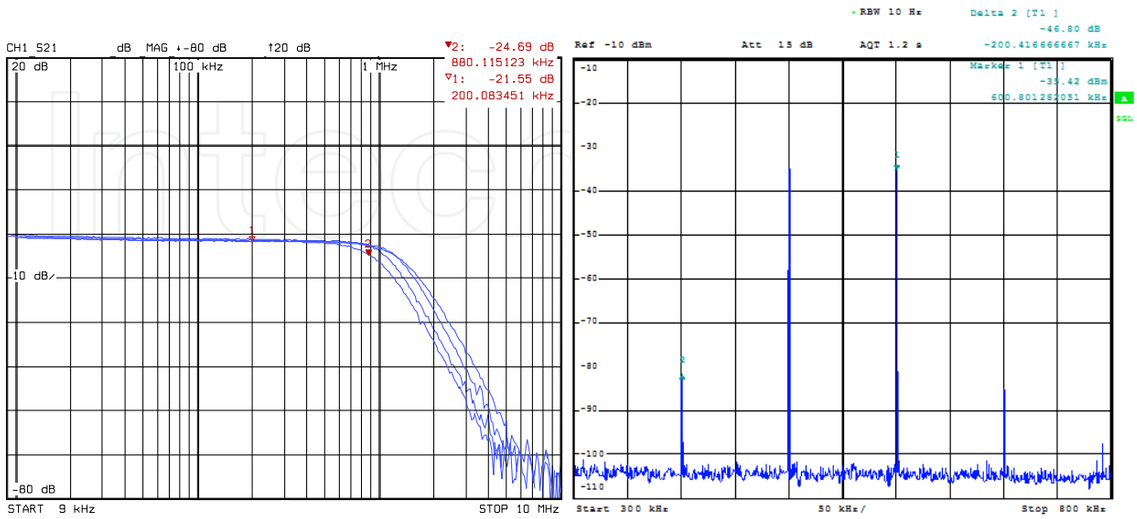


Fig. 5. Filter microphotograph.

Figure 6a illustrates the measured frequency tuning around the nominal frequency of 1 MHz. The cut-off frequency can be tuned from 800 kHz to 1.3 MHz. The measured two-tone intermodulation distortion for the filter is shown in Fig .6b. In this measurement, the cut-off frequency of the filter was set to the nominal value of 1 MHz. The frequencies of the input tones are at 500 and 600 kHz and the third intermodulation (IM3) products are at 400 and 700 kHz. Note that the IM3 of the filter is -46.8 dB, the noise figure is 46 dB and the input noise 85 nV/√Hz, which is approximately 85 µV in the 3 dB passband. Low noise behaviour is achieved in a low power environment mainly due to the use of only two amplifiers.



(a) (b)

Fig. 6. (a) Measured filter frequency response (b) Measured IM3 for the proposed filter.

A summary of the experimental results is given in Table 1.

Supply Voltage	1.2 V
Technology	0.18 μm CMOS
Silicon Area	0.12 mm^2
Transfer Function	Fourth-order Butterworth
Cut-off Frequency	1 MHz
Frequency tuning range	800 KHz - 1.3 MHz
DC Gain	10 dB
IIP3	16 dBm
Input-referred noise	85 μV
Static Power Consumption	290 μW

Table 1. Summary of experimental results.

3.2 Compact op-amp less CT ΣΔ modulator implementation for passive RFID applications

Combining sensors with passive RFID tags opens the way for new applications such as automotive and healthcare. As the passive RFID sensor nodes are intended to be powered by energy scavenging, ultra-low power consumption and robustness against process variations and changes in the supply voltage are essential requirements. In addition, low area occupancy is crucial in order to decrease the fabrication costs.

Low-bandwidth, moderate-resolution ADCs consuming a few microwatts are key elements for the sensor interface. Successive approximation register (SAR) converters are the typical choice for moderate-resolution low-frequency applications with ultra-low power requirements such as passive RFID. This type of converter achieves moderate resolution with very low power consumption and sets the state-of-the art in terms of energy efficiency. However, they consume large active area as the required DAC is normally implemented by a capacitor network. In this work the CT ΣΔ modulator architecture is proposed as an alternative to SAR architecture when the application also requires from very low area occupancy. CT ΣΔ modulators have become very popular over the last years, especially for lower power applications.

Traditionally, the loop filter is implemented either using an active-RC integrator or a gm-C approach. As it has been explained in the section 2 of this chapter, recent trends in low-power ADC design replace the internal op-amps (which usually are the most power consuming building blocks) with simple analogue circuitry. Following this trend, in this work a novel CT ΣΔ modulator implementation based on a local feedback is presented. The feedback provides a virtual ground node for reference subtraction without the need of op-amps or Operational Transconductance Amplifiers (OTAs). A first-order ΣΔ modulator prototype with low complexity at system level and minimum area occupancy has been designed in order to validate the idea.

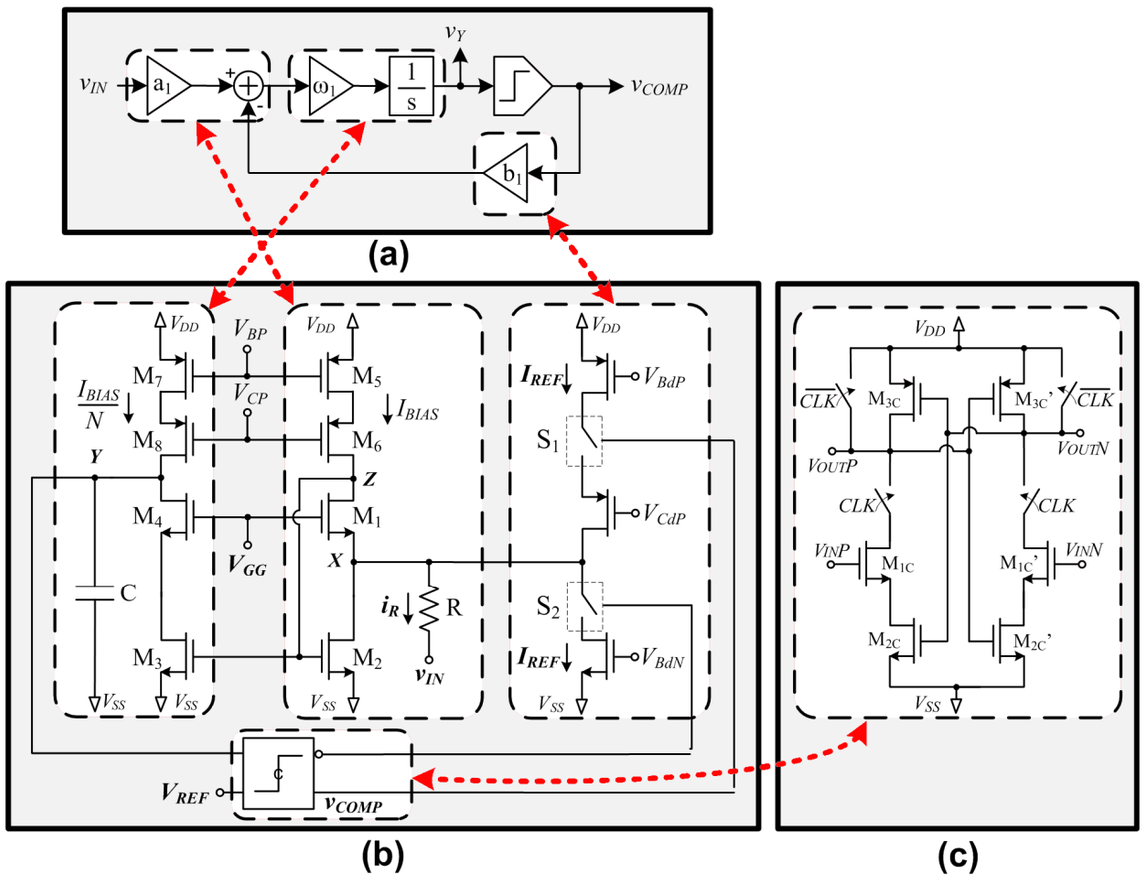


Fig. 7. First-order CT single-bit ΣΔ modulator. (a) Block diagram, (b) Proposed implementation, (c) Comparator schematic.

In Fig .7a the block diagram of a typical first-order CT single-bit ΣΔ modulator is shown. The modulator is made up of a comparator and a CT loop filter, which performs the subtraction and integration, as expressed in equation (1).

$$v_Y(s) = \omega_1 \frac{a_1 v_{IN}(s) - b_1 v_{COMP}(s)}{s} \tag{2}$$

The compact implementation shown in Fig 7.b is proposed, where the input stage, the integrator stage and the feedback DAC have been highlighted.

The input voltage, v_{IN} is converted into a current i_R by means of resistor R which connects the input signal to node X. Thanks to the feedback loop built up with transistors $M1$ and $M2$ and current source I_{BIAS}, the equivalent resistance at node X is extremely low.

In order to close the ΣΔ feedback loop the comparator controls two switches, S_1 and S_2, so that a reference current I_{REF} is injected or subtracted at node X depending on the comparator output. Therefore, the subtraction between the input signal and the comparator output is performed at node X in current mode. Note that both functions, the input voltage-to-current conversion and the feedback signal subtraction, are carried out by one resistor, two transistors and a current source. Then, the resulting current is copied and integrated in a capacitor.

By a proper selection of V_{GG}, so that the quiescent value of the input voltage (V_{IN}^{Q}) is equal to the bias voltage of node *X* (V_X^Q), the drain current of transistor *M2* is given by:

$$i_{D,M2} = I_{BIAS} + \frac{v_{in} + V_{IN}^{Q} - V_X^Q}{R} \pm I_{REF} = I_{BIAS} + \frac{v_{IN}}{R} \pm I_{REF} \tag{3}$$

As the input voltage is converted to current by a linear resistor, having a very low impedance at node *X* is crucial to achieve a good linearity at the input stage. This requirement is achieved thanks to the local feedback that keeps constant the current through transistor M1 in spite of output current variations at node *X*. Neglecting the body effect, the input impedance at node X is given by (Carvajal et al., 2005)

$$r_X = \frac{r_{o2}}{1 + g_{m1}r_{o2} + g_{m1}g_{m2}r_{o1}r_{o2}} \approx \frac{1}{g_{m1}g_{m2}r_{o1}}$$

which, for typical parameter values in the selected technology, is low enough to guarantee the linearity requirements for this application.

The current at the drain of *M2*, $i_{D,M2}$, is copied to node Y by the current mirror implemented with transistors *M3* and *M4*, where the current I_{BIAS} is removed. The resulting current is injected into capacitor *C* where the integration is carried out. Finally, the voltage at node *Y* is given by (in the s-Domain):

$$v_Y(s) = \frac{v_{IN}(s)}{RCs} \mp \frac{I_{REF}}{Cs} \tag{4}$$

Expressions (2) and (4) are equivalent if $a_1\omega_1 = 1/RC$ and $b_1\omega_1 V_{COMP} = I_{REF}/C$. Note that no additional circuitry is required to bias the node *Y*. To reduce power consumption, the current through *M3* (and *M7*) can be downscaled by modifying the gain of the current mirror. In our implementation a ratio of N=3 was chosen.

To save power, the dynamic latch-type comparator show in Fig .7c has been selected to close the modulator loop. Two switches open the latch branches during the reset phase so that the quiescent current consumption is zero.

To verify the proper operation of the proposed implementation, a first-order CT ΣΔ modulator prototype has been fabricated. The modulator digitalizes the signal coming from a MEMS accelerometer, which is a single-ended structure presently available in a 0.35μm CMOS technology. The ADC will be integrated in the same die with the MEMS accelerometer so it was designed in the same technology and with a single-ended input. The whole system is intended to be powered by an UHF RFID front-end which provides a 3V nominal supply voltage typical for the selected technology (Vaz et al., 2010). Fig. 8a shows a microphotograph of the fabricated prototype. The total area consumption (without pads) is only 110μm x 125μm for the whole proposed circuit which makes it, to the author's knowledge, the smallest ΣΔ modulator published for this range of specifications.

The measured output spectrum for a 7.85kHz sinusoidal input signal is shown in Fig. 8b. A peak SNDR (Signal-to-Noise plus Distortion Ratio) of 49dB has been obtained for a -5dBFS input signal. Fig .8c shows the measured SNR/SNDR versus input signal amplitude. It can be seen that the prototype achieves 56dB of Dynamic Range (DR), which means about 9 bits of ENOB over a 25kHz signal bandwidth. Experimental results are summarized in Table 2.

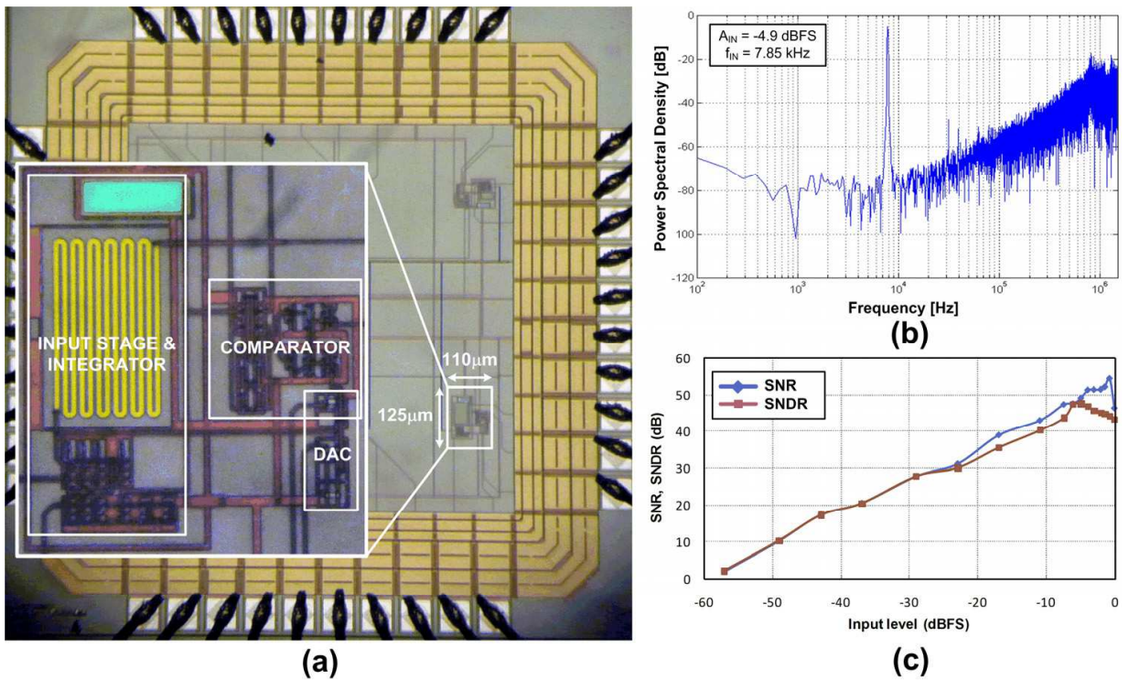


Fig. 8. (a) Circuit microphotograph, (b) Measured output spectrum, (c) SNR/SNDR versus input signal amplitude. Input signal frequency = 7.85 kHz. V_{DD} = 3V.

The designed modulator has also shown to be very robust against supply voltage and bias current variations. The DR remains over 52dB for a supply voltage variation in the range 2.25 to 5 volts even for a 50% decrease of nominal bias current.

The FOM defined by (5) has been used to have an estimation of the energy efficiency achieved by the proposed ΣΔ modulator implementation. The minimum power consumption

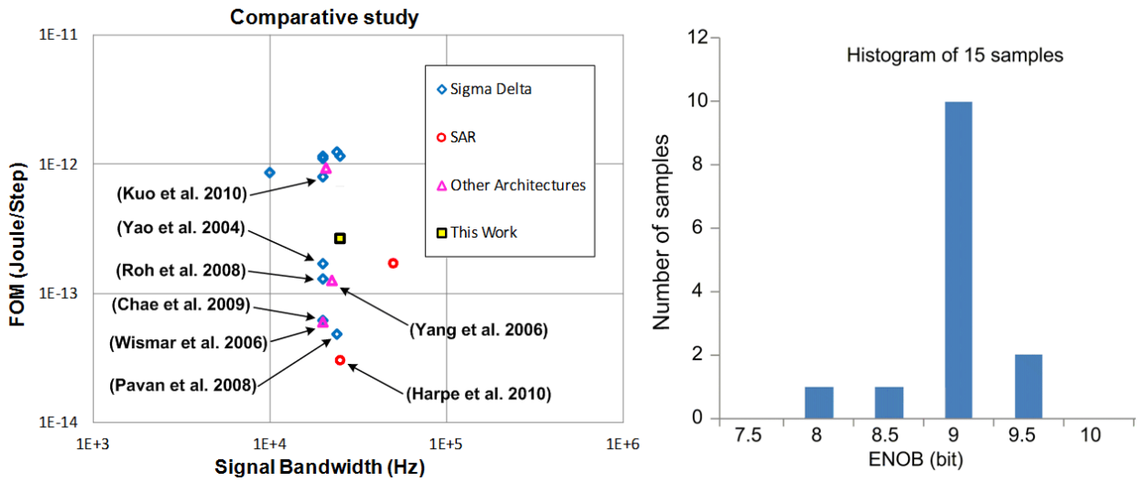
Sampling frequency (MHz)	3.2
Signal Bandwidth (kHz)	25
Oversampling ratio	64
Peak SNR (dB)	54.5 (@7.85kHz)
Peak SNDR (dB)	49 (@7.85kHz)
Dynamic range (dB)	56.2
ENOB (bit)	9.04
Input range (mVpp)	700
Power consumption (µW)	4.35 (@Vdd=2.25V)
Power supply (V)	3
PSRR (dB)	32
Vdd for ENOB > 7bits (V)	2.25 to 5
Active area (mm^2)	0.01375
Technology	AMS 0.35µm CMOS

Table 2. Summary of measured modulator performances.

(4.35µW) was measured for a 2.25V supply voltage, leading to a FOM of 0.267 pJ/step. This value places this work close to the most power efficient CT ΣΔ modulators recently published, despite that it has been implemented in a reasonable old technology.

$$FOM = \frac{P}{2^{ENOB} \cdot 2BW} \tag{5}$$

Fig. 9a gives a graphical representation of the state-of-the-art of power efficient ADCs in the same range of bandwidth. The measured performance of the proposed implementation is competitive in terms of energy efficiency compared with the state-of-the-art. The SAR converter (Harpe et al., 2010) sets the state-of-the-art and only a few ΣΔ modulators perform better than the proposed in this work.



(a) (b)

Fig. 9. (a) State of the art of ADCs regarding the selected FOM. (b) ENOB deviation for 15 measured samples (second version of the converter, V_{DD} = 3V, input signal frequency = 7.85 kHz.

Fig. 9b shows a histogram of the ENOB deviation for 15 samples fabricated. Every sample worked properly with an ENOB variation lower than than ±0.5 bits, which is an indication of the robustness of the proposed modulator implementation against the process variation.

A compact implementation for CT ΣΔ modulators based on a local feedback has been presented. In order to validate the idea, a first order CT ΣΔ modulator for a self powered sensor interface (9-bits of resolution and 25-kHz of signal bandwidth) has been designed in a 0.35µm CMOS technology. Experimental results confirm the idea and show that the proposed implementation leads to an extremely low area and highly power efficient ΣΔ modulator. The measured prototype has also shown to be very robust against process, supply voltage and bias current variations.

4. Conclusions

In this chapter, the need of minimizing power consumption in electronic devices has been pointed out. For this reason, a review of the most common techniques used by IC designers

with this purpose has been done. These techniques have been classified in four categories: biasing point optimization, digitally assisted techniques, analogue circuitry simplification and efficient use of biasing. In order to illustrate the large number of techniques that these categories involve, several references have been proposed through the chapter. Furthermore, two approaches based on the use of some of the reported techniques have been described. The first one proposes a micropower active-RC channel filter for an Ultra Low Power Bluetooth Receiver based on a zero-IF architecture. It uses a new topology of class-AB op-amp so that the current consumption is adapted to the output requirements. The second design proposes a compact op-amp less CT ΣΔ modulator for passive RFID applications. In order to reduce the power consumption, a local feedback technique is used.

5. Acknowledgment

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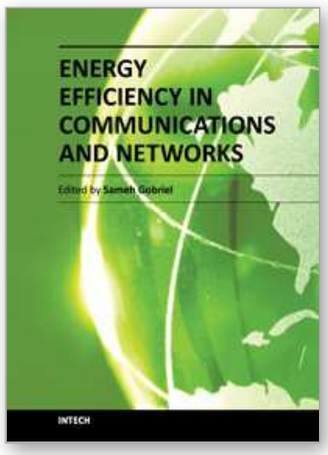

Energy Efficiency in Communications and Networks

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The topic of "Energy Efficiency in Communications and Networks" attracts growing attention due to economical and environmental reasons. The amount of power consumed by information and communication technologies (ICT) is rapidly increasing, as well as the energy bill of service providers. According to a number of studies, ICT alone is responsible for a percentage which varies from 2% to 10% of the world power consumption. Thus, driving rising cost and sustainability concerns about the energy footprint of the IT infrastructure. Energy-efficiency is an aspect that until recently was only considered for battery driven devices. Today we see energy-efficiency becoming a pervasive issue that will need to be considered in all technology areas from device technology to systems management. This book is seeking to provide a compilation of novel research contributions on hardware design, architectures, protocols and algorithms that will improve the energy efficiency of communication devices and networks and lead to a more energy proportional technology infrastructure.

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