Static linearity BIST for V_{cm}-based switching SAR ADCs using a reduced-code measurement technique

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***Abstract*—This work presents a reduced-code strategy for the static linearity self-testing of V_{cm}-based successive-approximation analog to digital converters (SAR ADCs). These techniques take advantage of the repetitive operation of SAR ADCs for reducing the number of necessary measurements for static linearity testing. In this paper we discuss the application of these techniques for the V_{cm}-based SAR ADC topology and present a practical BIST implementation based on an embedded incremental ADC. Electrical simulation results at transistor level are presented to validate the feasibility of the proposed on-chip reduced-code static linearity test.**

I. Introduction

The integrated successive approximation register (SAR) ADC based on V_{cm} switching has been widely used in the latest years due to their good trade-off between power efficiency and speed [1]. However, even though V_{cm}-based switching improves the linearity in comparison to conventional switching, these converters are still prone to static errors that may degrade its operation. Static linearity tests are then necessary in order to assure the correct functionality of the ADC, but they can be a very demanding and costly task that requires accurate and expensive test equipment. Another key aspect to be taken into consideration is the limited test access to internal nodes since CMOS scaling has enabled the wider use of tightly integrated mixed-signal SoCs.

Recent works have been presented in the literature that propose alternative techniques for reducing the complexity and requirements of ADC static linearity test. In this line, the recently proposed reduced-code static test technique, that relies in the repetitive operation of some ADC architectures, is of special interest [2]–[7]. The benefits are twofold: firstly, the number of necessary measurements for a complete static characterization is drastically reduced, and secondly, the reduced test complexity facilitates the on-chip implementation of the test apparatus in a Built-In Self-Test (BIST) fashion. Enabling ADC BIST may open the door to a number of advantages for enhanced testability, diagnosis and functional safety, such as in-the-field testing, on-line testing, in-situ diagnosis, adaptive operation, enhanced calibration, etc.

In this regard, a bit-weight extraction strategy based on the major-carrier transitions (MCTs) of the capacitive DAC (CDAC) in a SAR ADC was developed in [5] and further developed in [6] for measuring the static linearity using an embedded Incremental ADC (IADC). The technique was extended for split-capacitor CDACs (SCDACs) in [7], [8]. The voltages corresponding to MCT code lengths are internally generated through a modified operation of the SAR ADC, thus eliminating the need of a test stimulus generator, and digitized for further processing using the embedded IADC in a full-BIST fashion.

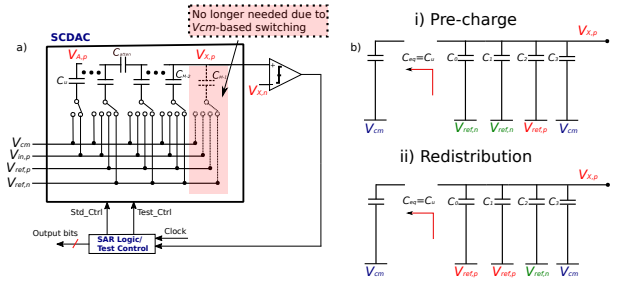

Fig. 1. V_{cm}-based Switching SAR ADC a) schematic and b) example of MCT code length voltage generation algorithm for $i = 2$.

In this paper we aim at extending the reduced-code static linearity test to V_{cm}-based switching SAR ADCs and proposing a practical on-chip implementation of the proposed technique.

II. Theoretical Basis

A. V_{cm}-based Switching SAR ADC operation

V_{cm}-based switching SAR ADCs, originally proposed in [1], are one of the SAR architectures with best trade-offs in terms of energy efficiency, linearity, area and control simplicity. The schematic of a differential split-capacitor V_{cm}-based Switching SAR ADC is shown in Fig. 1a. It consists of a $M \times L$-bit SCDAC, whose LSB section has L capacitors and the MSB section has $M - 1$ capacitors, a comparator and the digital control logic. The complete resolution for the V_{cm}-based switching SAR ADC is given by $N = M + L$. The negative CDAC is omitted in the figure, but its output is represented by $V_{X,n}$ on the negative input of the comparator. The digital logic is built with shift-registers and switch drivers that control the CDAC in order to perform a binary search operation. In the first cycle, the input voltage is sampled on the bottom plate of every capacitor of the array, while the upper plate is connected to V_{cm}. In the following cycle all bottom plates are connected to V_{cm}, and it can be shown that the top plates are charged to $V_{X_{p,n}} \approx 2V_{cm} - V_{in_{p,n}}$. The first output bit can hence be defined without the need of a MSB capacitor, halving the size of the MSB partial DAC and drastically reducing the switching energy consumption of the MSB bit

calculation. Additionally, since now the following capacitors are switched from V_{cm} to $V_{ref,p}$ or $V_{ref,n}$ depending on the output of the comparator, instead of all the way from $V_{ref,n}$ to $V_{ref,p}$, the power consumption for the following cycles is further reduced.

B. Proposed reduced test technique for V_{cm}-based switching

The static performance of a SAR ADC is mainly dependent of the accuracy of its internal DAC. The comparator adds other static errors like offset and gain, but those can be easily corrected in the post-processing phase. Thus, it should be possible to estimate the linearity of the complete SAR ADC by characterizing the static linearity of the DAC.

As presented in [7] for a traditional SCDAC SAR ADC, the core idea of the proposed reduced-code test technique is to employ the capacitive DAC to generate a voltage at nodes V_A and V_X in Fig. 1 that is proportional to the length of the code associated to each MCT of the partial capacitive DACs. These voltages are then digitized and employed for reconstructing the complete static characteristic of the ADC under test in a post-processing phase. Nevertheless, this process is not straightforward for the V_{cm}-based SAR ADC due to some particularities of this switching scheme.

As it was shown in [1], the first comparison does not depend on the capacitive array, which eliminates the need for the MSB capacitor and makes the INL ideally zero at the middle scale. Regarding the static characteristic of this structure, compared to the conventional SCDAC with M capacitors, this causes the DNL to be half the value of conventional switching, but distributed in two consecutive codes instead of one. It can be shown that this DNL splitting is repeated for the codes associated to each MCT. This fact is taken into account in post-processing for correctly mapping the complete transfer characteristic of the ADC under test.

Concerning the generation of differential voltages V_A and V_X, associated to the length of the MCT codes in the LSB and MSB sub-DAC arrays, respectively, we employ a modified operation of the control switches of the DAC array. The following description explains the procedure for the i-th capacitor. First, for generating the i-th voltage related to the i-th capacitor in the MSB sub-DAC, the i-th capacitor is connected to $V_{ref,p}$ while all the LSB capacitors from 0 to $i-1$ are connected to $V_{ref,n}$, the remaining capacitors being connected to V_{cm}, including the capacitors in the LSB sub-DAC. The negative path of the fully-differential CDAC performs the inverse of this procedure. The operation is similar for the LSB sub-DAC. As an example, this process is illustrated in Fig. 1b for the specific case of $i = 2$. This process is repeated for each capacitor in the array. By measuring these voltages and applying the methodology in [7] taking into account the DNL splitting effect in V_{cm}-based SCDAC SAR ADCs, it is possible to reconstruct the complete ADC static characteristic.

III. Practical On-Chip Implementation for BIST

Fig. 2 shows a conceptual schematic of the complete BIST for reduce-code measurements. The DC differential voltages

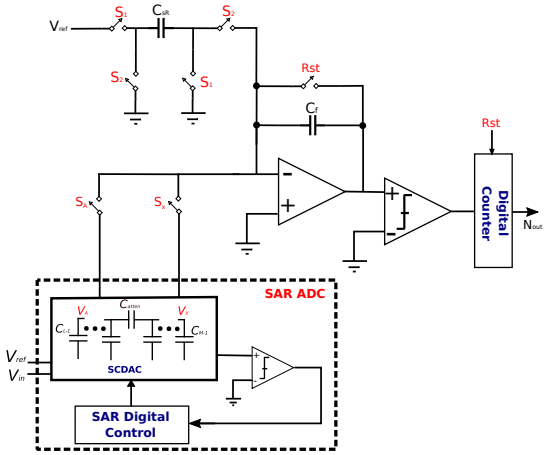

Fig. 2. Conceptual schematic of the Incremental ADC merged with the SCDAC of the SAR ADC.

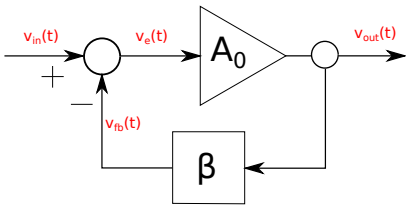

Fig. 3. General model of a feedback amplifier used for estimating the OTA minimum gain.

V_X and V_A are generated by the capacitive array and digitized by an embedded converter. In this implementation we have selected an Incremental $\Sigma\Delta$ ADC [9] for an efficient and accurate conversion. This family of converters is very suitable for accurately digitizing DC voltages. We employed a simple first-order IADC that consists of a switched-capacitor integrator, a comparator and a digital counter. It is important to note that the SCDAC of the SAR ADC is merged with the input integrator of the IADC as in a classical MDAC [10]. The switches S_X and S_A control the MSB and LSB partial CDAC connections to the test instrument.

A. Guidelines for the IADC design

The performance of the IADC is mainly limited by the non-idealities of the integrator. In this subsection we analyze the impact of the main non-idealities in the IADC building blocks and derive design guidelines for an accurate test. In particular we consider the effects of integrator leakage, and the dynamic behavior of the amplifier. The amplifier offset can be greatly compensated using well-known techniques such as auto-zeroing or chopper stabilization and it is not considered in our analysis. Other non-idealities in the IADC can be considered as second-order contributions.

First, let us consider the effect of a finite gain in the amplifier. The classical model of a negative feedback amplifier is shown in Fig. 3. Since the voltage error is given by $v_e(t) = v_{in}(t)/(1+\beta A_0)$, where β is the feedback factor and A_0 is the open-loop gain of the amplifier, we can derive the minimum DC gain of the OTA as a function of the IADC resolution R by defining a value of v_e that is smaller than

a fraction of one LSB of the IADC. To provide a sufficient design margin, we set this maximum allowable error to one-eighth of the IADC LSB. Hence, the minimum gain of the amplifier $A_{0min,dB}$ in dB is given by

$$A_{0min,dB} = 6.02(R+3) - 20\log(\beta\xi), \tag{1}$$

where ξ is defined as the ratio between the FS of the IADC and the LSB of the SAR ADC under test [6], [7].

Concerning the dynamic behavior of the amplifier, we can use a similar reasoning for estimating the minimum gain-bandwidth product and Slew Rate (SR). Considering a dominant-pole model for the amplifier, if we require the integrator output voltage to settle within one-eighth of the LSB precision to the ideal final value, it can be shown that,

$$v_{out}(t) = V_{out,final}\left(1 - \frac{1}{2^{R+3}}\right) = V_{out,final}\left(1 - e^{\frac{-1}{2f_{ck}\tau}}\right),$$

where $\tau = 1/(2\pi\mathrm{GBW})$ and f_{ck} is the integrator frequency. Then, it follows that the minimum gain-bandwidth $\mathrm{GBW}_{\min}$ can be estimated using

$$\mathrm{GBW}_{\min} = \frac{f_{ck}(R+3)\ln(2)}{\pi}. \tag{2}$$

Regarding the slew rate, the largest output variation is given by $V_s = \frac{C_{sR}}{C_f}(V_{ref,p} - V_{ref,n})$, and hence this value defines our worst case scenario. The output of the integrator is given by

$$v_{out}[n] = v_{out}[n-1] + \alpha V_s(1 - e^{\frac{-1}{2f_{ck}\tau}}),$$

where $\alpha = A_0/(1+A_0)$ is the leakage factor of the integrator. The minimum required SR can be determined as

$$\left.\frac{dv_{out}(t)}{dt}\right|_{max} = \mathrm{SR}_{\mathrm{limit}} = \alpha\frac{C_{sR}}{C_f}(V_{ref,p} - V_{ref,n})2\pi\mathrm{GBW}. \tag{3}$$

It is important to notice that the IADC operation frequency may be considerably smaller than the clock frequency of SAR ADC to significantly relax the design constrains of the IADC while maintaining test accuracy. Even though that will increase the reduced-code test time, a large margin for test time reduction is available since only one measurement per capacitor in the CDAC array is needed.

B. Case study

In order to validate the design guidelines presented above, this section provides an example of application in a practical case study. For this case study we designed a 40 MSPS (clock frequency of 480 MHz) 10-bit (6×4) SCDAC SAR ADC that will be used as the DUT. The SAR ADC features a MoM unit capacitor of $C_u = 9$ fF, using the V_{cm}-based capacitor switching for low power consumption. The SAR comparator is based on the well-known StrongARM latch topology. The full-scale of the SAR ADC is $\mathrm{FS} = 1.2\,\mathrm{V_{pp}}$ with an input common-mode voltage of 600 mV. The ADC and the embedded test instrument have been designed using STMicroelectronics 65 nm CMOS technology.

A first-order IADC was embedded for MCT-based reduced-code test as described above. The clock frequency of the first-order IADC was set to $f_{ck} = f_{ck,SAR}/16 = 30$ MHz. Taking into consideration the analysis in [7], we choose a resolution of 8-bits for the IADC (i.e. 256 cycles/sample) as a trade-off between test accuracy and design complexity. The reference voltages for the IADC are reused from the SAR ADC, $V_{ref,p} = 900$ mV and $V_{ref,n} = 300$ mV. The FS of the IADC is controlled by the feedback and integrating capacitors since the sampling capacitor is effectively replaced by the SAR capacitive array. The total capacitance of the array is $C_{Total} = 2^{M-1}C_u$, and the feedback and integrating capacitors have been set to $C_{sR} = C_f = 5C_u$, which gives an equivalent FS range for the IADC of $\mathrm{FS_{IADC}} = \frac{C_{sR}}{C_{Total}}2(V_{ref,p} - V_{ref,n})$. The minimum design specifications for the integrator, obtained by applying the design guidelines discussed above, are listed in Table I.

TABLE I
OTA INTEGRATOR SPECIFICATIONS

IADC resolution R	8
$f_{ck,OTA}$ (MHz)	30
$A_{0min,dB}$	65
GBW (MHz)	70
SR (V/μs)	340
PM (degrees)	> 45
Output range (mV)	$\pm$600
Equivalent input noise	minimize

To further reduce the design effort, the comparator in the IADC is reused from the ADC under test. The amplifier in the integrator was designed to comply with the specifications in Table I. The selected amplifier architecture is based on a fully-differential telescopic OTA with a second stage to increase the total gain, as depicted in Fig. 4. For simplicity, the biasing and the Common-Mode Feedback (CMFB) circuits are not shown. In order to validate the design of the amplifier, we run transistor level simulations for the nominal and analog process corners fast-fast (FF), fast-slow (FS), slow-fast (SF) and slow-slow (SS). The obtained simulation results are summarized in Table II. As it can be seen, all the target specifications were satisfied by the proposed design.

TABLE II
OTA SIMULATION RESULTS

	Nominal	FF	FS	SF	SS
Gain (dB)	74.51	73.23	74.93	74	74.97
GBW (MHz)	403.6	445.9	380.5	416.2	373.4
SR (V/μs)	464.7	605.2	651.6	376.3	387.1
Phase Margin (degrees)	49.94	50.81	52.63	46.07	49

IV. RESULTS

To validate the feasibility and performance of the proposed on-chip reduced-code test strategy, we performed transistor-level transient simulations of the complete system including the V_{cm}-based SAR ADC under test with the embedded

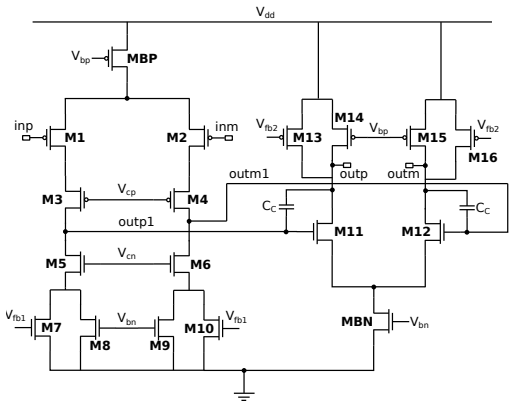

Fig. 4. Transistor-level schematic of the operational amplifier (bias and CMFB omitted, the latter generates the voltages V_{fb1} and V_{fb2}).

IADC for test. The digital logic controlling the approximation register and the execution of the test procedure has been implemented using behavioral VerilogA models to speed up simulations. The digital counter at the output of the IADC is also implemented using VerilogA. No degradation of the SAR ADC performed is observed due to the co-design of the IADC for test. Transistor-level simulations yield an ENOB of 9.9 bits for both the stand-alone SAR ADC and the complete system including the SAR ADC and the embedded test instrument.

In order to provide a realistic validation of the technique, we use the mismatch Monte Carlo models in the Process Design Kit (PDK) of the technology to generate samples of the SC-SAR ADC under test. A worst-case sample (3σ variation) in terms of static linearity was selected and characterized by transistor-level electrical simulation using both the proposed reduced-code test strategy and the standard histogram test using a high-resolution ramp stimulus with 128 hits-per-code. The obtained results for DNL and INL estimations are shown in Figs. 5a and 5b. It is important to notice that the reduced-code test only employs 9 measurements to derive the complete static characteristic, which represents less than 1% of the codes of the 10-bit SAR ADC under test.

The obtained rms error in the estimation of the INL is below 0.25 LSB, with a maximum error below 0.6 LSB. The total test time for the reduced-code test strategy was $460.8\,\mu$s while the standard 128 hits-per-code histogram test takes 3.28 ms. The obtained test time reduction represents a test time saving of 86% compared to the standard histogram.

V. Conclusion

This work presented an on-chip reduced-code test strategy for the static linearity test of V_{cm}-based switching SAR ADCs. The technique is based on the measurement of the length of the codes associated to the MCT transitions and takes into account the particularities of the V_{cm}-based switching strategy. It has been shown that the complete static linearity characteristic of an N-bit SAR ADC can be inferred with only $N-1$ measurements.

An on-chip implementation has been proposed based on an IADC embedded within the SAR ADC under test for digitizing the set of MCTs. We have provided practical design

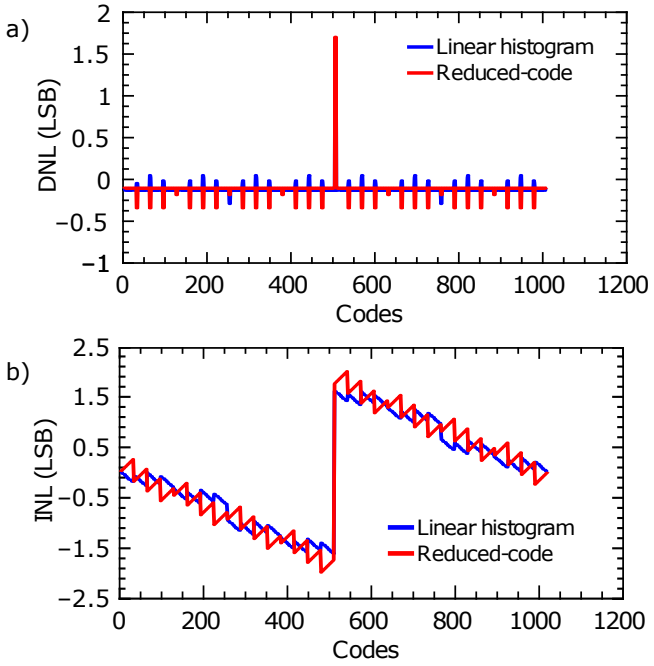

Fig. 5. Static linearity test results comparing the standard linear histogram test and the proposed V_{cm}-based reduced test technique, a) DNL and b) INL.

guidelines for a BIST implementation by considering the main design non-idealities of the proposed test instrument. Finally, the proposed test strategy has been validated by transistor-level simulations of a 10-bit (6×4) V_{cm}-based SCDAC SAR ADC under test with a first-order IADC as embedded test instrument. Obtained results show a test accuracy comparable with the standard histogram test with test time savings of 86% compared to a 128 hits-per-code histogram test.

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