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On-chip reduced-code static linearity test of V_{cm}-based switching SAR ADCs using an incremental analog-to-digital converter

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***Abstract*—This paper describes a BIST technique for the static linearity test of V_{cm}-based successive-approximation analog-to-digital converters (SAR ADCs). We discuss the application of reduced-code techniques for the V_{cm}-based SAR ADC topology and present a practical on-chip implementation based on an embedded incremental ADC. Simulation results are provided for validating the feasibility and performance of the proposed on-chip reduced-code static linearity test.**

I. Introduction

The integrated successive approximation register (SAR) ADC based on V_{cm} switching has been widely used in the latest years due to their good trade-off between power efficiency and speed [1]. However, even though V_{cm}-based switching improves the linearity in comparison to conventional switching, these converters are still very susceptible to static errors that may degrade the conversion performance. Hence, accurate static linearity tests are required in order to guarantee the converter operation and performance. However, these tests are usually a challenging and costly task, requiring accurate and expensive test equipment. Recent works have been presented in the literature that propose alternative techniques for reducing the complexity and requirements of ADC static linearity test. In this line, the recently proposed reduced-code static test technique, that relies in the repetitive operation of some ADC architectures, is of special interest [2]–[8]. The benefits are twofold: firstly, the number of necessary measurements for a complete static characterization is drastically reduced, and secondly, the reduced test complexity facilitate the on-chip implementation of a significant portion of the test equipment in a Built-In Self-Test (BIST) fashion. Enabling ADC BIST may open the door to a number of advantages for enhanced testability and functional security, such as in-the-field testing, on-line testing, adaptive operation, in-situ diagnosis, enhanced calibration, etc.

This paper focuses on extending the reduced-code static linearity test to V_{cm}-based switching SAR ADCs and proposing a practical on-chip implementation of the proposed technique. The rest of the paper is organized as follows. Section II describes the proposed reduced-code test technique for V_{cm}-based switching SAR ADCs. Section III proposes an on-chip implementation. Section IV demonstrates the feasibility of our proposal using realistic behavioral simulations. Finally, Section V summarizes our main contributions.

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II. Reduced-code test for V_{cm}-based switching SAR ADCs

The static linearity of a SAR ADC is mainly dependent of the static performance of its internal DAC. Thus, it follows that we could infer the static linearity of a SAR ADC by characterizing the static linearity of its DAC. As presented in [7] for a traditional Split-Capacitor DAC (SCDAC) SAR ADC, the core idea of the proposed reduced-code test technique is to employ the partial DACs to generate a DC voltage that is proportional to the length of the code associated to the Major Carrier Transitions (MCTs) of the partial DACs. These voltages are then digitized and employed for reconstructing the complete static characteristic of the ADC under test in a post-processing phase. This test has the additional advantage of not requiring a test stimulus. Nevertheless, this process is not straightforward for the V_{cm}-based SAR ADC due to some particularities of this switching scheme. As it was shown in [1], the first comparison does not depend on the capacitive array, which eliminates the need for the MSB capacitor and makes the INL ideally zero at the middle scale. Actually, for V_{cm}-based N-bit SCDAC SAR ADCs with a DAC splitting of L least significant bits and M most significant bits, the MSB array has $M-1$ capacitors, as the largest one is not needed. Regarding the static characteristic of this structure, compared to the conventional SCDAC with M capacitors, this causes the DNL to be half the value of conventional switching, but distributed in two successive codes instead of one. It can be shown that this DNL splitting is repeated for the codes associated to each MCT. This fact is taken into account in post-processing for correctly mapping the complete transfer characteristic of the ADC under test.

III. Practical on-chip implementation

Fig. 1 shows a conceptual schematic of the complete BIST scheme for reduce-code on-chip static test. The DC differential voltages V_X and V_A are generated by the capacitive array and digitized by an embedded converter. This implementation employs an Incremental $\Sigma\Delta$ ADC (IADC) [9] for an efficient and accurate conversion. This family of converters is very suitable for accurately digitizing DC voltages. We use a

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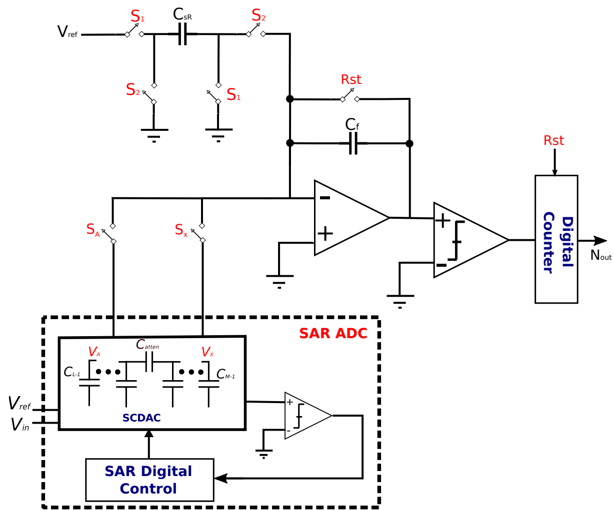

Fig. 1. Conceptual schematic of the Incremental ADC merged with the SCDAC of the SAR ADC.

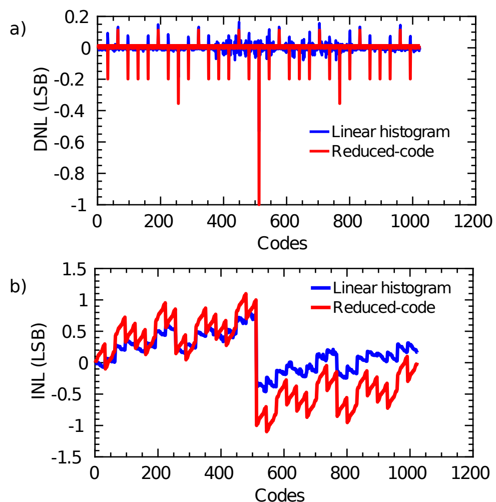

Fig. 2. Static linearity test results comparing the standard linear histogram test and the proposed V_{cm}-based reduced test technique, a) DNL and b) INL.

simple first-order IADC that consists of a switched-capacitor integrator, a comparator and a digital counter. It is important to note that the SCDAC of the SAR ADC is merged with the input integrator of the IADC as in a classical MDAC [10]. The switches S_X and S_A control the MSB and LSB partial CDAC connections to the test instrument.

IV. Case Study

In order to validate the proposed test strategy, this section provides an application example in a practical case study. For this case study we modeled in MATLAB a 10-bit (6×4) SCDAC SAR ADC designed in STMicroelectronics 65nm technology, that will be used as the DUT. A first-order IADC was embedded for MCT-based reduced-code test as described above. Taking into consideration the analysis in [7], we choose a resolution of 8-bits for the IADC (i.e. 256 cycles/sample) as a trade-off between test accuracy and design complexity. The reference voltages for the IADC are reused from the SAR ADC.

In order to provide a realistic validation of the technique, we generate a set of SC-SAR ADC samples employing the mismatch models provided in the Process Design Kit of the technology. We selected one of the worst-case generated samples (3σ variation in terms of static linearity) and characterized it using behavioral-level simulation. For comparison, the characterization was repeated using both the proposed on-chip reduced-code test strategy and the standard histogram test with a ramp test stimulus (considering 128 hits-per-code). Figs. 2a and 2b show the obtained results for DNL and INL measurements. It is important to notice that the reduced-code test only employs 9 measurements to derive the complete static characteristic, which represents less than 1% of the codes of the 10-bit SAR ADC under test. The obtained rms error in the estimation of the INL is below 0.4 LSB, with a maximum error below 0.8 LSB.

V. Conclusion

This work presented an on-chip reduced-code test strategy for the static linearity test of V_{cm}-based switching SAR ADCs. The technique is based on the measurement of the length of the codes associated to the MCT transitions and takes into account the particularities of the V_{cm}-based switching strategy. In this line, we have shown that the full static linearity performance of an N-bit SAR ADC can be computed from only $N-1$ measurements, which yields a significant reduction in test time the ADC under test. Behavioral simulation results from a full-BIST implementation based on an embedded IADC for MCT measurements show the feasibility of the approach.

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