SMASH $\Delta\Sigma$ modulator with adderless feed-forward loop filter

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A novel cascade $\Delta\Sigma$ modulator, which combines the benefits of SMASH topology and feed-forward loop filter, is presented in this letter. The proposed $\Delta\Sigma$ architecture is based on moving the power-hungry adder block from the quantizer input to the first integrator output. The proposed architecture shows a better OTA linearity and relaxed OTA DC-gain compared to conventional MASH and SMASH topologies. This feature makes the modulator topology more suitable than conventional MASH and SMASH topologies for low-voltage applications.

Introduction: Delta Sigma Modulators ($\Delta\Sigma$Ms) are widely used in low-power high-speed applications. Due to low oversampling ratio (OSR) in high bandwidth applications, higher order modulators can be used to meet the dynamic range (DR) requirement. However, the use of higher-order loop filter makes a $\Delta\Sigma$M severely susceptible to instability. Although employing MASH structure guarantees stable operation, it needs high-gain and power-consuming Operational Transconductance Amplifier (OTA), used in the integrators, to minimize the quantization error leakage due to analog and digital filter mismatches. The sturdy MASH (SMASH) structure has been published [1], and depicted in Fig. 1, in which the first stage quantization error is noise-shaped instated of canceling the error, to obviate the matching requirements. However, the modulator presented in [1] suffers from two drawbacks. First, a highly linear Digital-to-Analog Converter (DAC) is required in the added feedback path to the first stage input. Second, added feedback paths are sensitive to mismatch, which causes low-order quantization noise leakage. To circumvent these two drawbacks, an improved SMASH $\Delta\Sigma$M, shown in Fig. 2, has been introduced in which a unity Signal Transfer Function (STF) topology was utilized [2]. The main problem of the $\Delta\Sigma$M in Fig. 2 is that a relatively high-speed active adder is needed at the input of the quantizer and it consumes power. It is worth noting that although a passive adder consumes much less power, it is not suitable as it capacitively loads the second integrator. This increased loading results in more stringent requirements on the second integrator.

To overcome the aforementioned drawbacks, a cascade $\Delta\Sigma$M with modified unity STF feed-forward architecture [3] for low-power high-speed application is addressed in this letter. The main features of the proposed modulator are the following. First, the high-speed and power-hungry adder in front of the quantizer is removed and the preceding integrator performs this task. Second, the STF of the proposed modulator is modified to unity i.e. $STF = 1$. Third, taking the advantage of the SMASH topology, quantization error is canceled in the proposed architecture and fourth, the number of feedback DACs is less than what has been proposed in [1].

Proposed SMASH topology: The proposed modulator is illustrated in Fig. 3. The following strategies are used to overcome the drawbacks of two previous modulators.

- The summation block is moved back to the input of the second integrator, thus resulting in the addition operation being performed at the input of the second integrator. Therefore, the high-speed power-hungry adder is no longer needed.
- The STF of the modulator is restored to unity by inserting a direct feed-forward from the input of the modulator to the input of the second integrator with the transfer function of $1 - z^{-1}$. Having had the first stage of the proposed modulator, the NTF and STF of the first stage itself can be expressed as follows,

$$Y_{1\mathrm{st-stage}}(z) = STF_1.X(z) + NTF_1.E_1(z) \qquad (1)$$

  where $X(z)$ is the input signal, $STF_1 = 1$, $NTF_1 = (1 - z^{-1})^2$ and $E_1(z)$ stands for the quantization error of the first stage.
- Feedback paths from the second stage to the first one are omitted by inserting the modulator output back to the first stage input, and output bitstreams of both stages are digitally subtracted inside the loop filter of the first stage. Hence, the number of feedback DACs is less than the modulator proposed in [1].

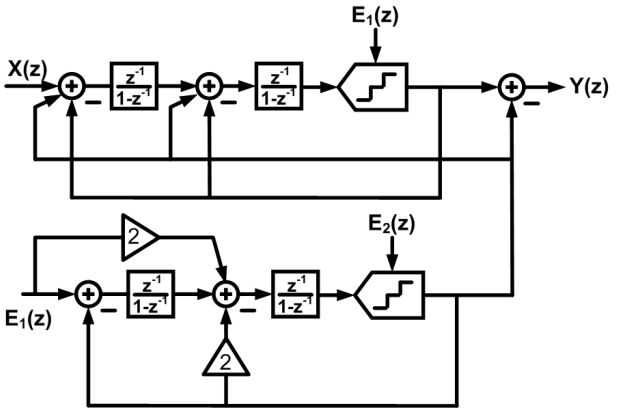

Fig. 1: Block diagram of the conventional SMASH architecture [1]

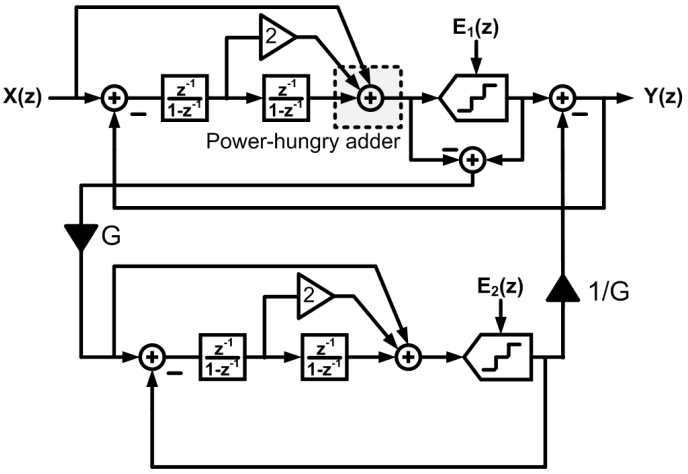

Fig. 2: Block diagram of the modified SMASH [2]

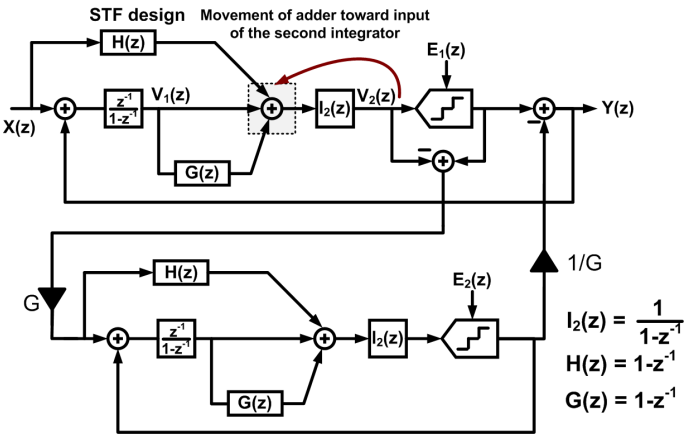

Fig. 3: Block diagram of proposed adderless SMASH $\Delta\Sigma$M

Note that, contrary to the conventional SMASH $\Delta\Sigma$M, the quantization error of the first stage is completely canceled without using any digital cancellation logic. Moreover, using interstage gain (denoted as G in Fig. 3) would not be effective in the conventional SMASH since $E_1(z)$ is not completely canceled out, and as a consequence further reduction of the $E_2(z)$ would not improve the noise suppression significantly. However, this drawback is solved in the proposed modulator. Having had above descriptions and using a linear model for the quantizers, the Z-domain transform of the modulator output is expressed by:

$$Y_{\mathrm{proposed-SMASH}}(z) = X(z) - \frac{1}{G}(1 - z^{-1})^4.E_2(z) \qquad (2)$$

where $X(z)$ is the input signal, G stands for the interstage gain and $E_2(z)$ is the quantization error of the second stage.

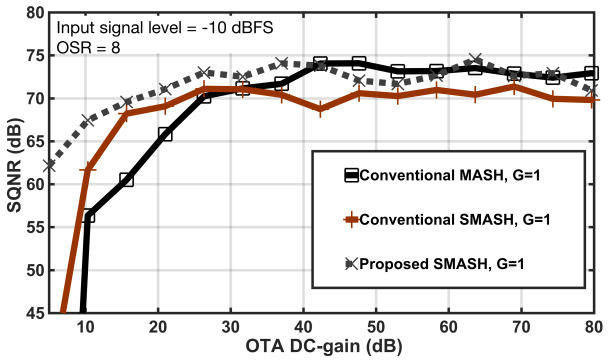

Fig. 4: SQNR versus OTA DC-gain

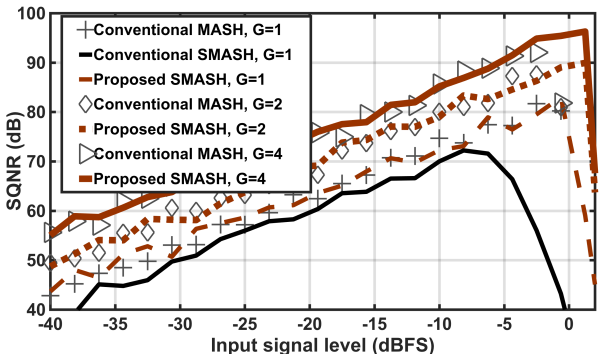

Fig. 5: SQNR versus input signal level

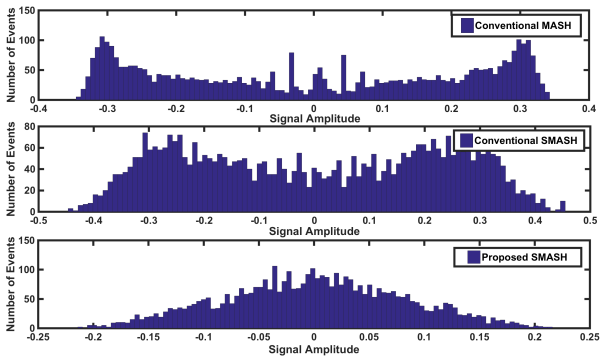

Fig. 6: First integrator output histogram

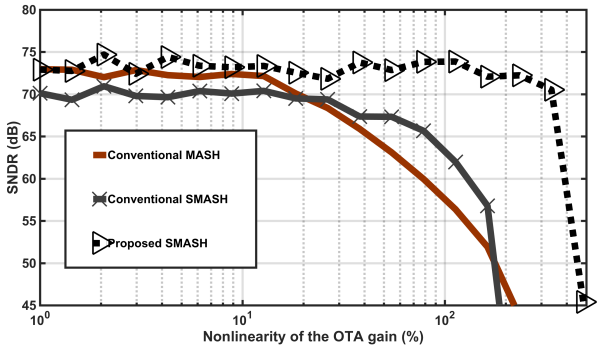

Fig. 7: Effect of OTA nonlinearity on the SNDR

Simulation results: For comparison purposes, both conventional MASH 2-2 $\Delta\Sigma$M and conventional SMASH 2-2 $\Delta\Sigma$M as well as proposed architecture are simulated by using SIMSIDES [4]. For all simulations, a 4-bit quantizer, $OSR = 8$ and 1-V reference voltage are considered. The OTA DC-gain requirement of the above-mentioned structures is illustrated in Fig. 4. It is shown that the proposed $\Delta\Sigma$M is more robust in terms of finite OTA DC-gain. Note that the conventional MASH structure needs an OTA with the DC-gain of at least 40-dB to avoid the Signal to Quantization Noise Ratio ($SQNR$) degradation from the maximum value, while the proposed architecture requires less than 20-dB OTA DC-gain. However, the $SQNR$ drastically drops below this value in a conventional SMASH topology.

Fig. 5 shows the $SQNR$ versus input signal level by comparing the conventional MASH and SMASH architectures with the proposed $\Delta\Sigma$M with $G = 1, 2$ and 4. An ideal (infinite) value of the OTA DC-gain is assumed for all cases. It is shown that the proposed modulator demonstrates better performance in terms of both maximum $SQNR$ and overload level. Moreover, the achievable maximum $SQNR$ can be increased by considering $G > 1$. The output histogram of the first integrator for all modulators is depicted in Fig. 6. It can be noted that the combination of unity STF and multi-bit quantizer results in a relaxation of the output swing for the proposed $\Delta\Sigma$M compared to conventional MASH and SMASH topologies. This is very important in a limited voltage headroom implementation.

The proposed SMASH topology is also more robust against OTA nonlinear DC-gain. This is illustrated in Fig. 7, where the influence of the front-end integrator OTA nonlinearity is shown and compared with both conventional MASH and SMASH topologies, by considering a DC-gain of 50-dB and an input signal level of -10-dB below Full-Scale range (dBFS).

Conclusion: A new adderless SMASH $\Delta\Sigma$M based on a feed-forward loop filter is presented. The main bottleneck of the feed-forward topology i.e. high-speed power-hungry adder is mitigated by moving the adder back to the input of the second integrator. The STF of the proposed SMASH $\Delta\Sigma$M is restored to unity which makes the proposed architecture robust to OTA nonlinearity. Unlike the conventional SMASH structure, quantization error of the first stage is fully canceled in the proposed architecture. As a consequence, the interstage gain can now increase the performance of the proposed modulator. All above-mentioned characteristics make the proposed architecture suitable for low-voltage, low-power and high-speed applications.

Acknowledgment: The authors acknowledge the National Sciences and Engineering Research Council of Canada for the support and CMC Microsystems for the design tools. This work was also partially supported by the Spanish Min. of Econ. and Comp. (supported by European RDF) under contract TEC2013-45638-C3-3-R.

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