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An Amplified Offset Compensation Scheme and its Application in a Track and Hold Circuit

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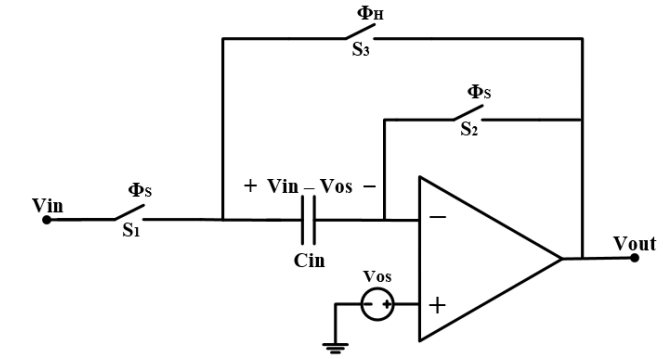
***Abstract* - This paper proposes a fully differential track and hold circuit using a new DC offset compensation scheme. It stores an amplified version of the offset during the hold phase, which is used in attenuated fashion during the track phase to compensate offset. This scheme is less sensitive to charge injection and other errors than conventional offset compensation schemes. Experimental results of a test chip in 0.18 µm CMOS technology verify the proposed scheme.**

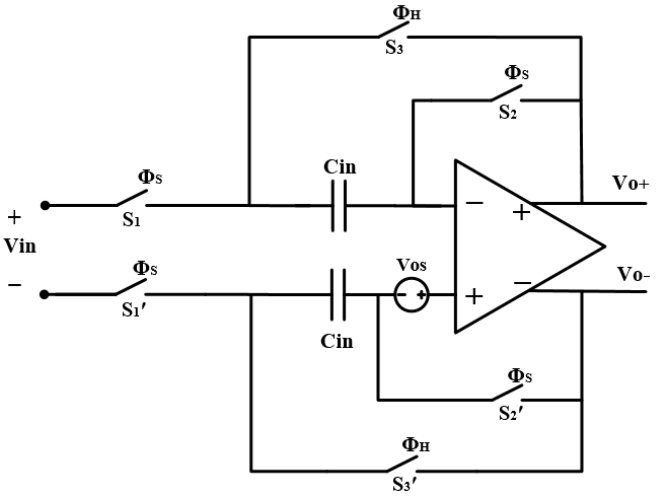
***Index Terms* –Sample and hold (S/H), Differential difference amplifier (DDA), Mixed-signal circuits, Offset compensation.**

I. Introduction

DC offsets drastically limit the performance and accuracy of analog and mixed-signal blocks, such as sample-and-hold (S/H) circuits. A common S/H circuit that cancels the input offset voltage of the op-amp [1] is shown in Fig. 1a and it operates as follows: 1) During the sample phase Φ_S, S_1 and S_2 are closed and S_3 is open, so, the op-amp is connected with unity gain feedback and the capacitor stores the value $V_{Cin}=V_{in}-V_{os}$. 2) During the hold phase Φ_H, S_1 and S_2 are open and S_3 is closed, so, C_{in} is connected to the output of the op-amp and the output voltage takes a value $V_{Cin}+V_{os}=V_{in}$. An advantage of this scheme is that the inputs of the op-amp always remain at a constant voltage (close to mid supply) and do not change with the applied input signal. Disadvantages of this scheme are that the accuracy of offset compensation is affected by charge injection Q_{inj} from S_2 when it opens. This introduces and error $\Delta V_o=Q_{inj}/C_{in}$ in the voltage V_{Cin} that leads to a modified value $V_{Cin}'=V_{Cin}+\Delta V_o=V_{in}-V_{os}+\Delta V_o$. Given that the offset voltage is very small, the charge injection error ΔV_o can be comparable to V_{os} unless large capacitors C_{in} are used. Increasing C_{in} (which is in the signal path) is detrimental to speed because it adds non-dominant poles. Also, the output resets to zero during the sample phase and this imposes a speed limitation. The fully differential (FD) configuration of the circuit shown in Fig. 1b alleviates the charge injection problem, however, the mismatch of charge injection of S_2 and S_2' and of the input capacitors still limits the accuracy in the offset cancellation. This scheme is representative of most offset cancellations schemes that store the relatively small value V_{os} at **face value** during one phase and compensates it during a second phase [2]-[4].



(a)



(b)

Fig. 1. Simple switched- capacitor sample and hold. (a): Single ended. (b): Fully differential.

A simple, non-offset compensated fully differential track and hold (T/H) circuit [1], [5] that does not reset the output of the op-amp to zero is shown in Fig. 2a. It is based on a two-stage Miller op-amp with two differential input stages (differential difference amplifier) [6]-[7] whose outputs are connected in parallel at nodes A and B to common active loads. The transistor level implementation of Fig. 2a is shown in Fig. 2c. Nodes A and B drive a FD output stage.

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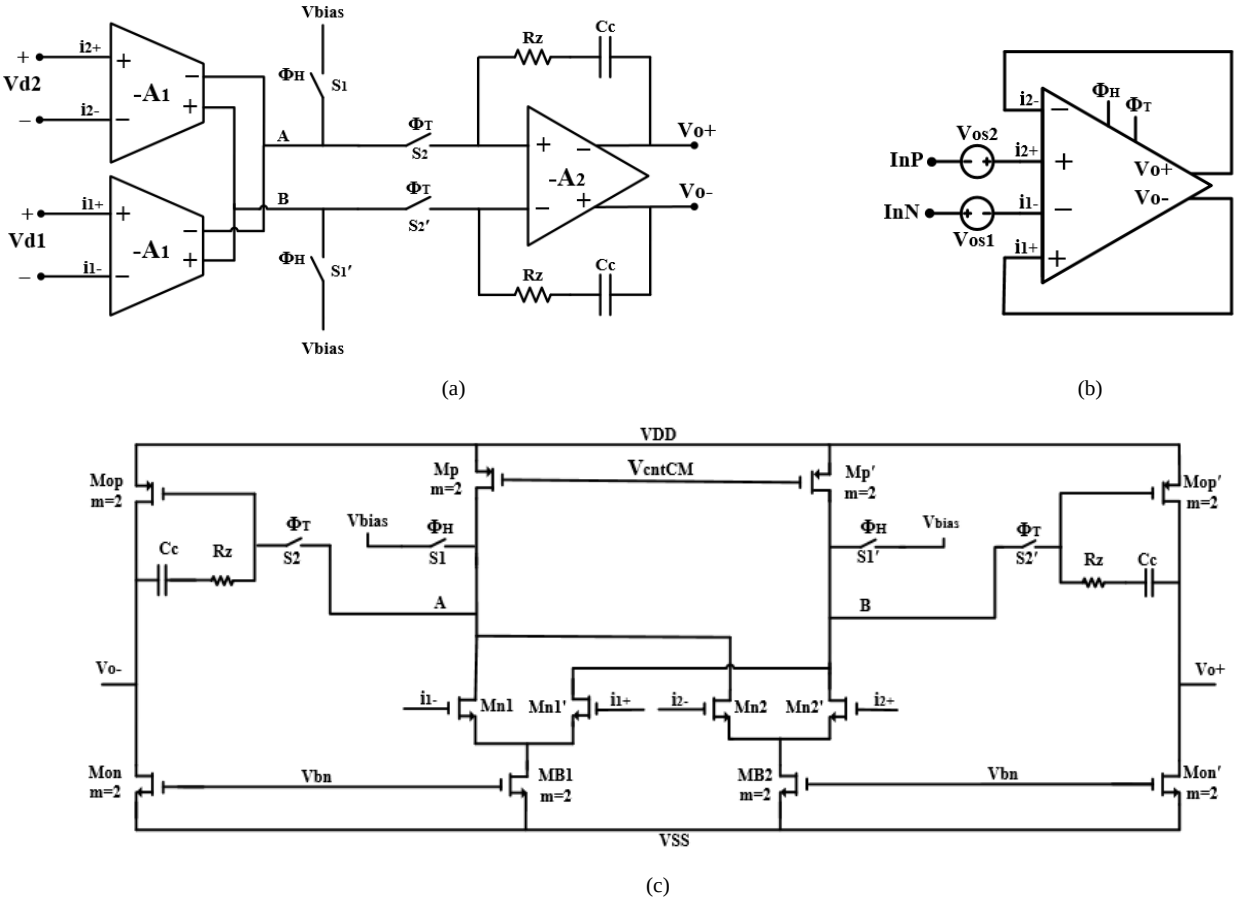

(a) (b)

(c)

Fig. 2. Clocked fully differential conventional T/H. (a): Internal structure. (b): Voltage follower configuration. (c): Transistor level schematic.

It operates as follows: During the track phase, switch S_2, S_2' are closed and S_1, S_1' are open. This connects the op-amp as a FD voltage follower (Fig. 2b), and the output voltage follows the input voltage including the offset error $V_o=V_{in}+V_{os1}+V_{os2}$. At the end of the track cycle, when S_2, S_2' opens, the output voltage is held during the hold phase in the compensation capacitors C_c and the outputs of the first stage (A_1) are connected to DC voltages V_{bias} in order to prevent their saturation. A sample and hold can be implemented by cascading two track and hold circuits with complementary control phases. This scheme allows higher operating speed since the output of the op-amp does not go to zero during the track phase Φ_T. An additional advantage is that no capacitors are inserted in series with the signal path.

In section II of this paper we present a modified offset compensated version of this circuit. It includes additional auxiliary circuitry that stores an amplified version of the total offset. This makes the scheme less sensitive to charge injection, and to other errors. Simulation and experimental results are discussed in section III. Summary and conclusions are given in section IV.

II. PROPOSED OFFSET COMPENSATED MILLER T/H

The track and hold (T/H) circuit of Fig. 3 is a modified version of the circuit of Fig. 2 that is able to compensate offset by storing its amplified version. This is done in order to make offset compensation less sensitive to charge injection and to other errors. A differential input stage (A_{oc1}) and an auxiliary differential output stage (A_{oc2}) have been added in order to store an amplified version of the total offset voltage. The outputs of three input stages (terminals A and B) are connected in parallel. Fig. 3c shows the transistor level schematic of the proposed T/H. The auxiliary input stage (A_{oc1}) is formed by transistors M_{n3}, and M_{n3}' while the auxiliary output stage (A_{oc2}) is formed by M_{ocp}, M_{ocn}, M_{ocp}', and M_{ocn}'. The proposed circuit works as follows:

1) During the hold phase Φ_H, switches S_3, S_3', S_5, and S_5', are closed (Fig. 4a). This connects the inputs of the main amplifier to ground while the auxiliary amplifier implements an amplifier with gain $G_{oc}=1+R_2/R_1$. Its output voltage is given by $V_{oc}=(1+R_2/R_1)(V_{os1}+V_{os2}+V_{os3})$.
2) During the track phase the main amplifier is connected as a FD buffer and the amplified offset V_{oc} is held by the compensation capacitors C_{coc} (Fig. 3b). In this case V_{oc} performs as a DC voltage source that generates a voltage V_X-V_X'$=V_{os1}+V_{os2}+V_{os3}$ at the input of the auxiliary amplifier. This compensates the offset of all input stages and leads to an offset free main amplifier output $V_o=V_{in}$.

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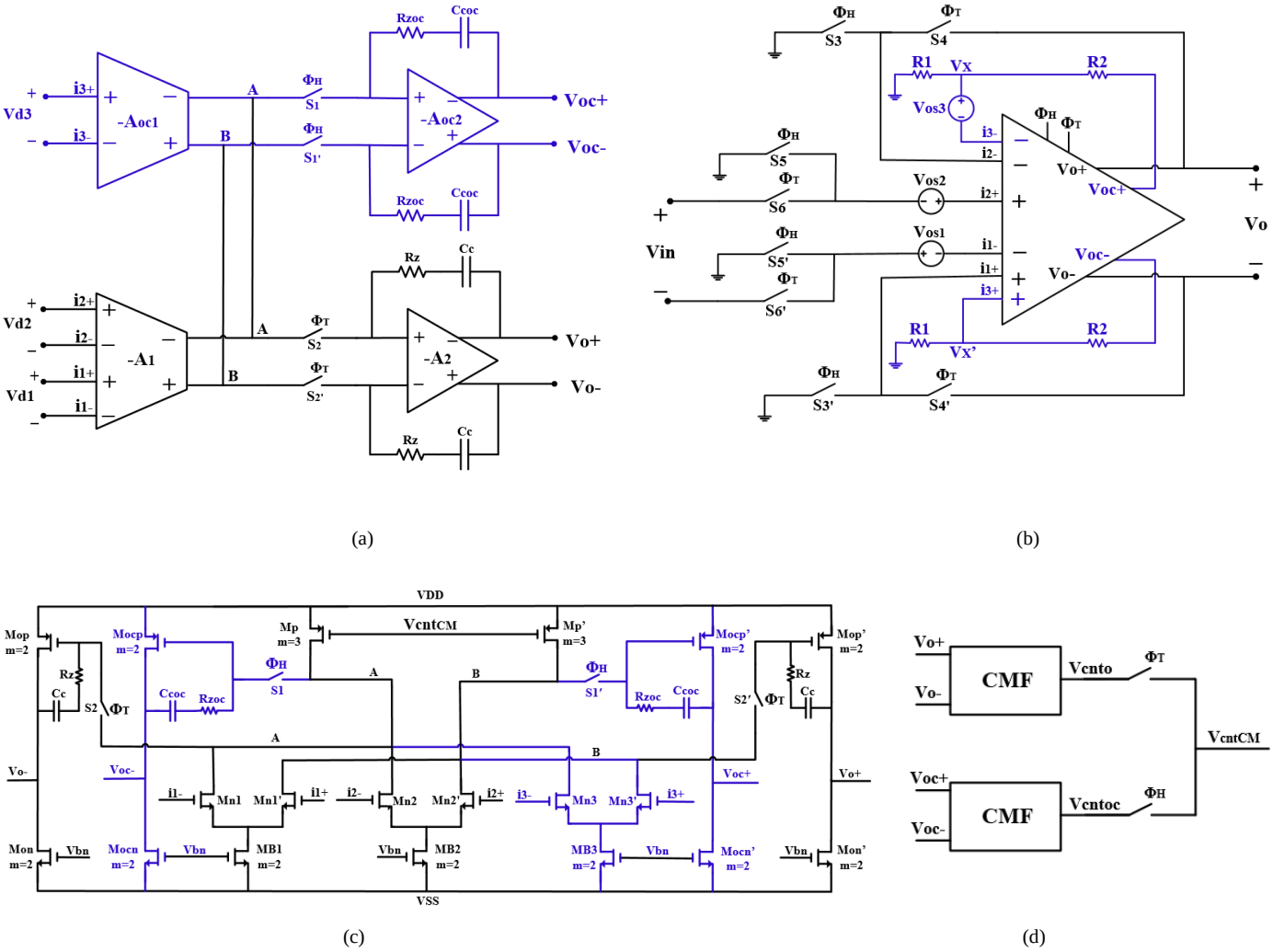

Fig. 3. Clocked fully differential offset compensation T/H. (a): Internal structure. (b): Voltage follower configuration. (c): Transistor level schematic. (d): Implementation of CMF in FD T/H.

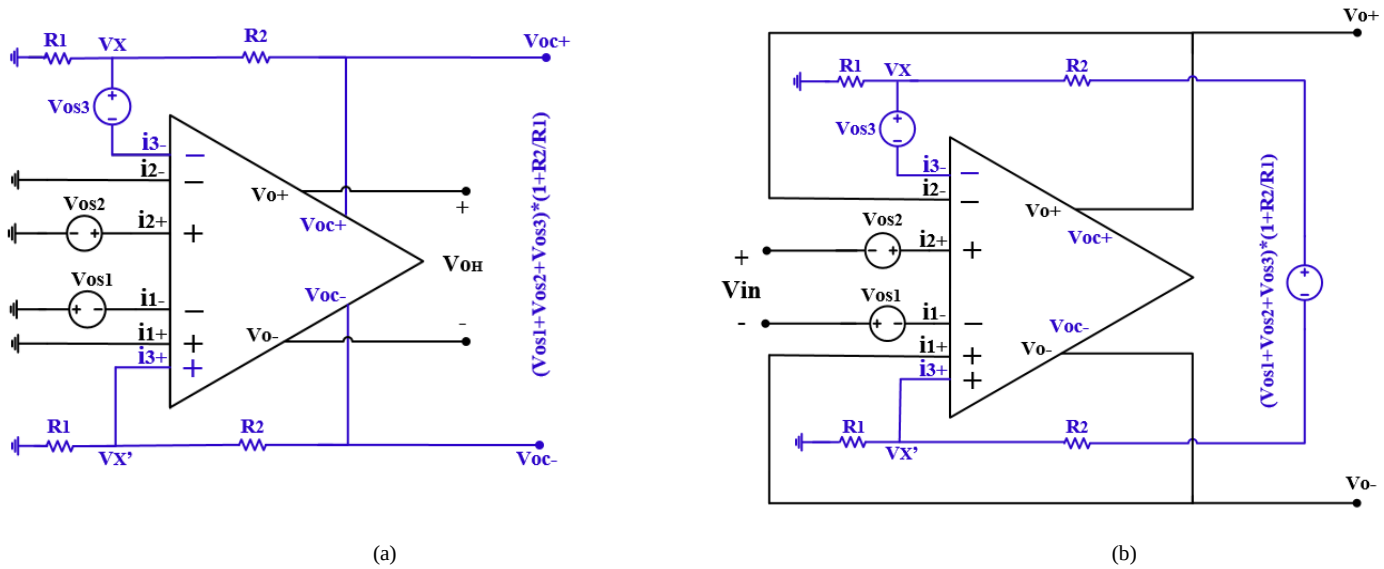

Fig. 4. Proposed T/H circuit including offset voltages. (a): During hold phase Φ_H. (b): During track phase Φ_T.

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Remarks:

a) The proposed scheme is less sensitive to charge injection errors than conventional schemes since it stores an amplified version of the total offset V_{oc} in C_c. In practice, G_{oc} is subject to gain errors due to the finite gain of the DC loop and to resistive loading. Given that the offset compensation voltage V_X-V_X'=V_{oc}/G_{oc} is an attenuated version of V_{oc} the gain errors are cancelled out and do not affect the accuracy of the proposed scheme.

b) Output offset compensation schemes in multistage comparators also store an amplified version of the input offset in capacitors in the signal path [8]. However, they are feedforward structures that have no global feedback.

c) Conventional auto zero techniques also use an auxiliary amplifier to store an offset compensation voltage V_{oscomp} in a capacitor given by $V_{oscomp}=(A_m/A_a)V_{osm}+V_{osa}$ where A_m and A_a are the gains of the main and auxiliary amplifiers respectively and V_{osm} and V_{osa} are their associated offsets [8]. It can be seen that V_{osm} is amplified by a factor A_m/A_a (typically about 10) while V_{osa} is not amplified. Due to this, the cancellation of V_{osa} remains sensitive to charge injection errors. Also, in auto-zeroing techniques the switches connected to the offset storage capacitors have a charge injection error that depends on the stored amplified offset voltage (V_{oscomp}). The switches do not have the same charge injection since their gate-source voltages are not equal. This is due to the fact that the switches transfer complementary voltages ($V_{oscomp}/2$, $-V_{oscomp}/2$) to the offset storage capacitors. This also makes conventional auto-zero techniques sensitive to charge injection even without mismatch in the switches. The approach proposed here is less sensitive to charge injection because all switches driving C_{coc}, and C_c (S_1, S_1', S_2, and S_2') have equal and constant gate-source voltages that do not depend on the amplified offset voltage V_{oc} stored in the Miller capacitor C_{oc}.

d) Note that the proposed scheme, as opposed to a ping-pong architecture, i.e. [9], stores an amplified version of the total offset during one phase. Ping-pong architectures use two independent auto zeroing stages operating with alternative phases.

e) The DC offset compensation loop (auxiliary stage) in the proposed scheme increases power consumption and area. Since the output of the auxiliary stage is not connected to a capacitive load, the compensation capacitor C_{coc} can be small. (Fig. 3c) and A_{oc2} can operate with low quiescent current and down scaled transistor sizes i.e. by a factor of 5 but at the same time with the same bandwidth as the main feedback loop. This allows to decrease the power and area requirements of the DC offset compensation circuitry and the quiescent power dissipation by %20.

f) In order to improve the accuracy of the offset compensation without the risk of saturating the output of the auxiliary amplifier, a moderate gain G_{oc}=20 was selected. In this case, with typical offsets V_{os}~5-10mV the output V_{oc} still represents an essentially amplified version of the total offset $V_{os}=V_{os1}+V_{os2}+V_{os3}$.

g) The proposed circuit uses two common mode feedback networks (CMF). Their common mode control voltages V_{cnto} and V_{cntoc} are connected alternatively to V_{cntCM} as shown in Fig. 3.

h) Resistors R_1, and R_2 in Fig. 3 contribute to input noise. In order to reduce this contribution, a capacitor (in parallel with R_2) can be used to limit the resistor's noise bandwidth.

III. SIMULATION AND EXPERIMENTAL RESULTS

A test chip prototype including a non-overlapping clock generator, and both the conventional and offset compensated Miller T/H circuits of Figs. 3 and 4 respectively were fabricated in 0.18 µm CMOS technology with NMOS and PMOS threshold voltages of approximately 0.45 V.

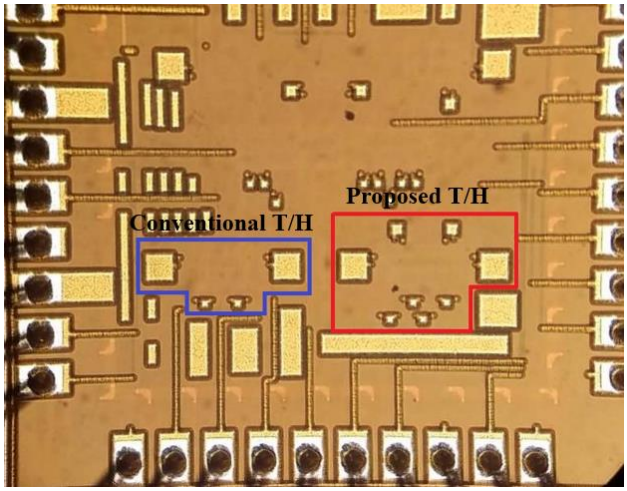

Fig.5. Photograph of test chip including offset compensator and conventional T/H designs.

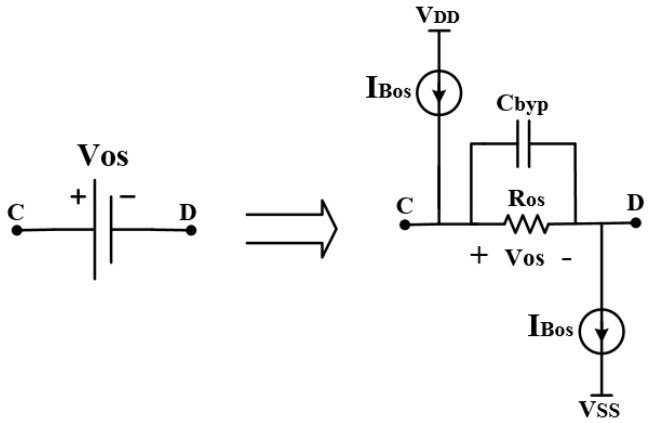

Fig. 6. Floating battery acting like an externally controllable DC offset source for test purposes.

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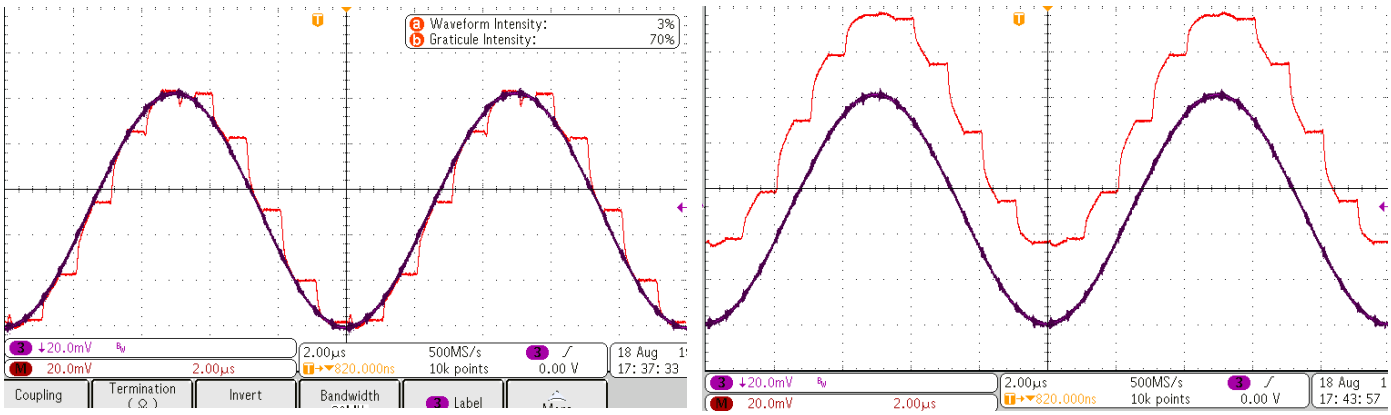

(a) (b)

Fig. 7. Experimental Input and output differential waveforms of fabricated circuit (100 mVpp at 100 kHz input signal, 1 MHz input clock, and 40 mV total offset). Horizontal scale 2 µs/div., vertical scale 20 mV/div. (a) Proposed T/H. (b) Conventional T/H.

The unit transistor dimensions in micrometer are $(W/L)p$=(100/0.7) and $(W/L)n$=(20/0.7). Sizes of PMOS and NMOS transistors of NAND and Inverter gates used in digital non-overlapping clock generator are respectively $(W/L)p_{(NAND,INV)}$=(0.88/0.22), and $(W/L)n_{(NAND,INV)}$=(0.44/0.22). PMOS and NMOS transistors in the complementary switches had dimensions $(W/L)psw=(W/L)nsw$=(0.22/0.22). Capacitances and resistors have values C_c=10 pF, C_{coc}=2 pF, R_z=3 kΩ, R_{zoc}=1 kΩ, R_1=8 kΩ, R_2=150 kΩ. Fig. 5 shows the micrograph of the fabricated chip. The dimensions of the conventional and offset compensated circuits were 372 µm × 190 µm (0.07 mm^2) and 400 µm × 270 µm (0.11 mm^2) respectively. Three independently controllable floating batteries generating offsets V_{os1}, V_{os2} and V_{os3} were included in the circuit for testing purposes. They were implemented as shown in Fig. 6 using two matched DC current sources I_{Bos} and a resistor R_{os}=5 kΩ in parallel with a small bypass capacitor C_{byp}=1 pF. The circuit was simulated and tested with dual supplies ±0.9 V; a bias current I_{bias}=200 µA and load capacitance C_L=23 pF. Simulations of the circuit of Fig. 3 (with Φ_H set to V_{SS} and Φ_T to V_{DD}) led to a DC open loop gain A_{ol}=53 dB and gain-bandwidth GB=40 MHz. The circuit was able to remove accurately large offsets even when the peak-peak input signal was as small as 50 mV and the total offset around 40 mV ($V_{os2}=V_{os3}=V_{os3}$=13.5 mV). Figs. 7a and 7b show the experimental input and output waveforms of the proposed offset compensated and conventional T/H. The circuits were tested with 100 mVpp 100 kHz input signal with a 1 MHz clock and a load capacitance C_L=23 pF. The total applied offset (controlled externally) was approximately 40 mV. Harmonic distortion measurements with the presence of total applied offset V_{os}=40 mV shows that SFDR is 7 dB higher in the proposed scheme (68 dB) than in the scheme without offset compensation (61 dB).

IV. CONCLUSION

A method for offset compensation in Miller (Integrating) sample and holds was presented. It stores an amplified version of the total offset in Miller capacitors and this amplification reduces its sensitivity to charge injection. Experimental results of a test chip in 0.18 µm CMOS technology validated experimentally that the circuit can compensate large DC offset voltages.

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