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An Enhanced Gain-Bandwidth Class-AB Miller Op-Amp With 23,800 MHz·pF/mW FOM, 11-16 Current Efficiency and Wide Range of Resistive and Capacitive Loads Driving Capability

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ABSTRACT A compact power-efficient class-AB Miller op-amp is introduced. It uses a simple auxiliary circuit that enhances the op-amp's gain-bandwidth product and helps to drive a wide range of capacitive and resistive loads with high static and dynamic current efficiency. Simple Miller compensation is used to obtain stability over a wide range of loading conditions. The op-amp's simulation and experimental results in strong inversion with 15μA bias current and in sub-threshold with 250nA bias current are shown. Its performance is measured in terms of dynamic and static current efficiency figures of merit $\text{FOM}_{\text{CEDyn}}$ and $\text{FOM}_{\text{CEStat.}}$ and using the conventional small-signal figure of merit $\text{FOM}_{\text{SS.}}$ Experimental results of op-amps fabricated in a 130nm CMOS technology are shown that validate the proposed approach.

INDEX TERMS Analog integrated circuit, class-AB amplifier, Miller compensation, voltage follower, wide range load.

I. INTRODUCTION

The conventional class-A (Conv-A) Miller op-amp with the NMOS differential input stage is shown in Fig. 1. It can provide relatively large positive output currents and a maximum negative output current that is limited by the quiescent current of the output transistors I_{MOutQ} determined by M_{ON}. This current also limits the slew-rate of the op-amp to a low value $SR = I_{MOutQ}/(C_c + C_L)$ and the current efficiency $CE{=}I_{outMAX}/I_{totQ}$ to a value $CE{=}I_{MOutQ}/(I_{MOutQ}{+}2I_B) < 1$ (CE<0.5 in most class-A op-amps) where I_B and I_{totQ} are the bias and total quiescent current of the op-amp. Some approaches [1], [2] have been published to implement power-efficient class-AB output stages that can provide transient maximum negative and positive output currents much larger than I_{MOutQ} during a limited period of time τ. The value of τ depends on the RC time constant of a high pass network used in the op-amp. These approaches are appropriate for purely capacitive loads and/or for resistive loads at signal frequencies $f \gg 1/(2\pi RC)$. This kind of op-amp is called here dynamic-class-AB op-amp. A simple implementation of such dynamic-class-AB Miller op-amp denoted "Free-Class-AB op-amp" (Free-AB) was reported in [1] and it is shown in Fig. 2. It requires just one additional large resistance device

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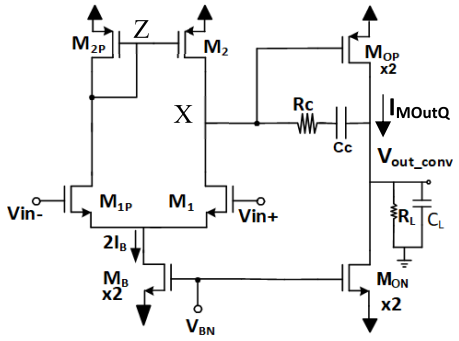

FIGURE 1. Class-A miller op-amp with NMOS input stage.

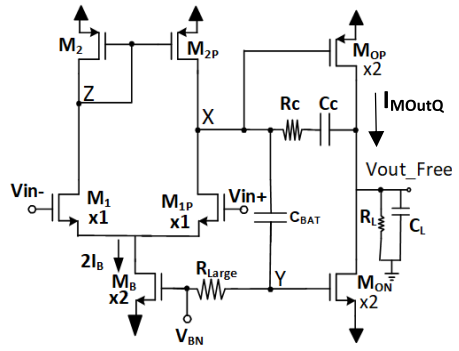

FIGURE 2. Free-Class-AB op-amp.

R_{Large} ∼100kΩs and a moderate-sized capacitor C_{BAT}∼pFs. This scheme is very efficient since it does not increase quiescent power dissipation or supply requirements. It is a dynamic approach that uses the capacitor C_{BAT} as a battery during a short period that passes fast transient voltage variations at node X to node Y with small attenuation. A limitation of the Free-Class-AB approach is that it can hold large peak negative output currents only during a period of time that is determined by the time constant $\tau = R_{Large}C_{BAT}$. Even though τ can be made relatively large (in the range of seconds) utilizing quasi-floating gate transistors [3] to implement values R_{Large} ∼ 10GΩs. However, it has the following disadvantages: a) it still cannot hold a large negative current (or voltage) at the output for a very long period of time or indefinitely as it is required in some applications (i.e., in temperature control, some biomedical and some instrumentation applications, etc.) and b) it can lead to a relatively long turn-on time of the op-amp which is not convenient for power management applications. Other reported approaches can deliver large negative currents indefinitely. These are called here "static-class-AB amplifiers" and can be used for high resistive loads (low valued resistance) that might require a large negative load current for an extended period of time or even indefinitely.

Most static-class-AB approaches [4]–[6] require relatively complex additional control circuitry. This can increase the supply requirements and static power dissipation. It leads to a degradation of the op-amp current efficiency CE, defined by $CE{=}I_{outMAX}/I_{totQ}$ where $I_{outMAX} = Min\{I_{outMAX}{}^{+}, |I_{outMAX}{}^{-}|\}$ is the minimum of the peak static positive and

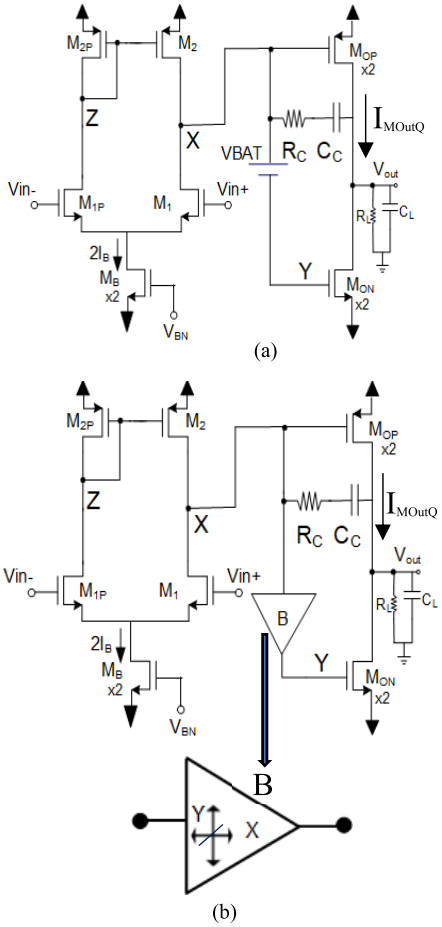

FIGURE 3. (a) Class-AB output stage of an op-amp with floating battery (b) Buffer with level shift acting as a floating battery.

negative output peak currents. For this reason, they cannot be used in modern CMOS technology that operates from reduced supply voltages with the requirement for high current efficiency (i.e., in IoT edge node applications). The circuits of [7] and [8] are popular static-class-AB output stages. However, they have very low CE with reduced supply voltage. The basic implementation of a static-class-AB (push-pull) output stage can be represented conceptually by the insertion of a circuit that mimics a floating battery V_{BAT} between the gates of the two output transistors as shown in the op-amp with an NMOS differential input stage of Fig. 3(a). In this scheme, the floating battery V_{BAT} transfers voltage variations at the gate of the PMOS output transistor (node X) to the gate of the NMOS output transistor (node Y). Positive voltage changes in node X lead to positive changes in node Y. This causes the current in the NMOS output transistor to increase and at the same time, the current in the PMOS transistor to decrease. When X decreases, Y decreases too, causing the current in the PMOS output transistor to increase and that of the NMOS output transistor to decrease. This "push-pull" operation generates negative output currents which can be larger than the static current I_{MOutQ} of the output stage. The practical implementation of the floating battery requires additional

control circuitry to establish the desired nominal quiescent current I_{MOutQ} at the output stage. This I_{MOutQ} is set by the quiescent gate voltage Y of the NMOS output transistor. This control circuitry automatically adjusts the value of V_{BAT} so that the quiescent gate-source voltage of the NMOS output transistor $V_{GSQN} = (V_{DD} - V_{SS}) - V_{SGQP} - V_{BAT}$ generates a quiescent current $I_{MOutNQ,}$ which matches the desired nominal quiescent current I_{MOutPQ} of the PMOS output transistor, where V_{GSQN} and V_{SGQP} are the gate source voltages of M_{ON} and M_{OP}. This is set by the quiescent value of the voltage at node X, which should match the quiescent voltage V_Z at node Z. In a robust design this should be independent of the value of the total supply voltage $V_{supply} = V_{DD} - V_{SS}$, of transistor/technology parameters and of temperature variations. A drawback of the basic scheme of Fig. 3(a) is that the peak positive variation of the voltage at node X is limited to a maximum value V_{SGQP} (but it is smaller in practice). This relatively small positive change in X transferred to node Y can lead to just a modest boosting in the negative output current (and in the negative slew rate and CE). Therefore, this basic scheme is characterized by a relatively low current efficiency CE with reduced supply voltages. Another way to represent the scheme of Fig. 3(a) is in terms of a unity gain auxiliary buffer with level-shift connected between nodes X and Y as shown in Fig. 3(b). Many authors have reported static-class-AB output stages based on direct implementations of the floating battery (i.e., [7]–[9]) of Fig. 3(a), where changes in X are transferred directly (in practice with attenuation) to Y as indicated before. The control circuitry increases the static power dissipation and the op-amp supply requirements and might not significantly boost the peak negative output current.

For this reason, most of the reported schemes based on the direct battery implementation are characterized by a *CE* value that is not much higher than that of a conventional class-A op-amp. A typical representative implementation of the scheme of Fig.3(b) based on the utilization of a source follower M_{VF} [9] is shown in Fig. 4 along with the required control circuit (enclosed in a box with dashed lines in Fig. 4b). In this implementation, the voltage follower transistor M_{VF} transfers variations from node X to node Y. If there is a body effect, it causes the variations at Y to be attenuated by approximately 20-30% w.r.to the variations at X. The inclusion of M_{VF} increases the op-amp's minimum supply requirements from $V_{DDsupplyMIN} = V_{GS}+2V_{DSsat}$ to a value $V_{DDsupplyMIN} = 3V_{GS}$ which prevents this scheme from being used in low voltage applications. A quiescent output current control circuit based on replicating the branches with the voltage follower and output transistors is shown in Fig. 4(b). The addition of the control circuit in this and other class-AB approaches (i.e., in [4]) increases the total quiescent power dissipation of the op-amp, reducing current efficiency and leading to a relatively modest boost of the peak negative output current.

In this paper, a power-efficient static-class-AB op-amp is reported that can drive both resistive and capacitive loads. Thus, it can provide static and dynamic positive and negative

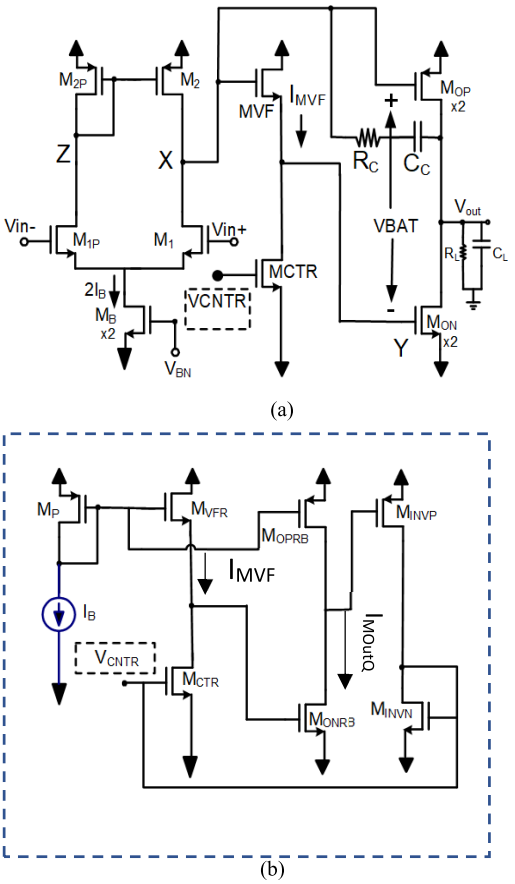

FIGURE 4. **(a) Example of Class-AB output stage using a VF as a battery with level shift (b) Replica bias control circuit for generation of V_{CNTR} so that quiescent output current is independent on V_{DD}, technology parameters, and temperature.**

load currents, which can be much higher than the quiescent current of the output stage I_{MOutQ}. This scheme uses a simple control circuit that does not increase the supply requirements and requires minimal additional quiescent current (15%). It is described in Section-II. The performance of the proposed op-amp is measured in terms of: a) the conventional small-signal Figure of Merit:$FOM_{SS} = f_u \cdot CL/P^Q$ here f_u denotes the unity gain frequency of the op-amp b) a large signal static current efficiency figure of merit: $FOM_{CEStat} = I_{outMAXRL}/P^Q$ and c) the conventional large signal dynamic current efficiency figure of merit:$FOM_{CEDyn} = SR \cdot C_L/P^Q$ which is related to the maximum dynamic output current in load capacitance C_L. FOM_{CEStat} is determined by the maximum DC output current in load resistor R_L (denoted $I_{outMAXRL}$) relative to the total quiescent power P^Q of the op-amp. Two additional figures of merit are also reported here in order to account for the Silicon area:

a) $AFOM_{CEDyn}=(SR\cdot C_L)/(P^Q\cdot Area)$,
b) $AFOM_{SS} = (f_u \cdot C_L)/(P^Q\cdot Area)$.

Where Area is the Silicon Area. Section-III shows the simulation results of the proposed class-AB amplifier in strong inversion and in subthreshold. Section-IV shows experimental results of a fabricated test chip prototype that

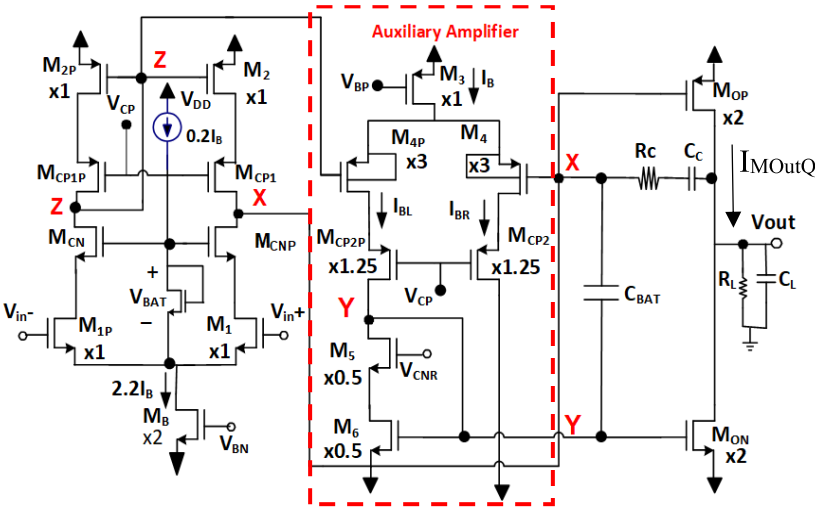

FIGURE 5. Proposed op-amp.

includes a conventional class-A, a Free-AB, and the proposed op-amp. All of them were fabricated on the same chip and operated with the same supply and bias currents. Section-V provides conclusions.

II. PROPOSED OP-AMP

In the proposed approach, a simple auxiliary amplifier is used to provide amplified voltage variations at node Y that are in phase with those at node X and set the quiescent output current I_{MOutQ} to a desired nominal value. The proposed op-amp is shown in Fig. 5. The auxiliary amplifier is formed by transistors M_3-M_6. Transistors M_4 and M_{4P} form a differential stage with a tail transistor M_3 that delivers a bias current I_B. The straightforward analysis shows that the small-signal gain from X to Y (assuming voltage at node Z is approximately constant) is given by $A_Y = V_Y/V_X = g_{m4}/(2R_Y)$ where R_Y is the resistance at node Y, and g_{m4} is the transconductance of $M_{4,4P}$. Transistors $M_{4,4P}$ have their sources connected to their bulk terminals and large W/L ratios to provide headroom to the tail transistor M_3 and increase the transconductance g_{m4} of M_4, M_{4P}. The voltage Y at the gate of the load transistor M_6 drives the output NMOS transistor M_{ON}, which is scaled up by a factor N=2 (as well as the PMOS output transistor M_{OP}) with respect to the unit size transistors used in the input stage. The quiescent voltage value of Y determines the quiescent current I_{MOutQ} in the output branch of the op-amp. The voltage V_{CNR} at the gate of cascode transistor M_5 is selected so that M_6 operates in triode mode close to the boundary of the saturation region. This causes the quiescent gate voltage Y to be higher than the value it would have if it were in saturated mode.

Consequently, a factor 12 times higher quiescent current flows in the output branch than in M_6(that has 0.5 times the size of unit size transistor) instead of a factor 4 times higher which would be the case if M_6 were in deep saturated mode. Positive signals in X larger than V_{SDsat4} cause all the tail current of M_3 to flow through M_6. This drives M_6 in deep triode mode and leads to a large positive voltage change in Y, resulting in large negative op-amp output currents. It can be seen that M_6 operates as an adaptive nonlinear load that increases its resistance (and the gain A_Y) for positive signals at node X. The nonlinear adaptive loads were introduced in [10] for applications in one-stage op-amps with improved slew rate and have been used since then by various authors [11], [12].

A telescopic differential input stage is used in order to achieve high open-loop gain even with low R_L values. When the op-amp drives a high resistive load (low valued R_L), the gain of the output stage is degraded. Consequently, the op-amp could have low open-loop gain and large gain-error with the conventional input stage, as shown in Figs. 1 and 2. The use of a high gain telescopic input stage in the proposed op-amp alleviates this problem. A capacitor C_{BAT} connected between the gates of M_{OP} and M_{ON} acts as a short circuit at high frequencies and helps to provide large negative dynamic currents to the capacitive load. Additionally, C_{BAT} eliminates the need for an additional compensation capacitor between node Y and the op-amp output as it is required in several reported class-AB op-amp implementations [12]–[14]. Conventional Miller compensation is used for stability purposes.

A. OPERATION

Class-AB operation. Let's assume the op-amp is used as a voltage follower. For positive input signals, the voltage at node X decreases, and the voltage at node Y also decreases according to $\Delta V_Y \approx A_Y \Delta V_X$. This increases the drain current of the PMOS output transistor M_{OP} and reduces the current of the NMOS output transistor M_{ON} resulting in a large positive op-amp output current. For negative input signals, the voltage at node X increases, and the voltage at node Y also increases by approximately a factor A_Y. (In practice it increases by a higher factor due to the nonlinear gain of A_Y that increases for large positive signals at X due to the operation of M_6 as nonlinear adaptive load). This reduces the current in the PMOS transistor and leads to a large increase in the drain current of

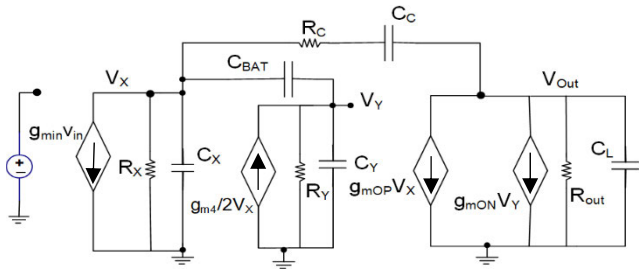

FIGURE 6. Small signal model of proposed static op-amp.

the NMOS output transistor M_{ON}. In this case, the op-amp can deliver peak negative output currents significantly higher than the quiescent current I_{MOutQ} of the output branch. This proposed scheme can work efficiently for resistive as well as for capacitive and mixed loads. For example, when a negative input step is applied for a resistive load, the proposed op-amp can provide a negative output voltage for an extended period of time or indefinitely.

Conversely, when a large capacitive load is used it requires large dynamic currents during the positive and negative edges. Assume a voltage follower with a resistive load $R_L = 200\Omega$ biased with $I_B = 15\mu$ A. If the input voltage changes from $V_{in} = 0$V to a negative DC voltage $V_{in} = -0.3$V the output terminal of the op-amp should provide, besides the dynamic current required by the capacitive load during the transition, a DC negative output current with value $I_{out} = V_{out}/R_L = -1.5$mA once the output settles to -0.3V. A conventional class-A op-amp with a quiescent current in the output branch $I_{MOutQ} = 30\mu$A can deliver a maximum negative output current limited to a value $I_{outMAXRL}{}^{-} = -30\mu$A. At the same time, a Free-Class-AB amplifier with the same quiescent current can provide a large negative current $I_{outMAXRL}{}^{-}$ only during a period determined by the time constant $\tau = R_{Large}C_{BAT}$.

B. AC ANALYSIS OF PROPOSED OP-AMP

The proposed op-amp uses conventional Miller compensation and a capacitor C_{BAT} like the Free-AB op-amp. This capacitor short circuits node X and Y at high frequencies, allowing high dynamic current efficiency and utilization of only one compensation capacitance C_C instead of two. It is common in several reported implementations of class-AB output stages [12]–[14]. A straightforward analysis leads to the well-known transfer function of a Miller op-amp given by (1). The small-signal model of the proposed op-amp is given in Fig. 6.

$$A_{OL}(s) = \frac{A_{OLDC}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{pDOMX}}\right)\left(1+\frac{s}{\omega_{pOut}}\right)} \tag{1}$$

The DC open-loop gain of the 1st stage of the proposed op-amp of Fig. 5 $A_{IDC} = V_X/V_d$ is given by (2).

$$A_{IDC} = g_{\min}(R_X) = g_{m1}(R_X) \approx (g_m r_o)^2 \Big/ 2 \tag{2}$$

where g_m and r_o are the transconductance gain and the unit size transistor's output resistance in the input stage (assuming for simplicity of notation equal g_m and r_o for PMOS and NMOS transistors). As indicated before, R_Y was selected so that the small-signal gain from node X to node Y has moderate value $A_Y \approx 1.5$. As indicated previously, this gain increases for large positive signals at X due to the nonlinear adaptive load.

The DC gain of the output stage A_{IIDC} is expressed by (3).

$$A_{IIDC} = \left(g_{mOut}{}^{eff}\right)_{dc}(R_{Out}) \tag{3}$$

Here, $(g_{mOut}{}^{eff})_{dc}$ is given by $(g_{mOut}{}^{eff})_{dc} = g_{mOP} + A_Y g_{mON}$ and R_{Out} is given by $R_{Out} = r_{OP}||r_{ON}||R_L$. Here, g_{mOP}, g_{mON} are the transconductance gains and r_{OP}, r_{ON} are output resistances of the output transistors M_{OP} and M_{ON} respectively. Hence, the total DC open-loop gain A_{OLDC} can be expressed by (4).

$$A_{OLDC} = A_{IDC}A_{IIDC} = (g_{m1}R_X)\left(g_{mOut}{}^{eff}\right)_{dc} R_{Out} \tag{4}$$

The dominant pole at node X is given by (5).

$$f_{PDOMX} = \frac{1}{2\pi R_X C_X} \tag{5}$$

where C_X is given by $C_X = (1-(-A_{IIDC}))C_C$ and R_X is expressed by $R_X = g_m r_o^2/2$. Thus, f_{PDOMX} can be expressed as (6).

$$\begin{aligned} f_{PDOMX} &= \frac{1}{2\pi R_X C_X} \\ &= \frac{1}{2\pi R_X (g_{mOP} + A_Y g_{mON}) R_{Out} C_C} \end{aligned} \tag{6}$$

The high-frequency pole at the output node is given by (7).

$$f_{Pout} = \frac{(g_{mOP} + g_{mON} + G_L)}{2\pi C_L} \tag{7}$$

where $G_L = 1/R_L$.

The zero is given by (8).

$$f_z = \frac{1}{2\pi C_C\left(R_C - \left(g_{mOut}{}^{eff}\right)_{hf}^{-1}\right)} \tag{8}$$

where the effective op-amp output conductance at high frequencies (at which C_{BAT} bypasses the auxiliary amplifier) is given by $(g_{mOut}{}^{eff})_{hf} = g_{mOP} + g_{mON}$.

From (4) and (6), the GBW of the proposed op-amp is given by (9).

$$GBW = A_{OLDC}f_{PDOM} = \frac{g_{m1}}{2\pi C_C} \tag{9}$$

From (3) and (7) it can be seen that the open-loop gain and the high-frequency output pole f_{POut} of the op-amp are strongly dependent on R_L. When the Op-amp drives a high load (low R_L/ high G_L) the DC gain of the output stage is degraded to low values $A_{IIDC} \ll 1$. This also degrades the op-amp DC open-loop gain. Thus, to prevent a large gain error in the proposed op-amp a telescopic input stage with high gain $A_I \sim 1{,}000$V/V is used as indicated before. In this case, even

TABLE 1. Values of design parameters of the proposed op-amp.

Parameter	Strong inversion	Sub-Threshold
I_B, I_{totQ} (μA)	15, 105	0.250,2.5
C_C (pF)	4-5.5	5
C_L (pF)	5-300	5-300
R_C (kΩ)	3-8.5	150
R_L(kΩ)	0.250-1000	7-1000
C_{BAT}(pF)	2	10
NMOS(unit transistor's W/L)(μm)	10/0.27	10/0.27
PMOS(unit transistor's W/L)(μm)	40/0.27	40/0.27

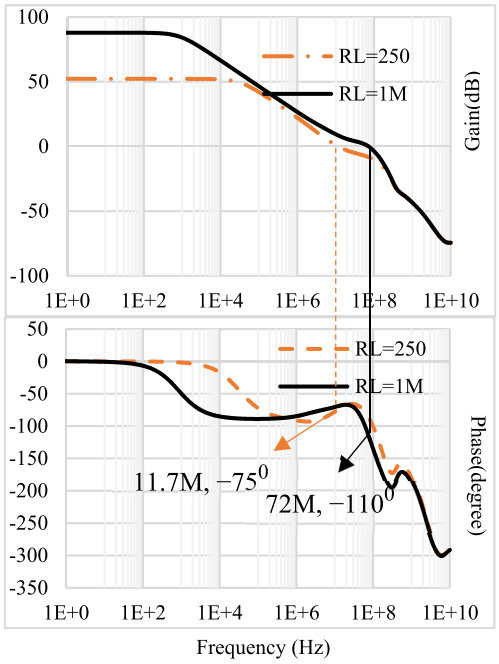

FIGURE 7. Open-loop frequency response of proposed op-amp in strong inversion for C_L = 5pF and resistive load R_L = 250Ω and 1MΩ.

with low R_L values the DC open-loop gain remains relatively high $A_{OLDC} = A_{IDC}A_{IIDC} \gg 1$. Table 1 shows the design parameters of the proposed op-amp, for strong inversion and sub-threshold conditions.

III. SIMULATION RESULTS

A. SIMULATION RESULTS IN STRONG INVERSION

The proposed, the conventional Class-A(Conv-A), and the Free-Class-AB op-amps of Figs. 1, 2, and 5 were designed in 130-nm CMOS technology with NMOS and PMOS unit transistor sizes $(W/L)_N = 10\mu m/0.27\mu m$ and $(W/L)_P = 40\mu m/0.27\mu m$. They were all simulated with the same bias current $I_B = 15\mu A$ and supply voltage 1.2V. The Conv-A and Free-Class-AB op-amp have conventional input stages with simple (non-cascoded) current mirror loads. Figs. 7, 8, and 9 show the open-loop responses of the proposed op-amp for various combinations of capacitive and resistive loads C_L and R_L. In the simulations, three values of capacitive loads: 5pF, 25pF, 300pF, and two values of resistive loads: 1MΩ and 250Ω are used. Table 2 summarizes

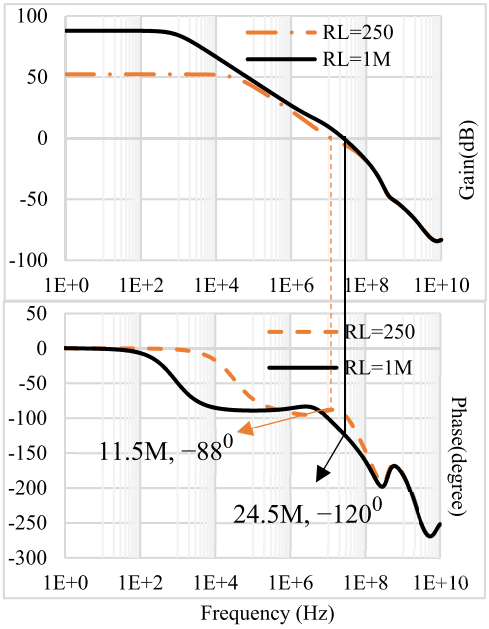

FIGURE 8. Open-loop frequency response of proposed op-amp in strong inversion for C_L = 25pF and resistive load R_L = 250Ω and 1MΩ.

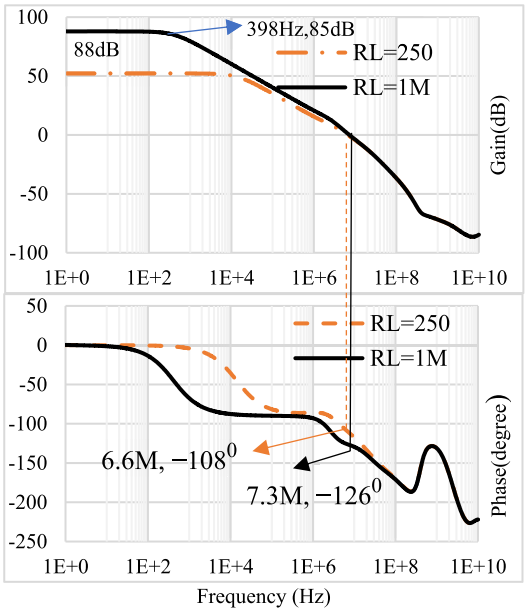

FIGURE 9. Open loop frequency response of proposed op-amp in strong inversion for C_L = 300pF and resistive load R_L = 250Ω and 1MΩ.

the open-loop response parameters obtained from AC simulations for the proposed op-amp, the conventional class-A, and the Free-Class-AB(Free-AB) op-amps. It can be observed that the proposed op-amp is stable for the wide range of combinations of capacitive and resistive load values used. For the Conv-A and Free-AB op-amps, the DC open-loop gains degrade severely to only 9.6dB for low valued load resistors, while for the same resistive loading conditions, the proposed op-amp still provides a relatively high DC open-loop gain of 52.2dB. Fig. 10 shows the transient response of the proposed op-amp for 5pF, 25pF, and 300pF load capacitors

TABLE 2. Open-loop response parameters of op-amps.

C_L (pF)	Open-loop DC Gain (dB)						Phase Margin (degree)						f_u (MHz)					
	R_L=1MΩ			R_L=250Ω			R_L=1MΩ			R_L=250Ω			R_L=1MΩ			R_L=250Ω		
	Conv-A	Free-AB	Prop	Conv-A	Free-AB	Prop	Conv-A	Free-AB	Prop	Conv-A	Free-AB	Prop	Conv-A	Free-AB	Prop	Conv-A	Free-AB	Prop
5	51.1	51.1	87.9	9.6	9.6	52.2	116	115	70	125	132	105	20	44	72	2	4.4	11.7
25	51.1	51.1	87.9	9.6	9.6	52.2	77	77	60	130	130	92	12.2	20.5	24.5	2	4.5	11.5
300	51.1	51.1	87.9	9.6	9.6	52.2	51	54	54	98	85	72	2	3.4	7.3	1.32	2.74	6.6
*Prop=Proposed op-amp																		

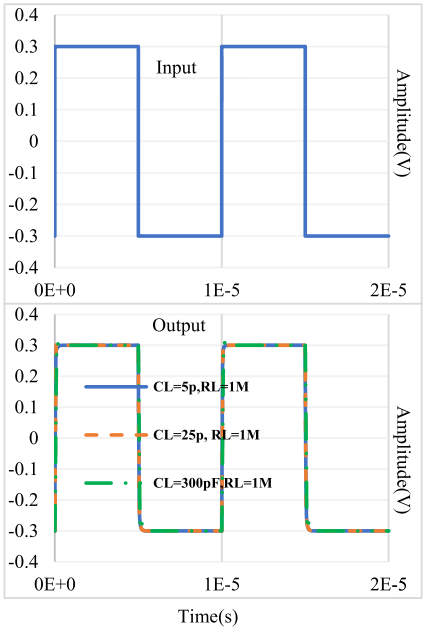

FIGURE 10. Simulated transient response of proposed op-amp for different capacitive loading condition in parallel with a fixed resistive load R_L = 1MΩ for ±300mV, 100kHz pulse.

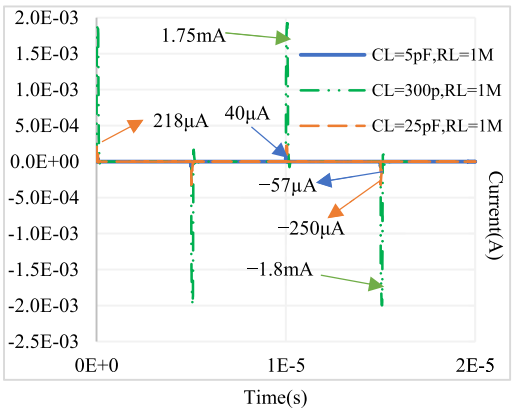

FIGURE 11. Output current of proposed op-amp for different C_L for R_L = 1MΩ.

with 1MΩ load resistors for a 100kHz input pulse with $600mV_{pp}$ (−300mV to 300mV) amplitude. Fig. 11 shows the capacitive load currents for different loading conditions.

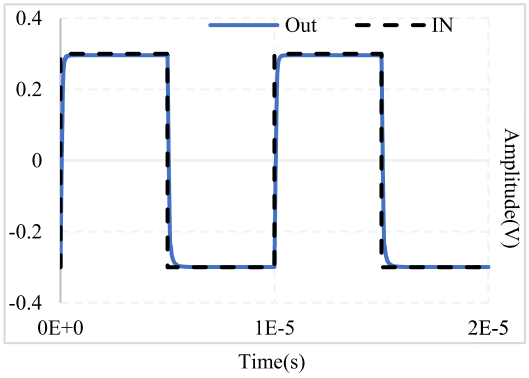

FIGURE 12. Proposed op-amp's transient response for C_L = 300pF in parallel with R_L = 250Ω for 100kHz (− 300mV to 300mV) input pulse.

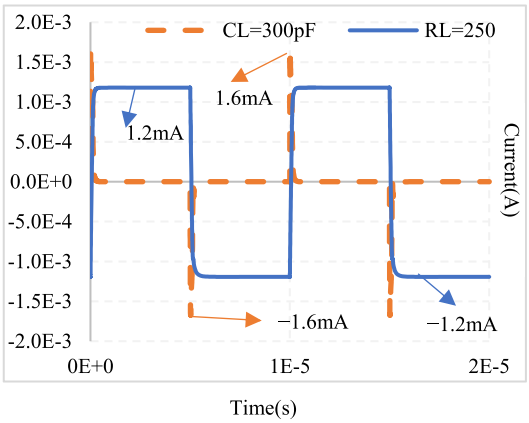

FIGURE 13. Dynamic and static output currents of the proposed op-amp for R_L = 250Ω and C_L = 300pF.

For a 300pF load capacitor, the proposed op-amp provides 1.75mA positive and 1.8mA negative peak output currents at the expense of 105μA total op-amp quiescent current I_{totQ}. Positive and negative slew rates are 6V/μs and −6 V/μs. It can be seen that the proposed op-amp has a very high dynamic current efficiency $CE_{Dyn} = I_{outCL}/I_{totQ} = 16$ where I_{outCL} is the load capacitor current.

Now, Fig. 12 shows the proposed op-amp's pulse response for C_L = 300pF and R_L = 250Ω. It can be observed that the op-amp can drive high capacitive as well as low resistive loads. The ±0.1% positive and negative settling times of the op-amp are 0.3μs and 0.7μs, respectively. Fig. 13 shows

TABLE 3. Corner analysis of the proposed op-amp at T = 90^0C.

		tt	ss	ff	fs	sf	SD
I_{totQ} (µA)	R_L (Ω)	110	110	115	111	108	2.3
A_{OLDC} (dB)	1M	84.5	88	76	87.6	76	5.4
PM (^{0})	1M	51	50	51	50	54	1.5
f_u (MHz)	1M	6.5	6.5	7.15	6.7	6	0.4
SR (V/µs)	1M	5.8	5.5	6.1	5.6	5.7	0.2
$I_{outMAXRL}$ (mA)	250	1.19	1.18	1.18	1.15	1.19	.01
THD/dB @R_L=250Ω, 50kHz, 300mV amplitude	250	−64.0	−64.1	−63.5	−64.1	−63.5	0.28

TABLE 4. Corner analysis of the proposed op-amp at T = 27^0C.

		tt	ss	ff	fs	sf	SD
I_{totQ} (µA)	R_L (Ω)	105	100	91	93	106	6
A_{OLDC} (dB)	1M	87.9	95	87	91	91	2.8
PM (^{0})	1M	54	50	50	48	49	2.03
f_u (MHz)	1M	7.08	8.8	8.4	8.5	9	0.7
SR (V/µs)	1M	5.8	5.5	6.1	5.6	5.9	0.2
$I_{outMAXRL}$ (mA)	250	1.19	1.18	1.18	1.18	1.19	0.004
THD/dB @R_L=250Ω, 50kHz, 300mV amplitude	250	−64.5	−64.7	−64.2	−64.7	−65.8	0.54

the output currents for $R_L = 250\Omega$ and $C_L = 300$pF. The maximum positive and negative currents in R_L are 1.2mA and −1.2mA, respectively. It can be seen that the proposed op-amp also has a high static current efficiency $CE_{stat} = I_{outMAXRL}/I_{totQ} = 11$. Thus, the op-amp can provide both dynamic and static output currents (to capacitive and resistive loads), which are much higher than its total quiescent current I_{totQ}.

In order to verify the sensitivity of the op-amp to process parameters and temperature, corner analysis of the proposed op-amp at temperatures 90°C, 27°C, and −20°C were performed. Tables 3, 4, and 5 show the results of the corner analysis.

TABLE 5. Corner analysis of the proposed op-amp at T = -20^0C.

		tt	ss	ff	fs	sf	SD
I_{totQ} (µA)	R_L (Ω)	109	115	106	115	104	4.5
A_{OLDC} (dB)	1M	89.5	89	88	88	89	0.6
PM (^{0})	1M	50	48	54	52	52	2.03
f_u (MHz)	1M	8.4	8	8.2	7.5	8.25	0.3
SR (V/µs)	1M	5.8	5.4	6	5.6	5.7	0.2
$I_{outMAXRL}$ (mA)	250	1.19	1.19	1.19	1.15	1.2	.02
THD/dB @R_L=250Ω, 50kHz, 300mV amplitude	250	−64.3	−64.5	−63.7	−65.0	−63.2	0.63

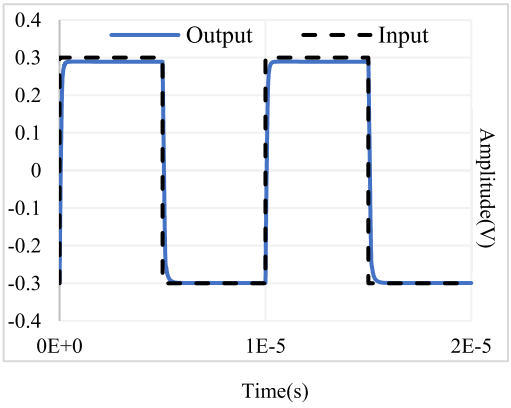

FIGURE 14. Transient response of the proposed op-amp for $R_L = 50$ || $C_L = 1000$pF for 100kHz (− 300mV to 300mV) input pulse.

From this analysis, it can be asserted that the proposed op-amp is robust against process and temperature variations.

Remark: If lower load resistors/higher load capacitors are required to be driven for some application, the proposed op-amp's output transistors can be scaled up as needed. For example, Fig. 14 shows the op-amp's transient response for a 50Ω resistive load in parallel with a 1nF capacitor load with the output transistors scaled up by a factor 4 w.r.to the size of the transistors used in the previously described op- amp.

In this case, the op-amp has approximately three times higher total quiescent current $I_{totQ} = 330\mu$A. Fig. 15 shows that the proposed op-amp can deliver a 5.8mA positive and 6mA negative output current to a 50Ω resistive load. It can provide 5.8mA positive and 4.2mA negative current to a 1nF capacitive load as well.

Fig. 16 shows the Conv-A and Free-AB op-amps' transient response with a 250Ω resistive load and 300pF capacitive load to a 100kHz 600mV$_{pp}$ input pulse in voltage follower

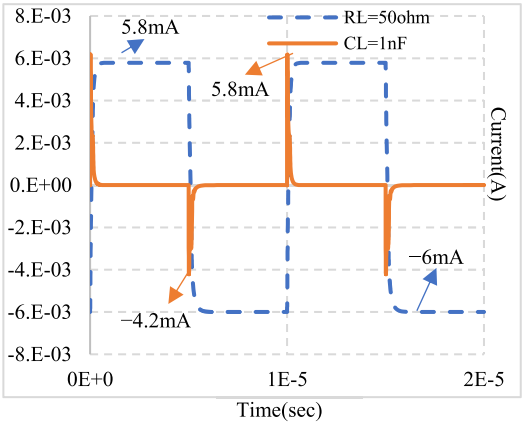

FIGURE 15. Transient current at $R_L = 50\Omega$ and $C_L = 1000$pF for 100kHz (− 300mV to 300mV) input pulse in the proposed op-amp.

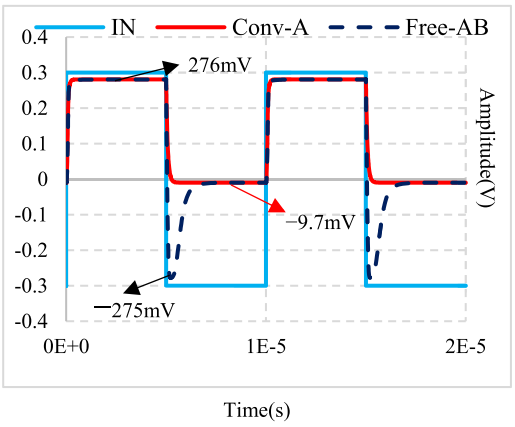

FIGURE 16. Conv-A and Free-AB op-amp's transient response for $C_L = 300$pF in parallel with $R_L = 250\Omega$ for 100kHz (− 300mV to 300mV) input pulse.

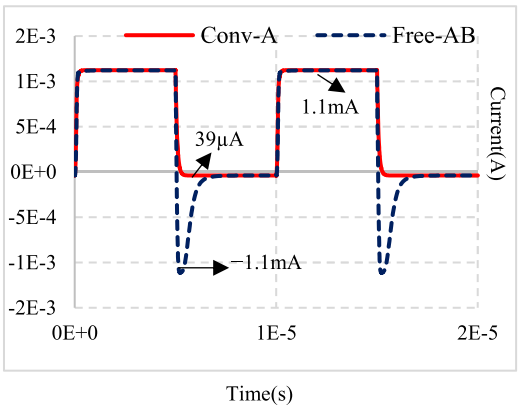

FIGURE 17. Currents in $R_L = 250\Omega$ for Free-AB and Conv-A op-amp.

configuration. The Conv-A op-amp's output voltages go from −9.7mV to 276mV, and the output voltages of the Free-AB op-amp go from −275mV to 276mV. However, the proposed op-amp's output can vary from −300mV to 300mV (shown in Fig. 12) for the same applied input. Notice that the Free-AB op-amp initially achieves −275mV output voltage during a short period of time and after approximately 1.2μs (that correspond to $3\tau = 3R_{Large}C_{BAT}$ time

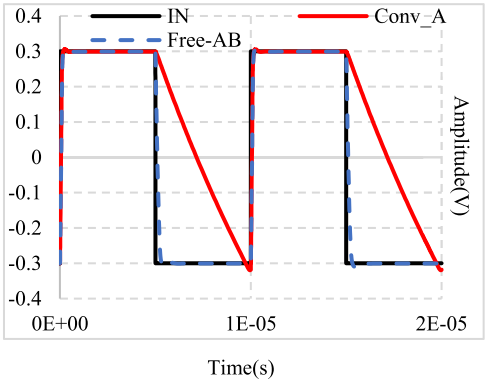

FIGURE 18. Transient response of Free-AB and Conv-A op-amp for ±300mV 100kHz pulse when $R_L = 1M\ ||\ C_L = 300$pF.

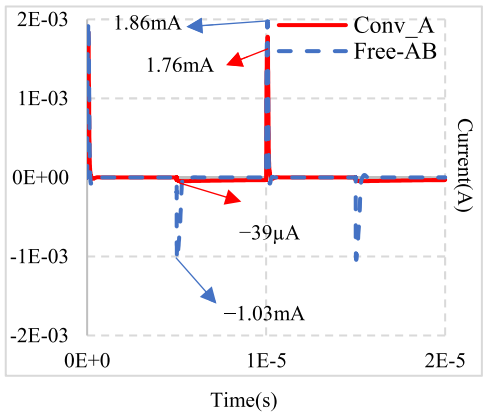

FIGURE 19. Dynamic currents in $C_L = 300$pF for Free-AB and Conv-A op-amp.

constants) C_{BAT} discharges, and the negative output voltage goes to −9.7mV, just like the Conv-A op-amp. In both cases, it is due to the maximum negative static output current limitation determined by the quiescent current I_{MOutQ} of the output branch. Fig. 17 shows the output currents in R_L in the Free-AB and the Conv-A op-amps for $R_L = 250\Omega$. As expected, the current in R_L for the Conv-A op-amp is limited by the quiescent current $I_{MOutQ} = 39\mu$A. In the Free-AB op-amp the output current in R_L after 1.2μs returns to $I_{MOutQ} = 39\mu$A. The slew rate of the Conv-A and Free-AB op-amp for $R_L = 1M\Omega$ can be obtained from Figs. 18 and 19. Fig. 18 shows the transient response of the Conv-A and Free-AB op-amps for $R_L = 1M\Omega||C_L = 300$pF. The positive output currents in C_L for the Free-AB and the Conv-A op-amps are 1.86mA and 1.76 mA. The negative output currents delivered to C_L are −1.03mA for the Free-AB and only −39μA for the Conv-A. The negative slew rates of the Free-AB and Conv-A op-amps are 3.4V/μs and 0.13 V/μs.

B. SIMULATION RESULTS IN SUBTHRESHOLD

The proposed and conventional op-amps were also simulated in sub-threshold with 1.2V supply voltage and a factor 60 times lower bias current $I_B = 250$nA. In this case, the op-amp can drive 5pF-300pF capacitive loads and resistive loads down to 7kΩ. Fig. 20 shows the transient

TABLE 6. Summary of the simulation results.

Parameters	Conv-A		Free-AB		Proposed op-amp	
	Strong inversion (SI)	**Subthreshold (ST)**	Strong inversion (SI)	**Subthreshold (ST)**	Strong inversion (SI)	**Subthreshold (ST)**
Technology (μm)	0.13	**0.13**	0.13	**0.13**	0.13	**0.13**
Supply (V)	1.2	**1.2**	1.2	**1.2**	1.2	**1.2**
I_{totQ} (μA)	68	**1.5**	68	**1.5**	105	**2.5**
Power(μW)	81.6	**1.8**	81.6	**1.8**	126	**3**
C_L (pF)	300	**300**	300	**300**	300	**300**
R_L(Ω)	1M/250	**1M/7k**	1M/250	**1M/7k**	1M/250	**1M/7k**
A_{OLDC} (dB)	51/9.7	**40.4/9.5**	51/9.7	**40.5/9.5**	88/52.2	**70/45**
PM (degree)	51/98	**51/103**	54/85	**50/102**	54/76	**55/82**
f_u(MHz) @R_L=1MΩ	4.5	**0.10**	5.4	**0.11**	10	**0.4**
SR(V/μs) @R_L=1M	0.1	**0.003**	3.3	**0.05**	6	**0.1**
$I_{outmax\ to\ RL}^{+}$(μA)	1127 @R_L=250 Ω	**41.4 @7k**	1127 @R_L=250 Ω	**41.4 @7k**	1200 @R_L=250 Ω	**42 @7k**
$I_{outmax\ to\ RL}^{-}$(μA)	39 @R_L=250 Ω	**0.7 @7k**	1100**/39 @R_L=250 Ω	**0.7 @7k**	1200 @R_L=250 Ω	**42 @7k**
FoM_{CEStat} @R_L=250 Ω (μA/ μW)	0.47	**0.38**	0.47	**0.38**	9.5	**14**
FoM_{CEDyn} @R_L=1M (V.pF/ μs.μW)	0.4	**0.5**	12	**8.3**	14	**10**
FoM_{SS} (MHz.pF/ μW)	17	**17**	20	**18**	24	**40**
***persist for 3τ						

response of the proposed op-amp in subthreshold for a 5kHz 600mV_{pp} (−300mV to 300mV) input pulse for 300pF||1MΩ and 300pF||7kΩ loading conditions. The ±0.1% positive and negative settling times are 9μs and 11 μs, respectively. Figs. 21 and 22 show the output current in the 300pF||1MΩ and 300pF||7kΩ loads. The output positive and negative static current in the 7kΩ load are 42μA when the 300pF capacitive load is there as well. The proposed op-amp can provide 39μA peak positive and 39μA peak negative dynamic output current for a 300pF load. In sub-threshold the total op-amp's quiescent current is $I_{totQsubTh} = 2.5\mu$A. Thus, it has a dynamic current efficiency $CE_{Dyn} = I_{outCL}/I_{totQsubTh} = 16$ and a static current efficiency $CE_{Stat} = I_{outMAXRL}/I_{totQsubTh} = 17$.

The total power dissipation of the op-amp in sub-threshold is 3μW. Fig. 23 shows the frequency response of the proposed op-amp in VF configuration for different capacitive and resistive loading conditions. From this frequency response, it can be asserted that, as expected, the proposed op-amp has higher bandwidth and can also drive a wide range of capacitive loads (C_L = 5pF-300pF) and resistive loads down to 7kΩ in subthreshold. Table 6 summarizes the simulation results for Conv-A, Free-AB, and proposed op-amps in strong inversion (SI) and sub-threshold (ST).

IV. EXPERIMENTAL RESULTS

A test chip prototype including the proposed, Conv-A, and Free-AB op-amps with C_C = 5.5pF, C_{BAT} = 2pF, R_C = 8.5kΩ, and R_{Large} = 200kΩ was fabricated in 130nm CMOS process technology. The circuits were tested with ±0.6V supply voltage and bias current $I_B = 15\mu$A. For testing purposes, all op-amps are configured in unity gain configuration as voltage followers. They were tested with two resistive loads (R_L = 1kΩ and R_L = 250Ω) in parallel with a 300pF load capacitor C_L. Fig. 24-26 show the experimental responses of the Conv-A, Free-AB, and proposed op-amps to a 100kHz ±600mV (rail to rail) triangular input signal with a 1kΩ load in parallel with a 300pF load capacitance. These are used to verify their input common-mode range.

Fig. 24 shows that the Conv-A op-amp has common mode input voltage range (CMIVR) from −40mV to 400mV. The lower value is determined by the quiescent current of the output branch. This value corresponds to a 40μA maximum negative output current on the1kΩ load resistor. The upper value is determined by the supply minus the drain-source saturation voltage of the PMOS output transistor. Fig. 25 shows that the Free-AB op-amp has CMIVR from −240mV to 440mV. The lower value (−240mV) indicates that the Free-AB op-amp initially can provide −240μA maximum negative output

TABLE 7. Summary of measurement results and performance comparison.

Parameter (units)	Proposed	[2] 2019	[16] 2016	[17] 2016	[18] 2015	[19]Fig.2 2014	[20] 2018	[21] 2019	[15] 2017
Inversion level	SI	SI	SI	SBT	SI	SI	SI	SI	SI
CMOS process (µm)	0.13	0.13	0.18	0.18	0.18	NA	0.18	0.18	0.18
Supply voltage (V)	± 0.6	± 0.6	1.8	0.7	±1.65	3.3	±0.9	1.8	±0.9
Capacitive load (pF)	300	50	200	20	20	30	25	5	23
Resistive Load(Ω)	1M/250	-	-	-	-	-	-	1k	-
SR(V/µs)	5.4	34	74.1	2.8	42	22	28	13.25	23.33
DC gain (dB)	87.8 @R_L=1M	83	72	57.5	82	68	90.8	105.5	67
PM (º)	54 @R_L=1M	62	50	60	NA	73	58.4	53	84
f_u(MHz)	10	63	86.5	3	NA	21.8	12.5	231.7	0.57
CMRR @DC (dB)	92	158	NA	19	85	75	68	-	-
PSRR+ @DC (dB)	86	67	NA	52.1	95	78	64	-	-
PSRR-@DC (dB)	90	50	NA	66.4	83	75	66	-	-
I_{outmax} to $R_{L=250\Omega}{}^{+}$ (µA)	1440	-	-	-	-	-	-	1200	-
I_{outmax} to $R_{L=250\Omega}{}^{-}$ (µA)	1000	-	-	-	-	-	-	-	-
I_{totQ}(µA)	105	158	6611	36.3	82	418	43	472	8.2
Power (µW)	126	190	11900	25.4	270	1380	80	850	14.5
Area (mm^2)	.025	.02	.07	.02	.02	.03	.021	0.45	0.03
Equivalent Input noise (nV/√Hz)	20 @ 1M	25@ 1M	0.8@0.1 M	100@1 M	-	-	27	194,224(@1Hz - 100MHz)	-
FOM_{CEDyn} (V.pF/ µs.µW)	12.8	9	1.25	2.2	3.2	0.47	8.8	.078	37
FOM_{SS} (MHz.pF/ µW)	23.81	17	1.45	2.36	NA	0.47	3.9	1.4	0.9
FOM_{CEStat} (µA/ µW)	8	-	-	-	-	-	-	1.4	-
$AFOM_{CEDyn}$ (V.pF)/ (µs.µW.mm^2)	514	447	18	110	155	16	419	0.17	1233
$AFOM_{SS}$ (MHz.pF)/ (µW.mm^2)	952	828	21	118	NA	16	186	3	30

*SI Strong-Inversion *SBT Sub-threshold

current. It can maintain this current only for a period of approximately three time-constants $\tau_{const} = R_{Large}C_{BAT}$. In this design $\tau_{const} = 0.4\mu$s. Hence the Free-AB op-amp can provide a relatively large output current only for approximately 1.2μs. Fig. 26 shows that the proposed op-amp has CMIVR from −300mV to 400mV. In this case, the lower value of the output is limited by the differential pair's headroom and not by the op-amp's maximum negative output current. The input differential pair's headroom HR_{DP} (where $HR_{DP} = V_{GS} + V_{DSsat}$) limits the common mode input range

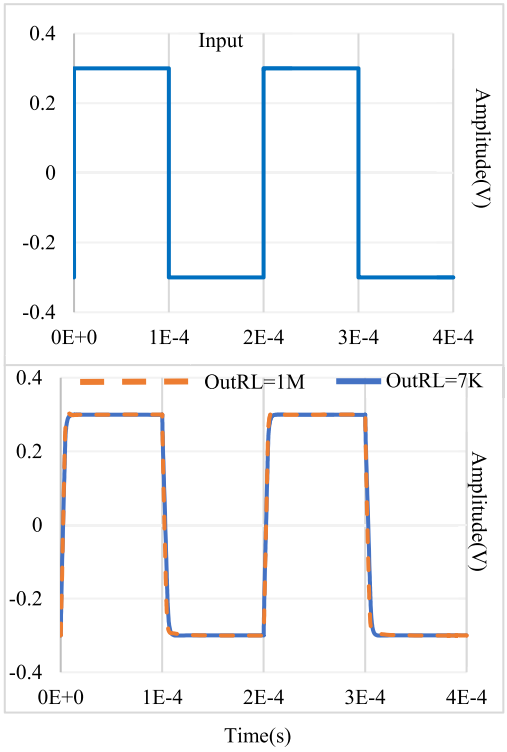

FIGURE 20. Transient response of the proposed op-amp in sub-threshold for C_L = 300pF in parallel with R_L = 1MΩ and 7kΩ to a 5kHz input pulse.

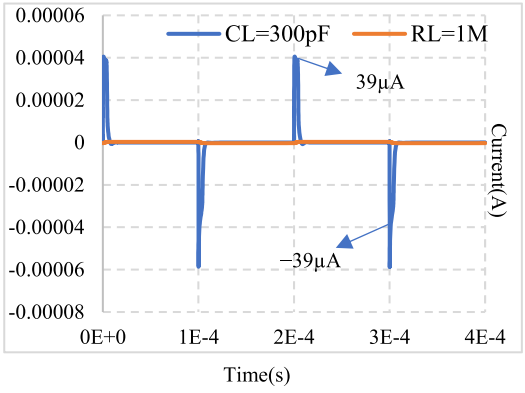

FIGURE 21. Output current of the proposed op-amp in sub-threshold for C_L = 300pF || R_L = 1MΩ.

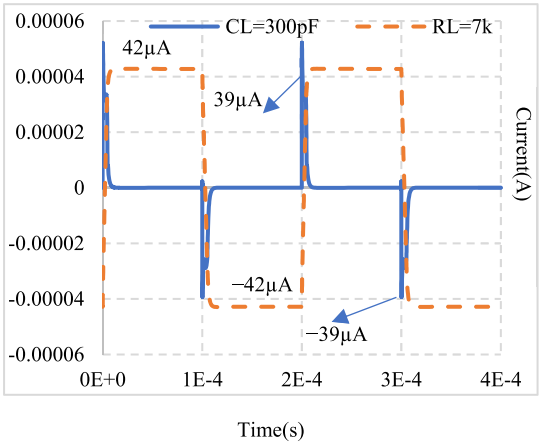

FIGURE 22. Output current of the proposed op-amp in sub-threshold for C_L = 300pF in parallel with R_L = 7kΩ.

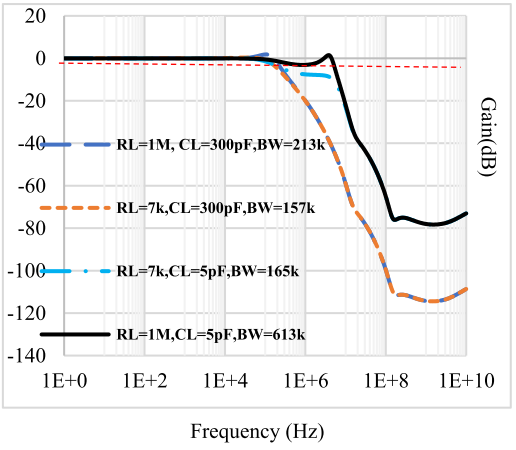

FIGURE 23. Frequency Response of the proposed op-amp in VF configuration in subthreshold.

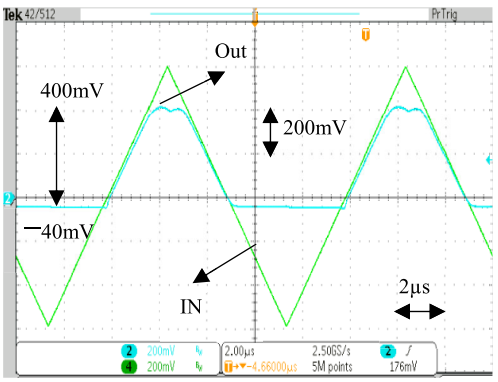

FIGURE 24. Experimental transient response of Conv-A op-amp for 100 kHz rail-to-rail triangular input signal for R_L = 1kΩ || C_L = 300pF load.

and prevents the input/output voltage in VF configuration to take values below −300mV. This happens as the input differential pair turns off for values lower than $V_{SS}+HR_{DP}$. Fig. 27 shows the experimental frequency response of all the op-amps in VF configuration for $R_L = 250\Omega||C_L = 300$pF load. The proposed, Free-AB, and Conv-A op-amps have a *BW* of 9MHz, 4.19MHz, and 1.9MHz. It can be seen that the proposed op-amp has essentially enhanced bandwidth (factor 4.7 higher than the conventional) which is in agreement with simulations.

Figs. 28-30 shows the transient responses of the Conv-A, Free-AB, and the proposed op-amp for a 100kHz 650mV_{pp} amplitude input pulse input with a 250Ω resistive load in parallel with a 300pF load capacitance. The Conv-A and Free-AB op-amps reach similar maximum positive values of +340mV due to the gain error and not due to current limitations. The maximum negative voltage of Conv-A op-amp can

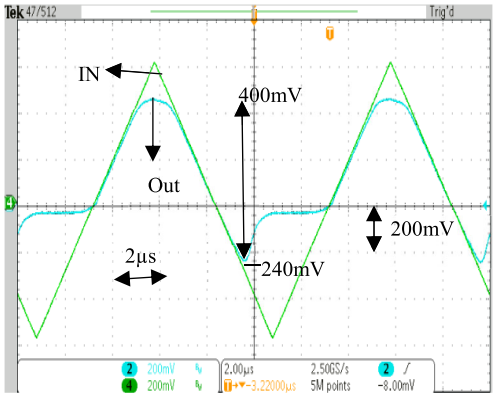

FIGURE 25. Experimental transient response of Free-AB op-amp to a rail-to-rail 100kHz triangular input signal for $R_L = 1k\Omega$ || $C_L = 300pF$ load.

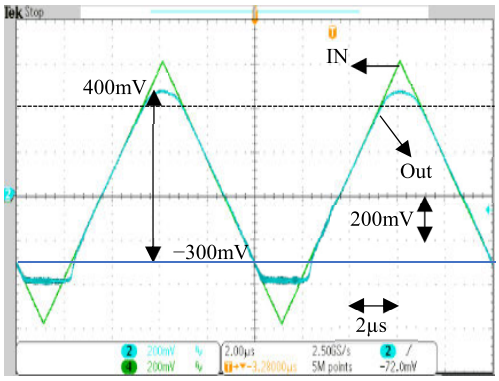

FIGURE 26. Experimental transient response of proposed op-amp for rail-to-rail 100kHz triangular input pulse for $R_L = 1k\Omega$ || $C_L = 300pF$ load.

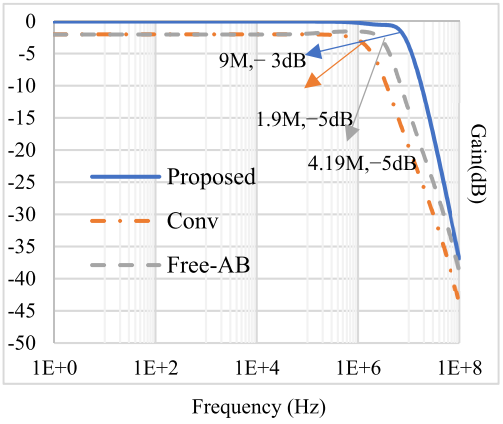

FIGURE 27. Frequency response of Conv-A, Free-AB, and proposed op-amp in VF configuration for $R_L = 250\Omega$ || $C_L = 300pF$.

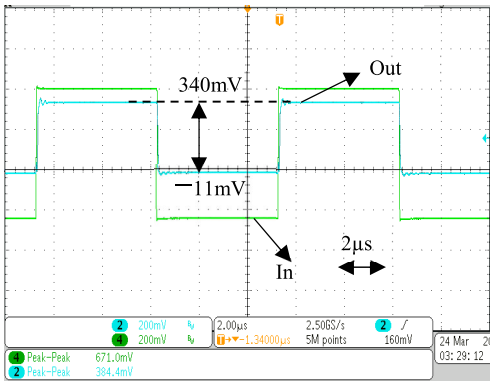

FIGURE 28. Experimental transient response of the Conv-A op-amp for $R_L = 250\Omega$ || $C_L = 300pF$ with 100kHz input pulse.

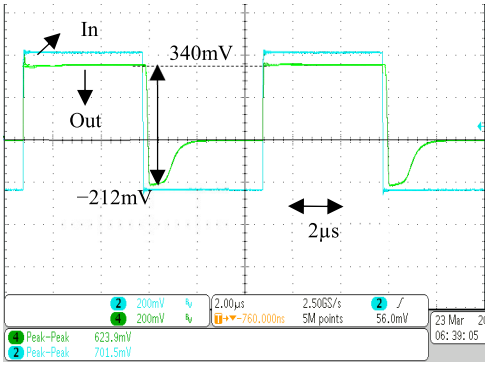

FIGURE 29. Experimental transient response of the Free- op-amp for $R_L = 250\Omega$ || $C_L = 300pF$ with 100kHz input pulse.

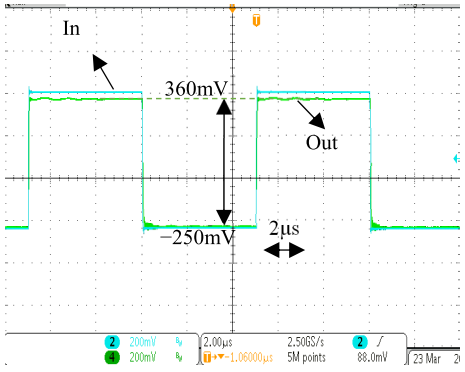

FIGURE 30. Experimental transient response of the proposed op-amp for $R_L = 250\Omega$ || $C_L = 300pF$ with 100kHz input pulse.

reach up to −11mV due to its current limitation in negative direction. The value of the corresponding $I_{outMAX} = -44\mu A$, which is close to I_{MOutQ}. For negative voltages, the Free-AB shows both gain error and current limitation (after it settles). However, the proposed op-amp can achieve −250mV in the negative direction that corresponds to a −1mA load current. Fig. 31 shows the micrograph of the Conv-A op-amp. It consumes 0.013mm^{2}Si area. Fig. 32 shows the micrograph of Free-AB op-amp which occupies 0.027 mm^2. The proposed op-amp takes 0.025 mm^{2}Si area. Its micrograph is given in Fig. 33. The proposed op-amp has a DC offset voltage of 0.5mV.

Table 7 shows a comprehensive comparison of the proposed op-amp with state-of-the-art op-amps. The proposed op-amp has the highest FOM_{SS}.

Though [15] has the highest FOM_{CEDyn}, its FOM_{SS} is 26 times lower than the FOM_{SS} of the proposed op-amp. Additionally, the circuit in [15] does not mention its resistive load driving capability FOM_{CEStat}. The proposed op-amp has a FOM_{CEStat} of 8. Thus, from the experimental results, it can be asserted that the proposed op-amp has enhanced

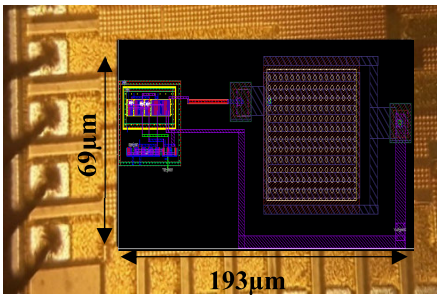

FIGURE 31. Micrograph of the Conv-A op-amp.

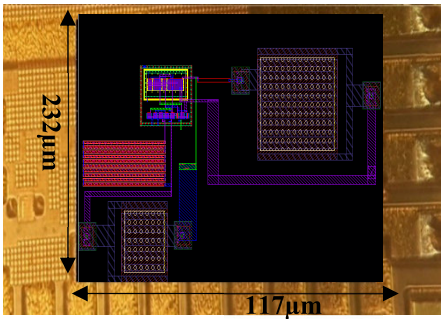

FIGURE 32. Micrograph of the Free-AB op-amp.

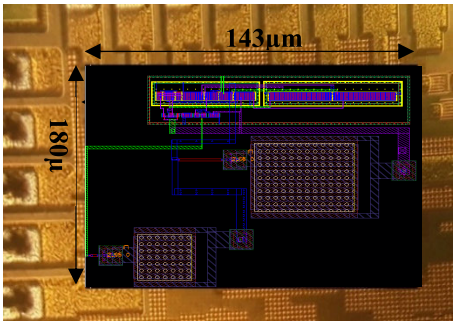

FIGURE 33. Micrograph of the proposed-AB op-amp.

bandwidth, and it is very efficient in driving a wide range of resistive and capacitive loads.

V. CONCLUSION

The proposed op-amp using a telescopic input stage, conventional Miller compensation, and a simple auxiliary amplifier that takes only moderate additional power dissipation (15%), can drive a wide range of resistive and capacitive loads with acceptable phase margin, greatly enhanced bandwidth, and high current efficiency. Experimental and simulation results verify these characteristics. The proposed op-amp is robust against process, temperature, and supply variations.

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