A thermal analysis for two modulation and control approaches for five-level diode-clamped rectifiers

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***Abstract*—This paper compares two recently published modulation and control approaches for a grid-connected five-level diode-clamped rectifier in terms of conducting losses. In this way, a prior analysis of the conducting time at steady state is presented for both approaches, and the usage of the most stressed switching device is calculated. The usage for this switching device is then compared with a typical nearest-two-level modulation strategy to show the efficiency of the studied approaches. Some simulations are also carried out to validate this comparison.**

***Index Terms*—Multilevel converters, Thermal analysis, Diode-clamped converter, Power control and modulation**

I. Introduction

The increasingly demand of cleaner, more flexible and more reliable electric energy is making a revolution in the power electronic scenario as new devices, topologies and algorithms are arising as a response to this demand [1]–[3]. In this context, device temperature concern is leading a new concept of power converter designing known as thermal management [4]. This is due to the undesired effects that high temperature or temperature changes may have on power device reliability and durability [5]. Consequently, temperature is a key point that has to be taken into account in order to extend power device lifetime [6].

The current going through each power device creates a power flow that yields cyclic heating and cooling intervals. Considering the different thermal expansions coefficients of the components inside the power device, these intervals create mechanical stress that are translated to aging and, consequently, reduced lifetime expectancy [5], [7]. Therefore, it is critical to reduce its magnitude such as to reduce long-term expenses [8]. In this sense, active thermal control (ATC) takes into account these effects to modify the overall performance such as to reduce the amplitude of these cycles or the averaged temperature level [9]. At the same time, the device temperature monitoring and the junction temperature estimation have become of great importance to estimate the power device health state and also to allow the active thermal control to act accordingly [10].

On the other hand, an appealing topology of converters, referred as multilevel ones, offers several advantages regarding grid current distortion and power device voltage limits, although the use of them entails more semiconductors devices in the system [11]. Depending on the topology, some semiconductors might be closed longer than others which entails more conducting losses and therefore bigger thermal aging effects. As a consequence, these devices are more likely to reach its lifetime end than the others which highly increase the cost of maintenance. As a result, several studies have been carried out to consider the thermal management into the control of multilevel converter [12]–[14].

One of the most common multilevel converter topologies used in the industry is the diode-clamped converter (DCC) [15]. In this regard, the three-level kind has been well accepted and spread along plenty of industrial applications [16]. However, the actual research on the five-level one has still room for improvements. That is why this paper focuses on the five-level diode-clamped converter topology and analyzes two of the modulation and control approaches previously published [17] that tackles the capacitor voltage unbalance issue. In the cited publication, the approaches are based on considering the duty ratios of each voltage level for each phase and modelling the current control and capacitor voltage unbalance with these variables. As a result, they consider all possible levels within a switching period. This fact could yield higher switching losses than other ones, although it could make the dissipated power to be more equally distributed among the semiconductors, reducing the thermal cycles and aging. Therefore, this paper revisits the two proposed approaches and compares them in terms of thermal effects.

The outline of the paper is as follows: Sect. II summarizes the used model, control and modulation

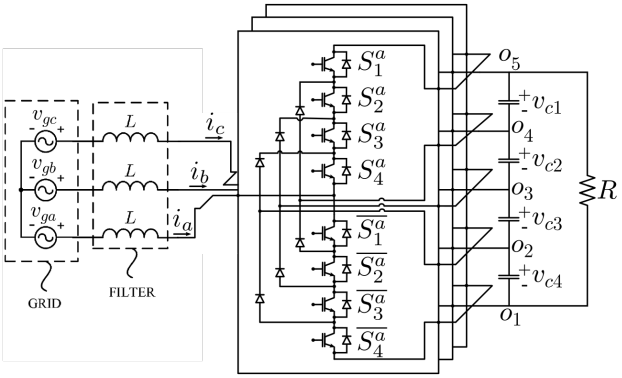

Fig. 1. Schematic of 5-level DCC

approaches; Sect. III presents a thermal analysis of this topology with the cited approaches; Sect. IV presents several simulations and its main comparisons; and, finally, Sect. V draws some conclusions about the contribution.

II. Model, Control and Modulation approaches

This paper focuses on a five-level DCC shown in Fig.1 . The modelling, control and modulation approaches used in this paper are retrieved from [17] and summarized in the next subsections.

A. Five-level DCC Model

The dynamics of the system are modelled using variables averaged over a switching period T referred as duty ratios. These duty ratios $d_{ij} \in [0, 1]$ are labelled for each phase $i = \{a, b, c\}$ and each level $j = \{1, 2, 3, 4, 5\}$ and reflects the part of a period T that phase i output is connected to level j, therefore $\sum_j^5 d_{ij} = 1$ which is a restriction for each phase. By performing a Clarke transformation using the power invariant form, the duty ratios can be expressed in $\alpha\beta\gamma$ frame instead of the abc one. The main advantage of doing so in a three-phase system is that variables $d_{\gamma j}$ are related to the zero-sequence component of the voltage output and therefore, they do not appear in the current dynamic. In this way, their value do not affect the current controller as long as saturation is avoided—i.e. $0 \leqslant d_{ij} \leqslant 1$—and they will be considered as degrees of freedom.

Defining the desired normalized output voltage of each phase as u_k for $k = \{\alpha, \beta\}$, its value can be achieved in averaged terms by fulfilling

$$u_k = -2d_{k1} - d_{k2} + d_{k4} + 2d_{k5}, \tag{1}$$

where duty ratios d_{k3} do not appear and therefore they will be obtained in abc frame by applying the $\sum_j^5 d_{ij} = 1$ restrictions. As a consequence, there are still 8 duty ratio values to obtain. Notice that component γ has been omitted due to the reason stated previously. Regarding the capacitor voltage unbalance, there are four signals to balance which yield three unbalancing signals referred as $\{v_{d1} = v_{c4} - v_{c1},\, v_{d2} = v_{c3} - v_{c2},\, v_{d3} = v_{c2} - v_{c1}\}$. Considering the previous definition of duty ratio in $\alpha\beta$ frame, the dynamics of these signals can be expressed accordingly,

$$C\frac{dv_{d1}}{dt} = -i_\alpha(d_{\alpha5} + d_{\alpha1}) - i_\beta(d_{\beta5} + d_{\beta1}) \tag{2}$$

$$C\frac{dv_{d2}}{dt} = -i_\alpha \sum_{j=\{1,2,4,5\}} d_{\alpha j} - i_\beta \sum_{j=\{1,2,4,5\}} d_{\beta j} \tag{3}$$

$$C\frac{dv_{d3}}{dt} = -i_\alpha d_{\alpha4} - i_\beta d_{\beta4} \tag{4}$$

B. Control Algorithm

Usually, in grid-connected rectifier applications, variables u_α, u_β come from the application of the current controller such as to achieve current and dc-link voltage regulation. Accordingly, it is assumed that a PI Controller, for the dc-link voltage regulation, is set in cascade with a proportional-resonant current controller [18] that results in the values of u_α, u_β. In summary, once that variables u_α, u_β are known, two restrictions are obtained from (1). The remaining six conditions comes from the balancing control. Inspired by (2)–(4), control signals $\{u_3, u_4, u_5, u_6, u_7, u_8\}$ and their corresponding control laws are defined such that

$$u_3 = (d_{\alpha5} + d_{\alpha1}) = k_{\text{bal}}\, i_\alpha v_{d1} \tag{5}$$

$$u_4 = (d_{\beta5} + d_{\beta1}) = k_{\text{bal}}\, i_\beta v_{d1} \tag{6}$$

$$u_5 = \sum_{j=\{1,2,4,5\}} d_{\alpha j} = k_{\text{bal}}\, i_\alpha v_{d2} \tag{7}$$

$$u_5 = \sum_{j=\{1,2,4,5\}} d_{\beta j} = k_{\text{bal}}\, i_\beta v_{d2} \tag{8}$$

$$u_7 = d_{\alpha4} = k_{\text{bal}}\, i_\alpha v_{d3} \tag{9}$$

$$u_8 = d_{\beta4} = k_{\text{bal}}\, i_\beta v_{d3}, \tag{10}$$

where k_{bal} is the balancing control parameter. In this way, the balancing is achieved at the same time that the 8 duty ratios are fully determined.

C. Modulation Stage

The duty ratios computation is straightforward but for the value of $d_{\gamma j}$ left as a degree of freedom until this stage. Considering the previous steps, duty ratios $d_{\alpha j}, d_{\beta j}$ for $j = \{1, 2, 4, 5\}$ are known so it can be returned to abc frame once the corresponding $d_{\gamma j}$ is also known. In this sense, two approaches are presented: the first one considers fixed values of $d_{\gamma j}$, whereas the second one selects the values of $d_{\gamma j}$ that makes one duty ratio d_{ij} equal to zero. By doing so, the phase i with a duty ratio $d_{ij} = 0$ does not commute at level j, avoiding additional commutations.

- Approach 1:

$$d_{\gamma j} = k_{\gamma j}$$

- Approach 2:

$$d_{\gamma j} = \max\left(\sqrt{2}d_{\alpha j}, \frac{d_{\alpha j}}{\sqrt{2}} - d_{\beta j}\sqrt{\frac{3}{2}}, \frac{d_{\alpha j}}{\sqrt{2}} + d_{\beta j}\sqrt{\frac{3}{2}}\right),$$

for $j = \{1, 2, 4, 5\}$, where $k_{\gamma j}$ are constant values and max is the function that retrieves the maximum value. However, in [17], approach 2 for $j = \{2, 4\}$ is not always applied as it could introduce "large jumps" within one switching period. Thus, duty ratio d_{i2} or d_{i4} could be equal to zero only in case d_{i1} or d_{i5} turned out to be also zero respectively, otherwise it applies the same law than approach 1 for the corresponding level. For the theoretical comparison, this latter restriction is skipped such as to emphasize the differences in both approaches. In this way, the values of d_{ij} for each phase i and $j = \{1, 2, 4, 5\}$ are obtained by using the inverse Clarke transformation. The remaining duty ratios d_{i3} are obtained from the $\sum_{j=1\to5} d_{ij} = 1$ restriction.

Finally, once all duty ratios are known, the levels they generate can be sequenced in a saw-tooth or stair-shaped waveform within a switching period to generate the voltage output of each phase.

III. Conducting losses of the studied approaches

It can be noted that the previous modulations will yield different losses profiles as the conducting time and turning-on/off cycles of the power devices differ depending on the levels used. The higher the duty ratio, the higher the conducting time of the power devices. Regarding the switching losses, they highly depends on the switching frequency, the point of operation and how the levels are sequenced, however in multilevel converter, as the device blocking voltage is reduced by the introduction of several levels, its effect is considerably reduced in comparison with two level topologies. Nevertheless, a trade-off comparison dependant of the operating point has to be made to determine which is the most suitable approach. Because of this, the switching losses has not been considered in this analysis as it would not yield any straight conclusion. Thus, the analysis will focus on a generic phase i and the conducting losses of the four upper semiconductors $\{S_1^i, S_2^i, S_3^i, S_4^i\}$ considering that the lower ones will have a symmetrical behaviour. Also, no dead time is considered as it can be emulated as an extension of the duty ratios [19]. Notice that whenever a switching device S_n^i is open, its complementary lower-side one $\overline{S_n^i}$ is closed. Hence, it is straightforward that four switching devices will be always connected. It is also worth to mention that the current will not always go through the switching device but through the anti-parallel diode depending on its direction, changing the losses profile. However, considering the periodical behaviour of the phase current and that this paper aims for a comparative analysis, it can be made assuming the worst-case conducting losses, usually the ones that are generated by the switching devices ($i_i \leqslant 0$). In this way, a variable called switching device usage ${S_n^i}^u$ can be modelled as

$$\begin{aligned}
{S_1^i}^u &\doteq \begin{cases} d_{i5}|i_i| & \text{if } i_i \leqslant 0 \\ 0 & \text{if } i_i \geqslant 0 \end{cases} \\
{S_2^i}^u &\doteq \begin{cases} (d_{i5} + d_{i4})|i_i| & \text{if } i_i \leqslant 0 \\ 0 & \text{if } i_i \geqslant 0 \end{cases} \\
{S_3^i}^u &\doteq \begin{cases} (d_{i5} + d_{i4} + d_{i3})|i_i| & \text{if } i_i \leqslant 0 \\ 0 & \text{if } i_i \geqslant 0 \end{cases} \\
{S_4^i}^u &\doteq \begin{cases} (d_{i5} + d_{i4} + d_{i3} + d_{i2})|i_i| & \text{if } i_i \leqslant 0 \\ 0 & \text{if } i_i \geqslant 0 \end{cases},
\end{aligned} \tag{11}$$

which represents the averaged current that goes through the device S_n^i over a switching period. The greater this value, the greater the conducting losses. A well-known approach to estimate the module's lifetime is the Coffin–Manson–Arrhenius model [20] that provides the number of cycles to fail (N). This model highlights the importance of

the cycling effect on the lifetime expectancy: the greater the temperature range of the cycle or the maximum reached temperature the smaller the value of N. Consequently, these two parameters would have to be managed to provide thermal management of the devices. To retrieve how $d_{\gamma j}$ affect them, let us consider that the value of $d_{\gamma j}$ increases monotonically the value of all duty ratios of level j. Notice that at steady state,

$$\begin{aligned} u_\alpha &= \sqrt{\frac{3}{2}} U \cos(\omega t), \quad i_\alpha = \sqrt{\frac{3}{2}} I \cos(\omega t + \sigma) \\ u_\beta &= \sqrt{\frac{3}{2}} U \sin(\omega t), \quad i_\beta = \sqrt{\frac{3}{2}} I \sin(\omega t + \sigma) \\ u_{3,\dots,8} &\approx 0 \end{aligned} \tag{12}$$

where U, I are the amplitude of the normalized output voltage and the phase currents in abc respectively; σ is the phase-shift of the currents; and ωt is the grid angle. Also, consider that from (12) and (5)–(10), variables $d_{\alpha j}$ and $d_{\beta j}$ for $j = \{2, 3, 4\}$ are equal to zero. Therefore, from (1) and (11)

$$S_n^{i\,u} = \left(T_{\alpha\beta\to i} [d_{\alpha 5}\, d_{\beta 5}]^{\mathrm{T}} + \sum_{j=\{5,\dots,6-n\}} d_{\gamma j}/\sqrt{3} \right) |i_i| \tag{13}$$

$$d_{\alpha 5} = \frac{u_\alpha}{4}; \quad d_{\alpha 1} = -\frac{u_\alpha}{4} \tag{14}$$

$$d_{\beta 5} = \frac{u_\beta}{4}; \quad d_{\beta 1} = -\frac{u_\beta}{4}, \tag{15}$$

for $n = \{1, 2, 3, 4\}$, $i_i \leqslant 0$ and being $T_{\alpha\beta\to i}$ the transformation vector from $\alpha\beta$ to phase i. Hence, the differences in the switching devices usage among phases is highly dependant on the values of the product $\sum d_{\gamma j}|i_i|$. On the other hand, the differences in the device usage within the same phase at steady state relies mainly in the $d_{\gamma j}$ value. The lower its value for level j, the more similar the usage for devices inside range $n < 6 - j$ and range $n \geqslant 6 - j$.

According to the studied approaches and the steady state conditions, the value of $\sum d_{\gamma j}|i_i|$ are:

- Approach 1:

$$\sum_{j=\{5,\dots,6-n\}} (d_{\gamma j})|i_i| = \sum_{j=\{5,\dots,6-n\}} (k_{\gamma j})|i_i| \tag{16}$$

- Approach 2:

$$\sum_{j=\{5,\dots,6-n\}} (d_{\gamma j})|i_i| = \begin{cases} d_{\gamma 5}^{\text{App2}}|i_i| & n \leqslant 2 \\ (d_{\gamma 5}^{\text{App2}} + d_{\gamma 3}^{\text{App2}})|i_i| & n > 2 \end{cases} \tag{17}$$

where $d_{\gamma j}^{\text{App2}}$ is the value of $d_{\gamma j}$ according to the second approach. Notice that $d_{\gamma 2}^{\text{App2}} = d_{\gamma 4}^{\text{App2}} = 0$ because of the steady state condition . The values of the first approach depends on the user, but the second ones are retrieved from the approach algorithm. Besides, notice that $d_{\gamma 3}$ for any approach can be obtained from applying the Clarke transformation to the restriction of $\sum_{j=1}^{5} d_{ij} = 1$ which results in the condition $\sum_{j=1}^{5} d_{\gamma j} = \sqrt{3}$. Therefore, the second approach can be applied at steady state in (17) and, in addition to (16), replaced into (13) to retrieve the general usage for the switching device $S_n^{i\,u}$. For the sake of comparison, the usage of $S_4^{i\,u}$—the most used switching device among the upper ones—will be depicted. Figure 2 shows the value of the usage $S_4^{i\,u}$ when $U = 1.60$ and normalized current along a grid period and different values of σ. The first approach is depicted as a mesh, while the second one is depicted as a surface. On the other hand, Fig. 3 depicts the results of integrating $S_4^{i\,u}$ over a grid period as a function of σ for different values of U for the first and second approach and also for the two nearest level modulation. Notice that σ is directly related to the power factor as $PF = cos(\sigma)$. Such as to picture the different performance of the approaches and the two nearest level modulation, Fig. 4 depicts the duty ratios of each switching device $S_{1,\dots,4}^i$.

It can be seen that the PF barely changes the overall usage and that the first approach offers a lower usage compared to the 2nd approach and two-level modulation. The first being better than the second is due to the minimization of the $d_{\gamma 5}$ and $d_{\gamma 1}$ values that reduces the commutations, but increases considerably the value of $d_{\gamma 3}$ which yields to more conducting time of the devices S_3^i and S_4^i. Besides, the bigger the duty ratios of levels $2, 3, 4$, the greater the usage for S_j^i with $j = \{2, 3, 4\}$ in comparison with S_1^i which yields in different number of cycles to fail.

IV. Simulation results

This section will present some results from applying the mentioned approaches into a model. The modulation algorithm is directly extracted from [17] and straightly applied to the model. The simulation parameters and circuit parameters are presented in Table I. To simulate different values of σ, three tests for each approach have been carried out where

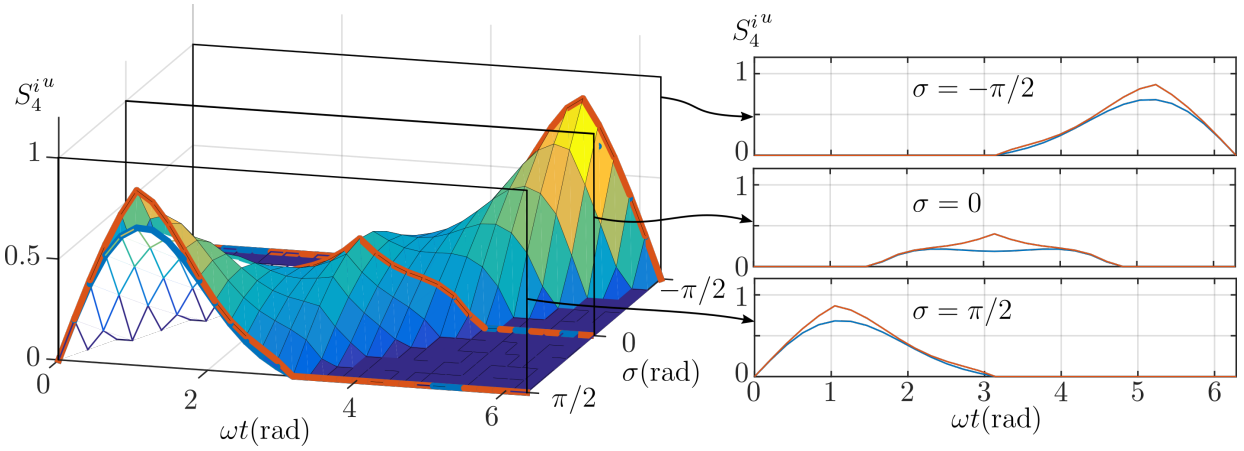

Fig. 2. Usage S_4^{iu} for $U = 1.60$ and normalized current along a grid period and different values of σ. Approach 1 is depicted as a mesh (red) while approach 2 is depicted as a surface (blue).

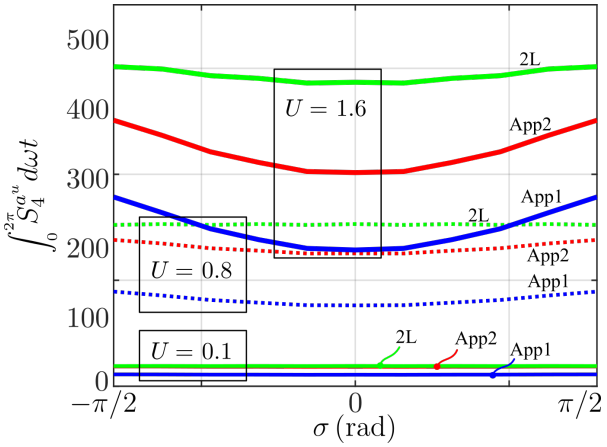

Fig. 3. Integral of the usage over a grid period considering different values of σ and U for the first approach, the second approach and the two nearest level modulation.

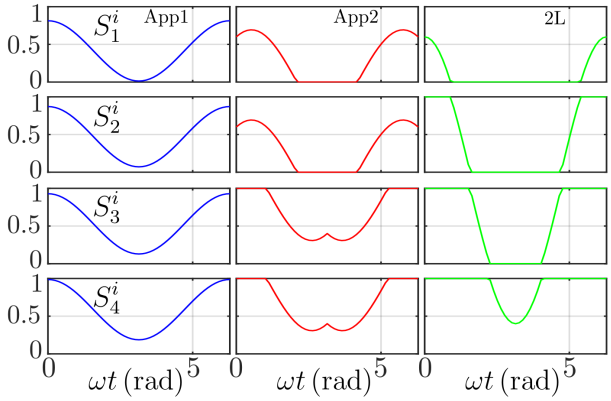

Fig. 4. Duty ratios of switching devices $\{S_1^i, S_2^i, S_3^i, S_4^i\}$ for the first approach (App1), the second approach (App1) and the nearest two level modulation (2L).

the reactive power reference (Q^r) and the dc-link resistor value (R) change as shown in Table I.

TABLE I
SIMULATION AND CIRCUIT PARAMETERS

Parameter	Value	Parameter	Value
L	2 mH	C	3300 μF
v_{dc}	800 V	v_{grid}	220 V_{rms}
k_{bal}	$2 \cdot 10^{-4}$	$k_{\gamma 2,4}$	0.1
$k_{\gamma 1,5}$	$(\sqrt{3} - 0.25)/2$	R	$[\text{inf}, 43, \text{inf}]$ Ω
Q^r	[-25,-10,5] kVA	f_{sw}	10 kHz

Similarly, these applied conditions resulted in the values of $U = \{1.4, 1.47, 1.6\}$ at steady state.

Figure 5 summarizes the results of the simulations where the main differences in the two approaches and the nearest two level modulation can be seen. The switching states are depicted in the first graph where it can be seen that, whereas the Approach 1 (App1) use all level every switching period, Approach 2 (App2) skip some of them. Similarly, the second graph shows the current through S_4^a including the anti-parallel diode. Notice again that Approach 1 conducts every period, in contrast to Approach 2. However, by looking at the third graph where the conducting losses are depicted according to the integrated IGBT model 5SNA1600N170100, it can be seen that the overall conducting losses are worse for Approach 2 when the current goes through the device ($i_a \leqslant 0$). Considering this, it can be said that Approach 1 offers a better profile for the conducting losses that, in global terms, will yield less thermal stress for the device. On the other hand, the conducting losses when the current goes through the diode is worse for the Approach 1 than the Approach 2, although diodes has usually

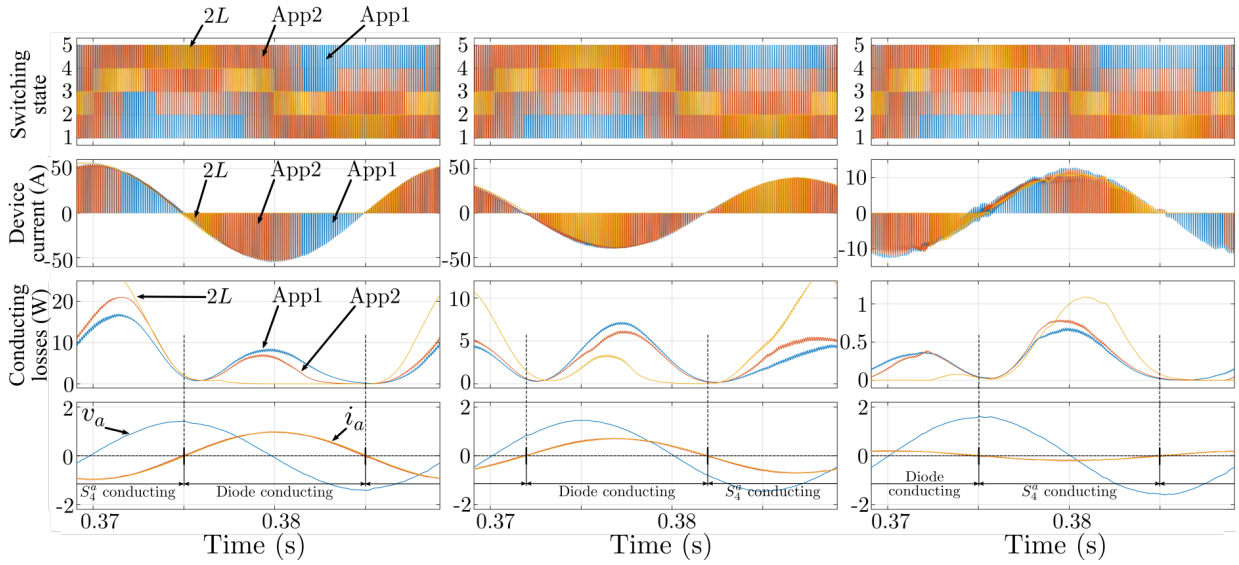

Fig. 5. Simulation results for the two approaches and the two level modulation approach for the three test considered in phase a. Upper graphs show the switching states; upper-mid graphs show the current thorugh the device S_4^a; lower-mid graphs show the conducting losses computed in simulation; and lower graphs show the normalized current and output voltage for phase a.

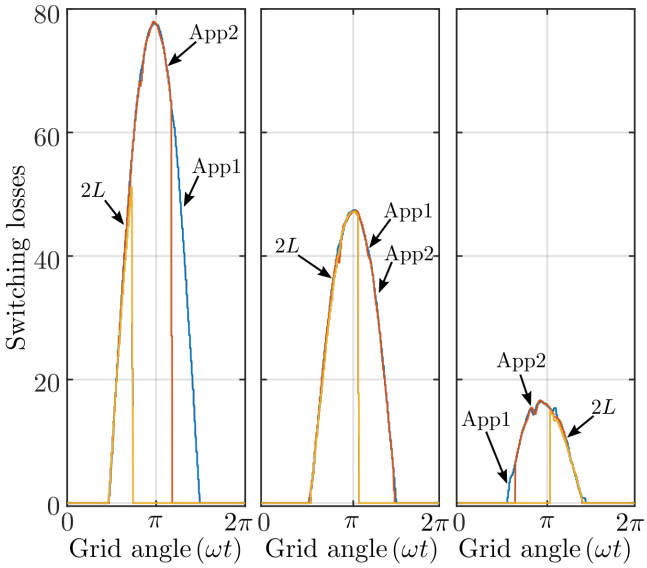

Fig. 6. Switching losses (W) of the approaches considered with a switching frequency of 10 kHz. The turn-on and turn-off energy has been retrieved from the datasheet of model 5SNA1600N170100 at 25 °C.

longer life expectancy and less voltage drop than the switching devices. Therefore, its impact on the equipment life expectancy is less strident. In any case, both approaches offer a better profile for the conducting losses than the two level modulation approach. Not only its integral is smaller but also the conducting losses are more "spread" over a grid period, reducing the thermal cycling effect.

In spite of not considering the switching losses in the analysis, for the approaches considered here, the first one yields a large number of commutations: 4 transitions per switching period; the second one yields less commutations: between 2 and 4 transitions per period; whereas the nearest two level modulation offers the best performance in this regard: 1 transition per period. Nevertheless, for the sake of comparison, Fig. 6 shows the switching losses of device S_4^a using the same IGBT model for these approaches under the three tests carried out. It can be seen that two nearest level modulation could cut down the switching losses to a 25% of those of the Approach 1, whereas the second could do so down to 67% depending on the test considered. It is also worth to mention that the two nearest level modulation offers the lowest switching losses but it could not be applied with no modification as it does no tackle the capacitor voltage balance issue. Any other approach which does so will increase the switching losses as more transitions will be inserted. Consequently, once the operating conditions are known, a trade-off comparison between conducting losses and switching losses has to be considered such as to select the more appropriate algorithm.

V. Conclusions

A brief conducting losses analysis of two modulations approaches for grid-connected five-level DCC has been presented in this paper. The results are also

compared with the well-known two nearest level modulation approach resulting in one modulation offering the better profile in terms of conducting losses. Not only the overall conducting losses are more reduced but also they are more distributed along a grid period, reducing both the maximum reached temperature and the cycling thermal effect. Because of the dependence to the operating conditions, switching losses were not considered in this analysis but it must no be skipped in a proper thermal design which will result in a trade-off for these modulation approaches.

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