Analog-to-Digital Converters for Efficient Portable Devices

Memoria presentada por

Sohail Asghar

Para optar al grado de Doctor por la Universidad de Sevilla

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RESUMEN

La transformación digital en la que se encuentra inmersa nuestra sociedad no hubiese sido posible sin el desarrollo experimentado por la industria de la Microelectrónica. El escalado tecnológico dictado por la ley de Moore ha hecho posible que se puedan integrar en un único chip miles de millones de componentes electrónicos (principalmente transistores) con unas dimensiones que se acercan a la escala de unos cuantos átomos de silicio. Además de los beneficios en términos de coste de producción y prestaciones, el aumento de los niveles de integración ha propiciado que el procesamiento de las señales sea realizado cada vez más por circuitos digitales, ya que éstos obtienen una mejora del rendimiento con el escalado de los procesos de fabricación en comparación con los sistemas electrónicos analógicos.

Una de las consecuencias de esta evolución es que la frontera entre el dominio analógico y el digital se ha ido desplazando con los años cada vez más al punto en el que se sensa o adquiere la información del entorno – como por ejemplo las señales electromagnéticas captadas por una antena en un teléfono móvil – o cualquier otra magnitud física detectada por un sensor de cualquier dispositivo. Todo ello tiene como consecuencia que los circuitos que realizan la transformación analógica a digital o ADC (de *Analog-to-Digital Converter*), sean unos elementos cada vez más esenciales en cualquier dispositivo electrónico. Sin embargo, el diseño de ADC eficientes en tecnologías CMOS nanométricas – más adecuadas para realizar circuitos digitales rápidos que circuitos analógicos precisos – supone afrontar una serie de retos científico-técnicos desde el nivel de abstracción más alto hasta su realización física en un chip de silicio.

De entre las diversas arquitecturas de ADC, el estado del arte está dominado por diversas técnicas de conversión que son más eficientes en función del ancho de banda de la señal que se necesita digitalizar y la precisión (resolución) de dicha digitalización. De todas ellas, las

denominadas Pipeline, SAR (de *Successive Approximation Register*) y Modulación Sigma-Delta (ΣΔM), o una combinación híbrida de ellas, son las que ofrecen unas mejores métricas de rendimiento. Este proyecto de tesis se centra en el diseño de dos de estos tipos de ADC: SAR y ΣΔM, considerando diseños en dos procesos tecnológicos diferentes, con aplicación en comunicaciones inalámbricas y en gestión de circuitos de energía para dispositivos portátiles.

Tras una introducción al contexto de la investigación desarrollada y una descripción de los fundamentos de ADC, se presenta la primera contribución de esta tesis, consistente en el diseño de ADC basados en ΣΔM reconfigurables para aplicaciones de sistemas de comunicación móvil. La primera parte de este estudio aborda los denominados convertidores de radiofrecuencia (RF) a digital, o RF-digital para aplicaciones de radio definida por software (SDR de *Software-Defined Radio*). Concretamente se presenta el procedimiento de síntesis y diseño a nivel de sistema de un modulador de tipo paso de banda (BP-ΣΔM), implementado mediante técnicas de circuito de tiempo continuo, con una frecuencia central es programable de forma continua de 0 a $0.25f_s$, siendo f_s la frecuencia de muestreo. La arquitectura del modulador es de lazo único con un filtro de tiempo continuo de cuarto orden y un cuantizador de 15 niveles. El lazo de realimentación está formado por un convertidor digital-analógico (DAC) con función de transferencia senoidal implementada con un filtro FIR con un menor número de coeficientes que las mostradas en el estado del arte, lo que facilita su programabilidad, al mismo tiempo que aumenta la robustez y reduce el consumo de potencia con respecto a otras aproximaciones similares. Estas características se combinan con técnicas de submuestreo para lograr una digitalización más robusta y eficiente energéticamente de las señales centradas en 0.455 a 5 GHz, con una resolución efectiva escalable de 8 a 15 bits dentro del ancho de banda de la señal de 0.2 a 30 MHz.

La segunda contribución en el ámbito de ADC de tipo ΣΔM, es un diseño e implementación en una tecnología CMOS de 90nm de un modulador reconfigurable paso-baja/paso-banda (LP/BP) con frecuencia sintonizable, lo que lo hace especialmente apropiado para receptores altamente programables con aplicación en sistemas de comunicación basados en SDR. Los resultados experimentales validan el rendimiento del modulador en un rango de frecuencia de DC a 18 MHz, con una SNDR de 45 a 64 dB dentro de un ancho de banda de señal de 1 MHz, mientras que el consumo de potencia de 22.8-28.8 mW.

La segunda contribución de esta tesis es un ADC de tipo SAR para su uso en gestión de la potencia de convertidores DC/DC empleados en chips PMIC (de "Power Management Integrated Circuits"). El convertidor que se propone hace uso de dos técnicas desarrolladas en esta tesis doctoral y que dotan a este tipo de circuitos de ventajas en eficiencia energética con respecto al estado del arte. La primera técnica se basa en emplear un rango de entrada que se extiende por encima de la tensión de referencia en un factor de 1.33 V, lo que permite digitalizar señales de 3.2V de amplitud con una referencia de 1.2 V. Además, se propone una técnica de compensación del offset del comparador que no requiere calibración y permite obtener un offset residual de 0.5LSB. El chip ha sido diseñado y fabricado en una tecnología CMOS de 130nm, obteniendo SNDR=69.3 dB, SFDR=79 dB y una linealidad de DNL=1.2/–1.0 LSB, INL=2.3/–2.2LSB, con un consumo de potencia de 0.9mW. Estas prestaciones lo sitúan entre los mejores ADC reportados para este tipo de aplicaciones.

La calidad de la investigación desarrollada en esta tesis ha sido reconocida por la comunidad científica internacional como se demuestra por las publicaciones en diversos foros de IEEE y que se recogen al final de este documento. Entre otras, cabe destacar un artículo en la revista *IEEE Transactions on Circuits and Systems –I: Regular Papers*, con un índice de impacto

de 3.934, situada en el primer cuartil de su categoría en el *Journal Citation Reports* (JCR) en la categoría de *Electrical and Electronic Engineering*.

Abstract

Recent advancements in complementary metal oxide semiconductor (CMOS) process technology and CAD tools for the designs of digital circuits have led to an enormous increase in the processing capabilities of digital signal processors in all types of electronics applications. In order to fully exploit these two advances, more and more signal processing is being shifted to the digital domain. Therefore, all types of electronic applications, ranging from highly sophisticated telecommunications systems and high-end servers to consumer electronics and handheld portable devices, require efficient digitization of the analog signals to enable the subsequent signal processing in the digital domain through the use of analog-to-digital converters (ADCs). As a result of this, new design techniques ranging from architectural to the physical level are required to fully exploit the advancements in the CMOS technology, particularly in smaller geometry nodes. This thesis project focuses on the design of ADCs in CMOS technology for two application areas i.e. wireless communication and power management integrated circuits (PMICs).

The first part of the thesis deals with two types of sigma delta modulators (ΣΔM) for wireless communication. Initially, a design methodology and modelling of a continuous-time 4^{th}-order band-pass (BP) ΣΔM for digitizing radio frequency (RF) signals in software-defined-radio (SDR) mobile systems is presented. The modulator architecture comprises two resonators and a 15-level quantiser in the feedforward path and a raised-cosine finite-impulse response (FIR) feedback digital-to-analog converter (DAC). The latter is implemented with a reduced number of filter coefficients as compared to previous approaches, which allows increasing the notch frequency (f_N) programmability of an ADC (operating with a sampling frequency of f_s) from

$0.0375f_s$-to-$0.25f_s$. These features are combined with sub-sampling technique to achieve an efficient and robust digitization of 0.455-to-5 GHz signals with scalable 8-to-15 bits effective resolution within 0.2-to-30 MHz signal bandwidth. Following this architecture, the modelling, design and implementation of a switched-capacitor (SC) fourth-order single-loop modulator with a 5-level embedded quantiser is presented. The loop filter in this modulator consists of a cascade of resonator with feedforward (CRFF) coefficients, which can be programmed to make the zeros of the noise transfer function (NTF) variable. As a result, the modulator can be reconfigured either as a low-pass (LP) or band-pass (BP) ADC with a tuneable f_N and an optimised loop-filter zero placement. The chip has been designed and implemented in a 1.2 V 90-nm CMOS technology. Experimental results validate the performance of the modulator over a frequency range of DC-to-18 MHz, featuring a Signal-to-Noise and Distortion ratio (SNDR) of 45-to-64 dBs within a signal bandwidth of 1 MHz while the power consumption is 22.8-28.8mW.

In the second part of this thesis, a 12-bit successive approximation register (SAR) ADC with an extended input range for a digital controller intended for controllers of DC/DC converter of power management integrated circuits (PMIC) is presented. Employing an input-sampling scaling technique, the presented ADC can digitize the signals with an input range of 3.2 V_{pp-d} ($\pm 1.33\ V_{REF}$). The circuit also includes a comparator-offset compensation technique that results in a residual offset of less than 0.5 LSB. The chip has been designed and implemented in a 0.13-μm CMOS process and demonstrates the state-of-the-art performance, featuring a SNDR of 69.3 dB and the Spurious Free Dynamic Range (SFDR) of 79 dB without requiring any calibration. Total power consumption of the ADC is 0.9 mW, with a measured differential non-linearity (DNL) of 1.2/−1.0 LSB and integral non-linearity (INL) of 2.3/−2.2 LSB.

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This journey has been quite long and daunting and would not have been possible without the support of lot of people. First of all, I am really grateful to my supervisors, Dr. José Manuel de la Rosa Utrera and Dr. Ivan O'Connel for giving me opportunity to work under their supervision. They helped me to develop my thesis with their constructive comments, curiosity and support. At some points, PhD seemed to be an impossible task, but their encouragement and guidance kept me on track. Their patience, dedication and support have been amazing through all the years of PhD.

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Sohail Asghar

Cork, Ireland

November 2020

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Abbreviations

A	Area
AAF	Anti-aliasing-filter
AC	Alternating current
ADC	Analog-to-digital converter
BBM	Break-before-make
BoM	Bill of material
BP ΣΔM	Band-pass sigma delta modulator
BW	Bandwidth
BWA	Binary weighted with attenuation capacitor
BE	Backward-Euler
CBW	Conventional binary weighted
CM	Common mode
C_{Spec}	Specific capacitance
CRFF	Cascade of resonators with feedforward
CRFB	Cascade of resonators with feedback
CMOS	Complementary metal-oxide-semiconductor
CT	Continuous time

C_U	Unit Capacitor
DAC	Digital-to-analog converter
DC	Direct current
DCL	Digital cancellation logic
DEM	Dynamic Element Matching
DNL	Differential non-linearity
DSP	Digital signal processing
DR	Dynamic range
DUT	Design-under-test
DPWM	Digital-pulse-width-modulator
DT	Discrete time
DWA	Data weighted averaging
ENOB	Effective number of bits
E_Q	Quantisation Error
FE	Forward-Euler
ILA	Individual level averaging
IBE	In-band error
ISI	Inter-symbol-interference

f_{MAX}	Maximum frequency
f_N	Notch frequency
f_S	Sampling frequency
FS	Full-scale
FoM	Figure of merit
GBW	Gain-bandwidth
HRZ	Half-return-to-zero
HP	High-pass
IC	Integrated circuit
IF	Intermediate frequency
INL	Integral non-linearity
ISI	Inter-symbol interference
ITRS	International technology roadmap for semiconductors
k	Boltzmann's constant
K_C	Pelgrom mismatch coefficient
LSB	Least significant bit
LP	Low-pass
MDAC	Multiplying DAC

MSB	Most significant bit
NF	Noise figure
NRZ	Non-return-to-zero
NTF	Noise transfer function
OBG	Out of band gain
Op-amp	Operational amplifier
OSR	Oversampling ratio
PAM	Pulse amplitude modulation
PCB	Printed circuit board
PDF	Probability density function
PLL	Phase locked loop
PWM	Pulse-width-modulator
PSD	Power spectral density
PMIC	Power management integrated circuits
R_{ON}	ON-resistance
P_Q	Quantisation noise
Q	Quality factor
QPSK	Quadrature phase shift keying

RF	Radio frequency
RMS	Root mean square
ROM	Read-only-memory
QoE	Quality of experience
RZ	Return-to-zero
SAR	Successive approximation register
SC	Switched capacitor
SI	Switched current
SDR	Software-defined-radio
ΣΔ	Sigma delta
SFDR	Spurious free dynamic range
S/H	Sample and hold
SNDR	Signal to noise and distortion ratio
SQNR	Signal to quantisation noise ratio
SNR	Signal to noise ratio
SR	Set-reset
STF	Signal transfer function
T	Absolute temperature

TDC	Time-to-digital converter
TF	Transfer function
THD	Total harmonic distortion
TI	Time-interleaved
V_{CM}	Common mode voltage
V_{IN}	Input sampled voltage
VLSI	Very large scale integration
V_{OUT}	Output voltage
V_{pp}	Peak-to-peak voltage
V_{REFN}	Negative reference voltage
V_{REFP}	Positive reference voltage
V_T	Threshold Voltage

Chapter 1: Introduction

1.1 Background

Integrated circuits (ICs) are an essential component in all electronic systems, especially for multimedia, mobile, automotive, communication, medical and portable applications. Most of the ICs in such electronic systems process and store the information in digital domain. At the same time, in order to communicate with the real world analog signals, analog-to-digital conversion is required, thus making ADCs an indispensable part of these systems.

Recent advancements in CMOS process technology led to it being the technology of choice for the realisation of modern ICs [1]. With the continuous and aggressive scaling of modern CMOS processes, digital circuits have benefitted most [2]. Transistors with lower feature sizes allow either to have more functionality on a die, or a reduction in die size for a given functionality, resulting in lower cost. Due to this, almost all the digital systems are being designed in CMOS technologies. However, this scaling has created various challenges for analog and mixed signal circuit designers. With the technology scaling; voltage headroom, oxide thickness and the intrinsic gain of transistors decreases [3]. Furthermore, the threshold voltage (V_T) scaling is not in the same order as the supply voltage. These factors not only make analog and mixed signal circuit design especially ADC designs more challenging but also increases the power consumption for a given performance as designs migrate to smaller and smaller geometries. Another limitation associated with lower technology nodes is the gate-leakage mismatch that dominates over conventional mismatch mechanisms [4]. When all these factors are combined, it creates a complex set of constraints on the design of mixed signal IC systems where the analog and digital circuits are integrated on a single silicon die. The primary design

challenge in current integrated system designs is to exploit the benefits of technology scaling for digital circuits while careful design planning around those said limitations posed by scaling on analog circuits. Needless to say, there is a strong interest in the design community on the ADC design in the scaled technologies as demonstrated by the Murmann's ADC survey which tracks the ADC publications [5].

1.2 Motivation

This thesis focuses on the design of ADCs in CMOS technologies for two application areas i.e. wireless communication and power management integrated circuits (PMICs).

The wireless communication industry has seen unprecedented levels of growth over the past 40 years. Over the years, various wireless communication standards have been introduced. Figure 1.1 shows evolution of different wireless communication standards and the associated data rates over the last 40 years [6]. It is interesting to note that the supported data rates are getting faster with each standard. In addition to this, a modern radio receiver would need to support today's evolving systems such as IoTs, video-on-demand and machine-to-machine communications etc. Due to these factors, there has been a continuous growth in interest towards the design of highly integrated multistandard RF receiver architectures.

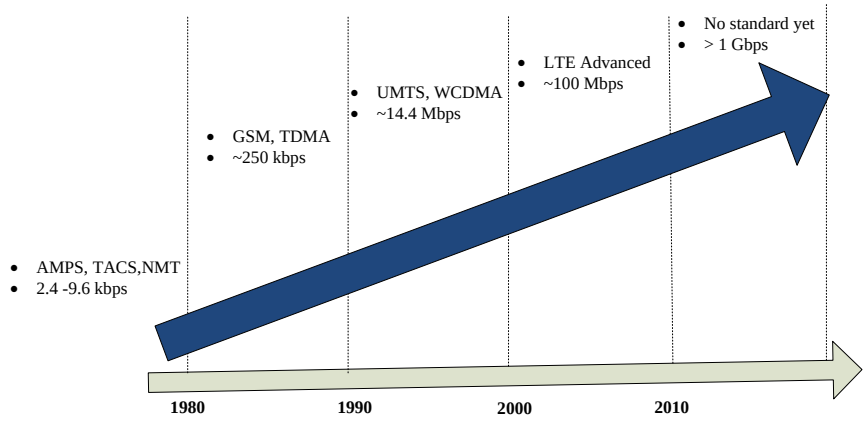


Figure 1.1. Evolution of different wireless communication standards [6].

PMIC is another important area of research in the context of IC design. These ICs generate, manage, control and distribute the stable voltages to other circuits and blocks in an electronic system. The continuous increase in the number of transistors in processors and microprocessors has equally benefitted all the computing applications ranging from data centres and servers to handheld and portable devices. However, power consumption and power management for these systems is one of the most important concerns. Typically, the data centres power and cooling expenditure are in the range of 10 to 15% of the total operational cost [7]. With the growing numbers of servers and their associated hardware capacity, energy efficiency is key to cost savings. Moreover, with the continuous increase of processing and memory capacity of different handheld and portable devices, energy efficiency is highly desired for a longer battery life [8]. Enhanced power management for such devices is very important for higher user quality of experience (QoE) [9]. Due to these factors, PMICs have got tremendous interest by the designer community. Furthermore, power management applications are also driving various other sectors such as automotive, healthcare, computing, artificial intelligence, neural networks, internet-of-things (IoTs) etc. As a result, PMICs have become an essential building block of electronic devices in order to optimise energy management, efficiency and sustainability. The global market for PMICs has reached to $46 billion by 2020 [10]. These factors are driving a renewed interest in the research of power management circuits specifically in the area of increased conversion efficiencies and reducing the associated Bill of Materials (BoM).

The ADCs employed for these two applications pose a wide range of design challenges [11]-[21]. Firstly, in the context of wireless communication, the natural evolution of radio receiver architectures leads to the integration of multiple radio standards into a single receiver. Furthermore, as a result of the advancements in very large scale integration (VLSI) technology

and CAD tools for the digital designs, there has been an enormous increase in the processing capabilities of digital signal processors (DSPs). These two factors have led to the emergence of the term "software-defined-radio" (SDR), first coined by Mitola [11]. A simplified block diagram of such receivers is shown in Figure 1.2. Such radios directly digitize the input RF signals just after the antenna thus transferring the entire signal processing to the digital domain, where software is used on a high performance DSP to perform the entire signal processing function in a flexible way [11]. The realisation of SDR architectures is primarily limited by the extremely power hungry specifications of such high performance ADCs [12]-[18]. Major design challenges include the wide bandwidth (BW), higher dynamic range (DR), high linearity and low power consumption. However, with recent advances in the BP-ΣΔM ADCs design techniques along with continuous scaling of the CMOS technologies, RF digitization is becoming a reality [12]-[19]. Some of these BP-ΣΔMs operating in RF frequency employ fixed notch frequency f_N in the NTF, to shape the quantisation noise away from the band of interest, to convert the input signal located at this frequency [13][14][18]. In order to successfully digitize the entire frequency range of the input RF signal, it needs to be placed within the modulator's passband. Other solutions include the use of reconfigurable BP continuous time (CT)-ΣΔMs with a tuneable f_N [12][15]-[18]. The first part of the thesis is dedicated to the architectural level exploration, modelling, design and implementation of different ADC architectures for the SDR applications. Two different architectures for these applications will be detailed in the first part of the thesis.

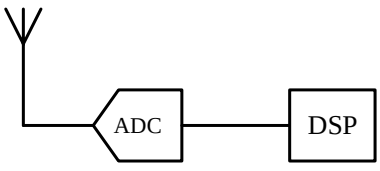


Figure 1.2. Ideal SDR based receiver architecture as proposed in [11].

In the context of PMIC design, with the increase in complexity of the current electronic systems, PMICs have become far more complex compared to a simple power supply design. A block-level diagram of a typical PMIC is depicted in Figure 1.3 [19] and the diagram represents the different sub-blocks and their functionalities at an abstract level. The most important sub-block is the output power management unit which largely consists of different DC/DC converters. In recent years, there has been a surge in digitally controlled DC/DC converters. The ADC plays a key role in such digitally controlled DC/DC converters, where it is used to digitize the sensed voltages and currents as illustrated in Figure 1.4 [21].

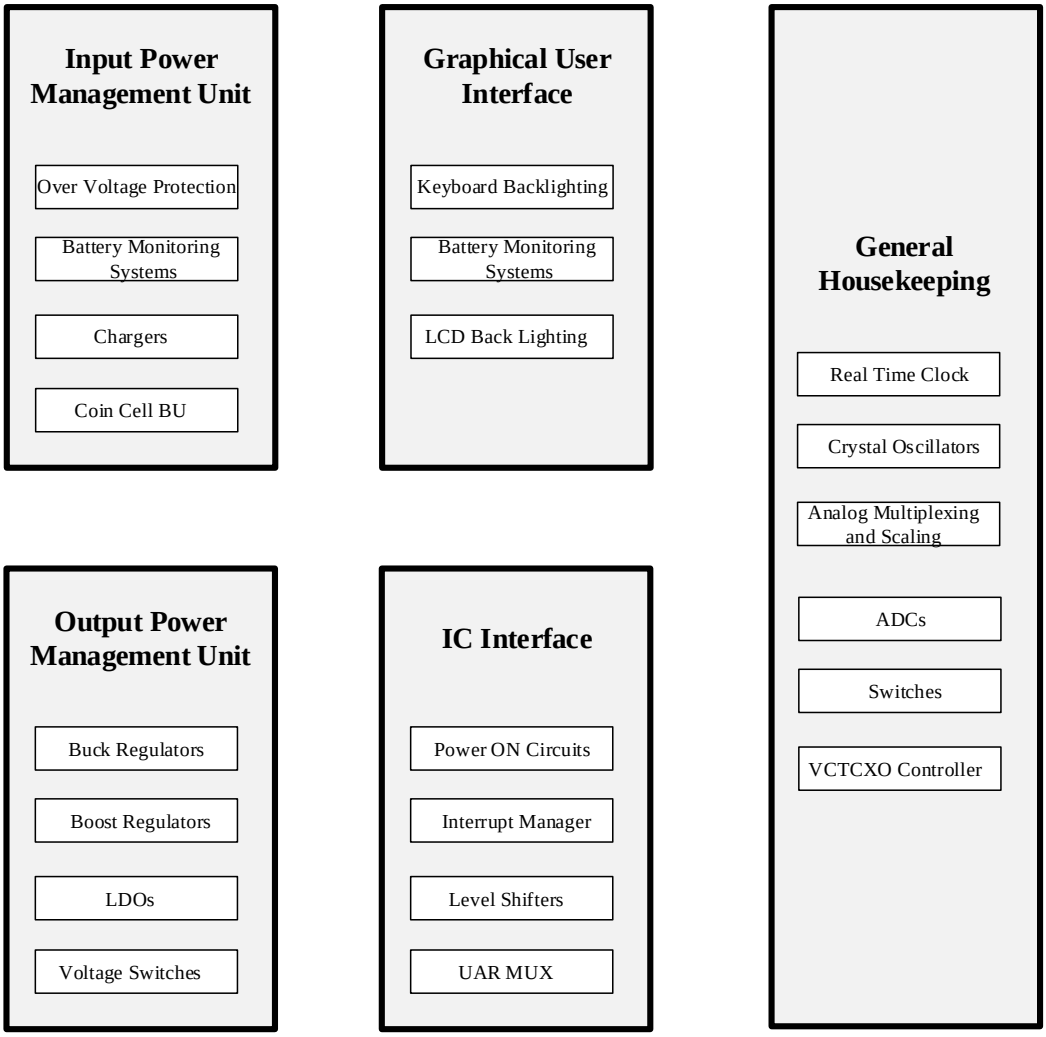


Figure 1.3. A simplified block level representation of PMIC [20].

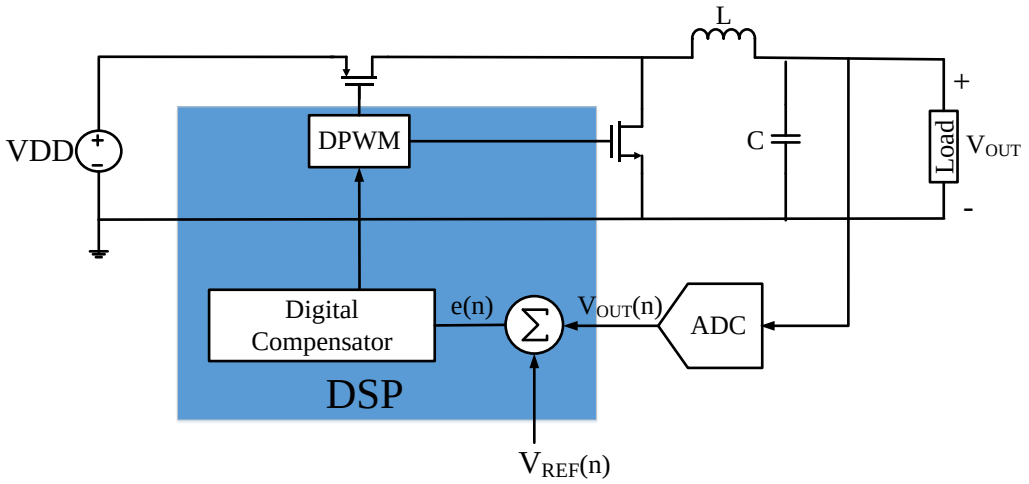


Figure 1.4. A digital controller of DC/DC converter with ADC.

Unlike conventional signal processing ADCs, these ADCs require excellent DC specifications e.g. DNL, INL, gain, offset and monotonicity. The second part of the thesis focuses on system level exploration, design and implementation of an ADC suitable for integration in a digitally controlled DC/DC converter solution. A comprehensive study of different ADC architectures suitable for this application, along with its design and implementation will be detailed in the second part of this thesis.

1.3 Thesis Organisation

The thesis is organised as follows:

Chapter 2 presents the general background of ADCs. Performance metrics and figure-of-merits (FoM) of ADCs are detailed in this chapter. Two major categories of ADCs, namely Nyquist rate and oversampling converters are also discussed briefly.

Chapter 3 presents a review of the working principles of noise shaping oversampled ΣΔM ADCs. Different topologies such as single-loop first and second-order modulators, single loop

higher order modulators, multiple loop or cascaded, as well as single and multibit quantiser implementations are explained in detail.

Chapter 4 presents an architectural level exploration and system level design of 4^{th}-order CT BP-ΣΔM ADCs for SDR applications. In the context of the SDRs comprising RF-to-digital converters, the concept of sub-sampled ΣΔM ADC is explained. A new methodology for the synthesis of CT BP implementation is also presented and discussed. Based on the said methodology, a 4^{th}-order CT BP-ΣΔM ADC has been modelled and simulated and results are presented.

Chapter 5 focuses on the design and implementation of a tuneable notch (i.e. f_N) 4^{th}-order SC ΣΔM aimed at intermediate frequency (IF) digitization. Starting from the coefficient synthesis, different architectural and circuit level techniques have been detailed in this chapter. Experimental characterization of the designed ADC is explained towards the end of the chapter.

Chapter 6 focuses on the design of the SAR ADC. Two broad categories of SAR ADCs are briefly detailed. Furthermore, SAR ADC sub-blocks i.e. sample-and-hold (S/H), DAC and comparator and their different design considerations are also detailed in this chapter. Following that, the circuit-level implementation of a 12-bit SAR ADC for power management applications is given. Different strategies for input scaling, comparator offset removal and linearity improvement along with experimental characterization are also detailed.

Chapter 7 summarises the main conclusions of the presented work and directions for potential future work.

Chapter 2: ADCs Background Study

2.1 Introduction

This chapter introduces the basic concepts of ADCs, including sampling and quantisation. ADC performance metrics are presented and examined. A basic introduction of two major categories of ADCs, namely Nyquist rate ADCs and oversampling ADCs is also given. Finally, two commonly used FoMs of ADCs are briefly explained.

2.2 Basic Concepts of ADCs

Analog signals are continuous in time and amplitude. ADC takes these signals and outputs a discrete time (DT) representation using a limited set of amplitude levels, at discrete time intervals. To achieve this, the input signal is both sampled in time domain and amplitude is quantised. This section examines the considerations associated with both steps.

2.2.1 Sampling

Sampling is the process of converting a CT signal into a DT signal. The minimum sampling frequency (f_S) required to acquire the information from the signal is twice the signal bandwidth also known as Nyquist frequency [22]. In the frequency domain, sampling produces the aliases of input signal at the multiples of f_S. As an illustration, Figure 2.1 depicts the signal-spectrum plots of input and output of sample and hold (S/H). Due to aliasing, signals or noise located at frequencies greater than the Nyquist frequency fold into the band of interest when sampled. An example of this problem is illustrated in Figure 2.2, where two signals located at different frequencies i.e. $f_S/2$ (Figure 2.2. (a)) and $3f_S/2$ (Figure 2.2. (b)) result in the same discrete time signal when sampled by an S/H as illustrated in Figure 2.2. (c).

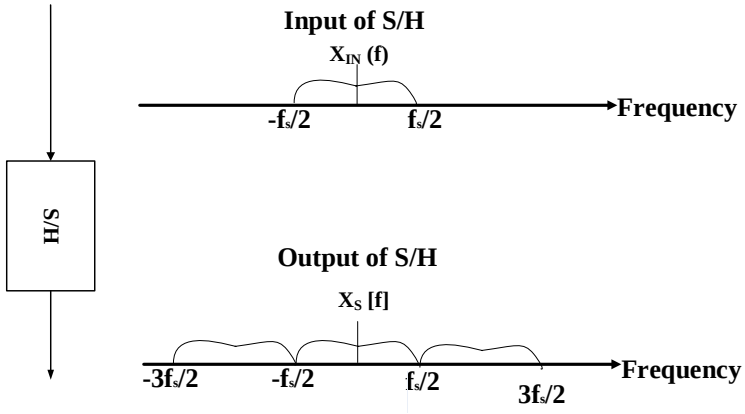
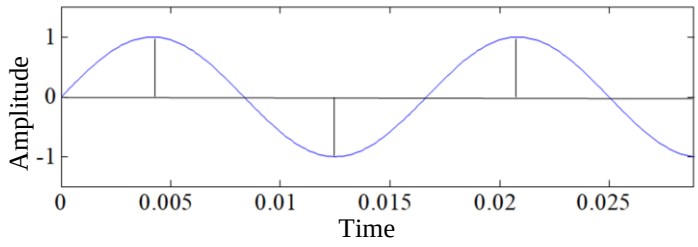
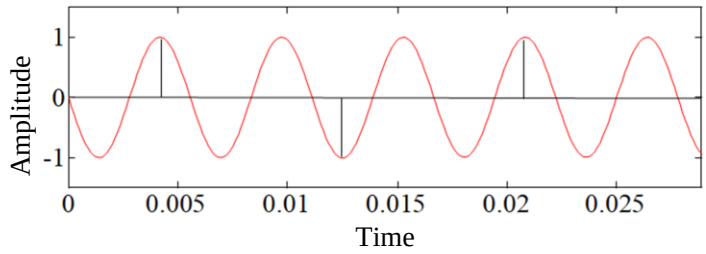


Figure 2.1. Input and output of an S/H.



(a)



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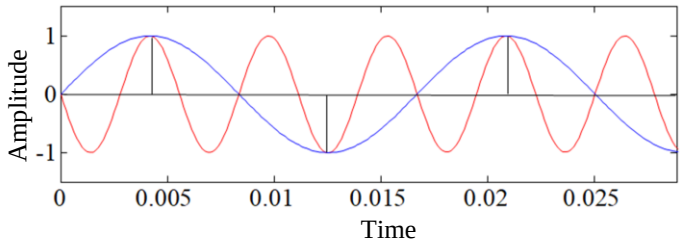


(c)

Figure 2.2. Aliasing due to two sinusoids (a) Input sinusoid at a frequency $f_S/2$ (b) Input sinusoid at a frequency $3f_S/2$ and (c) Output of the S/H.

To avoid this, usually anti-aliasing filters (AAF) are employed in front of the S/H circuit to suppress any out of band unwanted signals, from corrupting the baseband. Time and frequency domain plots of an S/H in the presence of a preceding AAF are depicted in Figure 2.3.

2.2.2 Quantisation

Quantisation is the process of discretising the signal with respect to amplitude. In this process, the signal amplitude is mapped to a limited set of values. The number of these sets of values depends on the resolution of the quantiser (also represented in bits). The difference between two consecutive output levels is called quantisation step and is represented by Δ, whereas the difference between the actual input level and the corresponding digital output level is termed as quantisation error (E_Q). The input-output characteristics of a quantiser along with its associated E_Q across the allowable range of input values are depicted in Figure 2.4 (a) and (b) respectively, demonstrating that for an input signal located within the valid input range of quantiser, the E_Q is bounded within [−Δ /2, Δ/2].

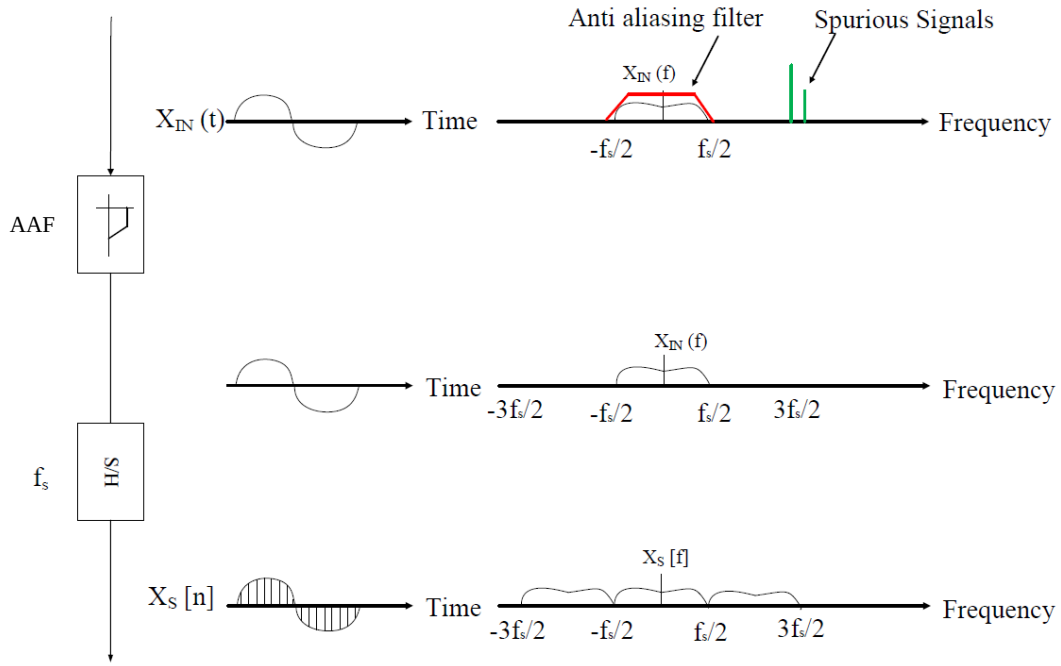


Figure 2.3. Time and corresponding frequency domain plots of an S/H with a preceding AAF.

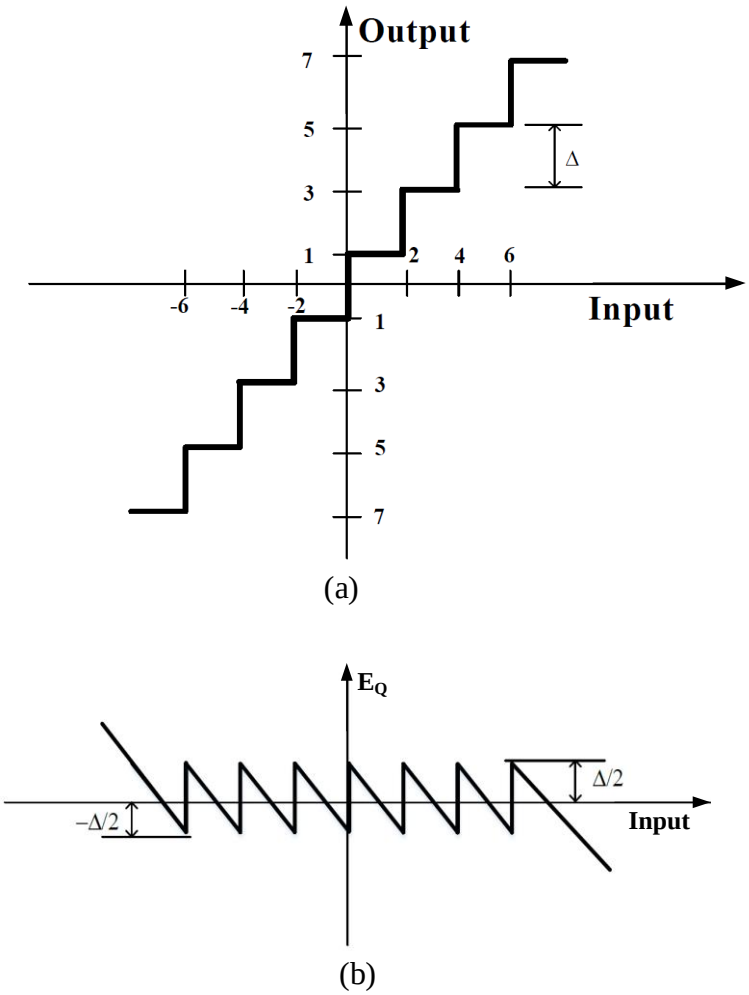


Figure 2.4. (a) Input-output characteristic of a quantiser (b) The corresponding E_Q.

When the input signal exceeds this range, E_Q increases monotonically, resulting in what is commonly referred as the overload or saturation of the quantiser (illustrated in Figure 2.4 (a)).

Due to its highly non-linear nature, the analysis of quantisers is not simple [23]. Specifically, in complex systems, like ΣΔM having a quantiser in the loop, the dynamics become quite complex and as a result more difficult to analyse. Due to this reason, many designers rely on simple models, like the "uniform white noise or additive model". Using such models, quantiser is replaced by its linearised version, thus making the analysis and design of the system simpler, while keeping a certain degree of accuracy.

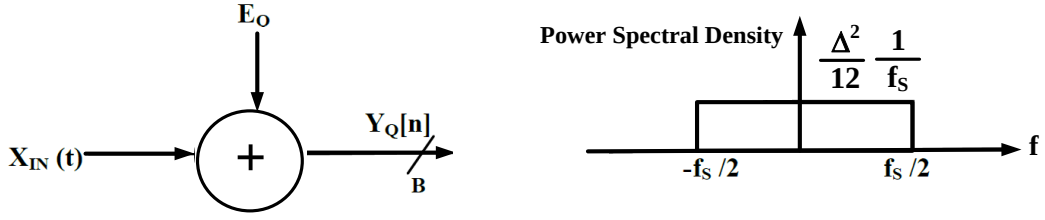
If it is assumed that the input signal changes rapidly from sample to sample by amounts greater than Δ, then the E_Q does not have any correlation from one sample to the next. As a result, it can be considered to have an equal probability of lying anywhere between -Δ/2 and Δ/2, provided that no overloading occurs. Based on this, the quantiser can be modelled as an additive uniform white noise source [23]. A block diagram of this model is illustrated in Figure 2.5 (a). Based on this model, the E_Q can be approximated by a uniform random number distributed between -Δ/2 and Δ/2 [24][25]. In this way, the total quantisation power can be approximated to $\Delta^2/12$, with a white power spectrum as shown in Figure 2.5 (b) [26] .

2.3 ADC Performance Metrics

ADC specifications can be divided in two broad categories: AC or dynamic specifications and DC or static specifications [27]. This section describes the various performance metrics associated with these categories.

2.3.1 AC Performance

The performance of the ADC in the frequency domain is characterised by AC performance metrics which are extracted from the digital outputs of the ADC by assuming a sinusoid as an input test signal. The imperfections of the ADC sub-blocks introduce noise and distortion into the digitized output.



(a) (b)

Figure 2.5. (a) Linear quantiser white noise model and (b) The associated white noise spectral density.

Thereby these metrics indicate the accuracy, noise and distortion of the digitized output. Important AC specifications include signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), dynamic range (DR) and effective number of bits (ENOB). All these specifications are briefly described in the following while a graphical illustration of these metrics versus input sinusoid amplitude is given in Figure 2.6 [28].

2.3.1.1 Signal to Noise Ratio

SNR is the ratio of the power at the frequency of an input sinusoid to the total in-band-noise power at the output of the ADC (in dBs) for specific input amplitude [1][28]. This parameter is also expressed in V_{RMS}, or %. SNR accounts for the linear performance of the ADC and therefore in-band-noise associated with harmonics is not included. For an ideal ADC having input sinusoid amplitude of "X" and considering the quantisation noise of P_Q, the SNR is represented as:

$$SNR = 10\log_{10}\left[\frac{X^2}{2P_Q}\right]. \qquad (2.1)$$

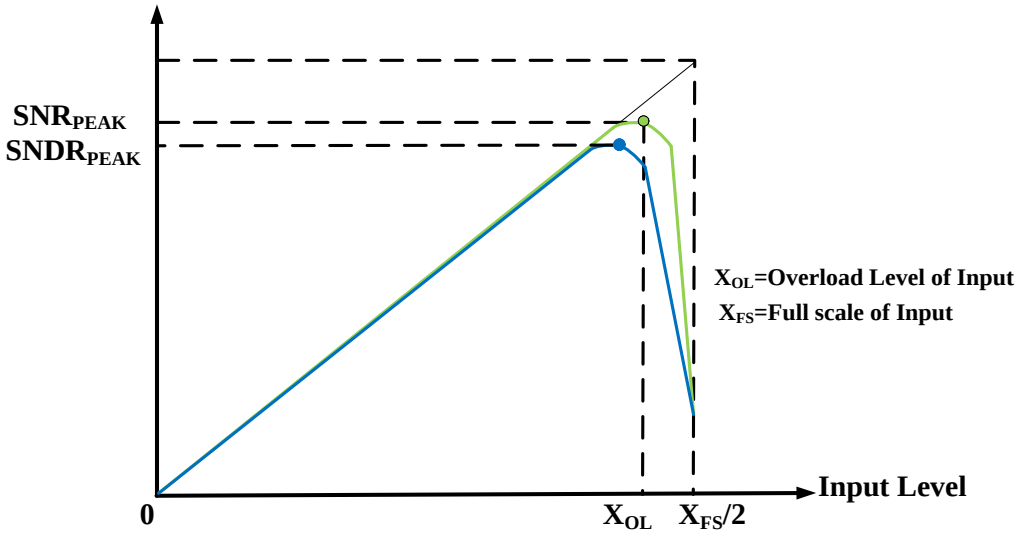


Figure 2.6. AC performance metrics on a typical SNR curve of a ΣΔM ADC [28].

2.3.1.2 Signal to Noise plus Distortion Ratio

SNDR is the ratio of the input signal power and the in band noise power while taking into account the harmonics at the ADC output as well [1]. The magnitude is typically expressed in dBs. Figure 2.6 illustrates a typical SNDR curve of a ΣΔM. For the larger input amplitudes, the curve deviates from the SNR due to the distortions. SNDR is usually calculated for $f_{IN} < BW/3$, where f_{IN} is the frequency of input sinusoid and BW is the bandwidth, so that second and third harmonics lie within the band of interest [28].

2.3.1.3 Dynamic Range

DR is the ratio of the output power of a sinusoid having maximum amplitude to the output power of the minimum detectable input signal for which SNR=0 dBs [28]. The maximum amplitude of the input signal can be characterised as peak-to-peak, zero-to-peak or root mean square (rms). The minimum detectable signal is the rms noise measured with no applied signal. For a sinusoidal input signal with maximum amplitude at the ADC input $X_{FS}/2$ having quantisation noise of P_Q, the DR can be represented as:

$$DR = 10\log_{10}\left[\frac{\left(X_{FS}/2\right)^2}{2P_Q}\right]. \tag{2.2}$$

2.3.1.4 Effective Number of Bits

The DR of an ADC is reduced due to noise, distortion and other non-idealities present. A given input cannot be resolved beyond a certain number of bits of resolution, which is known as effective number of bits (ENOB) [28]. ENOB can be represented as:

$$ENOB = \frac{\left(DR|_{dB} - 1.76\right)}{6.02}. \tag{2.3}$$

For ΣΔM ADCs, instead of a DR in (2.3), $SNDR_{PEAK}$ is used [28].

2.3.1.5 Overload Level

In the context of ΣΔM ADCs, OL is another important AC performance metric. As illustrated in Figure 2.6, the SNR of the ADC starts dropping for input amplitudes close to half of the full scale of input. In that sense, it is considered as the maximum input amplitude for which the ADC can function correctly.

2.3.2 DC Performance

The DC specifications of the ADC give the performance measures of ADC with steady state analog inputs. These specifications are more important in instrumentation and measurement applications such as temperature, pressure or weight etc. In such applications, ADC input signals are located near DC and possess very low bandwidths. Important DC specifications include DNL, INL, gain error and offset.

2.3.2.1 Differential Non-Linearity

The output of an ADC is represented in bits, whereby the difference between two consecutive output levels is equal to one least significant bit (LSB). DNL is the deviation of difference of two consecutive output levels from the ideal difference (one LSB) [29]. Due to non-idealities of the ADC, it can be higher than 1 LSB. As an example, Figure 2.7 illustrates the input-output characteristic of a 3-bit ADC having a DNL of 1 LSB. For an N-bit ADC, DNL can be represented as:

$$DNL[i] = \left[\frac{V_{i+1} - V_i}{LSB} \right] - 1 \cdot \tag{2.4}$$

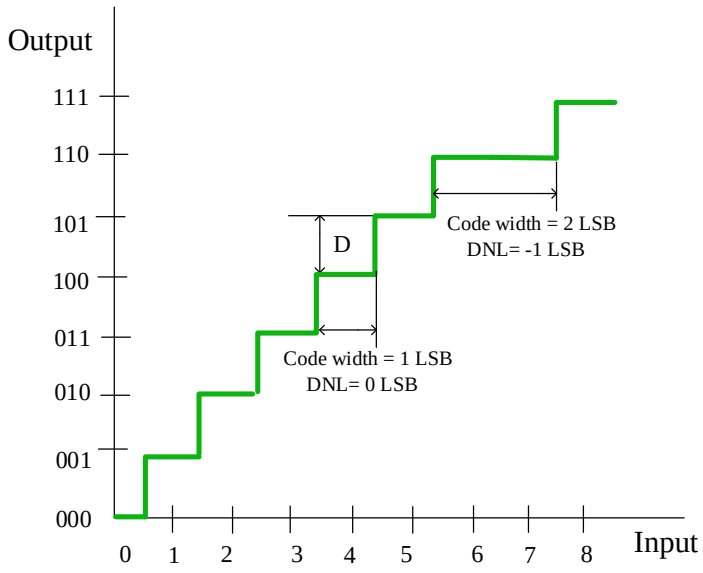


Figure 2.7. Input-output characteristic of a 3-bit ADC having 1 LSB DNL.

where "*i*" represents the output level such that $0 < i < 2^N-1$. If the DNL becomes larger than 1 LSB, a missing code can result. If the output code always increases with increasing input ADC is said to be monotonic. For an ADC to be monotonic, DNL should never exceed beyond -1 LSB. A non-monotonicity situation can be catastrophic if ADCs are being employed in feedback control systems.

2.3.2.2 Integral Non-Linearity

The INL of the ADC at a specific input is the cumulative sum of the DNL till that point [29]. It can be represented as:

$$INL[i] = \sum_{m=1}^{m=i-1} DNL[m]. \tag{2.5}$$

Where "*i*" represents the output level such that $0 < i < 2^N-1$. As an example, Figure 2.8 illustrates the INL of a 3-bit ADC at different points.

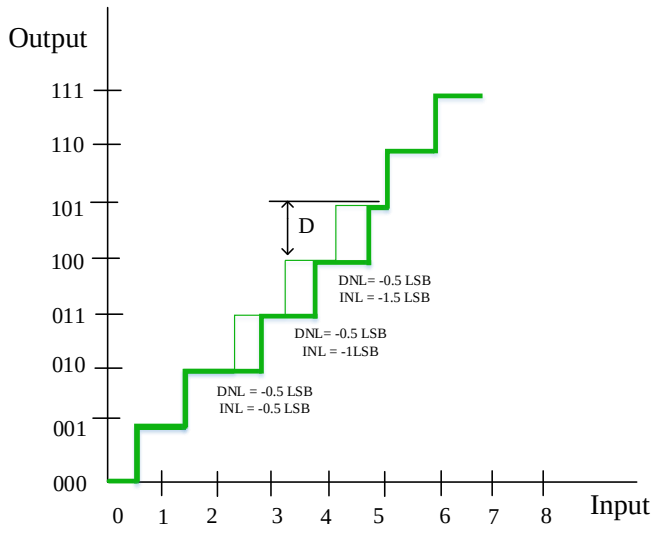


Figure 2.8. Input-output characteristic of a 3-bit ADC with INL, shown as cumulative sum of DNL.

Larger INL not only degrades the DC performance of the ADC, but in addition adds noise and distortion in the digitized signal, thus degrading the SNR. Therefore, the total amount of noise at the output of an ADC is the sum of quantisation noise and the noise introduced due to INL and can be represented as [30]:

$$V_{noise}^{\ 2} = \frac{\Delta^2}{12} + \underbrace{\frac{\Delta^2}{12}\sum_{i=0}^{2^N-1} INL_i^{\ 2}}_{INLNoise}. \tag{2.6}$$

2.3.2.3 Offset

The transfer function (TF) of an ADC is the relationship of the input to the ADC versus the code's output by the ADC. Offset error shifts the TF curve of the ADC linearly, as illustrated in Figure 2.9. The magnitude of offset error is equal to the difference between ideal start points (0.5 LSB) to actual start point [31]. As an example, Figure 2.9 (a) and (b) illustrates the input-output characteristic of a 3-bit ADC having positive and negative offset, respectively.

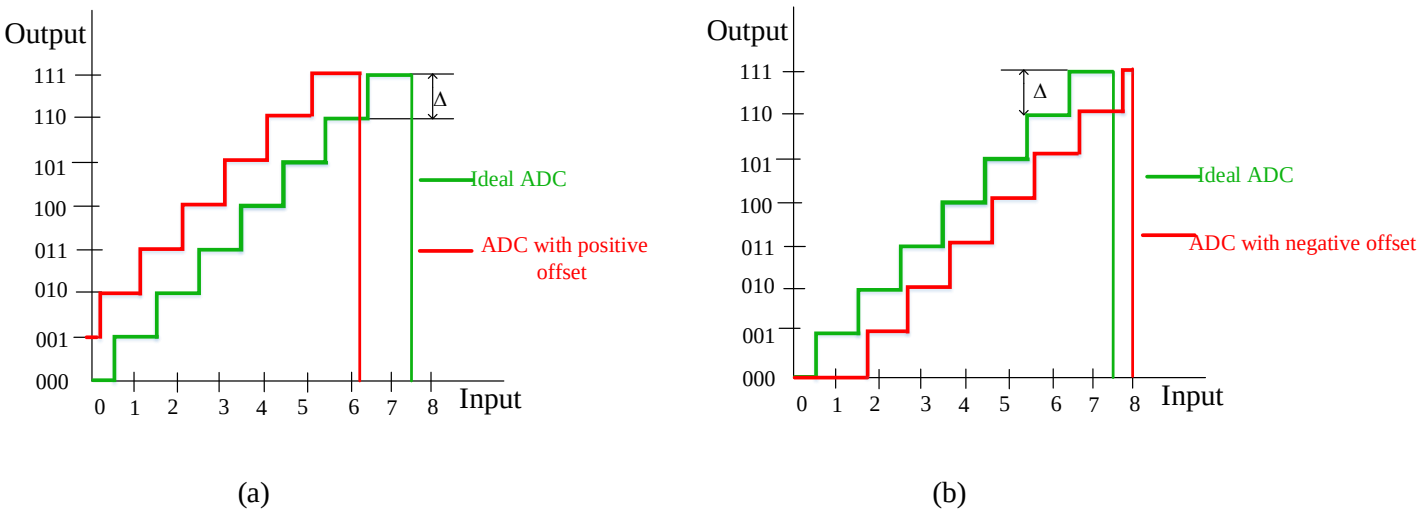


Figure 2.9. Input-output characteristic of a 3-bit ADC having (a) Positive offset (b) Negative offset.

Offset in an ADC is typically caused due to mismatches of the circuit components (transistors, capacitors, resistors etc.) and can move with ageing. Depending upon the application, different strategies can be adopted to remove the offset errors [32][33].

2.3.2.4 Gain Error

Gain error, also known as full scale error is the difference between the full scale output code and the actual value of the input providing full scale at the output [31]. Although important, this error can be removed from the digital output. The gain error of an ADC is characterised after calibrating the ADC readings for the offset.

As an example, Figure 2.10 illustrates the input-output characteristic of a 3-bit ADC having positive and negative gain errors, respectively. Note that the gain error impacts the maximum input signal.

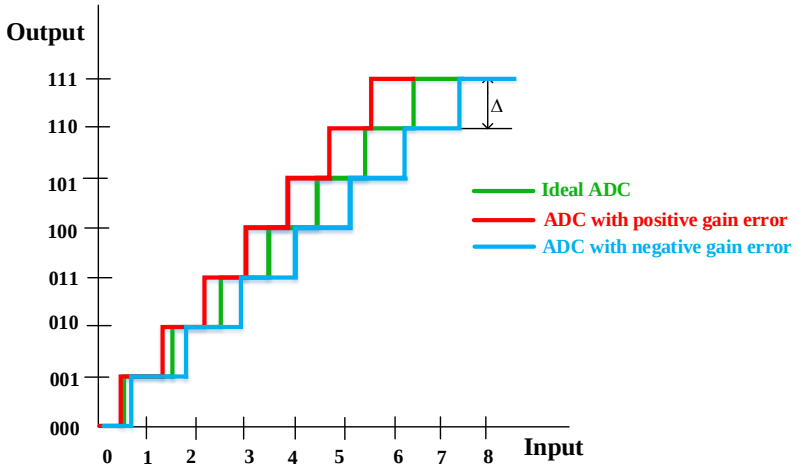


Figure 2.10. Input-output characteristic of a 3-bit ADC with positive and negative gain error.

2.4 Nyquist-rate ADCs

Nyquist-rate ADCs sample at twice the BW of input signals [27]. A block diagram of a Nyquist-rate ADC along with different sub-blocks is shown in Figure 2.11 while Figure 2.12 illustrates the time and frequency plot of the signal at the inputs and outputs of different sub-blocks of the ADC. The input signal X(t), after passing through the AAF, is sampled by the S/H and then passes through the quantiser. Sampling the input signal does not introduce any error in the signal spectrum, provided the Nyquist criteria are fulfilled.

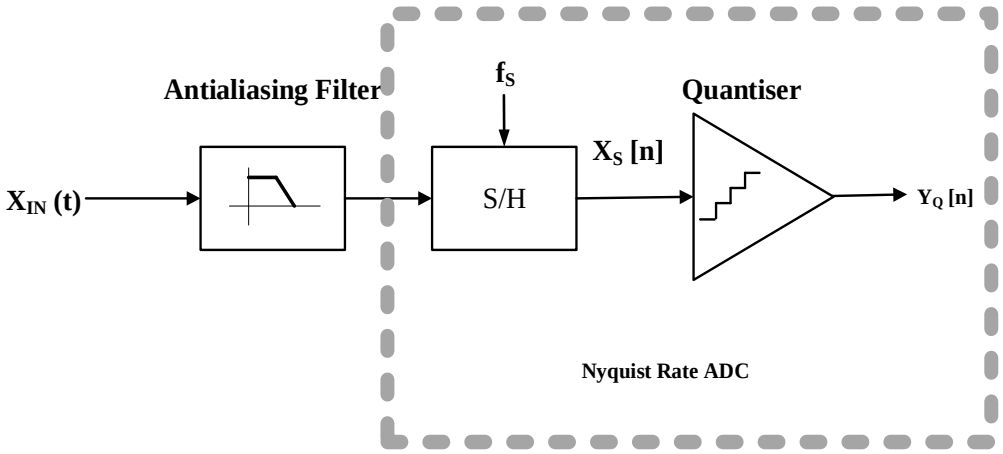


Figure 2.11. Arrangement of blocks in a Nyquist ADC.

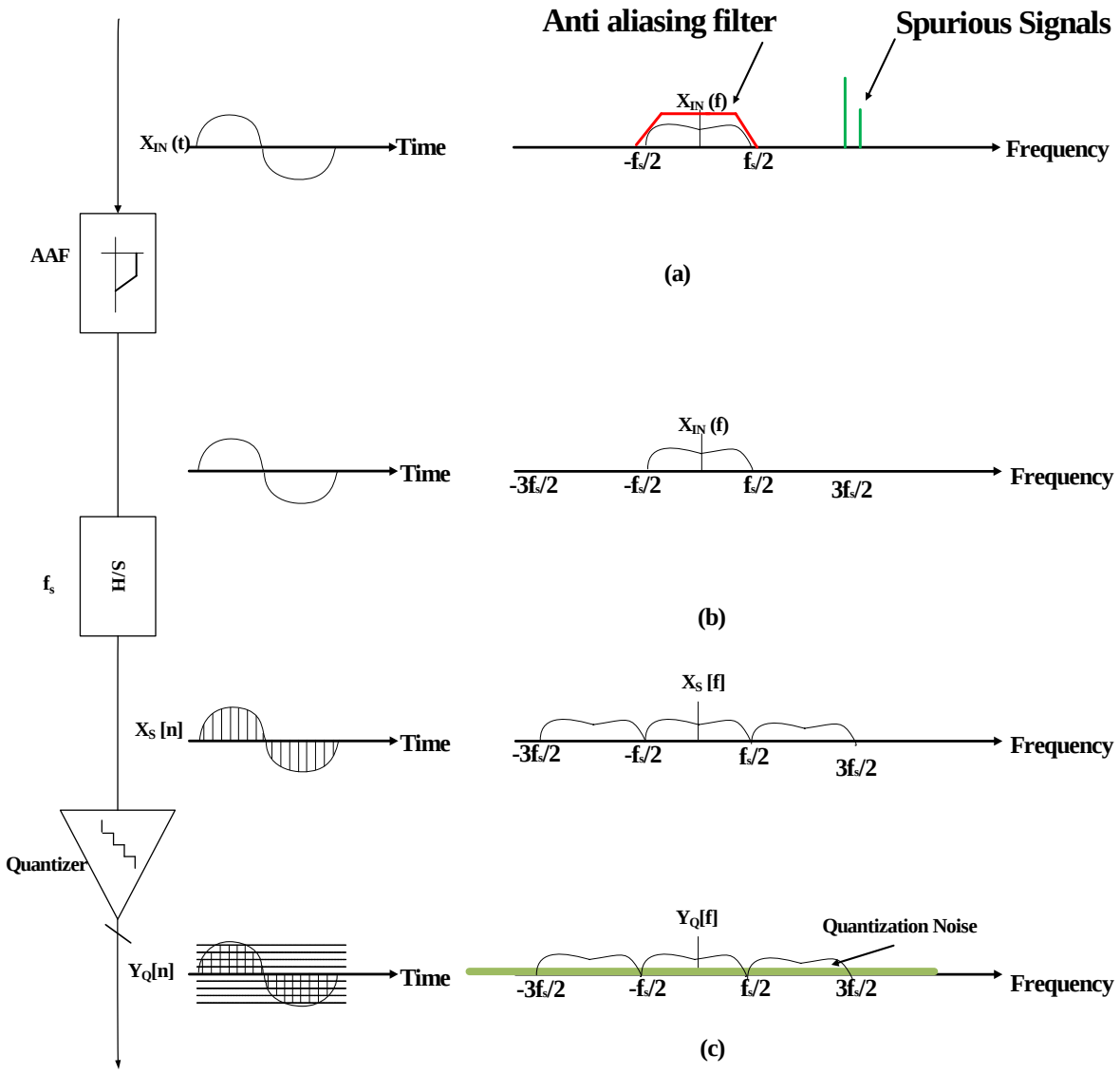


Figure 2.12. Time and frequency domain plots of signal at different nodes of Nyquist-rate ADC (a) Input signal (b) Output of AAF (c) Output of S/H (c) Output of quantiser.

The quantiser maps the amplitude values of the sampled signals into a set of discrete values, and introduces quantisation noise, which is equal to the difference between quantised value, $Y_Q[n]$, and corresponding input, $X_S[n]$. It has been shown in section 2.2.2 that for the case where the quantisation levels are separated by Δ, the E_Q can be approximated by a uniform random number distributed between $\pm\Delta/2$, that can be modelled as white noise spread over the frequency range of 0-to-f_S [23] [24].

The noise introduced by the quantiser is dependent upon the resolution (or quantisation step i.e. Δ) of the quantiser and is given by $\Delta^2/12$ [23]. The quantisation noise, P_Q, also determines the signal-to-quantisation-noise ratio (SQNR). If the maximum input amplitude applied to an N-bit quantiser is in the non-overload region is $X_{FS}/2$, then its corresponding power at the ADC output can be approximated as:

$$P_{OUT} = \frac{(X_{FS}/2)^2}{2} \cong \frac{(2^N \Delta/2)^2}{2} = \left(2^{2N-3}\Delta^2\right) \tag{2.8}$$

Therefore, the SQNR of the ideal ADC or $SQNR_{MAX}$ is given by:

$$SQNR_{MAX} = \frac{P_{OUT}}{P_Q}. \tag{2.9}$$

Here P_Q is the quantisation noise and is given by:

$$P_Q = \frac{\Delta^2}{12} \tag{2.10}$$

Employing the expression for P_{OUT} and P_Q from (2.8) and (2.10) in (2.9) gives,

$$SQNR_{MAX|dB} = 6.02N+1.76 \tag{2.11}$$

2.5 Nyquist-rate ADC Architectures

Nyquist ADCs can be realised with various architectures. Each architecture involves different trade-offs among speed, accuracy, power and area. A brief overview of three of the most important architectures namely flash, SAR and pipeline ADCs and their trade-offs are given here.

2.5.1 Flash ADC

Flash ADCs, also known as parallel ADCs, digitize the inputs with the fastest conversion time. High speed of such ADCs comes at the cost of the number of comparators employed, as 2^N-1 comparators are required for an N-bit flash ADC [27]. A block level diagram of a 2-bit

flash ADC is shown in Figure 2.13. It consists of a resistor ladder that generates the appropriate reference voltages, comparator array and a thermometer-to-binary encoder. The comparator-array compares the input voltage against the reference voltages generated by the resistor ladder. Digital circuitry at the output of the comparator array maps the thermometric output to binary. All the comparators work in parallel and thus the conversion is completed in one conversion cycle.

Flash ADCs have the highest data rate of all ADCs, but the number of comparators, power and area increase exponentially with the number of bits. Also the matching requirements of the comparators are another limitation in achieving medium to higher resolution [27].

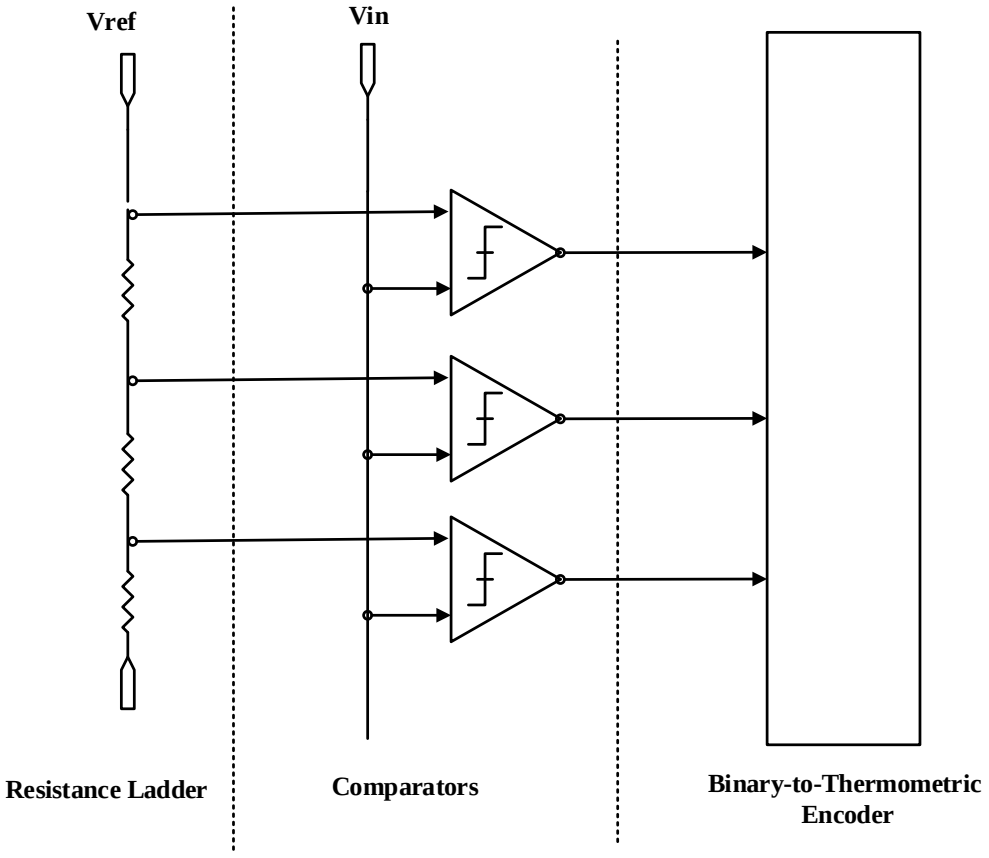


Figure 2.13. Flash ADC.

2.5.2 SAR ADC

The SAR ADC is a preferred architecture for the low power applications as it consists of only one active block i.e. comparator [34]. A simplified block level diagram of SAR ADC is shown in Figure 2.14, which consists of an S/H, a digital-to-analog converter (DAC), comparator and digital SAR logic [34] [35].

The SAR ADC operation is as follow:

1) The input signal is sampled with an S/H.
2) The sampled input signal is compared against the different voltages generated from the DAC. During the first bit trial also known as the most significant bit (MSB) trial, V_{IN} is compared with the half of the reference voltage ($V_{REF}/2$).
3) The resultant MSB sets the search region for the next bit trial. Based on the binary search algorithm result, during the second bit trial (MSB-1 bit trial), one quarter of reference voltage ($V_{REF}/4$) is either added or subtracted from the previously applied reference and compared with input.
4) The process is performed for each of the N-bit trials.

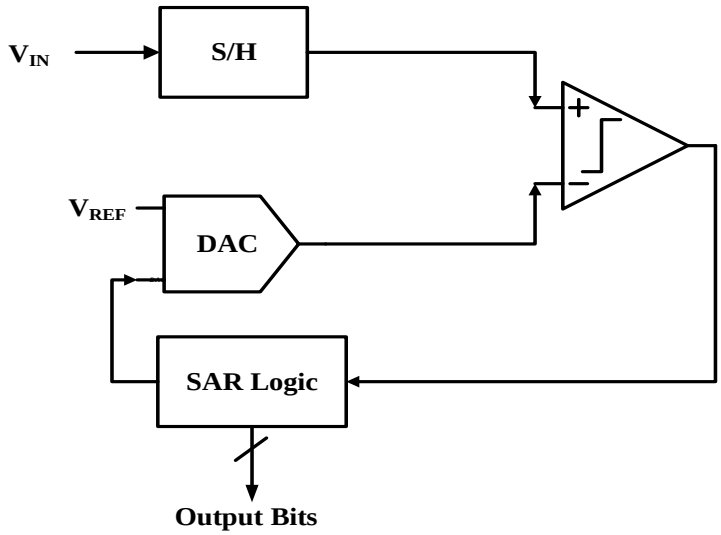


Figure 2.14. Basic SAR ADC.

There are two main limitations associated with the SAR ADC architecture. Firstly, due to the matching limitations of the current CMOS technologies, achieving resolution higher than 10-bits in SAR ADC requires extra measures, especially calibration. Secondly, this ADC works in a sequential manner resulting in lower speed compared to their flash counterparts [27]. Using various techniques (such as time interleaving), the speed of SAR ADCs can be increased but at the cost of design complexity [36].

2.5.3 Pipeline ADC

A pipeline ADC employs a cascade of low-resolution ADCs to achieve the higher resolutions as shown in Figure 2.15. It consists of multiple coarse-ADCs arranged in series. Each coarse-ADC consists of three major blocks: a sub ADC, a DAC, and a residue amplifier.

The ADC functions in a sequential way. As shown in Figure 2.15, input voltage is applied to the first stage that generates a digital output. This digital output is then subtracted from the input signal using the DAC generating a residue signal. This residue or error signal is passed through an amplifier before being fed as the input signal into the next stage. The remaining stages operate in a similar manner. The digitized outputs from all the stages are combined using a digital block to generate the final output [37].

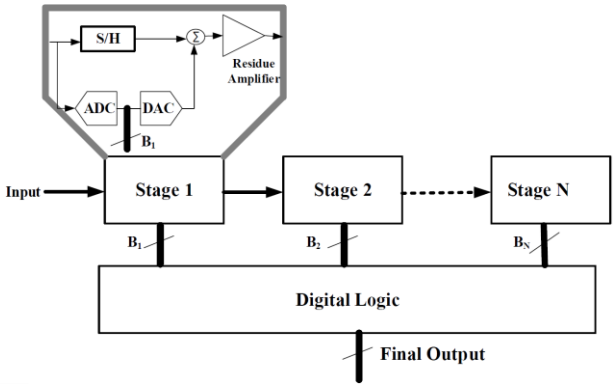


Figure 2.15. Pipeline ADC

These types of ADCs are suitable for achieving higher resolutions with smaller number of comparators than flash ADCs. The major drawbacks of these ADCs are latency and higher power consumption.

2.5.4 Limitations of Nyquist-rate ADCs

One of the important limitations of Nyquist rate architectures is that the circuitry required and hence power and area consumption, increases for every additional bit of resolution. Also, due to the matching limitations of the different components in the CMOS process, attaining a resolution higher than 10-bits in some architectures like SAR, flash etc. require additional measures like calibration, segmentation etc. [27][38] . Hence, these architectures are typically limited to low and medium resolution applications.

2.6 Oversampled ADCs

Oversampled ADCs employ a sampling rate i.e. f_S, much higher than the Nyquist rate. Two advantages of such ADCs compared to Nyquist-rate ADCs are the relaxed specifications of AAF and lower quantisation noise and enhanced resolution.

The ratio of f_S and Nyquist-rate in such ADCs is known as oversampling ratio (OSR) and is given as:

$$OSR = \frac{f_S}{2 \quad BW}. \tag{2.12}$$

It was previously stated in section 2.2.2 that the quantiser maps the sampled input to a discrete set of values and introduces quantisation noise with power equal to $\Delta^2/12$ [25][26]. If f_S is increased above Nyquist frequency, the quantisation noise power remains the same but now it is distributed over the wider frequency range and hence the in-band noise is reduced by the same ratio.

Figure 2.16 (a) and (b) illustrates the Nyquist-rate and oversampled ADCs along with their power spectral density (PSD) of quantisation noise, respectively. Oversampled ADCs are typically followed by a LP filter and down-sampler which is commonly referred as the decimation filter.

The quantisation noise in the band of interest is given by:

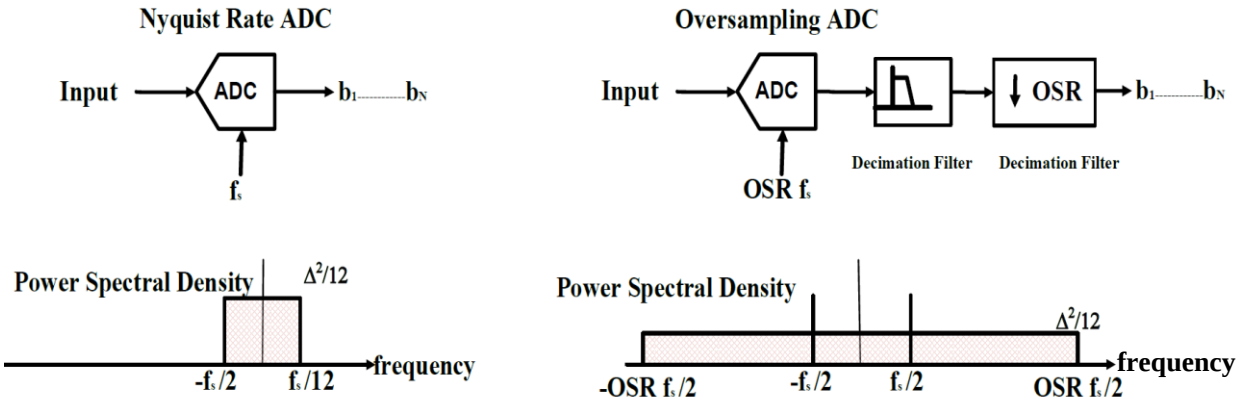
$$P_Q = \frac{\Delta^2}{12\,OSR} \tag{2.13}$$

Applying the same procedure as described in section 2.4, the $SQNR_{MAX}$ can be calculated as follow:

$$SQNR_{MAX} = \frac{P_{OUT}}{P_Q} \cong \frac{\left(2^N \Delta/2\right)^2 OSR}{\Delta^2/2} = \left(\frac{3}{2}2^{2N}\right)OSR \quad . \tag{2.14}$$

$$SQNR_{MAX} = \left(6.02N + 1.76 + 10\log_{10} OSR\right)dB. \tag{2.15}$$

In other words, oversampling by a factor of 4, increases the $SQNR_{MAX}$, by 6 dB or one bit.



(a) (b)

Figure 2.16.Quantisation noise of (a) Nyquist-rate ADC (b) Oversampled ADC.

In order to further reduce the P_Q in the band of interest, it can be processed using the feedback, also known as ΣΔM ADCs. In recent years, ΣΔ modulation has become the primary technique in analog-to-digital conversion for realising ADCs with resolutions higher than 12-to-14 bits, especially in the context of modern audio, industrial and measurement applications [5][28][39]-[42]. A detailed analysis of ΣΔM ADCs is presented in chapter 3.

2.6.1 Limitations of Oversampled ADCs

There are two major limitations associated with the oversampled ADCs. When used with higher OSR rates, the required power consumption becomes too high [28]. The second problem is associated with the linearity requirements of the quantiser that increases with the resolution. Consider a 6-bit ADC that employs oversampling to obtain an effective in-band resolution of 10-bits. In this case, the quantiser should meet the linearity requirements of a 10-bit (or higher) ADC.

2.7 Figures of Merit

In order to be able to compare the various ADC architectures, conversion rates, resolutions and their implementation in a variety of process technologies, a FoM is used.

Two most widely used ADC FoMs in different scientific publications are the 'Walden FoM' (FoM_W) and the 'Schreier FoM' (FoM_S) and are calculated as [43][5]:

$$FOM_W = \frac{P}{f_s 2^{ENOB}} \tag{2.16}$$

$$FoM_S = SNDR(dB) + 10\log_{10}\left[\frac{P}{2^{ENOB} DOR}\right]. \tag{2.17}$$

The FoM_W specifically focuses on quantisation noise limited ADCs and emphasises the relationship between conversion energy and quantisation. Based upon this FoM, the conversion

energy increases by a factor of two when doubling the conversion accuracy (6dBs in SNDR or one extra ENOB). Therefore, a lower FoM_W means a more power efficient ADC. On the other hand, the FoM_S specifically addresses thermal noise limited designs. It reflects that to reduce the in-band thermal noise by 50%, the resultant energy consumption increases by a factor of four. Therefore, a better ADC is characterised by a higher FoM_S. Figure 2.17 and Figure 2.18 illustrate the FoM_W and FoM_S of the different ADCs reported in different scientific publications over the years [5]. These two figures show the historical progress in ADC performance with a focus on energy per sample, SNDR and speed. The dotted lines in the figure show the implicit performance barriers. Over the years, a significant improvement in the ADC performance can be observed.

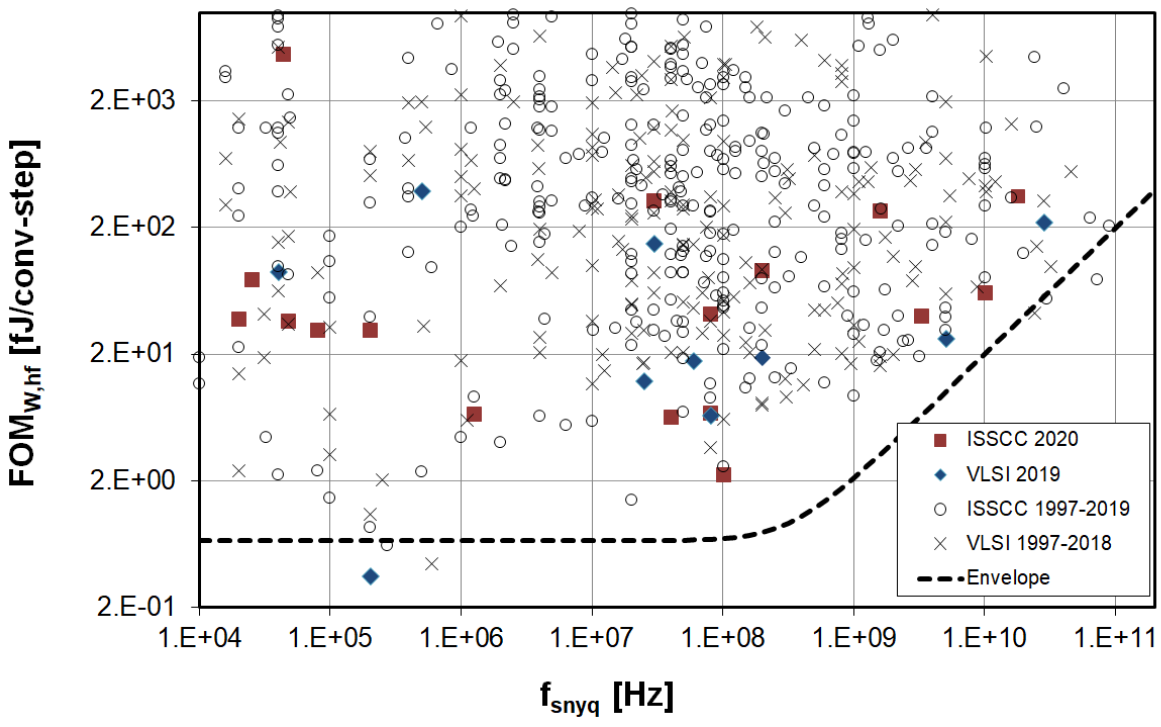


Figure 2.17. FoM_W versus DOR for different ADCs published in VLSI and ISSCC [5].

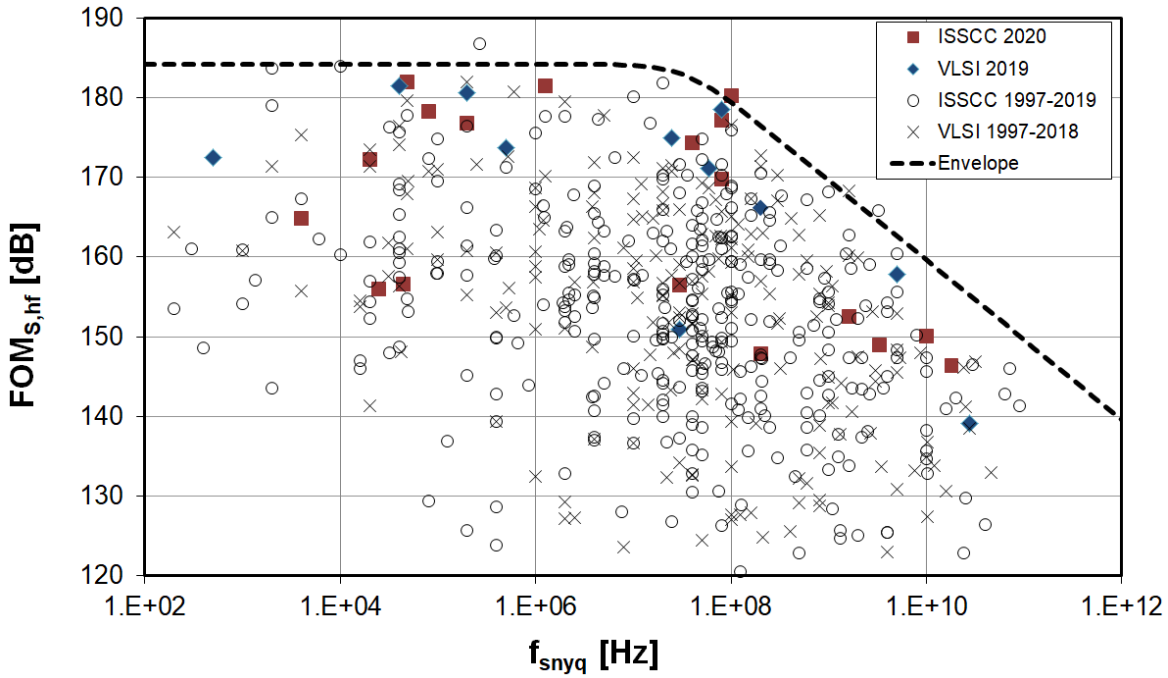


Figure 2.18. FoM$_S$ versus DOR for different ADCs published in VLSI and ISSCC [5].

As an illustration Figure 2.19 and Figure 2.20 shows the FoM$_S$ versus BW and ENOB for the four different architectures namely flash, pipeline, SAR and ΣΔMs. Both these figures have been drawn by extracting the data from [5].

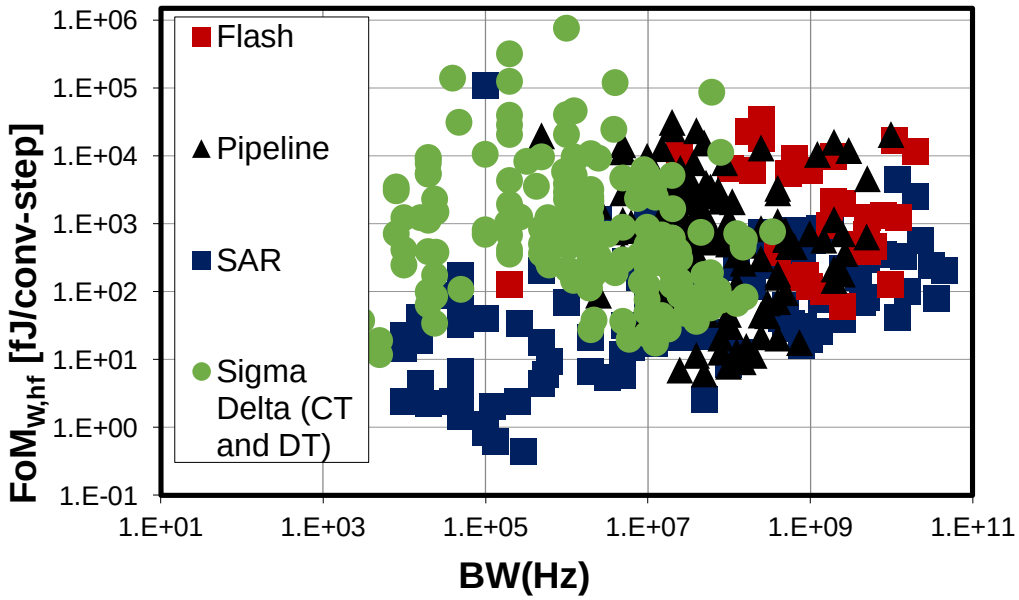


Figure 2.19. FoM$_W$ versus BW plot of the reported architectures in [5].

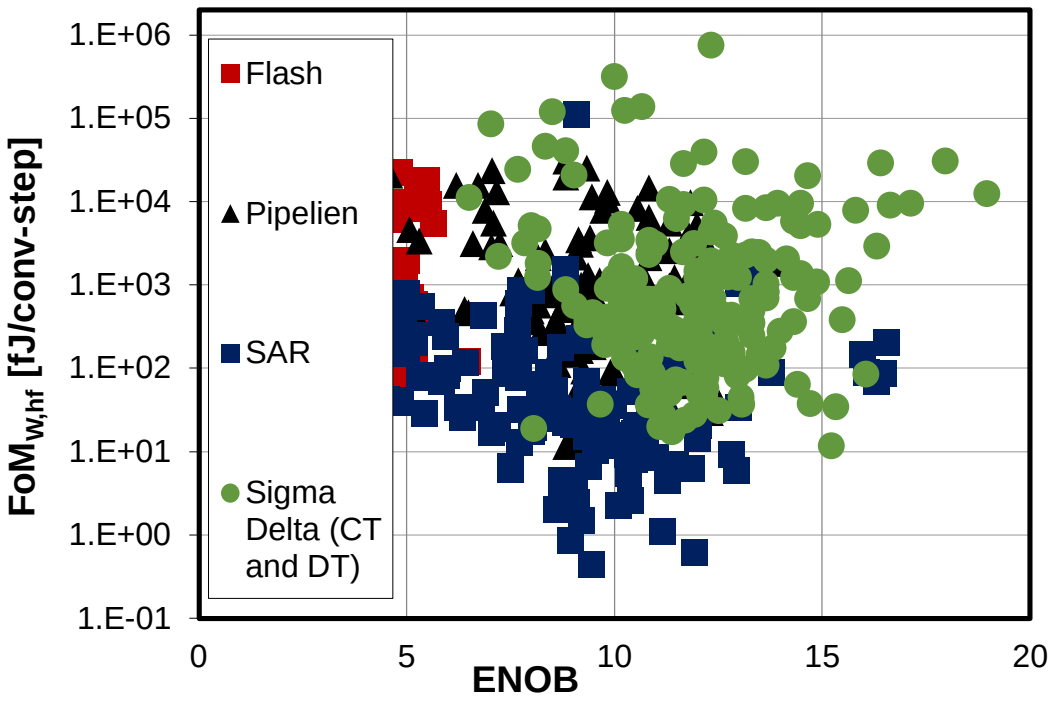


Figure 2.20. FoM_S versus DR plot of the reported architectures in [5].

For higher BWs (in the range of few hundred MHz to GHz) and (comparatively) lower resolutions (4-to-7 bits) flash ADCs are the most prevalent architectures. While the pipeline ADCs dominate for the higher resolutions (greater than 12-bits). ΣΔMs are another attractive option to achieve higher resolutions with comparatively lower power consumption and less precise components (a detailed discussion is given in Chapter 3 and 4). SAR ADCs have shown better performance in terms of power consumption for moderate sampling rates (from a few kHz to hundreds of MHz) while achieving a resolution in the range of 10-to-12 bits.

In a nutshell, there has been a huge improvement in ADC performance over the years in terms of achievable performance with reduced power and area consumption. The main reasons for such evolution are innovations in architecture, system and circuit level design techniques. Moreover, due to the increased digital performance of the continuously down scaling CMOS

technologies, digitally assisted analog components can achieve higher precision. This fact has also benefitted the ADCs.

Another interesting fact observed from [5] is that there has been a surge in hybrid-type architectures e.g. noise shaping SAR ADCs or replacing the internal quantiser of a ΣΔM with a SAR ADC. Moreover, time-based quantisers along with digital-assisted analog circuits have also been increasingly used to get better resolution with lower power and area consumption [5].

2.8 Conclusion

The basic principles of sampling and quantisation have been presented in this chapter. A few of the important performance metrics have also been described briefly. In addition, two important types of ADCs namely Nyquist-rate ADCs and oversampling ADCs along with their limitations have also been examined. Finally, two important FoMs have been discussed. These FoMs are very useful when comparing different ADC implementations.

Two types of the ADCs highlighted in this chapter, have different applications. On one end, Nyquist-rate ADCs, specifically SAR ADCs can achieve medium to high resolution in modern CMOS technologies with moderate or low power consumption while one the other end the ΣΔM ADCs are better suited for much higher resolution applications. In the following chapters, architectural level exploration, modelling, design, implementation and experimental characterization of both types of these ADCs for two important application areas i.e. wireless communication and PMICs are given.

Chapter 3: ΣΔM ADCs

3.1 Introduction

It has been discussed in the previous chapter that oversampling improves the achievable performance of ADCs. The maximum achievable SQNR of an N-bit ADC when oversampled by a factor of OSR, is given as:

$$SQNR_{MAX} = 6.02N + 1.76 + 10\log_{10}OSR \quad (3.1)$$

Equation (3.1) demonstrates that increasing the OSR by a factor of 4 yields one additional bit (6 dB) in resolution. The sole dependence on OSR to achieve the higher resolution ADC results in prohibitively large sampling rates. Oversampling combined with ΣΔ modulation (ΣΔM) is an effective way of obtaining higher resolution. In these ADCs, the quantisation noise is suppressed in the signal band by the noise shaping and hence for a given OSR, better resolution is achieved.

In recent years, ΣΔ modulation has become an important technique in analog-to-digital conversion for realising ADCs with a resolution higher than 12-bits, especially in the context of modern audio, industrial and measurement applications [5][12]-[19][27][28][39]-[42]. First introduced in 1962 [46], the use of such types of ADC gained importance with the advancements in CMOS processes. In current system-on-chip designs, a major portion of the silicon CMOS die consists of digital logic. As ΣΔM ADCs are based on the signal processing techniques (noise shaping), these ADCs are more suited for such applications [47]. ΣΔM ADCs can achieve higher resolutions with comparatively low-resolution analog circuits compared to their Nyquist rate counterparts [28]. Moreover, these ADCs impose lower requirements in terms of matching and tolerance for the different analog and mixed signals blocks e.g. comparators and op-amps used

[27]. These advantages have resulted in an increased interest in the design of ΣΔM ADCs [12]-[14][27][28][39]-[42][45].

This chapter introduces the basic concepts and different implementation alternatives for ΣΔM ADCs. The outline of this chapter is as follows. Section 3.2 presents the principles of noise shaping and ΣΔM ADCs. Different topologies such as single-loop first and second-order modulator, single loop higher order and multiple loop or cascaded are also described in the same section. Multibit converters are addressed in section 3.3. Section 3.4 details the BP-ΣΔM ADC while continuous time implementations of ΣΔM ADC and time-encoded quantiser based ΣΔM ADC are discussed in sections 3.5 and 3.6, respectively.

3.2 Working Principle of ΣΔM ADCs

Oversampled ADCs combined with feedback result in quantisation noise shaping that reduces the error in the band of interest [45][46]. Feedback has long since been used in electrical systems for error reduction [48]. If the forward path gain is high enough, the average value of the feedback path approaches the input and hence the quantisation noise is reduced. A basic configuration of ΣΔM ADC is shown in Figure 3.1 (a) and (b), where X(z), Y(z) and E(z) represent the input signal, the output and quantisation noise of the modulator, respectively. The forward path consists of a filter H(z) with higher gain in the band of interest and a quantiser. Due to the negative feedback, "Y(z)" is subtracted from the input X(z). The difference between these two signals is frequency weighed with the loop filter H(z). The input signal is passed to the output without attenuation while the difference is attenuated by the filter. The resultant output from the filter is passed to the quantiser that generates the next output i.e. "Y(z)". This output is again fed back to the input summing node for the next comparison. As a result of this strategy,

most of the error (or quantisation noise) is suppressed in the signal band and pushed towards higher frequencies [28].

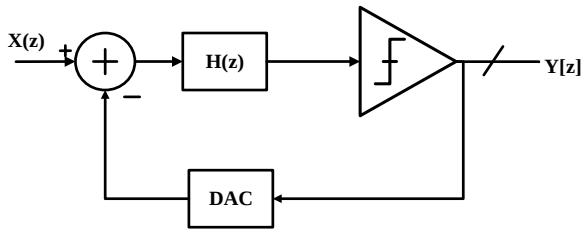
A linearized form of this model is shown Figure 3.1 (b), where the quantiser has been replaced with a white noise model (as described in chapter 2). Therefore, the ADC can be considered to have two inputs i.e. an input signal, X(z), and quantisation noise source, E(z), and one output, Y(z). The output of the ADC can be written as:

$$Y(z) = H(z) \cdot [X(z) - Y(z)] + E(z). \tag{3.2}$$

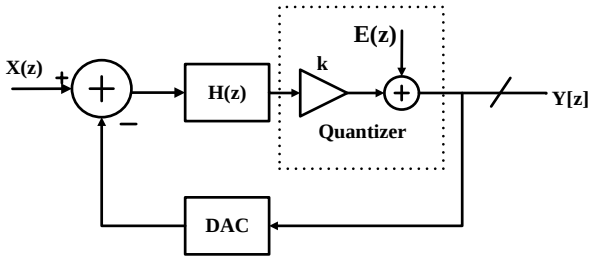
Where H(z) is the loop filter TF. Hence, (3.2) can be rearranged as:

$$Y(z) = \frac{H(z)}{1 + H(z)} \cdot X(z) + \frac{1}{1 + H(z)} \cdot E(z) \ . \tag{3.3}$$

$$Y(z) = STF \cdot X(z) + NTF \cdot E(z) \ . \tag{3.4}$$



(a)



(b)

Figure 3.1. (a) A basic ΣΔM ADC (b) Linearised model of ΣΔM ADC.

Where the signal transfer function (STF) and the noise transfer function (NTF) are respectively given by:

$$\mathrm{STF} = \frac{\mathrm{H(z)}}{1+\mathrm{H(z)}} \tag{3.5}$$

$$\mathrm{NTF} = \frac{1}{1+\mathrm{H(z)}}\,. \tag{3.6}$$

If the H(z) has a high gain at low frequencies, the STF approaches unity. Therefore, the output signal is an accurate representation of the input signal. Contrary to this, the NTF behaves as a high-pass (HP) filter and thus blocks the quantisation noise at the lower frequencies, shaping the quantisation noise away from the lower frequencies, where the input signal resides thus extending the achievable SQNR.

The concept of the noise shaping can be easily extended to BP signals, resulting in noise shaping the quantisation noise away from the band-of-interest, now centred at a frequency other than DC, which is also referred as BP ΣΔM. This will be explained in the following sections.

Over the years, several ΣΔM ADCs have been proposed [5][12]-[19][27][28][39]-[42]. Starting from a simple first-order modulator, various implementation alternatives are briefly described in the following sections.

3.2.1 First-order LP ΣΔM

A first-order LP modulator is shown in Figure 3.2. The forward path of the modulator consists of a single discrete time LP filter H(z). The TF of the integrator is given by:

$$\mathrm{H(z)} = \frac{\mathrm{z}^{-1}}{1-\mathrm{z}^{-1}} \tag{3.7}$$

Considering Figure 3.2 and employing the relationship given in (3.3), output of the first-order ΣΔM is given by:

$$Y(z) = z^{-1} \cdot X(z) + \left(1 - z^{-1}\right) \cdot E(z) \ . \tag{3.8}$$

Therefore, NTF and STF become:

$$NTF = \frac{Y(z)}{E(z)} = 1 - z^{-1}, \tag{3.9}$$

$$STF = \frac{Y(z)}{X(z)} = z^{-1}. \tag{3.10}$$

The STF in equation (3.10) signifies that the input signal is passed to the output with a single delay, while the NTF (equation (3.9)) indicates that the quantisation noise is differentiated by the modulator loop. The differentiator signifies a HP function, thus shaping the quantisation noise away from the lower frequencies and towards higher frequencies.

As an example, a sinusoidal input signal having a frequency of 31 kHz has been digitized at a sampling rate of 128 MHz (OSR=2048). The output spectrum of the ADC is shown in Figure 3.3, depicting the noise shaping with a slope of 20 dB/dec. It is evident that the quantisation noise is no longer flat and is shaped out of the band of interest into the higher frequencies.

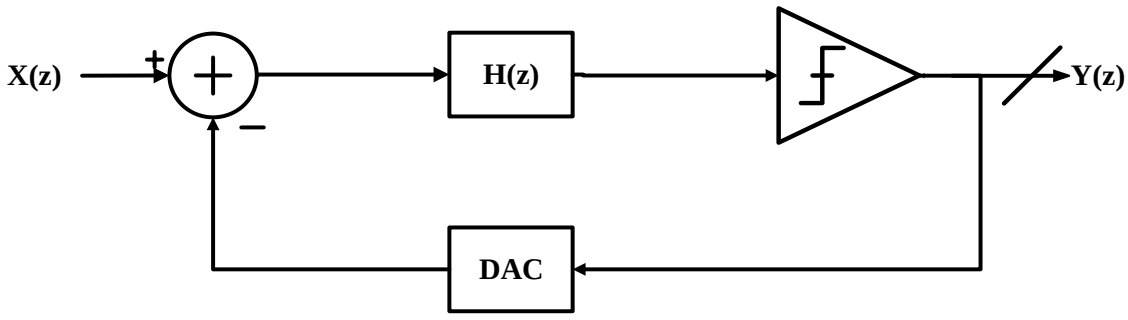


Figure 3.2. First-order ΣΔM.

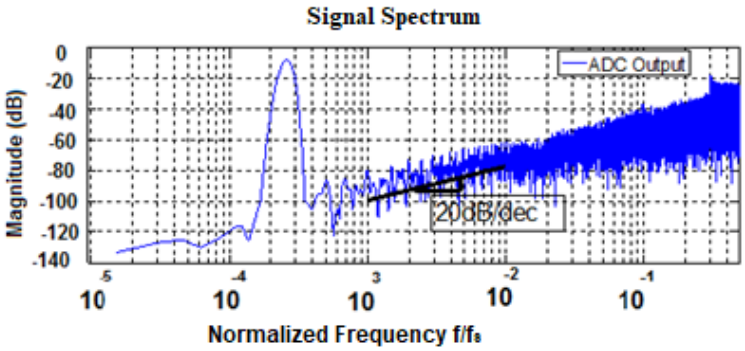


Figure 3.3. Magnitude spectrum of a first-order ΣΔM depicting a noise shaping with a slope of 20 dB/dec.

The in-band quantisation noise of a first-order ΣΔM ADC for a given OSR and single bit quantiser can be approximated as [28][49]:

$$P_Q \approx \frac{\pi^2}{3}\frac{1}{OSR^3}\frac{\Delta^2}{12} \tag{3.11}$$

$SQNR_{MAX}$ of an ADC is the ratio of full-scale input and the quantisation noise and is given by:

$$SQNR_{MAX} = \left[\frac{S_X}{P_Q}\right] \tag{3.12}$$

Where, S_X =Full-scale input (3.13)

$$S_X = \frac{1}{2}\left[\frac{\Delta}{2}\right]^2 \tag{3.14}$$

Using (3.11-3.14), the $SQNR_{MAX}$ (in dBs) of first-order ΣΔM ADC can be written as:

$$SQNR_{MAX} \approx 10\log_{10}\left[\frac{9}{2}\frac{OSR^3}{\pi^2}\right] \tag{3.15}$$

The above expression shows that doubling the OSR, increases the $SQNR_{MAX}$ by 9 dB compared to 3 dB improvement using oversampling alone.

3.2.2 Second-order LP ΣΔM

In a second-order LP ΣΔM, quantisation noise is shaped by second order in the forward path. As an illustration, Figure 3.4 shows a second-order modulator where two integrators are introduced in the forward path to obtain the second order shaping. The output of this modulator is expressed as follows:

$$Y(z) = z^{-2} \cdot X(z) + \left(1 - z^{-1}\right)^2 \cdot E(z) \tag{3.16}$$

The associated NTF and STF are:

$$NTF = \frac{Y(z)}{E(z)} = \left(1 - z^{-1}\right)^2 \tag{3.17}$$

$$STF = \frac{Y(z)}{X(z)} = z^{-2} \tag{3.18}$$

The NTF described in equation (3.17) signifies that the quantisation noise is now being double-differentiated, $(1- z^{-1})^2$, by the modulator loop resulting in higher noise-suppression in the band of interest (or higher noise shaping). As an example, an input sinusoid having a frequency of 31 kHz has been digitized at a sampling rate of 128 MHz (OSR=2048). Figure 3.5 shows the output spectrum of the ADC illustrating the noise shaping with a slope of 40 dB/dec indicating the second-order noise shaping.

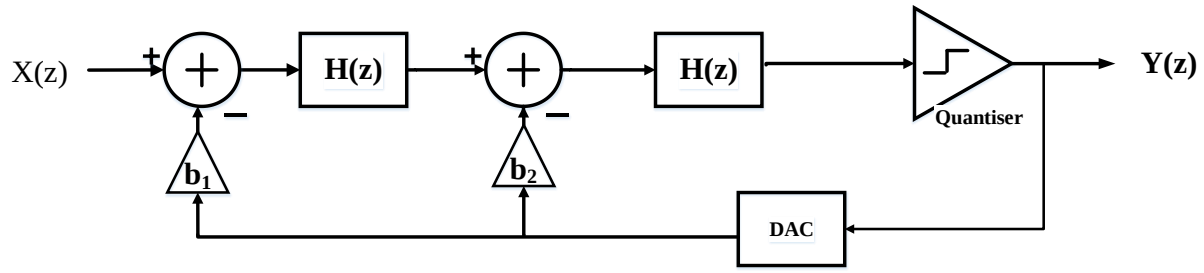


Figure 3.4. Second-order ΣΔM.

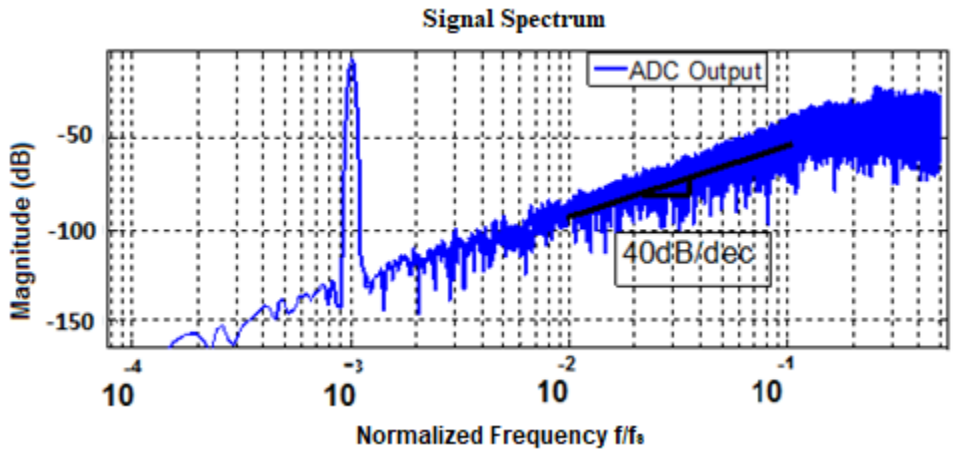


Figure 3.5. Magnitude spectrum of a second-order ΣΔM depicting noise shaping with a slope of 40 dB/dec.

The quantisation noise and the $SQNR_{MAX}$ of a second-order ΣΔM ADC for a given OSR and single bit quantiser can be approximated as [28][49]:

$$P_Q \approx \frac{\pi^4}{5}\frac{1}{OSR^5}\frac{\Delta^2}{12} \quad . \tag{3.19}$$

Using expressions for S_X from (3.13) and P_Q from (3.19), the $SQNR_{MAX}$ (in dBs) is given by:

$$SQNR_{MAX} = 10\log_{10}\left[\frac{15\,OSR^4}{2\,\pi^4}\right]. \tag{3.20}$$

Equation (3.20) shows that doubling the OSR increases the $SQNR_{MAX}$ by 15 dB compared to 9 dB improvement of first-order ΣΔM ADC.

3.2.3 Higher Order ΣΔM ADC

In order to suppress the quantisation noise more effectively at targeted frequencies, additional filtering stages can be introduced in the forward path. As an example, a higher order ΣΔM consisting of "L" integrators is depicted in Figure 3.6. Using (3.3)-(3.6), output of modulator i.e. Y(z), NTF and STF of ΣΔM can be written as:

$$Y(z) = z^{-L} X(z) + (1 - z^{-1})^{L} \cdot E(z) \tag{3.21}$$

$$NTF = \frac{Y(z)}{E(z)} = (1 - z^{-1})^{L} \tag{3.22}$$

$$STF = \frac{Y(z)}{X(z)} = z^{-L} \tag{3.23}$$

Considering a single-bit quantiser having order L, the quantisation noise and $SQNR_{MAX}$ for a given OSR can be approximated as:

$$P_Q \approx \frac{\pi^{2L}}{2L+1} \frac{1}{OSR^{(2L+1)}} \frac{\Delta^2}{12}, \tag{3.24}$$

$$SQNR_{MAX} = 10\log_{10}\left[\frac{3\,(2L+1)OSR^{(2L+1)}}{2\,\pi^{2L}}\right]. \tag{3.25}$$

The achievable $SQNR_{MAX}$ with an order of 0-to-5, over a wide range of OSR values is depicted in Figure 3.7. It shows that by increasing the loop order, higher noise quantisation suppression can be achieved at lower frequencies. In reality, the achievable performance for a higher order loop filter (L > 2) is far less than shown in Figure 3.7 due to the stability issues [50]. Unlike the first and second-order single bit modulators, the out-of-band gain (OBG) increases significantly for the higher order modulators. As a result, internal states of the modulator or the integrator outputs and quantiser input saturate more easily.

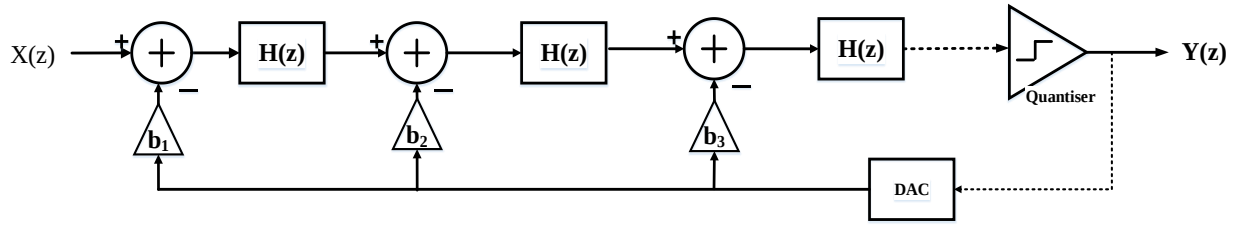


Figure 3.6. A higher order ΣΔM.

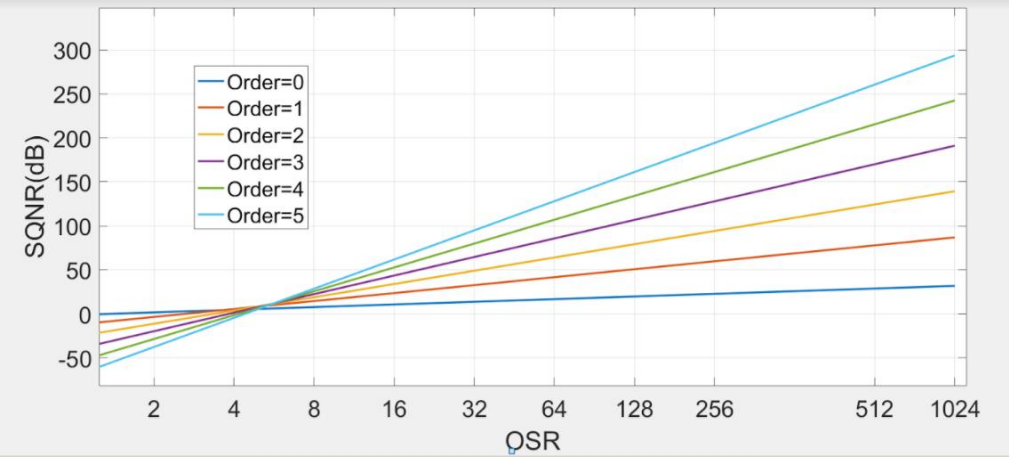


Figure 3.7. Achievable $SQNR_{MAX}$ of a ΣΔM ADC over a wide range of OSR and order.

Furthermore, larger input signals can produce low frequency, high amplitude limit cycles at the input of the quantiser [44][45][50]. These cycles are difficult to predict with the commonly used quantiser model. Different measures can be adopted to cater to stability issues. The loop filter coefficients can be scaled to keep the OBG lower. Two other measures include limiting the input signal range and the use of a multibit quantiser [50][51].

3.2.4 Cascaded or Multistage Noise Shaping

As explained in the previous section, an increase in the order of loop filter enhances the quantisation noise suppression but introduces stability problems. One way to increase the order while maintaining the stability is the cascading of stable first or/and second-order stages resulting in a high order stable system as illustrated in Figure 3.8 [52]-[56]. Each stage in the modulator processes the quantisation noise from the preceding stage while the outputs of all the stages are combined in digital domain, in a way that quantisation noise of all the stages gets cancelled, except the quantisation noise from the last stage [44][54][55]. The final output available from the digital block (known as digital cancellation logic (DCL)), has the quantisation noise shaping equal to the sum of orders of all the cascaded stages.

As ADCs with L>2 are not unconditionally stable, only first and second-order single loops are typically used. As an example, a 1-1-1 cascaded ΣΔM is shown in Figure 3.8. In order to analyse the noise shaping, consider the quantisation noise introduced by three stages are $E_1(z)$, $E_2(z)$ and $E_3(z)$. Using the linearised model, output of the modulator can be written as follow:

$$Y(z) = z^{-3} \cdot X(z) + (1 - z^{-1})^3 \cdot E(z). \tag{3.26}$$

If the error cancellation functions are chosen below,

$$\begin{aligned} H_1(z) &= z^{-1}, \\ H_2(z) &= (1 - z^{-1}), \\ H_{12}(z) &= z^{-1}, \\ H_3(z) &= (1 - z^{-1})^2 \end{aligned} \tag{3.27}$$

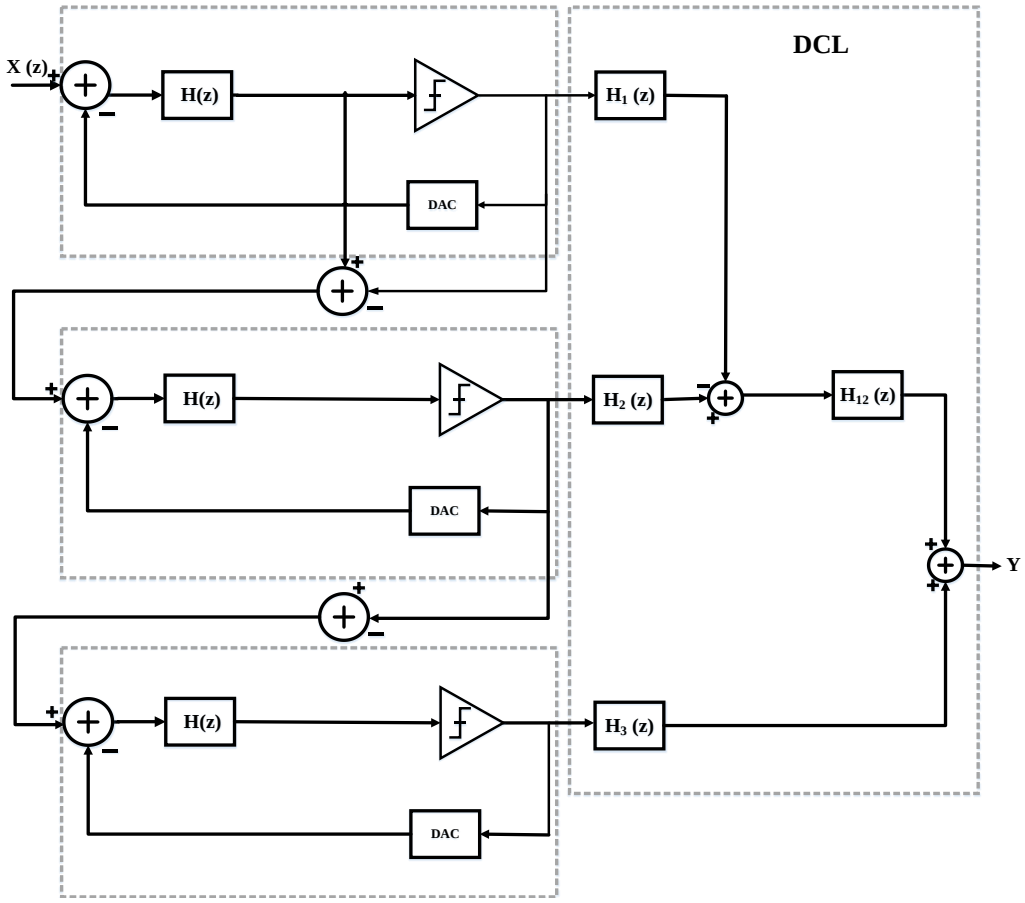


Figure 3.8. A 1-1-1 cascaded ΣΔM.

Equation (3.26) implies that the quantisation noise is now being triple-differentiated, $(1- z^{-1})^3$, by the modulator loop resulting in third order noise shaping in the band of interest.

One of the major drawbacks of cascaded ΣΔM ADCs is the noise leakage [28]. The operation of the cascaded topologies is based on the cancellation of the quantisation errors of all the stages, except the last one in the DCL. This cancellation is only perfect if the TF of the analog part and DCL are perfectly matched. However, due to several effects such as the mismatches (of capacitors, resistors or current sources etc.), the finite DC gain of op-amps and the finite closed-loop pole of the integrators, the analog TF is not ideal. As a result some of the noise from the initial stages is not fully cancelled in the DCL and appears at the output of the modulator and consequently achievable performance is degraded [56][57].

3.3 Multibit ΣΔM ADCs

As discussed previously, the achievable performance of higher order modulators diminishes either due to instability in single loop architectures or noise leakage in the cascade architectures. An alternate way to enhance the performance is using a multibit quantiser within the modulator. Each additional bit introduced in the quantiser improves the $SQNR_{MAX}$ by 1-bit (or 6 dB). The achievable $SQNR_{MAX}$ of an L^{th} order modulator having an N-bit quantiser can be represented as follows [58]:

$$SQNR_{MAX} = 10\log_{10}\left[\frac{3}{2}(2^N - 1)\frac{(2L+1)OSR^{(2L+1)}}{\Pi^{2L}}\right]. \qquad (3.28)$$

The achievable $SQNR_{MAX}$ over a range of oversampling ratios, modulator orders and quantiser bits is shown in Figure 3.9. In addition to the SQNR enhancement, another advantage associated with multibit quantisation is illustrated in Figure 3.10.

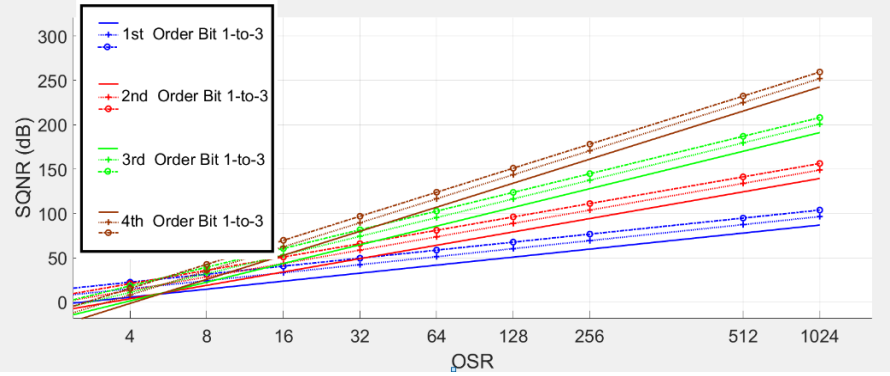


Figure 3.9. Achievable $SQNR_{MAX}$ over a range of OSR, order and quantiser bits.

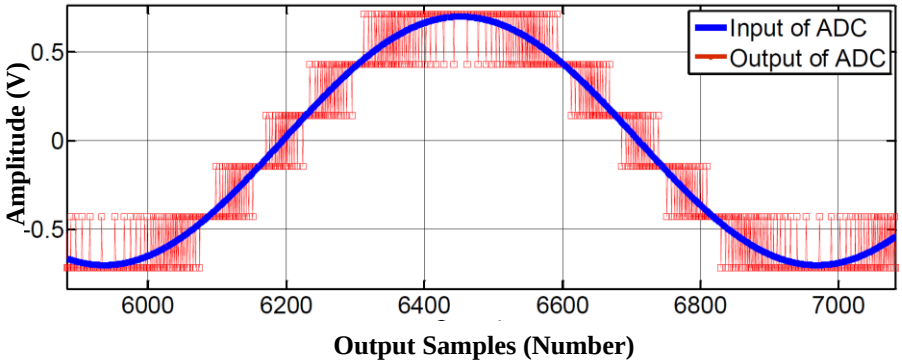


Figure 3.10. Input and output of first-order of ΣΔM ADC having multibit quantiser.

The output of such modulators follows the input more closely than their single bit counterparts. Therefore, the output swing requirements of the integrators are reduced. As a result, the slew-rate requirements and the power consumption are reduced [59]. There are two major limitations associated with multibit quantisers, which are typically implemented as a flash ADC. Firstly, the circuit complexity increases with each additional bit. Second limitation is related to the non-linearity due to mismatches in multibit feedback DAC [58]. A detailed analysis of this problem is performed in the following section.

3.3.1.1 DAC Non-linearity

A single-bit DAC has inherent linearity as it consists of a single switched element (capacitor, current or resistor etc.). Any deviation from its nominal value does not result in a non-linearity because the single element is switched either positive or negative. Contrary to this,

a multibit DAC suffers from non-linearity. Figure 3.11 (a) and (b) illustrate a ΣΔM ADC with a multibit quantiser and its associated linearised model. The errors associated with multibit quantiser and feedback DAC are represented by "E_{ADC}" and "E_{DAC}", respectively. E_{ADC} is introduced in the same path as that of the quantisation error and hence it is attenuated by the loop filter and suppressed in the signal band. The DAC errors are introduced in the feedback path and are therefore not shaped. This results in a non-linearity in the modulator. The most commonly used technique to reduce the impact of DAC non-linearity is called dynamic-element-matching (DEM) [60]. Using this technique, the one-to-one correspondence between an input code and the associated DAC error is broken and as a result the in-band distortion is reduced.

Over the years various DEM techniques have been developed [50]. Four major types of DEM include randomization [61], data weighted averaging (DWA) [62], clocked averaging [63] and individual level averaging (ILA) [60]. The major limitations of DEM are extra cost in terms of area and power.

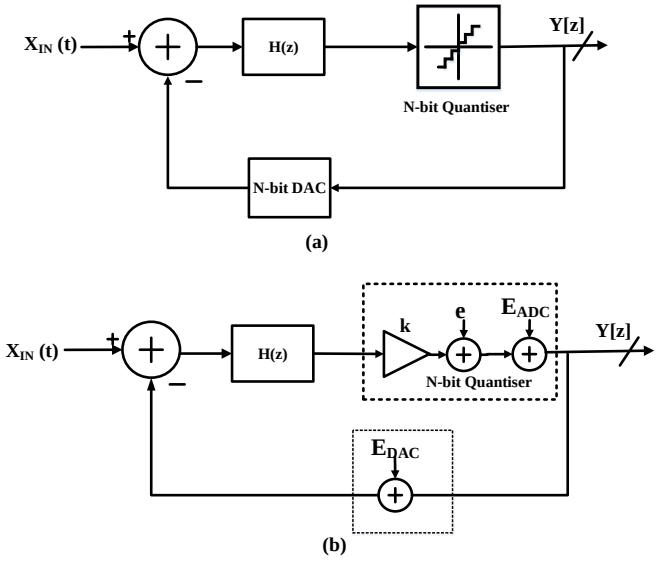


Figure 3.11. (a) A simple model of ΣΔM ADC having multibit quantiser and DAC (b) Linearised model of ΣΔM ADC with multibit quantiser and DAC.

3.4 BP-ΣΔM ADCs

As previously mentioned, ΣΔM ADCs typically have the quantisation noise suppressed at lower frequency or DC. BP-ΣΔM ADCs operate on the same principle but suppress the noise at some higher frequencies [12]-[19][40][64][65]. In the LP architectures, LP filters or integrators have been employed in the forward path. The TF of an integrator has a pole at DC which becomes zero of the NTF, hence suppressing the quantisation noise at the lower frequencies. In BP-ΣΔM ADCs, these integrators are replaced with BP loop filters resulting in an NTF having zeroes at desired notch frequencies (f_N), hence, shaping the quantisation noise away from the band of interest, into both the higher and lower frequencies. The digital output of the modulator can be translated to DC by a digital mixer and then digital LP and decimation filters are used to obtain digital baseband data, subsequently to be processed by the DSP.

3.4.1 Design of BP-ΣΔM ADCs

The most common way to design the BP filters (also referred as resonators) required in a BP-ΣΔM is to take the integrators of an already designed LP modulator and to apply a LP-to-BP transformation. A general LP-to-BP transformation is given as [66]:

$$z^{-1} \longrightarrow \frac{-z^{-2} + \cos\left(2\pi \frac{f_N}{f_s}\right) z^{-1}}{1 - \cos\left(2\pi \frac{f_N}{f_s}\right) z^{-1}} . \tag{3.29}$$

Where:

f_N = Resonant or notch frequency

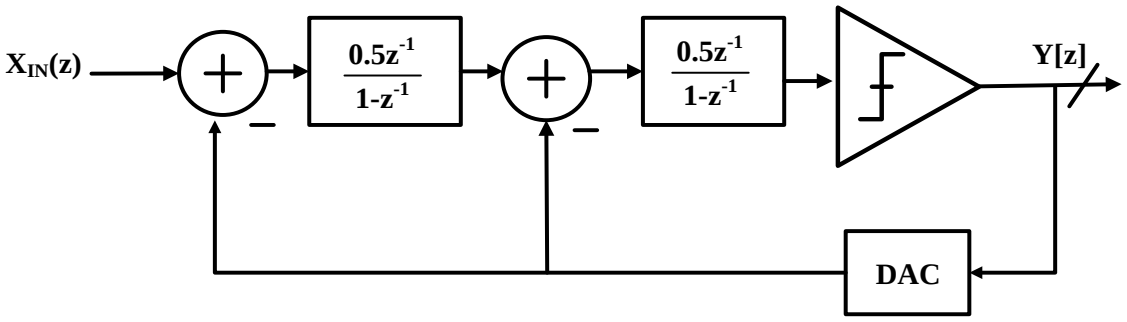
and f_S= Sampling frequency

Using this transformation, the poles of the resonators can be placed anywhere between 0 (i.e. $f_N = 0$) and π (i.e. $f_N = f_S/2$). One of the most important cases is with pole= $\pi/2$ or $f_N=f_S/4$. For this particular case, the LP to BP transformation (3.29) reduces to:

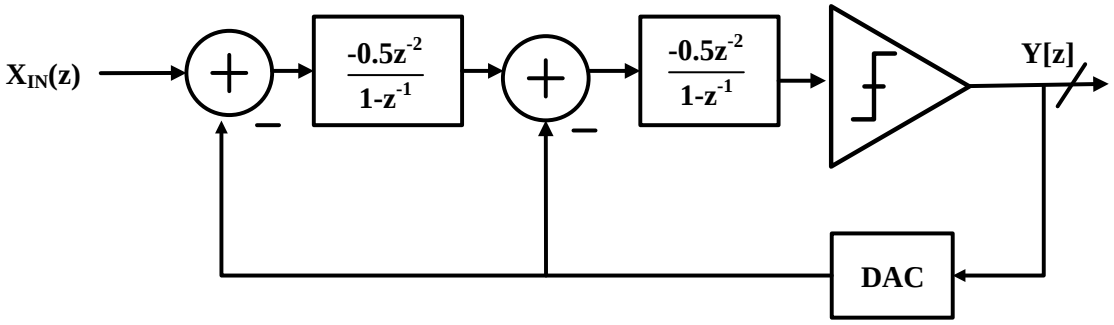
$$z^{-1} \longrightarrow \frac{-z^{-2} + \cos\left(\frac{\pi}{2}\right)z^{-1}}{1-\cos\left(\frac{\pi}{2}\right)z^{-1}} \quad , \tag{3.30}$$

$$z^{-1} \longrightarrow -z^{-2}. \tag{3.31}$$

Equation (3.31) results in a BP-ΣΔM ADC that suppresses the quantisation noise around $f_S/4$. This transformation is illustrated in Figure 3.12 (a) and (b) for a second-order LP-ΣΔM, which is mapped to a 4th-order BP-ΣΔM. Due to this transformation, the zeros of NTF are mapped to ± fs/4, reducing the quantisation noise. The achievable resolution and DR of this 4th-order BP-ΣΔM is the same as the original second-order LP-ΣΔMs. This is due to the reason that only two zeros of NTF are located at $f_S/4$, while the other two are located at $-f_S/4$, hence the quantisation noise is only suppressed with a second-order TF. Moreover, the resulting BP architecture preserves all performance metrics ($SQNR_{MAX}$, IBN, stability etc.) of its LP original counterpart. Figure 3.13 (a) and (b) shows the output spectrum of the LP and BP modulators of Figure 3.12 (a) and (b), respectively.

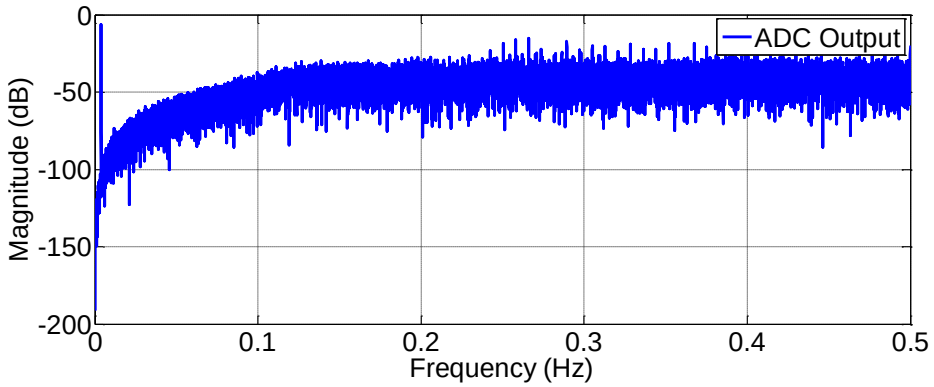


(a)

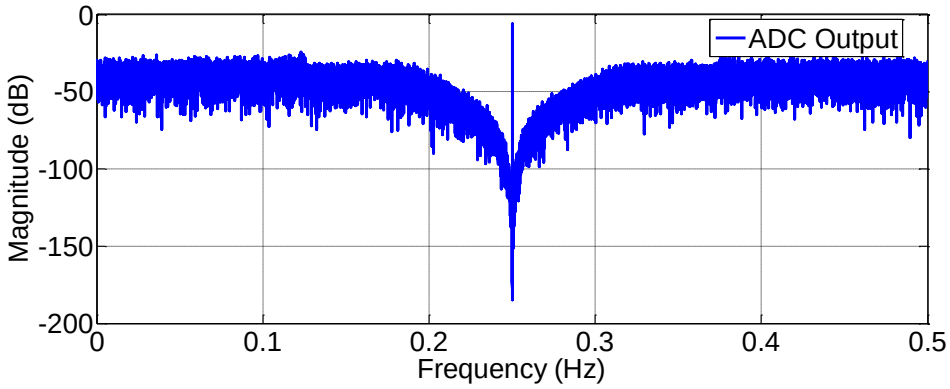


(b)

Figure 3.12 (a) Second-order LP-ΣΔM ADC (b) Equivalent 4th-order BP-ΣΔM ADC.



(a)



(b)

Figure 3.13. Spectrum plots of ADCs outputs (a) A second-order LP-ΣΔM ADC (b) Fourth order BP-ΣΔM ADC.

One major disadvantage associated with these modulators is the increased complexity over an equivalent LP modulator.[67][70].

As the BP-ΣΔMs can digitize the input signals at higher frequencies, these architectures are better suited for the direct digitization of the different wireless communication standards [12]-[19]. This trend has been further fuelled by the faster scaled CMOS technologies, innovative system level architectures and faster amplifiers [5][28][39][64][65][67][71]. First part of this thesis focuses on the utilization of the noise shaping capabilities of the BP architectures for the SDR applications to achieve the desired resolutions over wider bandwidths at higher input frequencies. In that context, two different architectures of BP-ΣΔMs capable of digitizing a wider range of wireless communication standards have been introduced. An exhaustive analysis of these modulators is given in chapters 4 and 5.

3.5 Continuous Time ΣΔM ADCs

The majority of the reported ΣΔM ADCs in the previous 30 years have been implemented using DT filters, with SC or switched current (SI) techniques as described in [68] and [69], respectively. The achievable performance of DT-ΣΔMs is limited by settling accuracy of discrete time integrators and resonators at higher sampling frequencies [70]. More importantly, incomplete settling of the first integrator is a big design concern since it must settle within the resolution of the whole ADC within one clock cycle. Therefore, for higher bandwidth applications, DT-ΣΔMs are not a suitable option. An alternate option is to realise these filters using continuous time architectures. The performance of CT-ΣΔM ADCs is not limited by settling accuracy and hence they can operate at higher sampling frequencies [28][70][71].

A generalised form of CT-ΣΔM ADC is shown in Figure 3.14 [70][72][73]. This architecture consists of an AAF, a CT loop filter H(s) along with quantiser and decimation

filters. There are some other advantages associated with CT ΣΔMs, as well. Unlike the discrete time implementation, the sampling operation in CT modulators takes place inside the ΣΔM loop (at the quantiser). As a result, all of the errors associated with sampling circuit including aliasing are noise-shaped [70]. Moreover, the loop filter also provides some degree of implicit anti-aliasing. As a result, specifications of the front end AAF are greatly reduced and in some cases, it is no longer required. Another advantage of a CT implementation is associated with the input driving circuitry of the ADC. The input capacitors in DT modulators are kept large enough to reduce overall thermal noise of the ADC. Such capacitors require larger input buffers resulting in huge power consumption. Moreover, switching noise introduced by the input circuitries degrades the achievable performance of the overall digitizing system [70]. On the other hand, due to the absence of sampling capacitors in CT implementations, complexity of input driving circuitry is reduced.

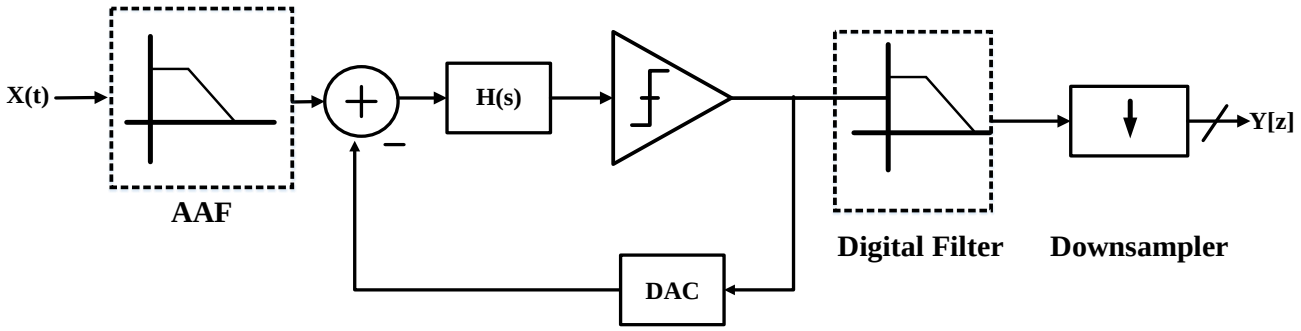


Figure 3.14. Arrangement of different blocks in a CT-ΣΔM ADC with AAF.

3.5.1 Synthesis of CT-ΣΔM ADC

A CT modulator can be synthesised from a given DT modulator by means of loop-filter transformation.The two modulators are equivalent if, for the same input waveform, input to the quantiser at sampling instants are equal [70]. For this purpose, the modulator loop is opened as depicted in Figure 3.15(a) and (b) for LP DT-ΣΔMs and LP CT-ΣΔMs, respectively.

The transformation can be represented in mathematical form as:

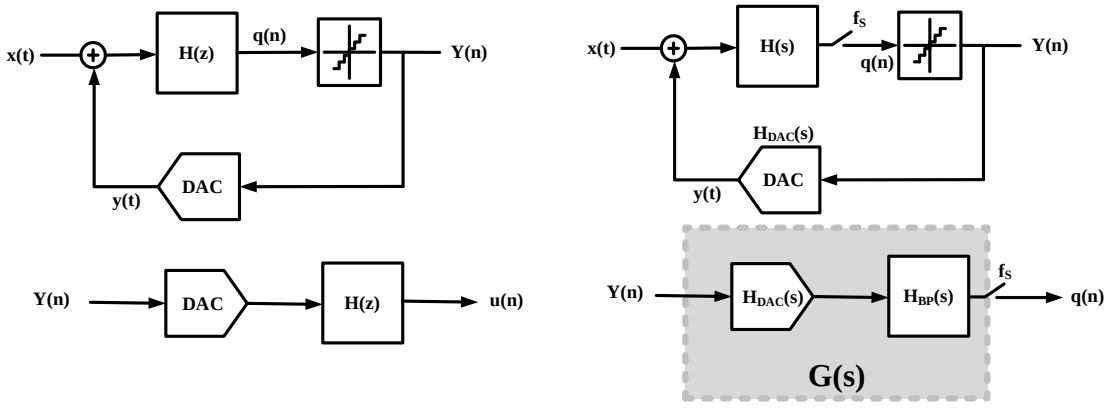
$$L^{-1}(G(s)) = z^{-1}\left(H(z)\right)\Big|_{t=nT_S} . \tag{3.32}$$

where

$$G(s) = H(s).H_{DAC}(s) . \tag{3.33}$$

Here H(s) and $H_{DAC}(s)$ are the loop and DAC TFs in CT modulators, respectively. The DAC can take different waveforms and as a result $H_{DAC}(s)$ can vary. The most common DAC architectures employed are non-return-to-zero (NRZ), return-to-zero (RZ) and half-delayed-return-to-zero (HRZ) which are depicted in Figure 3.16 and can be expressed as:

$$h_{DAC}(t) = \begin{cases} 1 & a \le t \le b \quad 0 \le a \le t \le b \le T_S \\ 0 & \text{Otherwise} \end{cases} \tag{3.34}$$



(a) (b)

Figure 3.15. Loop filter in ΣΔMs for (a) DT and (b) CT implementations.

In the S-domain, equation (3.34) is given by:

$$H_{DAC}(s) = \frac{e^{-as} + e^{-bs}}{s}. \tag{3.35}$$

Employing this transformation, the loop filter coefficients for the CT-ΣΔMs can be calculated. A more detailed analysis of the CT design methodology is presented in chapter 4.

3.5.2 Limitations of CT-ΣΔM ADCs

Two major drawbacks associated with CT-ΣΔM ADCs are the high sensitivity to clock jitter and excess loop delay (ELD) in the feedback DAC [70].

In CT modulators, the feedback waveform is integrated over time and thus the modulator performance is extremely sensitive to every deviation from the exact, ideal waveform of that feedback signal. Another limitation is associated with the loop filter coefficients which are realised by an RC or g_mC product that can have the mismatches in the range of 20%. As a result of this, the stability of such modulators becomes a big concern, specifically in higher order modulators [70] .

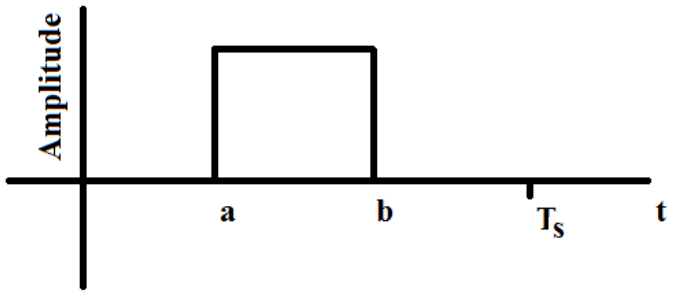


Figure 3.16. Rectangular shaped DAC waveform.

3.6 Timed-Encoded Quantiser Based ΣΔM ADCs

Instead of the amplitude, multibit quantiser can also be implemented by using the timing information of the signal for the digitization. One of the important types of such architectures is a voltage controlled oscillator (VCO)-quantiser as depicted in Figure 3.17 [54][75]. Here the quantisation is performed by the voltage-to-frequency conversion. These quantisers typically consist of an oscillator and a counter that counts the number of edges within a given time period. The result is directly related to the input signal, thus a digital representation of the input amplitude is obtained. The major limitation associated with such architectures is the nonlinear operation of the voltage-to-frequency conversion within the VCO. This problem can be overcome by using a phase detector instead of a frequency detector, as detailed in [75].

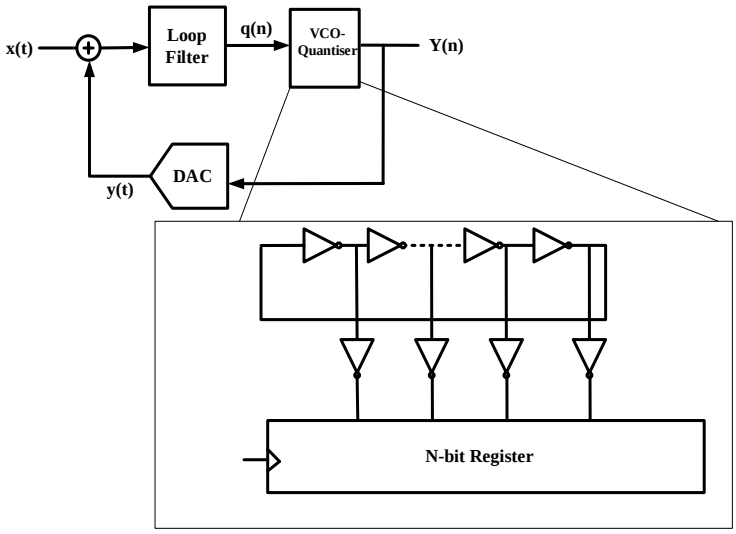


Figure 3.17. A VCO-quantiser based ΣΔM ADC

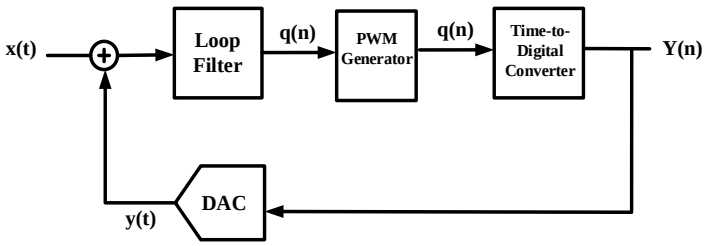


Figure 3.18. A PWM-quantiser based ΣΔM ADC

Another alternate to the quantiser is the pulse-width-modulator (PWM) as illustrated in Figure 3.18 [76]. The PWM converts the voltage into a pulse and then a time-to-digital converter (TDC) generates the digital representation of the input. The limited DR is one of the important concerns associated with PWM based quantisers [76].

3.7 Conclusion

The basic operational principles for the oversampled noise shaping ΣΔM ADCs were described in this chapter. For resolutions higher than 12-bits, oversampled ΣΔ modulation is a well-established technique compared to Nyquist rate ADCs. Different implementation alternatives of ΣΔM ADCs, including single loop, cascaded, multibit, BP and CT etc. were briefly described. Finally, time-encoded quantiser based ADCs were also discussed.

Due to high resolution requirements and the latest innovations at architectural-level and circuit-level design techniques, ΣΔM ADCs have become an important choice for use in communication related applications [5][28][39][41][49][52][71]. The next chapter describes a ΣΔM suitable for realising an SDR receiver.

Chapter 4: ΣΔM Based SDR Receivers

4.1 Introduction

An SDR receiver performs most of the signal processing in the digital domain thus allowing the programmability and adaptability to ever-emerging wireless communication standards. In these architectures, as illustrated in Figure 4.1, the ADC is ideally placed directly after the antenna so that all RF signals are directly digitized while the entire signal processing functions (e.g. mixing, filtering, channel selection etc.) are performed on the DSP using software [11].

The efficient implementation of a SDR receiver architecture is still far from a reality, which today is mostly limited by the unfeasible power-hungry specifications required for the ADC to digitize at the higher input frequencies[12]-[19][40][64][65][77]-[79]. This chapter describes an architectural-level exploration and system-level design of such ADCs. Firstly, the details about the system level design of a multistandard RF receiver and ADC are discussed in section 4.2. Following that, section 4.3 describes the previously reported RF-to-digital converters. Section 4.4 details the specifications of the targeted architecture. In order to achieve a true SDR receiver using an RF-to-digital converter, the concept of sub-sampled ΣΔM ADC is described in section 4.5.

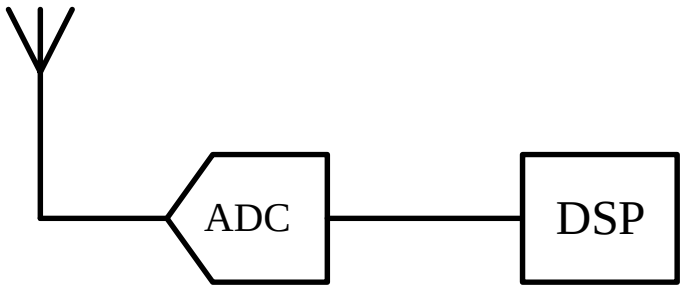


Figure 4.1. Ideal SDR bases receiver architecture as proposed in [11]

The CT BP-ΣΔM based RF-to-digital architecture proposed in this thesis is described in section 4.6. A new methodology for the synthesis of CT implementation for BP-ΣΔM ADC is then presented in section 4.7. The simulation results associated with this implementation are presented in section 4.8.

4.2 Multistandard Receivers

A direct-conversion multistandard RF receiver consists of an antenna, low noise amplifier (LNA), different types of filters, mixer and an ADC as depicted in Figure 4.2. Depending upon the wireless standard (e.g. 2G/3G/4G cellular, WLAN, Bluetooth, GPS, broadcasting etc.), the required specifications of the receiver sub-blocks vary. Each wireless communication standard has a different set of associated requirements for the different receiver sub-blocks [80]. The important performance metrics of the RF receiver include sensitivity, selectivity, noise figure (NF), DR and linearity (IIP2, IIP3 and 1-dB compression point $P_{1\text{-dB}}$).

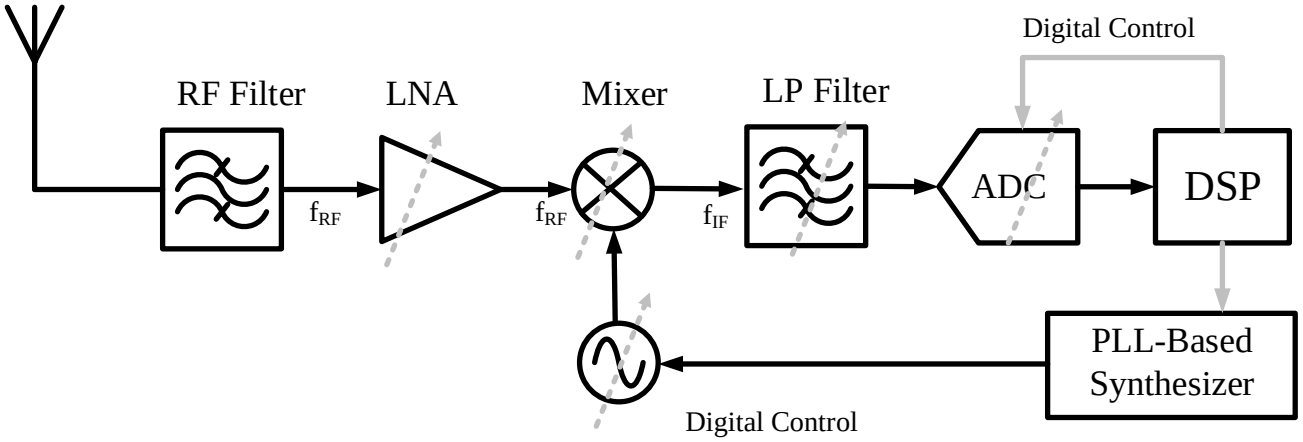


Figure 4.2. A direct-conversion multistandard RF receiver.

With the ever-growing number of wireless communication standards, realising a single reconfigurable RF receiver capable of multimode operation has become very challenging. One approach to implement a multistandard receiver is to use multiple dedicated receivers in parallel. Although simpler in terms of implementation, this approach is extremely expensive from an area perspective. Moreover, with the continuous evolution of wireless standards, scalability of such architecture remains an important question.

Over the years, various multistandard receiver architectures have been reported. One of the important examples is described in [81]. This architecture consists of 4 LNAs for the RF signals located between 0.1-to-6 GHz bands. Following this, the signal passes through a mixer and a series of filtering and amplification stages and is finally digitized with a SAR ADC. Another example of a multistandard receiver has been reported in [82]. The implemented receiver operates over an input frequency range of 0.8-to-5 GHz. The receiver uses a passive FET mixer driven by a capacitive coupled RF transconductor. Following that, a series of CT and DT analog filters are used to achieve a higher degree of anti-aliasing. Another interesting implementation has been presented in [83], that operates over the frequency range of 0.4-to-6 GHz. This architecture consists of a split front end with one operating low-band RF path (0.4-to-3 GHz) using an 8-phase passive mixer and a high-band RF path (3-to-6 GHz) using a 4-phase passive mixer. The baseband bandwidth can be reconfigured over the range of 0.5-to-50 MHz to cater for the LTE and future standards. [84] and [85] are two other interesting architectures where the output of the baseband ΣΔM ADC is used to achieve filtering at RF. [84] is capable of processing the analog signals located in the range of 0.5-2.75 GHz while achieving a peak SNDR of 38 dBs over a BW of 10 MHz. [85] achieves an SNDR of 45 dBs for 18 MHz bandwidth

signals located at a carrier (RF) of 0.9 or 1.8 GHz. Several other notable receiver implementations reported in previous years are [6][80][86][89]-[93] .

One major drawback of the mostly reported architectures is that the signal processing blocks preceding the ADC needs to be reconfigurable to support the multiple standards. This complexity increases with the on-going evolution of new wireless communication standards [86]. The simplest solution to this problem is to place the ADC directly after the antenna (as illustrated in Figure 4.1). In this architecture, the whole band of the input signals is directly digitized and the signal processing functionalities (channel selection, filtering, down-conversion etc.) are performed in the digital domain in a flexible way. This concept was first proposed by Mitola [11]. Although more attractive from a flexibility point of view, realising an ADC for such architectures is quite complex and extremely challenging. Most of the current wireless communication standards lie within the RF rage of 0.5-to-5 GHz [86]. The ADC, if implemented with a Nyquist rate ADC, would require a sampling rate in the range of 10 GHz. Moreover, without having a preceding down conversion and filtering stages, the ADC would require a resolution of 15-to-20 bits over a BW of 5 GHz. Assuming a Nyquist rate ADC operating at 10 GHz, having 15-bit resolution and a 15 fJ/conversion (considering the state of art implementations from [5]) results in a power consumption of 15 W, making it an impractical option for different hand-held devices [41][42].

The specifications of such an ADC can be highly reduced if a BP ADC with a reconfigurable notch is employed. Such BP ADC need to have an optimised performance across certain f_N [12][78][87][89]. A block level representation of an SDR-based receiver with such a BP ADC is shown in Figure 4.3. Here the incoming RF signals from the antenna passes through an RF filter and an amplifying stage and is then directly digitized by BP ADC. This ADC

digitizes only the frequency band of interest located across its centre frequency (or f_N) with relatively lower power consumption compared to Nyquist-rate ADCs (that digitizes the whole range of inputs from DC-to-$f_S/2$).

4.3 BP-ΣΔM ADCs for SDR Based Receivers

Over the years, various implementations of BP-ΣΔM ADCs targeting RF digitization have been reported. Two important examples of such ADCs are reported in [13] and [91]. Both of these ADCs are SC based implementations. These architectures either digitize the signals at input frequencies or first down-convert them inside the ΣΔM loop to baseband before digitization. One of the important concerns associated with SC ΣΔM are the settling requirements. For input signals located in the GHz range, the required f_S become excessively large due to the OSR requirement for the desired resolution. Meeting the settling-time constraints in typical SC implementations with such higher sampling rates is nearly impractical [70].

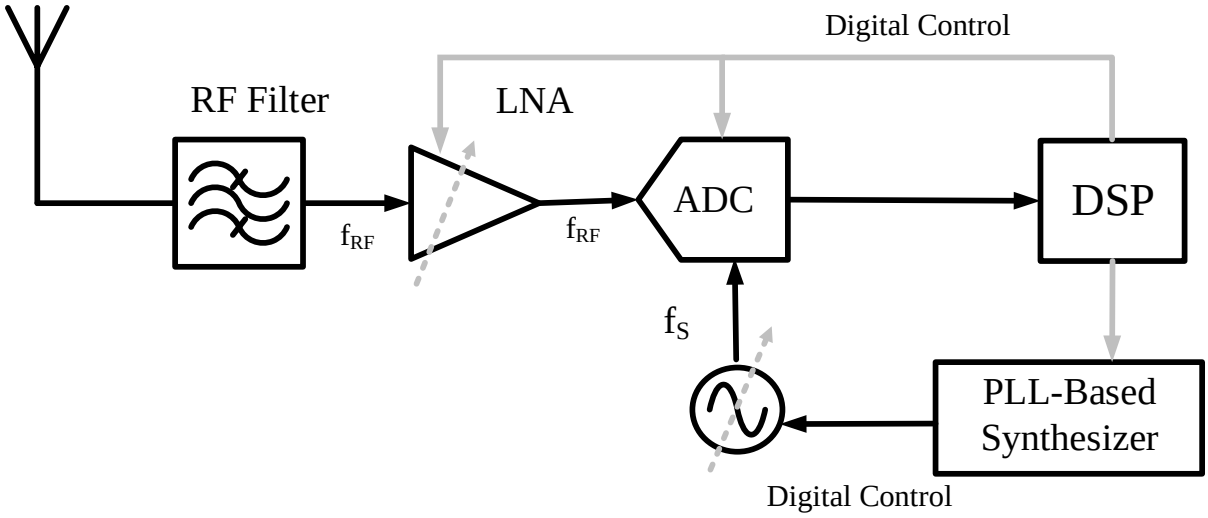


Figure 4.3. A modified version of SDR receiver based on tuneable notch BP ADC.

Contrary to this, the performance of CT ΣΔMs is not limited by settling accuracy as in CT implementations; the feedback waveform is integrated over time [70]. There are certain other advantages associated with the CT implementations as previously discussed in section 3.5. These include implicit anti-aliasing filtering, lower power consumption and absence of a front-end high speed S/H circuit, lower digital switching noise, reduced supply/ground noise and reduced sensitivity to glitches etc. All these benefits have made them a preferable option for the BP RF-to-digital converters [70].

Various CT ΣΔMs operating with GHz-sampling have been demonstrated in recent years. A brief summary of the different designs reported in literature is given in Table 4.1.

Table 4.1. CT ΣΔM ADC based architectures operating in GHz range.

	Order	**Technology**	**Carrier or Centre Freq.(GHz)**	**Clock Freq. (GHz)**	**Mode**	**BW (MHz)**	**Power (mW)**	**SNDR (dB)**
[12]	6	65nm CMOS	0-1	4	0-to-fs/4	35-150	550	69
[13]	4	40nm CMOS	2.22	8.88	fs/4	80	164	42
[14]	4	40nm CMOS	0.12	0.48	fs/4	50	7.6	63
[16]	2	0.13µm CMOS	0.8-2	2.6-3.4	Tuning range of 1.2 GHz	1	41	40-50
[40]	4	40nm CMOS	2.44	6.1	fs/4	80	52.8	41
[77]	4	0.5µm SiGE	1	4	fs/4	20	450	37
[78]	4	0.25µm SiGe	0.95	3.8	fs/4	1	75	59
[79]	4	0.13µm SiGe	2	40	fs/20	120	1600	50
[87]	6	90nm CMOS	2.4	3	4fs/5	60	40	40
* [92]	4	40nm CMOS	1	4	fs/4	100	312	58.5
[94]	4	0.25um SiGe	2.1-2.2	5	Tuning range of 0.1 GHZ	10	330	46.6
[95]	4	65nm CMOS	0.26	1.04	fs/4	10	123.7	63.3
[96]	6	65nm CMOS	0.18-0.22	0.8	Tuning range of 0.04 GHZ	25	35/36	69
[97]	2	0.13µm CMOS	2.442	3.256	3fs/4	25	26	34
[98]	6	40nm CMOS	0.7-0.8	3.2	fs/4	20	20	70
[99]	4	0.13µm CMOS	2.2-2.5	2.9-3.3	Tuning range of 0.1 GHZ	25	19	43

* Power consumption given in table for this architecture is for the whole receiver chain i.e. ADC + digital down-conversion + digital beam forming

An important example is [13], which can digitize the signals located at 2.22 GHz while operating at an f_S of 8.88 GHz. One notable implementation is reported in [87], that employs sub-sampling technique to enable the ADC to digitize the signals located at 2.4 GHz with f_S of 3 GHz. Architecture reported in [94] is another interesting implementation. It is a tuneable 4^{th}-order CT ΣΔM designed in 0.25-μm SiGe BiCMOS technology that employs an f_S of 3 GHz, while the f_N can be tuned over the range of 2.1-to-2.2 GHz. Two other examples are [95] and [96] which are 4^{th} and 6^{th} order modulators, respectively. These ADCs operate at f_S of 1.04 and 0.8 GHz while digitizing the signals located at 0.26 and 0.18-to-0.22 GHz, respectively. [97] and [98] are two other important examples operating at f_S of 3.256 and 3.2 GHz, respectively while digitizing the signals located at 2.442 and 0.7-to-0.8 GHz. Both of these ADCs employ LC BP filters. The most recent example is [99] that also employ LC BP filters. While employing a sampling rate of 2.9-to-3.3 GHz, this ADC can digitize the signals located over the range of 2.4-to-2.5 GHz.

Most of the state-of-art BP-ΣΔMs (as described in Table 4.1) operate in the GHz range and employ a fixed centre (or notch or f_N). The applied input RF signals need to be placed within the passband of the modulator for the proper digitization. Considering the SDR receiver architecture from Figure 4.3, in order to digitize the complete RF spectrum, a tuneable phase locked loop (PLL) synthesiser would be required to operate over a larger range of frequencies. Moreover, variable output data rates complicate the interface of the modulator and DSP.

Another solution to this issue is to use the reconfigurable BP CT-ΣΔMs with tuneable f_N that can reduce the need of widely tuneable PLL. However, very few BP CT-ΣΔMs with tuneable f_N have been proposed until now. One such implementation is reported in [12]. It is a sixth order modulator that operates at 2-to-4 GHz with the tuning range of DC-to-1 GHz. Another important example [16] proposed an architecture with a tuneable range of 0.8-to-2 GHz.

One of the critical considerations of such CT BP-ΣΔMs is the implementation of the loop filters. Most of the reported modulators (targeting SDR applications) have been implemented with LC resonators. These resonators show better performance in terms of power, linearity and speed compared to G_m-RC or G_m-C resonators at higher frequencies [100]. However, the major limitation of LC resonator-based modulators is that only one feedback loop is supplied to a simple LC filter. It does not give the proper loop impulse response to realise the required notch NTF with full control over tuning of feedback coefficients which are required for a tuneable f_N [77]. The LC resonator has a second-order TF while it has only one internal node in the modulator. As a result, CT-to-DT equivalence becomes impossible due to the loss of parity between the order of the loop filter and the number of internal nodes. One approach to overcome this problem has been reported in [77]. It is an LC BP-ΣΔM that employs two types of feedback waveforms (RZ DAC and HRZ DAC), which provides enough degrees of freedom for the CT-to-DT equivalence [77]. Another important technique (known as FIR technique) employs multiple paths with non-return-to-zero (NRZ) DAC and different fractional clock delays [101] [102].

This above analysis indicates that BP ADCs required in the SDR receiver architecture of Figure 4.3 can be realised with CT BP-ΣΔMs. These BP-ΣΔMs need to have a wide tuning of f_N and can be implemented with LC resonators due to their better performance at higher sampling rates. In the following sections, firstly the specifications of such BP-ΣΔM ADC are derived. Following that a design methodology for the synthesis of widely tuneable LC resonator-based BP CT-ΣΔMs architecture is presented.

4.4 Modulator Specifications

The conceptual block diagram of the SDR receiver, shown in Figure 4.3, has been used for the derivation of specifications for the targeted CT BP-ΣΔM. In this architecture, the input

signal, after being filtered and pre-amplified by the LNA, is digitized by a CT BP-ΣΔM and the subsequent signal processing is carried out by a DSP in digital domain. The focus of this section is to derive a meaningful set of specifications for the ADC to ensure that the input signal can be appropriately digitized.

For the successful digitization of a signal, it should be able to work properly over the whole DR of input while satisfying the minimum NF and linearity requirements. The required SNR for the ADC depends on two important factors namely, the *noise floor* and the *signal power*. The fundamental noise floor is due to the atmospheric noise received by the antenna and is given by [41]:

$$\mathrm{PSD} = 10\log\left[\frac{\mathrm{B.T}}{0.001}\right] \cong -174\,\mathrm{dBs}\,. \tag{4.1}$$

Where B is the Boltzmann's constant ($1.38\text{x}10^{-23}$ J/K) and T is the temperature in Kelvin. For the incoming signal having a bandwidth of BW, the rms noise power can be written as [41]:

$$\mathrm{PSD\_noise} = -174\ \ \mathrm{dBs} + 10\log 10(\mathrm{BW}) \tag{4.2}$$

The LNA and the filter (as shown in Figure 4.3), also introduce some noise in the signal path. If the total noise figure from the antenna to the ADC input is NF (dB), then the total noise at the ADC input is increased by NF (dB). Hence, the required SNR of ADC can be written as:

$$\mathrm{SNR} = \mathrm{P_C} - \left[\mathrm{PSD_{noise}} + 10\log(\mathrm{BW}) + \mathrm{NF} + \mathrm{LNA_{GAIN}}\right]. \tag{4.3}$$

Where $\mathrm{P_C}$ is the maximum input power (i.e. blocker) after attenuation due to the off-chip filters, BW is the bandwidth of desired band that needs to be converted, NF is the noise figure up to input of ADC (including LNA and filter) and $\mathrm{LNA_{GAIN}}$ is the gain of the LNA.

In order to derive the required specifications of the ΣΔM ADC, different wireless standards considered are GSM, EDGE, GPRS, CMDA-2000, WCDMA, WLAN (IEEE 802.11a/b/n), WiMAX and LTE. For the whole range of wireless standards, the ADC specification derivation is quite complicated and involves multiple trade-offs between LNA_{GAIN}, input signal level, maximum blocker level, NF etc. The LNA_{GAIN} for most of the wireless receivers is between 15-to-20 dBs [103]-[105]. Furthermore, in modern wireless receivers due to the lower quality factor (Q) of the on-chip BP filters, out-of-band blockers are typically attenuated by off-chip SAW filters prior to LNA [104]. Therefore, by employing the expression of required SNR of ADC from equation (4.3), while considering an LNA_{GAIN} of 15dB, on/off chip of 15 dB blocker attenuation, a NF of 3 dB and taking a number published works ([5][12]-[19][28][39][40][64][65][67][71][77]-[80][106][107]) into account, Table 4.2 has been derived. This table serves as a reference for the achievable performance of the proposed architecture.

Table 4.2. Resolution requirements for different wireless communication standards.

Standard	**Carrier Frequency (MHz)**	**Bandwidth (MHz)**	**SNR (dBs)**
GSM	850-1900	0.2	90
EDGE	850-1900	0.2	90
GPRS	850-1900	0.2	90
CDMA	450-2100	1.25	65
IEEE 802.11a	5000	20	50
IEEE 802.11b	2400	5.5	50
IEEE 802.11n	2400/5000	20/40	50
LTE	700-3500	5/10/20/40/100	70-75

4.5 Sub-sampling

In order to handle all the standards mentioned in Table 4.2 , the ADC is required to digitize the signals with carrier frequencies ranging from 0.455 GHz (CDMA-2000) to 5.093 GHz (WiMAX) with channel bandwidths varying from 0.2 MHz (GSM) to 30 MHz (LTE).

The sampling rates in conventional BP-ΣΔMs are typically four times of the input frequency (or f_N), which simplifies the subsequent down conversion in the digital domain [50]. When such ADCs are used for input signals located in the GHz range, the sampling rates become prohibitively high. As an example, considering the WiMAX standard with a signal band located at 5.093 GHz would require a sampling rate of 20.372 GHz. Such higher sampling rates pose several design related issues. First, the specifications of the different building blocks of the ADC increase directly with the sampling rates [28][77]. Moreover, the performance of the CT BP-ΣΔM ADCs is very sensitive to the clock jitter in the feedback path [70]. Realising the clock generation circuit with such higher sampling rates with lower jitter is difficult and challenging [108]. The power of the DSP following the ADC is also directly proportional to the operating frequency.

Sub-sampling is an efficient way to overcome the challenge of operating at higher sampling rates. In these architectures, the input signal located at a certain high frequency is sampled with the sampling rates lower than the Nyquist-rate [109]. The bandwidth of the signal of interest is usually much lower than the sampling rates. The resultant signal bandwidth is still oversampled thereby avoiding aliasing between replicas. An ideal S/H block operating at a sampling frequency of f_S generates aliases of input and image signal. Assume the input of the S/H block is an RF signal located at a frequency, f_{RF}, such that f_{RF} is much higher than f_S. At the output of the S/H, aliases of the input signal are located at $mf_S + f_{RF}$ where “m” is an integer

number, as depicted in Figure 4.4. Furthermore, aliases of the image signal exist at (m + 1) f_S – f_{RF}. The alias of the original signal or the image signal located within the range 0-to- $f_S/2$ can be used to extract the original RF signal [87] [97].

The same concept can be extended to the BP-ΣΔM ADCs. If an RF signal is passed through a sub-sampled ΣΔM, one alias of the signal exists at a lower frequency f_N, within range 0-to- fs/2 and that can be calculated as [110]

$$f_N = \begin{cases} \text{rem}\ (f_{RF}, f_S), & \text{if} \left\lfloor \dfrac{f_{RF}}{0.5 f_S} \right\rfloor = \text{even} \\ f_S - \text{rem}\ (f_{RF}, f_S), & \text{if} \left\lfloor \dfrac{f_{RF}}{0.5 f_S} \right\rfloor = \text{odd} \end{cases} \tag{4.4}$$

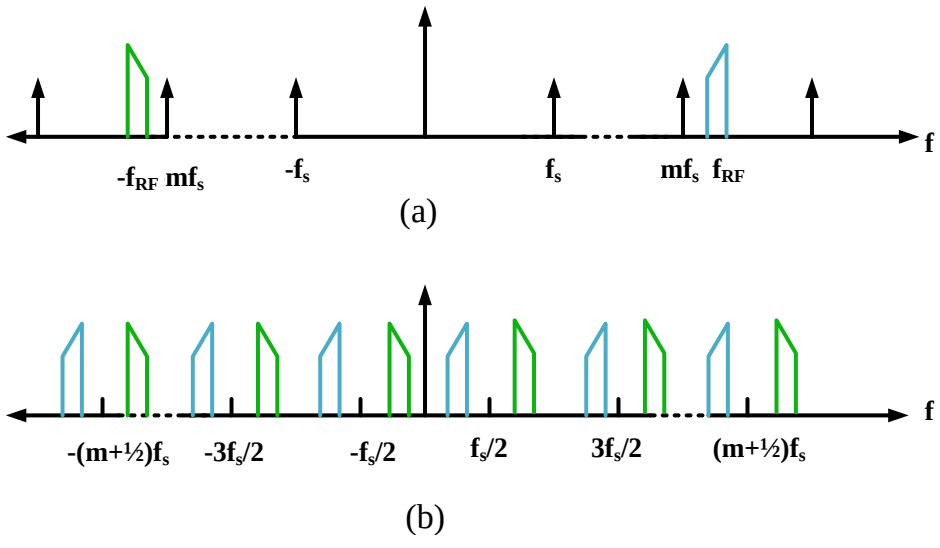


Figure 4.4. (a) Input signal at frequency f_{RF} to an ideal S/H operating at f_S (b) Output of the S/H showing the replicas of the original and image signal.

Where, rem(x, y) stands for the remainder of x and y. Equation (4.4) can be employed to realise a sub-sampled BP-ΣΔM ADC. For a given standard, if f_S and f_{RF} are selected in a way that f_N is equal to the centre frequency of BP-ΣΔM, one replica of the input (RF) signal can be extracted with the noise shaped at f_N. As an example, assume a BP-ΣΔM ADC is operating at a sampling frequency of f_S, with a passband centre frequency of $f_S/5$. Assume an incoming signal located at frequency of $4/5f_S$, is input to the ADC. Therefore, using equation (4.4):

$$\left\lfloor \frac{f_{RF}}{0.5f_S} \right\rfloor = 1 = \text{odd}.$$

Therefore: $$f_N = f_S - \text{rem}\ (f_{RF}, f_S) = f_S/5.$$

Hence, as depicted in Figure 4.5, the output spectrum of the ΣΔM ADC has one digitized alias of the input signal with quantisation noise shaped at $f_S/5$. This alias is considered as the output signal of interest and can be applied to the DSP for the further signal processing (such as downconversion, filtering, channel selection etc.).

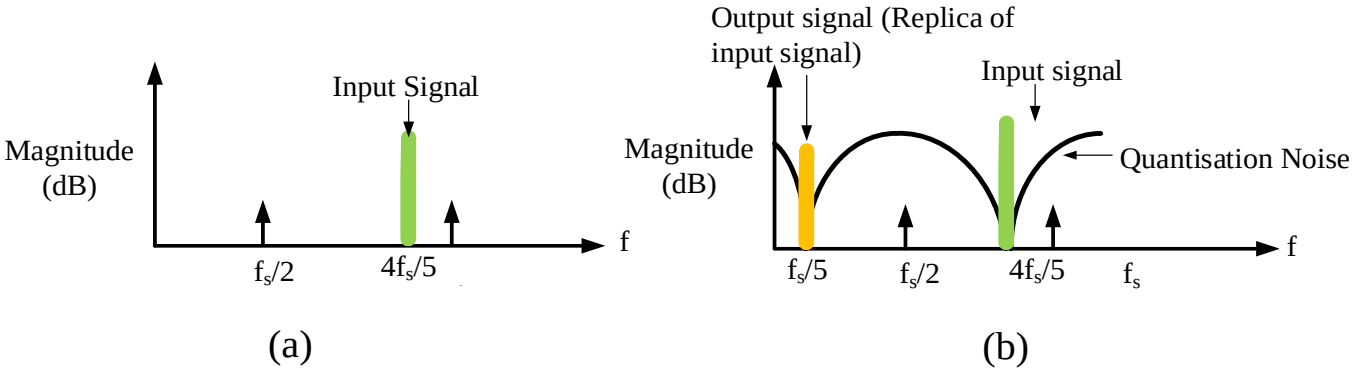


Figure 4.5. (a) Input of BP-ΣΔM ADC with a centre frequency of 4/5 f_S (b) Output spectrum of BP-ΣΔM ADC with quantisation noise shaping at $f_S/5$ [111].

For a sub-sampled ΣΔM ADC, to down-convert an RF signal without overlapping, three conditions need to be fulfilled:

- $f_S > 2BW$ (Nyquist theorem),
- $f_N - BW/2 > 0$,
- $f_N < f_S - BW/2$.

As an example, consider the GSM/EDGE_850 standard that has a carrier frequency of 881.5 MHz and the BW of the signal of interest is 25 MHz. Using (4.4), a sub-sampled ΣΔM ADC centred at 118.5 MHz, operating at f_S of 1 GHz sampling rate, can be used to digitize the input signal.

4.5.1 Raised Cosine DAC

Two important limitations associated with the sub-sampled BP-ΣΔM ADC are attenuation of the feedback signal (i.e. output of feedback DAC in ΣΔM loop) and jitter in the feedback DAC waveform.

In the ΣΔM loop, input signal is largely attenuated by feedback DAC. Figure 4.6 shows the frequency response of the different rectangular shaped DACs ([16][116]). The DACs i.e. NRZ, RZ and HRZ behave as LP filters. Therefore, the signal located at f_{RF} being fed back is attenuated and as a result of that the SNR of the modulator is degraded. In order to overcome this issue, the bandwidth of the feedback DAC needs to be increased. One approach to alleviate this issue was proposed in [112] and [113]. With the zero insertion at the output of the quantiser, the bandwidth of the feedback signal is increased and hence feedback signal degradation can be reduced. Employing sine-shaped DACs, e.g. raised-cosine DAC, strength of feedback signals can also be increased [114] [115]. Figure 4.7 illustrates the time domain plot of a raised-cosine DAC.

The frequency response of different shaped DACs (shown in Figure 4.6) depicts that raised-cosine DACs have better magnitude response at frequencies larger than f_S compared to NRZ and RZ DACs. Another important advantage of the raised-cosine DAC is associated with the timing jitter as shown in Figure 4.8 (a) and (b) [16]. Rectangular shaped DACs i.e. (NRZ, RZ and HRZ) are more sensitive to feedback pulse jitter at the rising and falling edges of the feedback as the slope of the pulse is maximum at those instants [70].

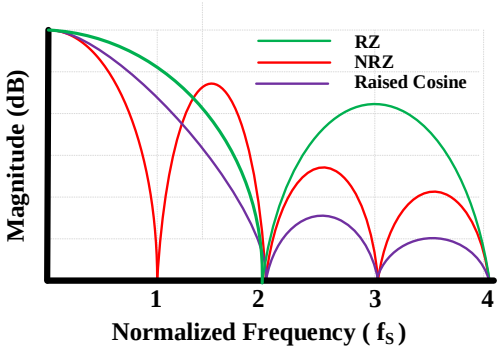


Figure 4.6. Frequency response of NRZ, RZ and raised-cosine DACs.

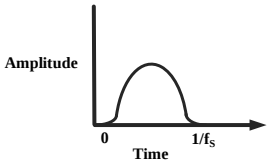


Figure 4.7. Graphical illustration of a sine-shaped DAC (Raised cosine DAC).

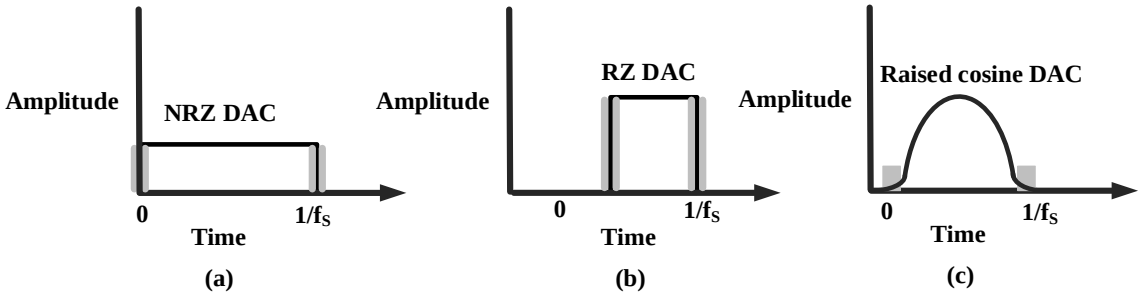


Figure 4.8. Illustration of timing jitter on 3 types of DACs (a) NRZ DAC (b) RZ DAC and (c) Raised cosine DAC.

In the raised-cosine DACs, the sinusoidal pulse and the sampling clock are aligned therefore, the DAC gets switched during sampling instant of the sinusoidal pulse. Hence, the slope of the feedback pulse is zero at this instant, making it less sensitive to the timing jitter as depicted in Figure 4.8 (c). Another important advantage associated with these DACs is the removal of inter-symbol interference (ISI) [16][70]. Due to these reasons raised-cosine DACs are a preferred option in higher sampling rates sub-sampled CT BP-ΣΔM ADCs [16] [97][117].

4.5.2 Sampling Frequency Selection

In order to determine the f_S for a sub-sampled BP-ΣΔM ADC in a SDR receiver, as shown in Figure 4.3, a number of wireless standards (GSM, EDGE, GPRS, CMDA-2000, WCDMA, Bluetooth, WLAN (IEEE 802.11a/b/n), WiMAX and LTE) have been considered. Handling of all these operating modes in the ADC requires that the signals are digitized with carrier frequencies ranging from 0.455 to 5.093 GHz and with channel bandwidths varying from 0.2-to-30 MHz. As mentioned in section 4.3, the sampling rates in conventional BP-ΣΔMs are typically four times the input (or notch) frequency. Therefore, for higher input frequencies, sub-sampling can be employed. Using the relation given in equation (4.4) and taking the three basic conditions of sub-sampling ($f_S > 2BW$ (Nyquist theorem), $f_N - BW/2 > 0$ and $f_N < f_S - BW/2$) into account, f_S and f_N for the different wireless communication standards have been calculated and are summarised in Table 4.3. As a summary of this table, a CT BP-ΣΔM with f_N range of 0.04-to-0.2485f_S, capable of operating at f_S of 1-to-2 GHz, can ideally digitize the wider range of wireless standards.

Table 4.3. f_S selection for BP-ΣΔM ADC for different wireless communication standards (in normal and sub-sampled modes).

Standard	**f_{RF} (GHz)**	**f_S (GHz)**	**f_{IF} (or f_N) (GHz)**	**f_{IF} /f_S**	**BW of whole band (MHz)**	**BW of channel (MHz)**
GSM/ EDGE_850	0.8815	0.25	0.1185	0.474	25	0.2
		0.5	0.1185	0.237		
		1	0.1185	0.1185		
		4	0.8815	0.220375		
GSM/ EDGE_900	0.94	0.25	0.06	0.24		
		0.5	0.06	0.12		
		1	0.06	0.06		
		4	0.94	0.235		
GSM/ EDGE_1800	1.8425	0.5	0.1575	0.315	75	0.2
		1	0.1575	0.1575		
GSM/ EDGE_1900	1.96	0.25	0.04	0.16	60	0.2
		0.5	0.04	0.08		
		1	0.04	0.04		
UMTS	2.14	1	0.14	0.14	60	3.84
		2	1.86	0.93		
WIMAX (1.A, 1.B, 2.D, 2.E, 2.F)	2.35	0.5	0.075	0.15	100	3.5/5/8.75/10
		1.25	0.075	0.06		
		2.5	0.075	0.03		
		5	0.075	0.015		
WIMAX (10.A)	5.075	0.5	0.075	0.15	175	5/10
		1.25	0.075	0.06		
		2.5	0.075	0.03		
LTE-A	2.3	1	0.3	0.3	--	100
		2	0.3	0.15		
		1	0.3	0.3		

4.6 Proposed RF-to-Digital ΣΔM ADC Architecture

The block diagram of the proposed modulator is shown in Figure 4.9. It is a 4^{th}-order, CT BP-ΣΔM that consists of two LC resonators. To reduce the impact of the feedback signal attenuation and to increase the immunity to timing jitter, a raised-cosine feedback has been used. Owing to their better performance at higher frequencies, the modulator employs two LC resonators. As explained earlier, the LC resonator has a second-order TF, but it has only one internal node and hence making CT-to-DT equivalence impossible due to the loss of parity. Previous LC BP ΣΔM implementations overcame this problem by using a combination of two

differently shaped DACs or multi-feedback FIR-DACs [77][102]. In the proposed modulator, half-delayed FIR based raised-cosine DACs have been used.

Two additional feedback paths, with gains of c_0 and c_1, are included to compensate for the ELD. The latch driving the first compensation path, i.e. the path with gain c_0, has the opposite phase to the clock signals driving the quantiser and the other feedback paths. The second compensation path is introduced with a full sampling-period delay. In this way, the modulator exhibits a full digital delay between the quantiser output and all inputs of DAC thus allowing half a clock cycle for quantiser operation. Furthermore, a minimum of one complete delay exists between the modulator outputs and the input of the quantiser through both compensation paths. This gives a full sampling-period delay margin for the quantiser and DAC operation.

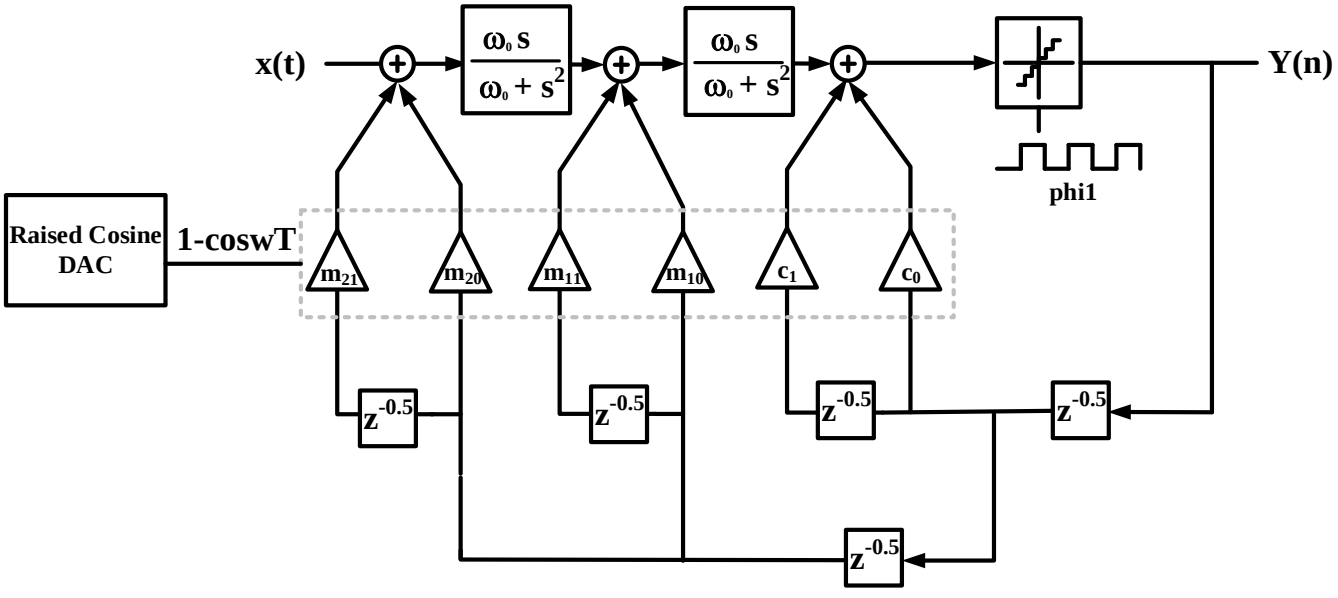


Figure 4.9. A 4th-order CT BP-ΣΔM ADC.

Compared to previous approaches based on raised-cosine FIR feedback DACs [102] , this architecture uses a two-tap FIR structure instead of a three-tap. Therefore, the total number of feedback paths required is 6 (which is much smaller than 16 reported in [102]). This reduction in the number of the loop-filter coefficients improves the coefficient mismatch performance. The mismatches are particularly critical in SDR applications, since a high degree of configurability in coefficients is required to support widely programmable notches.

4.7 Design Methodology for CT BP-ΣΔM with Reconfigurable f_N (0-to-0.25 f_S)

Three steps of the proposed design methodology steps for the system level design of the CT BP-ΣΔM ADC consisting of 2 LC resonators, targeting the RF-digitization are given in the follows:

1. The calculation of the feedback and the feedforward coefficients of the 4^{th}-order CT BP-ΣΔM ADC, which consists of two LC resonators, depicted in Figure 4.9, for range of notch frequencies (ranging from 0-to-0.25 f_S) [88].
2. By using the sub-sampling technique, signals located at frequencies higher than $0.5f_S$ can be translated to the lower notch frequencies and subsequently converted. If f_S is selected in such a way that RF signals lie within the range $0.75f_S$ -to-f_S , $1.75f_S$-to-$2f_S$, $2.75f_S$-to-$3f_S$, $3.75f_S$-to-$4f_S$, $4.75f_S$-to-$5f_S$, etc. then a replica of these signals is translated to frequency range of 0-to-$0.25f_S$. Other replicas are located at 1-to-$1.25f_S$, 2-to-$2.25f_S$ and so on.
3. Using the coefficients derived in step 1, RF signals located at much higher frequencies can be successfully digitized.

The design flow adopted for the modulator with a reconfigurable f_N (ranging from 0-to-0.25f_S) is as follows:

Step 1: The NTF of a 4th-order BP DT-ΣΔM for the different notches is calculated.

Step 2: Using a modified-Z transform technique, the coefficients of the continuous time LC BP-ΣΔM (equivalent to first step DT BP-ΣΔM ADC) are calculated.

Step 3: Using these coefficients, an ideal system level model is simulated and then the output is processed, in Matlab® [119].

Three steps of the above-mentioned methodology are elaborated for the case of an f_N = 0.2f_S in the following. The same methodology can also be used for the derivation of the coefficients for other notches as well.

1. NTF for a 4th-order BP-DTΣΔM

By replacing a LP filter in the ΣΔM ADC with a BP filter, noise suppression can be obtained at the resonance frequency of the filter. A discrete time low-pass TF can be transformed into a band-pass TF with lower and upper cut-off frequencies, ω_{c1} and ω_{c2}, respectively using following expression [66]:

$$z^{-1} \rightarrow \frac{-z^{-2} + \frac{2k\alpha}{k+1} z^{-1} \frac{k-1}{k+1}}{\frac{k-1}{k+1} z^{-2} - \frac{2k\alpha}{k+1} z^{-1} + 1}. \tag{4.5}$$

where “α" and “k” are passband scaling parameters and given respectively by:

$$\alpha = \frac{\cos\left(\frac{\omega_{C2} + \omega_{C1}}{2}\right)}{\cos\left(\frac{\omega_{C2} - \omega_{C1}}{2}\right)}, \tag{4.6}$$

and $$k = \cot\left(\frac{\omega_{C2} - \omega_{C1}}{2}\right)\tan\left(\frac{\Omega_C}{2}\right). \quad (4.7)$$

All the frequency variables (ω_{c1}, ω_{c2} and Ω_C) are normalised in such a way that 0 to $f_S/2$ maps to 0 to π.

Now, consider the case where the resonant frequency is $\omega_{o,}$ such that $\omega_{c1} = \omega_o - \Delta$ and $\omega_{c2} = \omega_o + \Delta$. If Δ is chosen to be zero then $\omega_{C2} = \omega_{C1}$. Using this in (4.6) and (4.7), the resultant "α" and "k" become $\cos(\omega_0)$ and 0, respectively. Employing these values of α and k in (4.5), we obtain the following transformation:

$$z^{-1} \rightarrow \frac{z^{-2} + (\cos\omega_0)z^{-1}}{(\cos\omega_0)z^{-1} + 1}. \quad (4.8)$$

Using this transformation, any low-pass NTF can be converted to the equivalent BP NTF, with the desired zeroes at any frequency between 0 and $f_S/4$, while maintaining the stability and causality criteria of the original NTF.

Once the NTF is decided, the loop TF can be calculated as:

$$H(z) = 1 - \frac{1}{NTF} \quad (4.9)$$

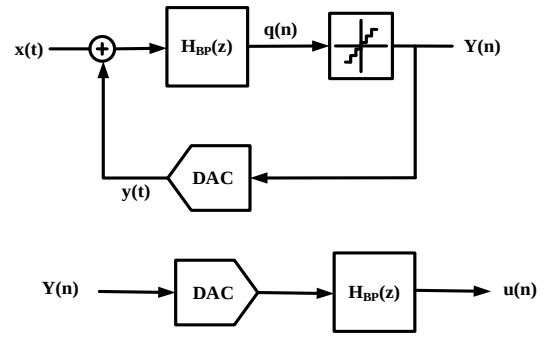
As an example, for an f_N of $0.2f_S$ (as pointed out earlier in this section) $H_{BP}(z)$ can be represented as:

$$H_{BP}(z) = \frac{-0.55z^{-4} - 0.55z^{-3} - 0.9z^{-2} - 0.25z^{-1}}{(z^{-2} + 0.618z^{-1} + 1)^{-2}}. \quad (4.10)$$

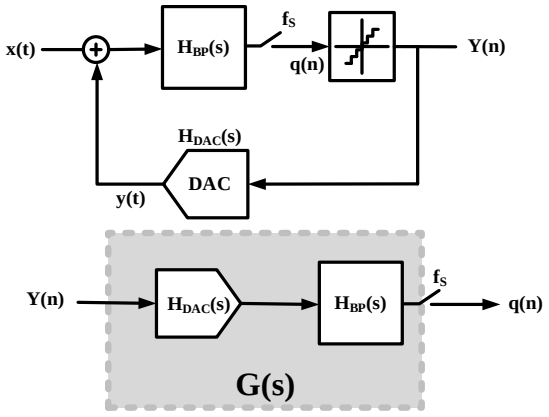
2. Modified-Z Transform Technique for CT-DT Transformation

In order to realise a DT NTF using a 4th-order LC resonator based CT BP-ΣΔM, as shown in Figure 4.9, a CT-to-DT transformation is required. These two modulators are equivalent if, for a given input waveform, the input to the quantiser at the sampling instants are equal as depicted in Figure 4.10 (a) and (b) [70]. It can be represented as [16]:

$$L^{-1}(G(s)) = Z^{-1}(H(z))\Big|_{t=nT_s}. \tag{4.11}$$



(a)



(b)

Figure 4.10. Loop filter in ΣΔM for (a) DT implementation (b) CT implementation.

Here G(s) is the loop TF of the CT BP-ΣΔM ADC from the output of quantiser to its input and is given by:

$$G(s) = H_{BP}(s).H_{DAC}(s). \tag{4.12}$$

Where, $H_{BP}(s)$ and $H_{DAC}(s)$ are the loop and DAC TFs, respectively. The TF of a raised-cosine DAC operating at a frequency ω_{DAC} is given as follows:

$$h_{DAC}(t) = [u(t) - u(t-1)][1 - \cos(\omega_{DAC} t)]. \tag{4.13}$$

Where u(t) is the unit step function.

In S-domain the same can represented as follows:

$$H_{DAC}(s) = \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} \quad . \tag{4.14}$$

The TF of the LC resonator having a resonant frequency ω_0, is given as follows:

$$H_{LC}(s) = \frac{\omega_0^2}{(\omega_0^2 + s^2)} \quad . \tag{4.15}$$

The continuous time BP-ΣΔM ADC considered here is a 4th-order modulator (as shown in Figure 4.9), with 6 feedback paths (with feedback coefficients m_{21}, m_{20}, m_{21}, m_{11}, m_{10}, c_{11}, c_{10}, respectively). Therefore, the overall loop TF i.e. G(s) can be written as:

$$G(s) = \left[\begin{array}{c} m_{21} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} \left(\frac{\omega_0^2}{(\omega_0^2 + s^2)} \right)^2 e^{(-1.5T)s} + m_{20} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} \left(\frac{\omega_0^2}{(\omega_0^2 + s^2)} \right)^2 e^{(-0.5T)s} + \\ m_{11} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} \left(\frac{\omega_0^2}{(\omega_0^2 + s^2)} \right)^2 e^{(-T)s} + m_{10} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} \left(\frac{\omega_0^2}{(\omega_0^2 + s^2)} \right)^2 e^{(-0.5T)s} + \\ c_{11} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} e^{(-T)s} + c_{10} \frac{\omega_{DAC}^2}{s(\omega_{DAC}^2 + s^2)} e^{(-0.5T)s} \end{array} \right] \tag{4.16}$$

In order to make this LC-based CT BP-ΣΔM work equivalent with the corresponding DT BP-ΣΔM, the condition mentioned in (4.11) needs to be fulfilled, i.e.,

$$Z\left[L^{-1}(G(s))\right] = H(z)\,. \tag{4.17}$$

For a 4th-order BP modulator with a notch frequency of $0.2f_S$ (based upon the example mentioned at the start of this section), we have the following relationship:

$$H_{BP}(z) = \frac{-0.55z^{-4} - 0.55z^{-3} - 0.9z^{-2} - 0.25z^{-1}}{\left(z^{-2} + 0.618z^{-1} + 1\right)^{-2}} \tag{4.18}$$

Therefore:

$$Z\left(L^{-1}(G(s))\right) = \frac{-0.55z^{-4} - 0.55z^{-3} - 0.9z^{-2} + -0.25z^{-1}}{\left(z^{-2} + 0.618z^{-1} + 1\right)^{-2}} \tag{4.19}$$

For CT-to-DT transformation of this architecture, the modified Z-transform technique is used. The FIR-based DACs used here have half delays. The modified Z-transform is a promising technique to calculate the Z transform of a CT system with delays which are not integral multiples of sampling time [102]. The modified Z-transform of a function A(s) can be represented as:

$$Z_m\left[A(s)\right] = \sum_{\text{pi poles of } A(s)} \text{Residue of}\left(\frac{A(s)\,e^{-mTs}}{(z - e^{-mTs})}\right). \tag{4.20}$$

Using the modified Z-transform, the Z-transforms of all feedback paths of CT BP-ΣΔM (i.e. m_{21}, m_{20}, m_{11}, m_{10}, c_{10}, c_{11}) are calculated and their sum is equated with the corresponding DT loop TF. The Z-transform of all the feedback paths is represented in partial fraction form. As an example, the transfer functions of paths with two and one resonator have the partial fraction form of:

$$TF_{2\_Resonator} = \Sigma\left(\frac{a_1}{(\pi + z)^2} + \frac{a_1^*}{(\pi + z)^2} + \frac{a_2}{(\pi + z)} + \frac{a_2^*}{(\pi + z)} + \frac{b_1}{z^2} + \frac{b_2}{z}\right) \tag{4.21}$$

$$TF_{1\_Resonator} = \Sigma\left(\frac{c_1}{(\pi + z)^2} + \frac{c_1^*}{(\pi + z)^2} + \frac{b_1}{z^2} + \frac{b_2}{z}\right). \quad (4.22)$$

Equations (4.21) and (4.22) show that in addition to the fixed poles for a specific notch frequency, two additional terms i.e. $\frac{b_1}{z^2}$ and $\frac{b_2}{z^2}$ are also produced. Equations (4.23) to (4.26) show the partial fraction form of all the four paths for a $0.2f_S$ notch frequency are given by:

$$TF_{m20} = - \frac{(0.31+0.22i)}{(-0.309-0.95i+z)^2} - \frac{(0.31-0.22i)}{(-0.309-0.95i+z)^2} - \frac{(0.31+0.12i)}{(-0.309-0.95i+z)} - \frac{(0.31-0.12i)}{(-0.309-0.95i+z)} + \frac{0}{z^2} + \frac{0.65}{z} \quad (4.23)$$

$$TF_{m21} = - \frac{0.38}{(-0.309-0.95i+z)^2} - \frac{0.38}{(-0.309-0.95i+z)^2} - \frac{(0.39-0.27i)}{(-0.309+0.95i+z)} - \frac{(0.39-0.27i)}{(-0.309-0.95i+z)} + \frac{0.11}{z^2} + \frac{0.78}{z} \quad (4.24)$$

$$TF_{m10} = \frac{(0.49-0.35i)}{(-0.309-0.95i+z)} - \frac{(0.49+0.35i)}{(-0.309-0.95i+z)} - \frac{1}{z^2} + \frac{0}{z^2} \quad (4.25)$$

$$TF_{m11} = \frac{(0.18-0.58i)}{(-0.309-0.95i+z)} - \frac{(0.49+0.58i)}{(-0.309+0.95i+z)} - \frac{0.43}{z^2} - \frac{0.61}{z^2} \quad . \quad (4.26)$$

The two additional paths in front of the quantiser, shown in Figure 4.9, were introduced with delays of $0.5T_s$ and $1.5T_s$ for the ELD compensation. The output samples from the quantiser are shaped by the raised-cosine DAC while passing through these paths. The Z-transform of a

raised-cosine DAC with half delay is given by $2z^{-1}$. Therefore, the TFs of compensation paths can be written as:

$$TF_{C0} = 2z^{-1} \quad , \quad TF_{C1} = 2z^{-2} . \tag{4.27}$$

As described previously, the DT loop TF having a notch at $0.2f_S$ is given by:

$$H_{BP}(z) = \frac{-0.55z^{-4} - 0.55z^{-3} - 0.9z^{-2} + -0.25z^{-1}}{\left(z^{-2} + 0.618z^{-1} + 1\right)^{-2}} . \tag{4.28}$$

Equations (4.23) to (4.26) show that the Z-transforms of the 4 paths (i.e. m_{21}, m_{20}, m_{11}, m_{m10}) are composed of two terms. The first of which involves the poles at $\pi/2.5$ (i.e. $0.2f_S$) and second of which includes z^{-1} and z^{-2}. In order to calculate the resonators feedback coefficients of the architecture, the terms with the poles located at $0.2f_S$ (i.e. -0.309-0.95i+z and -0.309+0.95i+z) are combined and equated with 4^{th}-order DT BP loop filter of (4.28).The terms involving z^{-1} and z^{-2} are combined and the equated with the compensation paths. The resulting coefficients for this notch frequency are:

$$m_{21} = 0.037,\ m_{20}=0.048,\ m_{11}=0.53,\ m_{10}=0.30,\ c_1=0.25,\ c_0=0.$$

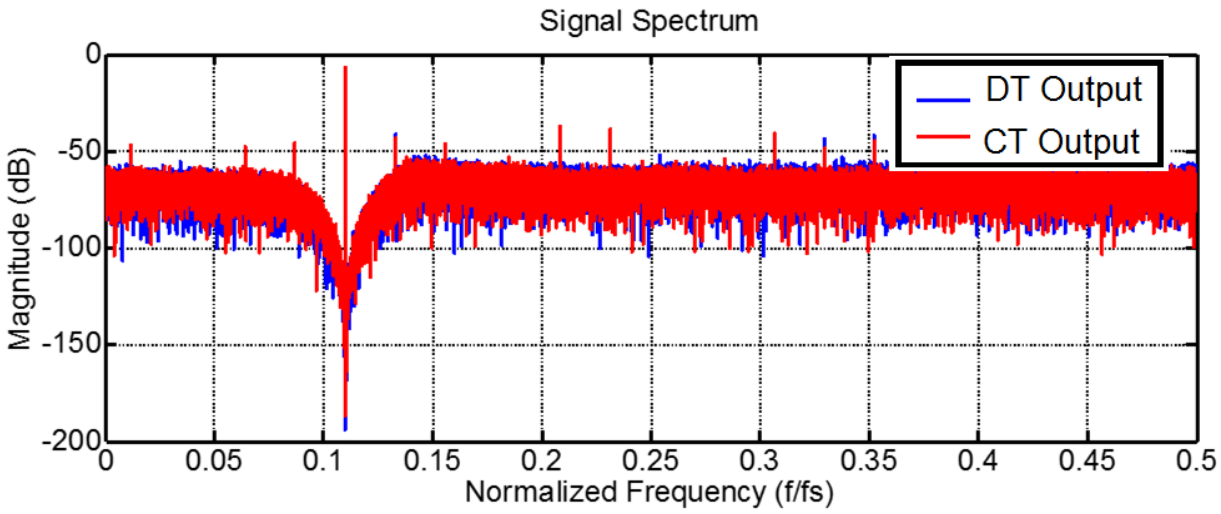
By employing the same methodology, the coefficients over a range of frequencies can be derived.

4.8 Simulation Results

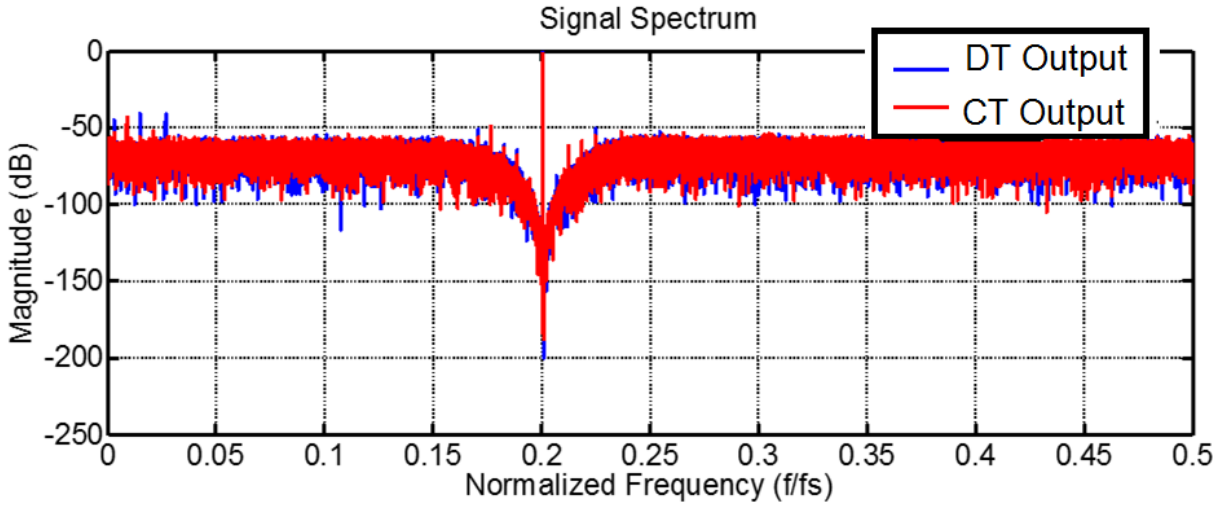
The aforementioned DT-to-CT transformation was applied to the different notch frequencies. Based upon this transformation, the feedback coefficients have been calculated. Figure 4.11 shows the spectrum plots of a 4^{th}-order DT and its equivalent CT modulator at the different notch frequencies, thus proving the validity of CT-to-DT transformation. Figure 4.11

(a) to (c) illustrate the output spectrum plots at three notch frequencies, namely $0.12f_S$, $0.2f_S$, and $0.25f_S$, respectively. Figure 4.12 (a) to (c) depicts the output spectrum plots for the three different cases while operating in normal and sub-sampling modes at the different values of input (f_{RF}) and sampling frequencies (f_S). Figure 4.12 (a) shows the spectrum of an input frequency of 0.44 GHz with a sampling rate of 2 GHz. Figure 4.12 (b) and (c) illustrate the spectrum plots of two sub-sampled cases for two input frequencies of 2.14 GHz and 5.2 GHz with sampling frequencies of 1 and 2.5 GHz , respectively. Figure 4.13 depicts SNR-versus-input level curves for these three cases proving the accuracy of the design methodology.

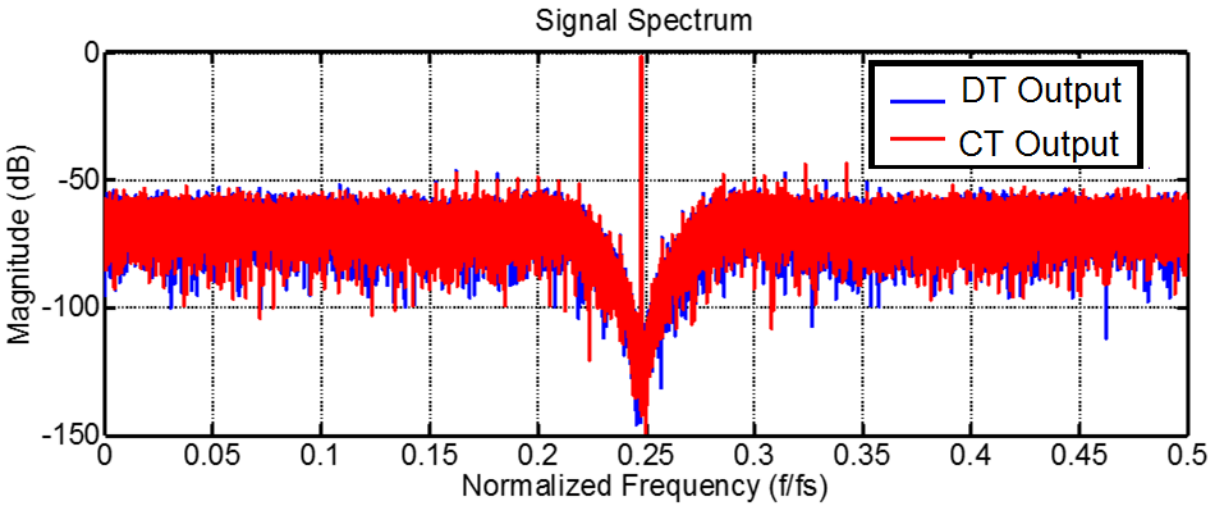
As stated in section 4.6, one of the benefits of the proposed architecture is the reduced number of coefficients, which directly translates to lower mismatch sensitivity and circuit-element tolerances. As an illustration of the robustness of the proposed modulator, Figure 4.14 shows the histogram of SNR of a 150-run Monte Carlo simulation. The variation in the achievable SNR is for the three different cases namely 0.44 GHz with a sampling rate of 2 GHz in normal mode, 2.14 GHz and 5.2 GHz in sub-sampling mode with sampling frequencies of 1 and 2.5 GHz, respectively). A standard deviation of 10% was considered in all the loop-filter coefficients. The resultant maximum deviation of the SNR is within ±5 dBs. Table 4.4 shows the achievable performance for the different input and sampling frequencies.


Signal Spectrum
DT Output
CT Output
Magnitude (dB)
0
-50
-100
-150
-200
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Normalized Frequency (f/fs)

(a)

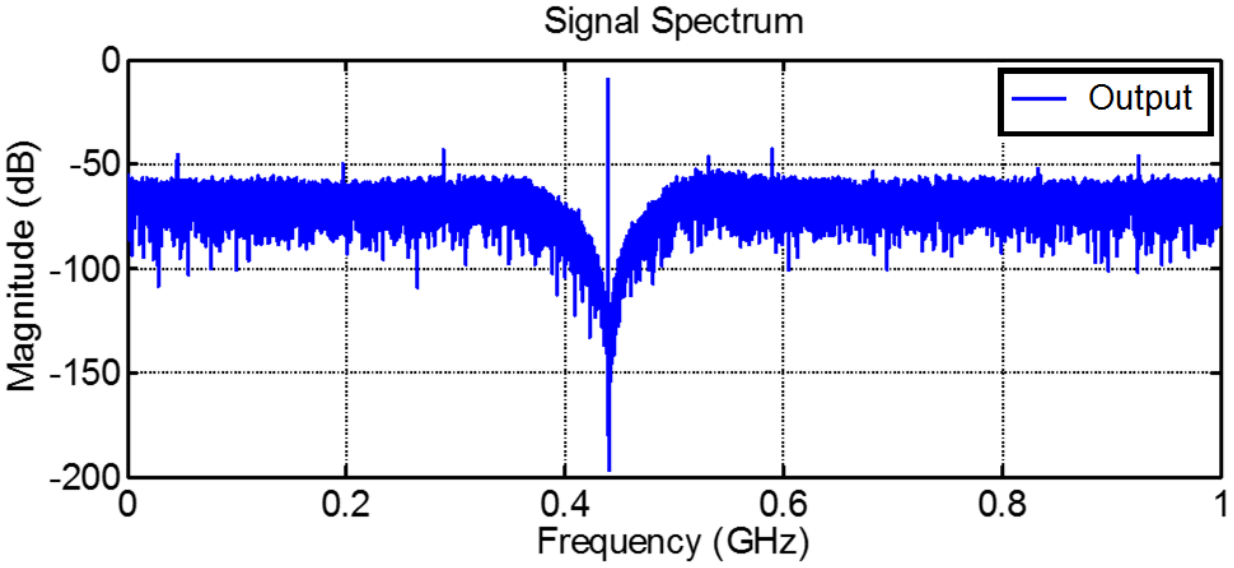

Signal Spectrum
DT Output
CT Output
Magnitude (dB)
0
-50
-100
-150
-200
-250
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Normalized Frequency (f/fs)

(b)

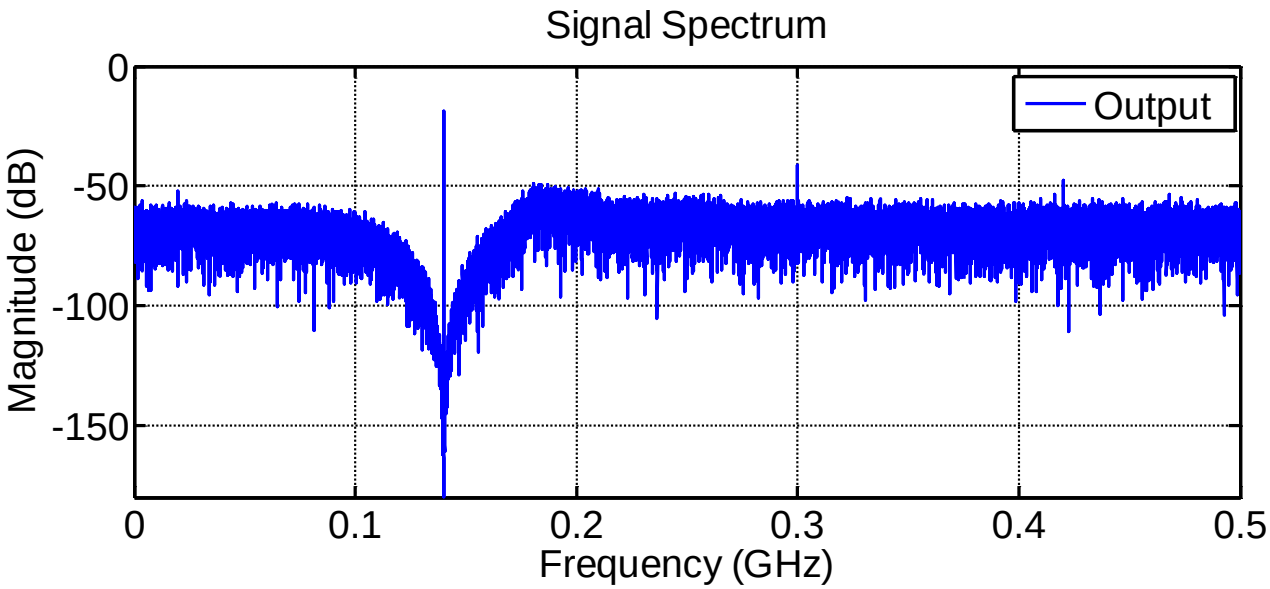


(c)

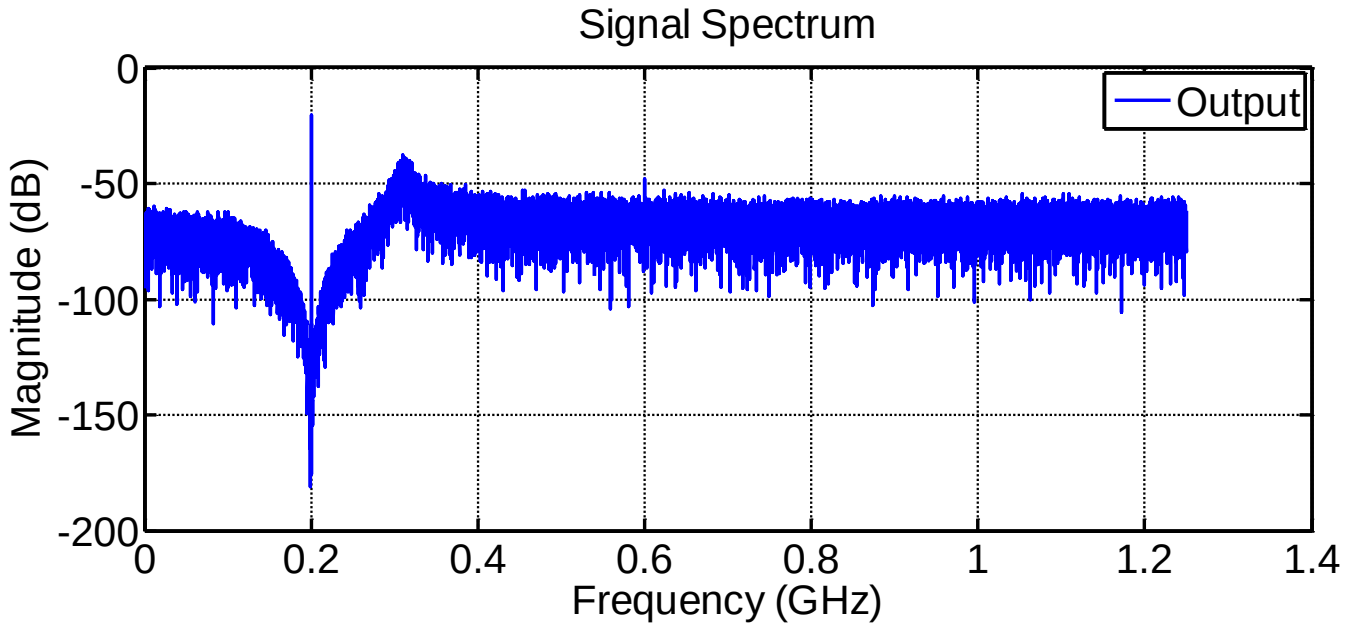
Figure 4.11. CT-to-DT transformation at three different notch frequencies (a) $0.12f_S$ (b) $0.2f_S$ (c) $0.25f_S$.



(a)



(b)



(c)

Figure 4.12. Modulator output spectra for the different cases of f_{RF} and f_S (a) f_{RF} = 0.44 GHz, f_S = 2 GHz (normal mode) (b) f_{RF} = 2.14GHz, f_S = 1 GHz (sub-sampling mode) and (c) f_{RF} = 5.2 GHz, f_S = 2.5 GHz (sub-sampling mode).

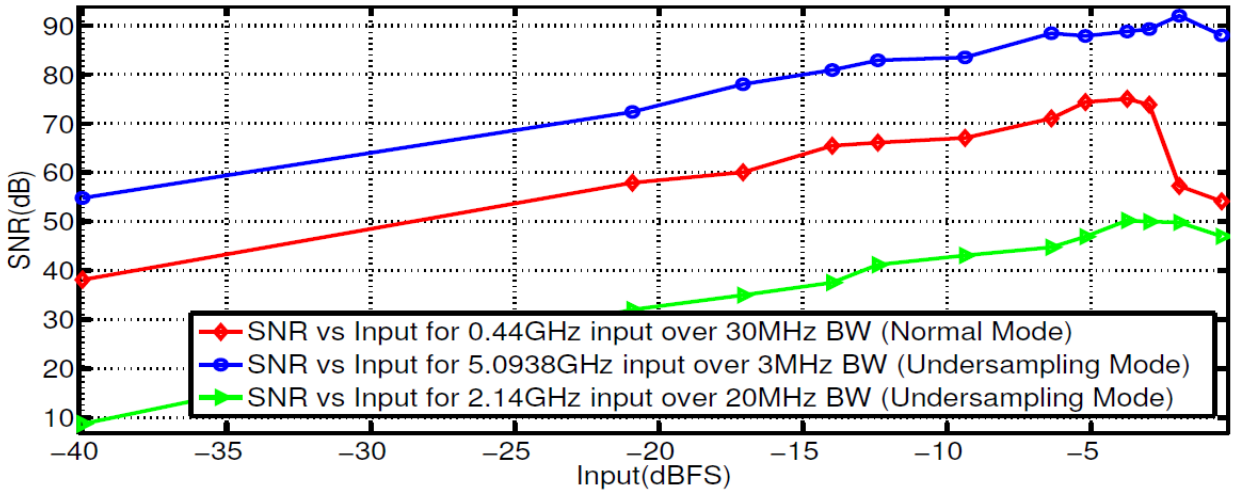
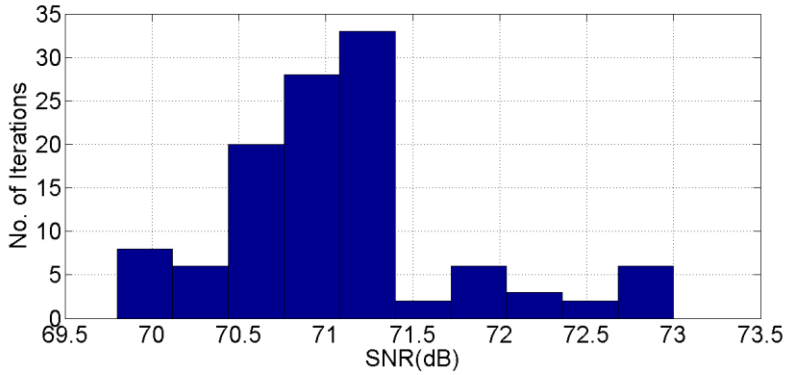
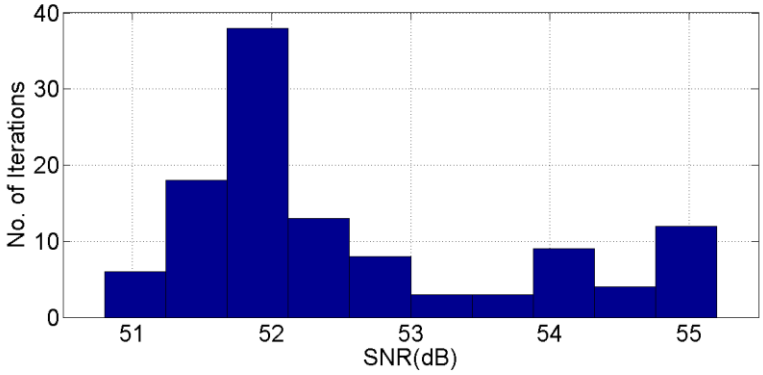


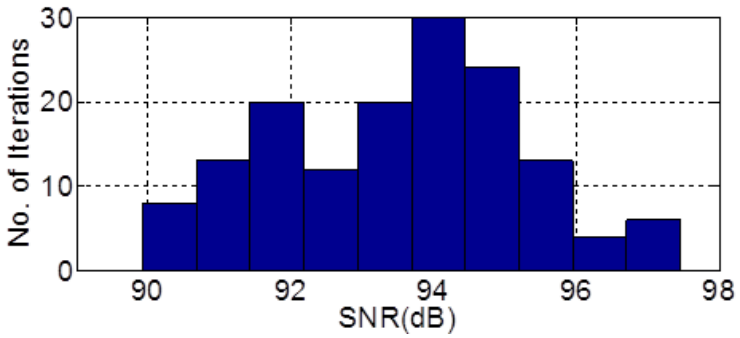
Figure 4.13. SNR vs. input for different cases of f_{RF} and f_S (f_{RF} = 0.44GHz, f_S = 2GHz (normal mode), f_{RF} = 2.14 GHz, f_S = 1 GHz (sub-sampling mode) and f_{RF} = 5.2 GHz, f_S = 2.5 GHz (sub-sampling mode)).



(a)



(b)



(c)

Figure 4.14. SNR histograms for the different cases of f_{RF} and f_S (a) f_{RF} = 0.44GHz, f_S = 2GHz (normal mode) (b) f_{RF} = 2.14GHz, f_S = 1GHz (sub-sampling mode) and (c) f_{RF} = 5.2 GHz, f_S = 2.5 GHz (sub-sampling mode).

Table 4.4 . Summary of the achievable performance of the modulator in normal and sub-sampling mode.

Mode	**f_{RF} (GHz)**	**f_S (GHz)**	**f_N (MHz)**	**f_0 (f_{IF} /f_s)**	**BW (MHz)**	**SNR (dB)**
Normal	0.15 -to-1	4	0.15 -to-1	0.0375 to 0.25	30	65 to 78
Sub-sampling	2.14	1	0.14	0.14	20	54
	3.75	2	0.25	0.125	20	48
	5.093	2.5	0.0938	0.0375	20	52

4.9 Conclusions

An outline of the different SDR based architectures was described in detail in this chapter. A 4th-order CT BP-ΣΔM ADC with a raised-cosine FIR feedback DAC capable of operating in normal and sub-sampling modes for RF-to-digital conversion was presented. The reduced number of loop-filter coefficients in the design resulted in a better robustness to mismatch, while ensuring the stability and complete equivalence between the discrete-time system and the continuous-time implementation. The system level simulation results for three different wireless communication standards spanning over an input frequency range of 0.44-to-5 GHz proved the accuracy of the presented methodology and architecture. The same methodology can be extended

to other standards as well. These advantages make the presented modulator a suitable option for direct RF digitization in next generation SDR mobile systems.

Chapter 5: A 4th-Order Variable Notch Frequency CRFF ΣΔM ADC

5.1 Introduction

It was proposed in the previous chapter that a CT BP-ΣΔM operating in the GHz range consisting of two reconfigurable LC BP filters, along with an FIR-based raised-cosine DAC can digitize a wide range of input signals. But to realise such a modulator with LC BP filters requires high Q and programmable inductors with a subsequent penalty of area [120][121]. Moreover, CT modulators suffer more due to the clock jitter [70]. Considering the fact that the required sampling rates are in GHz range (Table 4.3), realisation of a clock source with excellent accuracy is extremely difficult. An important alternative to the problem is the reconfigurable DT SC-based BP-ΣΔMs with variable f_N that operates at fixed f_S. For this purpose, the RF signals are downconverted to some lower frequencies and then a DT BP/LP ΣΔM is employed to digitize the RF/IF signals. DT ΣΔM are more robust to clock jitter and better suited for achieving reconfigurability [44][45][49][50]. In such DT architectures, the capacitors implementing the loop filter coefficients are reconfigured to obtain the desirable notch in the NTF [122][123]. The output of the ADC can then be downconverted in the digital domain for the digital processing.

This chapter describes the design and implementation of a 4th-order reconfigurable SC single-loop CRFF LP/BP-ΣΔM with 5-level quantisation, intended for IF digitization. Different architectural and circuit-level reconfiguration approaches are combined to achieve a tuneable notch frequency LP/BP-ΣΔM ADC with adaptive power consumption. The outline of the chapter is such that following the introduction, section 5.2 describes the analytical model of the modulator and synthesis procedure of coefficients. Section 5.3 is dedicated to circuit level non-

idealities and the resulting behaviour of the modulator. The description of macromodel implementation and corresponding results are given in section 5.4. The transistor-level implementation of the whole modulator is described in section 5.5 while layout details are given in section 5.6. Finally, section 5.7 details test-setup, experimental characterization and comparison with other state of the art designs.

5.2 Modulator Architecture

A 4th-order cascade of resonator with feedforward architecture has been selected for this prototype because compared to its cascade of resonator with feedback (CRFB) counterpart, this architecture requires a reduced number of coefficients. This essentially leads to less area requirement in terms of capacitors and hence less silicon area and hence reduced cost [44].

A 4th-order DT CRFF based ΣΔM ADC consisting of two resonators is shown in Figure 5.1. Each resonator consists of one Forward-Euler (FE) and one Backward-Euler (BE) Integrator. Two feedback coefficients (g_1 and g_2) across the integrators are used to realise resonators. A direct feedforward path from the input to the adder guarantees a unity STF. This way, only the error signal is processed by the internal integrators [124][125].

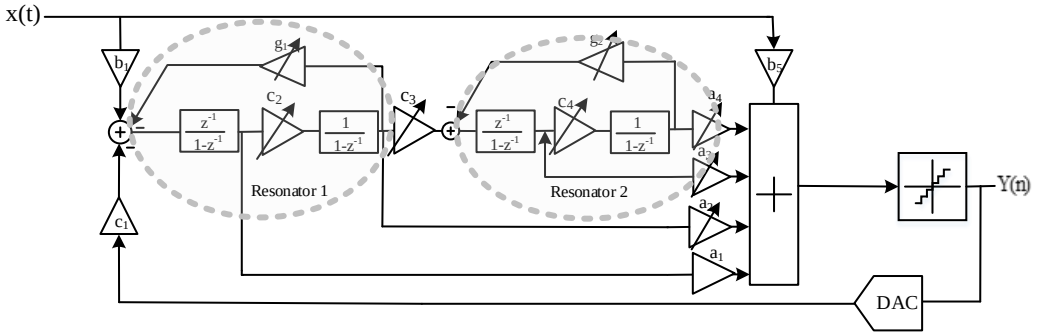


Figure 5.1. Reconfigurable 4th-order CRFF ΣΔM architecture.

To scale the input of the integrators, the coefficients c_1, c_2, c_3 and c_4 can be employed. This strategy relaxes the output swing requirements of integrators.

The transfer functions of the resonators in the forward path of the modulator are given by [126]:

$$H_1(z) = \frac{c_2 z^{-1}}{1 + (g_1 c_2 - 2)z^{-1} + z^{-2}}, \tag{5.1}$$

$$H_2(z) = \frac{c_4 z^{-1}}{1 + (g_2 c_4 - 2)z^{-1} + z^{-2}}. \tag{5.2}$$

Solving for the poles of $H_1(z)$ and $H_2(z)$ in (5.1) and (5.2), the centre (notch) frequencies (i.e. f_{N1} and f_{N2}) of the resonators can be found and are given by:

$$f_{N1} = \cos^{-1}\left(\frac{2 - c_2 g_1}{2}\right) \tag{5.3}$$

$$f_{N2} = \cos^{-1}\left(\frac{2 - c_4 g_2}{2}\right) \tag{5.4}$$

Equations (5.3) and (5.4) indicate that f_N can be programmed by varying the "c" and "g" coefficients. Using these resonators in a ΣΔM, the noise shaping can be obtained over a range of notch frequencies.

5.2.1 Synthesis of the Loop-Filter Coefficients

Schreier's Matlab® Delta-Sigma toolbox [127] has been employed for the derivation of the values of the ΣΔM loop-filter coefficients for the CRFF architecture. It has been shown that f_N can be programmed by varying "c" and "g" coefficients. These coefficients are going to be implemented with the capacitor ratios. A wider range of the f_N requires highly reconfigurable coefficients resulting in a huge number of switches and capacitors to realise them. Therefore,

these coefficients have been synthesised only for 22 different distinct values of f_N spaced at 0.01 f_S (where f_S being the sampling rate). The derived coefficients have been optimised to minimise the integrator's output swing (below 20 % of the full-scale range). As a result of this the swing requirements of the op-amps in the integrators are reduced.

The values of coefficients, g_1, g_2, c_1 and c_2 get changed for each f_N according to equations (5.1) and (5.2). Further, to maintain the same noise-shaping behaviour, i.e. the same NTF for all f_N; the feedforward coefficients (a_1 to a_4) are also modified. Also, multiple iterations were made to optimise the coefficients such that they can be realised with feasible capacitor-ratios. As an illustration, Table 5.1 gives the set of coefficients derived for an f_N of 0.03 f_S. This table shows that coefficients b_1 and c_1 can be easily realised with capacitor ratios of 0.25. Moreover, it can be observed that all coefficients are multiples of either 0.0625 or 0.125. This leads to a straight-forward binary-weighted implementation of the sampling capacitor with a fixed integrating capacitor. A summary of all coefficients derived for the full range of reconfigurability, along with the number of bits required to implement them, are given in Table 5.2.

5.2.2 System Level Simulation Results

As a first step, using Simulink® blocks, architecture similar to Figure 5.1 has been developed. The derived coefficients can be used for the behavioural simulation of this system. In order to check the validity of derived coefficients, behavioural simulations have been carried out over an input frequency range of 0-to-22 MHz with a sampling rate of 100 MHz.

Table 5.1. Modulator coefficients for f_N = 3 MHz.

Coef.	Value	Coef.	Value	Coef.	Value	Coef.	Value
b_1	0.25	a_1	3.00	c_1	0.25	g_1	0.0625
b_2 b_3 b_4	0.00	a_2	3.25	c_2	0.50	g_2	0.1250
b_5	1.00	a_3	2.75	c_3	0.50		
		a_4	1.125	c_4	0.25		

Table 5.2. Maximum and minimum values of all coefficients along with the number of bits required for the implementation.

Coefficients	Min.	Max.	No. Of Bits
b_1	0.25	0.25	--
$b_2 b_3 b_4$	0	0	--
b_5	1	1	--
a_1	3	3	--
a_2	0.125	3.875	5
a_3	0.125	3.875	5
a_4	0.125	3.875	5
c_1	0.25	0.25	--
c_2	0.125	1.875	4
c_3	0.125	1.875	4
c_4	0.125	1.875	4
g_1	0.0625	1.875	5
g_2	0.0625	1.875	5

The results obtained in this way are processed in Matlab®. Figure 5.2 to Figure 5.9 represent the plots of input of a -6 dBFS input signal, at the different notches frequencies of 3, 6, 9, 12, 15, 18 and 22 MHz, respectively.

The same coefficients derived for f_S =100 MHz can be used for f_S = 200 MHz to increase the tuning range of the notch to 44 MHz. As an illustration, Figure 5.10 shows the SNDR-versus-amplitude curves obtained over the whole f_N tuning range (0-to-44 MHz) and considering a signal bandwidth of 1 MHz while employing sampling rates of 100 MHz and 200 MHz, respectively.

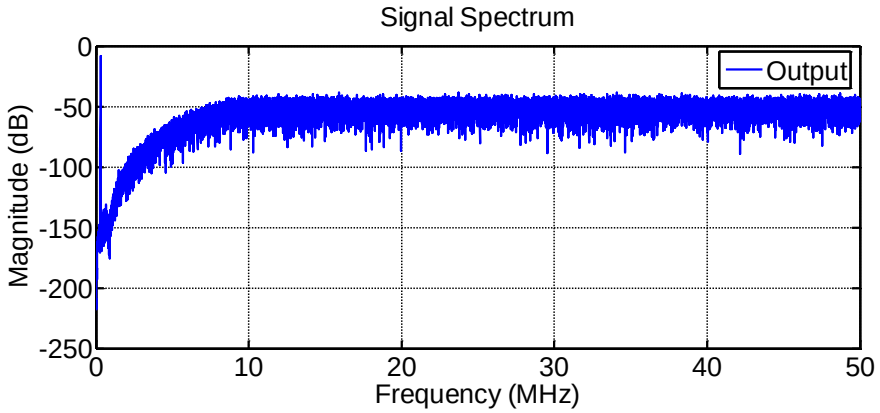


Figure 5.2. Output spectrum plot of an input of 300 kHz for ideal model with the ADC operating in the LP-mode (f_S =100 MHz).

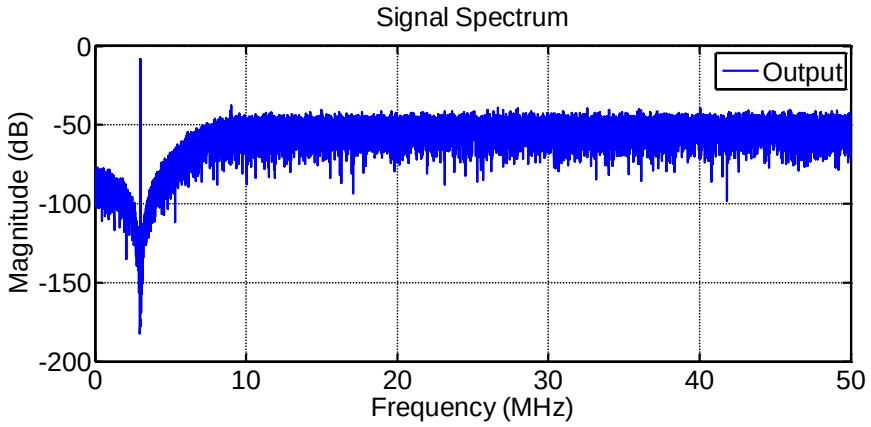


Figure 5.3. Output spectrum plot with f_N = 3 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

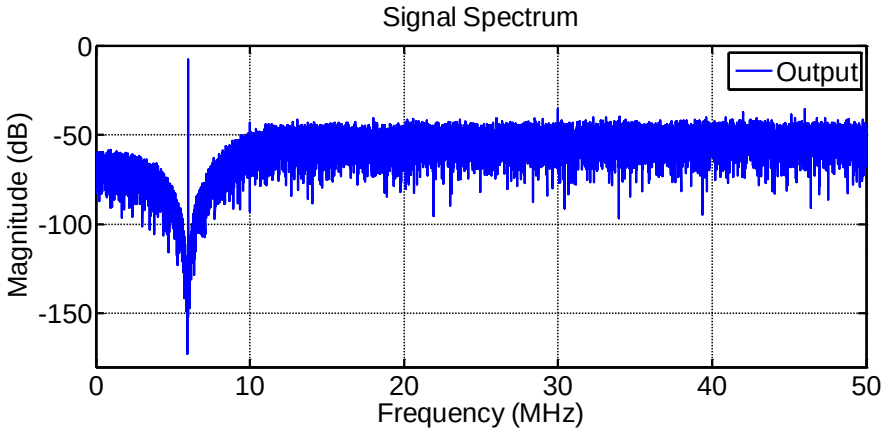


Figure 5.4. Output spectrum plot with f_N = 6 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

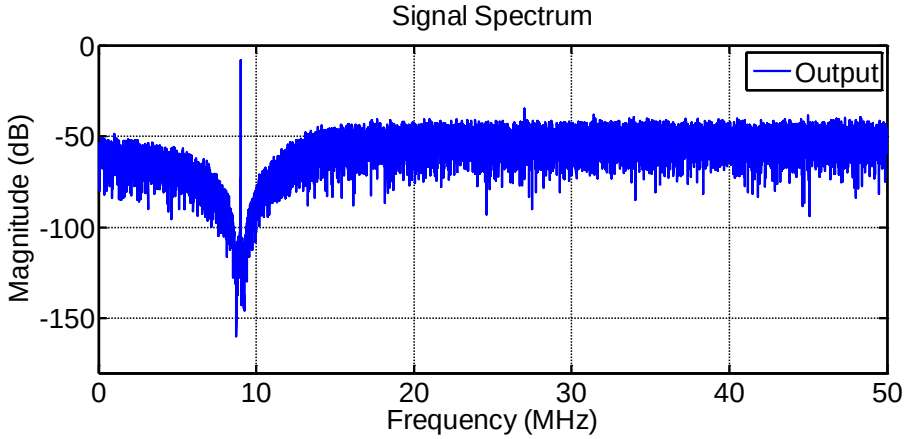


Figure 5.5. Output spectrum plot with f_N = 9 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

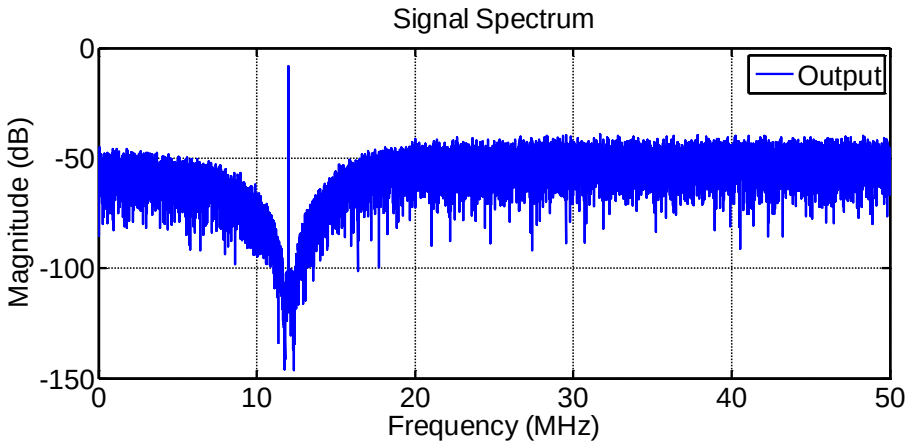


Figure 5.6. Output spectrum plot with f_N = 12 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

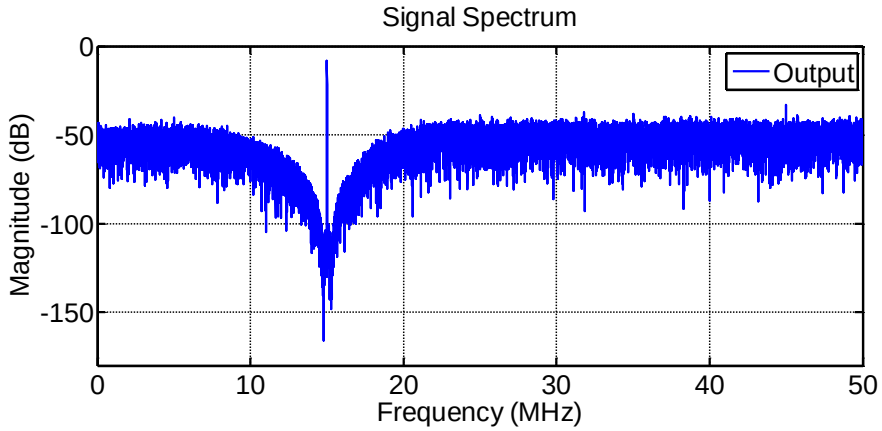


Figure 5.7. Output spectrum plot with f_N = 15 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

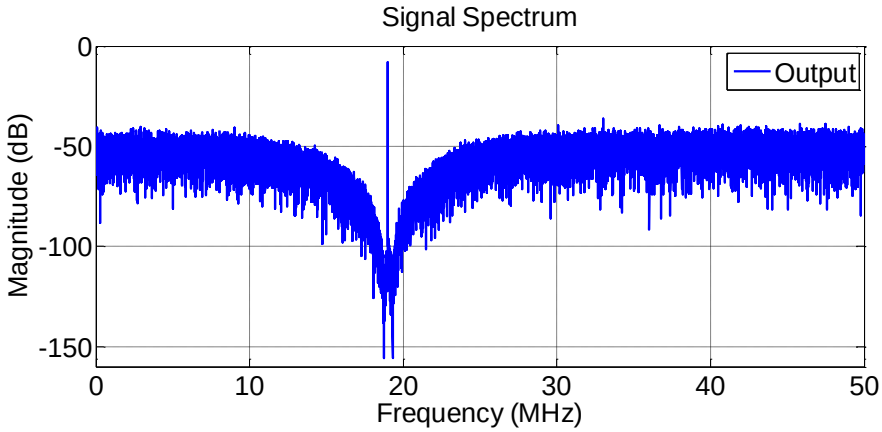


Figure 5.8. Output spectrum plot with f_N = 18 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

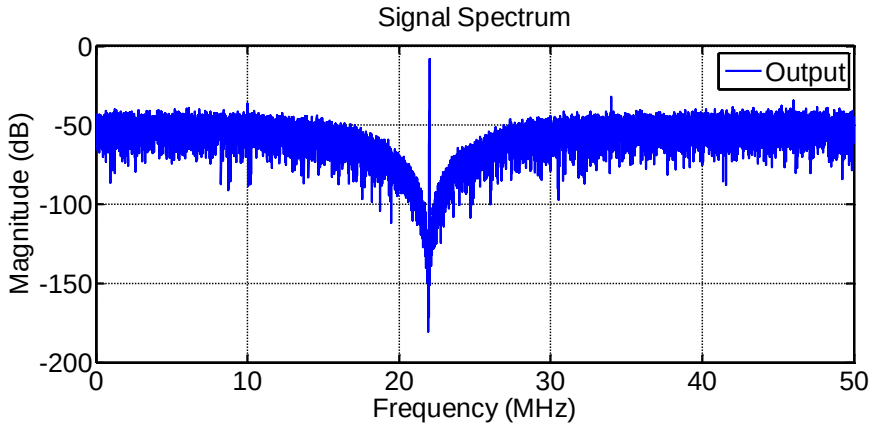


Figure 5.9. Output spectrum plot with f_N = 22 MHz for ideal model with the ADC operating in the BP-mode (f_S = 100 MHz).

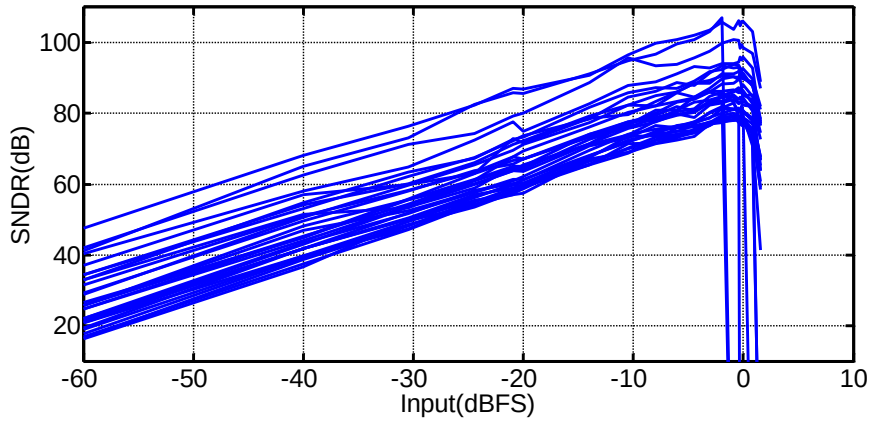


Figure 5.10. SNDR vs. input amplitude for a bandwidth of 1 MHz and f_N from 0 to 44 MHz (while employing f_S = 100 MHz for the tuning range f_N = 0-to-22 MHz and f_S = 200 MHz over the tuning range f_N = 23-to-44 MHz).

5.3 Impact of Circuit Errors and High-Level Sizing

In order to transform the system-level architecture to a circuit-level implementation, a systematic design flow has been adopted [128]. In this section, initially a capacitor calculation strategy for a given in-band error (IBE), is examined. Following that, a parametric analysis of different non-idealities of the op-amp employed in integrators and simulation results are presented.

5.3.1 Sampling Capacitor Calculations for a Given IBE

The major contribution of input referred noise for this ADC comes from the first resonator [129][130]. In order to calculate the sampling capacitors, a conceptual single-ended SC schematic shown in Figure 5.11 has been used. This schematic represents the arrangement of integrators in the modulator. The four sampling capacitors in front of each of the four integrators are represented by C_{sb1}, $C_{sc2,}$ C_{sc3} and C_{sc4}. While, C_{i1} to C_{i4} are the integrating capacitors of the respective integrators. The sampling capacitors in front of adder's op-amp are C_{sb5}, C_{sa2}, $C_{sa2,}$ C_{sa3} and C_{sa4}. Moreover, C_{sg1} and C_{sg2} are two capacitors to implement resonance coefficients (i.e. g_1 and g_2).

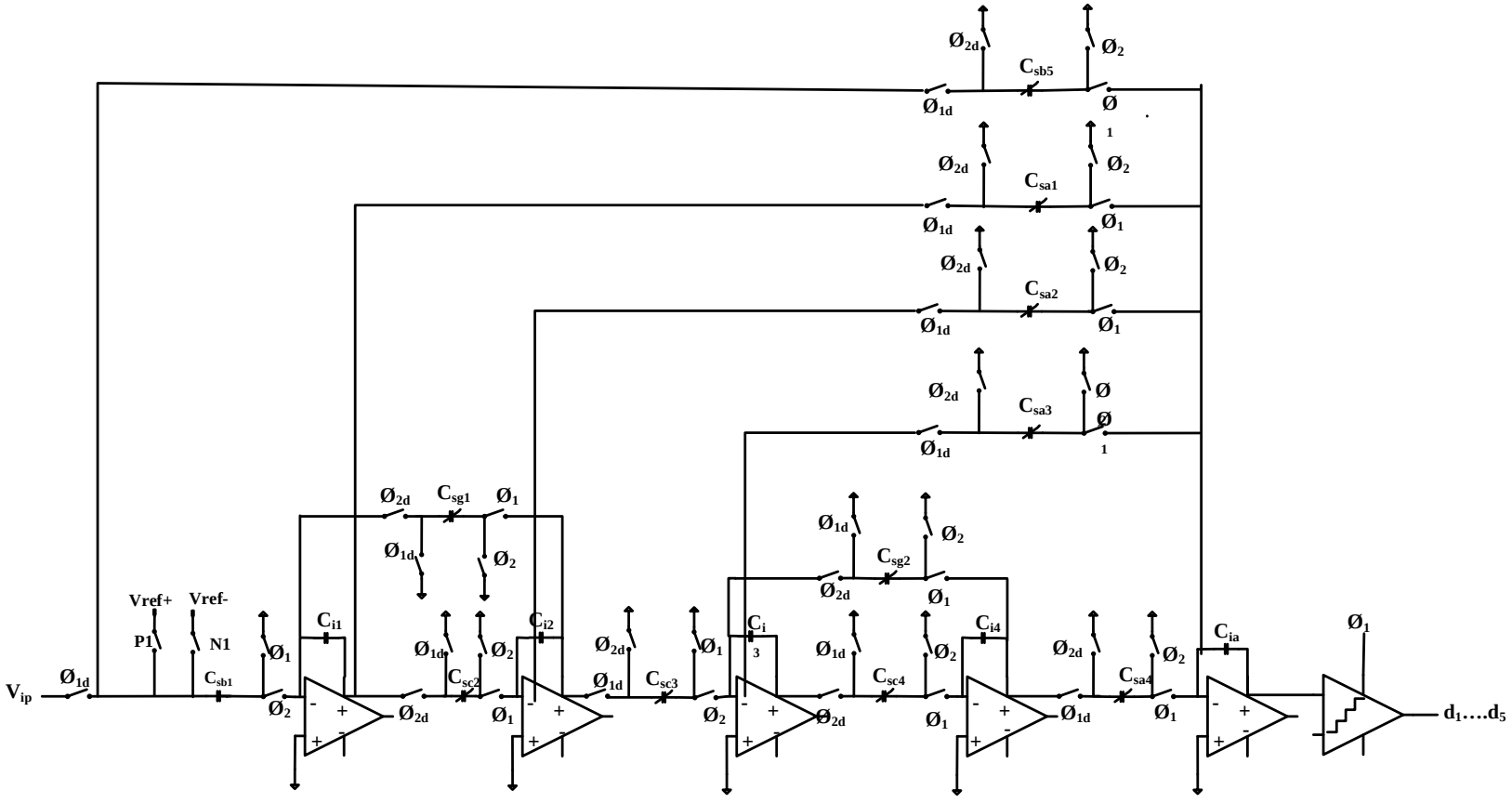


Figure 5.11. Conceptual SC schematic of the loop filters and adder in the proposed ΣΔM.

The f_N programmability is achieved by using the variable sampling capacitors (for back-end integrators and active adder) and variable resonance capacitors (i.e. C_{sg1} and C_{sg2}). The outputs from the feedback DAC (P1-P4 and N1-N4) are used to control the feedback switches (i.e. switches controlling 4 equal parts of C_{sb1}).

For this architecture, the differential input referred noise at a specific (notch) frequency "f_N" can be estimated as [130] :

$$\text{Average} \quad \text{Noise} = \frac{4kT}{OSR}\left[\frac{1}{C_{sb1}} + \frac{C_{sg1}}{C_{sb1}^{\,2}} + \frac{\left|1 - e^{-i2\pi fN}\right|^2}{b_1^{\,2} C_{sc2}}\right]. \tag{5.5}$$

Where, b_1 is the scaling factor for the first integrator, given by capacitor ratio C_{sb1}/C_{i1}. As the first integrator sampling capacitors are shared with the DAC, the term involving the DAC capacitances has been omitted.

In order to simplify (5.5), g_1 can be represented as follows:

$$g_1 = \frac{C_{sg1}}{C_{i1}}. \tag{5.6}$$

Therefore:

$$C_{sg1} = g_1 C_{i1}. \tag{5.7}$$

Further, b_1 can be written as:

$$b_1 = \frac{C_{sb1}}{C_{i1}}. \tag{5.8}$$

Also, C_{i1} is given by,

$$C_{i1} = \frac{C_{sb1}}{b_1}. \tag{5.9}$$

Putting this value of C_{i1} in (5.7), gives:

$$C_{sg1} = \frac{g_1 C_{sb1}}{b_1}. \tag{5.10}$$

When equation (5.10) is further rearranged:

$$\frac{C_{sg1}}{C_{sb1}^{\ 2}} = \frac{g_1}{b_1 C_{sb1}}. \tag{5.11}$$

Putting value this value in (5.5), the average in-band noise can be written as:

$$\text{AverageNoise} = \frac{4kT}{OSR}\left[\frac{1}{C_{sb1}} + \frac{g_1}{b_1 C_{sb1}} + \frac{\left|1 - e^{(-i2\pi)f}\right|^2}{b_1^{\ 2} C_{sc2}}\right]. \tag{5.12}$$

Equation (5.12) shows various trade-offs of the sampling capacitor calculations. The input referred noise is inversely related to the sampling capacitor in the first and second integrators (i.e. C_{sb1} and C_{sc2}) but increases with f_N. As an illustration, Table 5.3 shows the different values of C_{sb1} and C_{sc2} and the resultant IBE. Using this approach, different combinations of C_{sb1} and C_{sc2} were investigated at different notch frequencies to have realisable capacitance values, while maintaining the average IBE within a desirable range. The coefficient b_1 and hence the sampling capacitor of the first integrator (C_{sb1}), remains the same over the whole range of f_N. In terms of second, third and 4th integrators, the sampling capacitors are varied to realise the variable coefficients. Based on the required value of the sampling capacitor for a specific f_N, the switches can be turned ON or OFF to realise the desired value. A detailed explanation about the SC implementation, along with detailed schematics of the capacitor implementation will be explained in the next section.

Based on the above analysis, the values of all sampling, integrating and resonant capacitors (used to implement g_1 and g_2) have been derived. Table 5.3 details the sampling capacitor values of the front end two integrators and achievable IBE. The final values of the modulator capacitors derived and number of bits required to implement them are given in Table 5.4. Finally, Table 5.5 summarises the binary weighted sampling and resonant capacitors for all integrators.

Table 5.3. f_N, sampling capacitors of first and second integrator and corresponding IBE.

No.	f_N (MHz)	Average in-band noise (dB)	C_{sb1} (pF)	C_{sc2} (pF)
1	22	-89	0.25	1.237
2	13	-77	0.4	0.190
3	8	-87	0.5	0.175
4	2	-81	0.25	2.200

Table 5.4. Summary of the sampling and integrating capacitor values (pF).

		Min.	Max.	Bits
First Integrator	C_{sb1}	0.2	0.2	--
	C_{sg1}	0.05	1.55	5
Second Integrator	C_{i1}	0.8	0.8	--
	C_{sc2}	0.1	1.5	4
	C_{i2}	0.8	0.8	--
Third Integrator	C_{sc3}	0.1	1.5	4
	C_{sg2}	0.05	1.55	5
	C_{i3}	0.8	0.8	--
Fourth Integrator	C_{sc4}	0.05	0.75	4
	C_{i4}	0.4	0.4	--
	C_{a1}	1.5	1.5	--
	C_{a2}	0.05	1.55	5
Adder	C_{a3}	0.05	1.55	5
	C_{a4}	0.05	1.55	5
	C_{ia}	0.4	0.4	--

Table 5.5. Binary weighted sampling and resonant capacitors for 4 integrators

Integrator	Capacitor	Physical Value (pF)
First Integrator	C_{sb1}	0.20
	C_{ub1}	0.05
	C_{i1}	0.80
Second Integrator	C_{uc1}	0.10
	C_{uc2}	0.20
	C_{uc3}	0.40
	C_{uc4}	0.80
	C_{i2}	0.80
Third Integrator	C_{uc1}	0.05
	C_{uc2}	0.10
	C_{uc3}	0.20
	C_{uc4}	0.40
	C_{uc5}	0.80
	C_{i3}	0.80
Fourth Integrator	C_{uc1}	0.05
	C_{uc2}	0.10
	C_{uc3}	0.20
	C_{uc4}	0.40
	C_{i4}	0.40
First Resonance Capacitor	C_{ug1}	0.05
	C_{ug2}	0.10
	C_{ug3}	0.20
	C_{ug4}	0.40
	C_{ug5}	0.80
Second Resonance Capacitor	C_{ug1}	0.05
	C_{ug2}	0.10
	C_{ug3}	0.20
	C_{ug4}	0.40
	C_{ug5}	0.80

5.4 Parametric Analysis of Op-amps Non-idealities

The non-idealities of the op-amps used to realise the integrators of the ΣΔM ADC degrade the TF of integrators and hence degrade the performance of the overall ADC. Most important of these non-idealities include finite DC gain, limited transconductance, limited output currents and input referred noise.

Considering an op-amp with a DC gain of A_o, The SC integrator's TF is given as [28][131]:

$$H(z) = g_S\left(1-\frac{1+g_s+g_p}{A_O}\right)\left(\frac{z^{-1}}{\left(1-\frac{g_s}{A_O}\right)z^{-1}}\right). \tag{5.13}$$

Where $g_S = \frac{C_s}{C_i}$,

and $g_P = \frac{C_p}{C_i}$.

Here C_s, C_i and C_p are the sampling, integrating and input parasitic capacitances of the integrator, respectively. Equation (5.13) shows that a finite DC gain results in a leaky integrator and shifts the pole of the NTF. The finite DC gain becomes a major concern in the band-pass modulators as it causes the shift in the notch of NTF when operating at higher notch frequencies. Another important parameter is the gain-bandwidth (GBW) of the op-amps which depends on the transconductance. The impact of GBW on the transfer function of integrator is given by [28][131]:

$$H(z) \approx g_s(1-\varepsilon_{ST})\left(\frac{z^{-1}}{1-z^{-1}}\right). \tag{5.14}$$

Where,
$$\varepsilon_{ST} \approx 1 - e^{-\pi \frac{GBW_{\varphi_2}(Hz)}{f_S}} \quad (5.15)$$

Equations (5.14) and (5.15) show that lower GBW results in higher IBE. Moreover, finite slew rate, which is dependent upon the output current, also results in distortion at the output of ΣΔM ADC [28].

A parametric analysis for these non-idealities has been carried out using SIMSIDES, a Simulink-based time-domain simulator for ΣΔMs [119]. This tool can analyse the circuit level non-idealities of DT and CT integrators at the behavioural level and gives a good estimate about the specifications of different building blocks. The parametric analysis for these three important specifications of the op-amps i.e. DC gain, transconductance and output current has been carried out in an incremental fashion. The analysis has been performed for different notch frequencies for each of the two sampling frequencies (i.e. 100 and 200 MHz).

5.4.1 Sampling Frequency f_S = 100 MHz

Figure 5.12 to Figure 5.17 present the parametric analysis results of different non-idealities at two different notches, namely 6 and 22 MHz (i.e. SNDR vs. non-idealities). Figure 5.12 shows the impact of finite DC gain on the modulator achievable SNDR for a notch centred at 6 MHz with a signal strength of -6 dBFS and a BW of 1 MHz. The first and second op-amps require gain in excess of 45 dB, while a DC gain of 30 dB is adequate for the 3rd and 4th integrators.

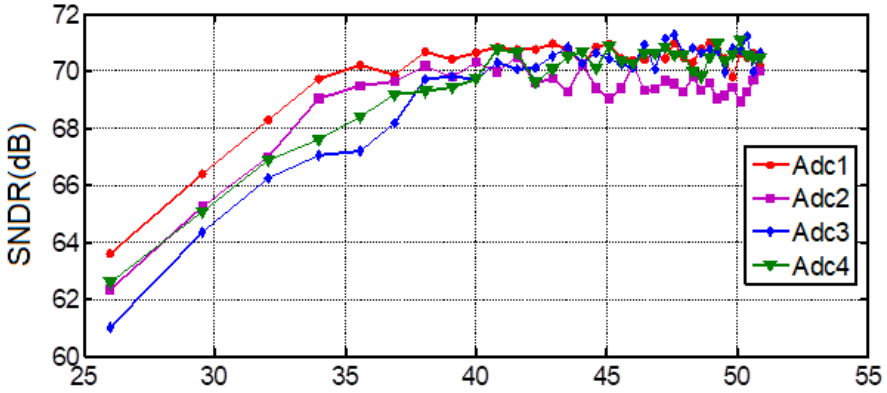


Figure 5.12. SNDR vs. DC gain (f_N = 6 MHz, f_N = 100 MHz).

After adjusting the DC gains of the all 4 op-amps to 46 dBs, a parametric analysis has been performed for the transconductance, (see Figure 5.13). The first and second op-amps require a higher transconductance (in the range of 4-to-5 mA/V). While, 3rd and 4th op-amps require a transconductance in the region of 3 mA/V. Employing the same methodology as mentioned above, a parametric analysis has been performed for the output current. Figure 5.14 shows the corresponding result.

Same parametric analysis for these three specifications was also completed with f_N of 22 MHz. Figure 5.15 to Figure 5.17 depict the corresponding results. These figures illustrate that the op-amps specifications become much more demanding for higher notch frequencies. If the op-amps can cope with the required specifications of higher notches, the lower frequency requirements are automatically met. Therefore, the specifications of op-amps have been tuned to operate correctly at 22 MHz. Table 5.6 details the selected parameters, determined using the above-mentioned criteria. Table 5.7 depicts the SNDR signals with different bandwidth at two different notch frequencies with the selected parameters of op-amps for an input of -6 dBFS.

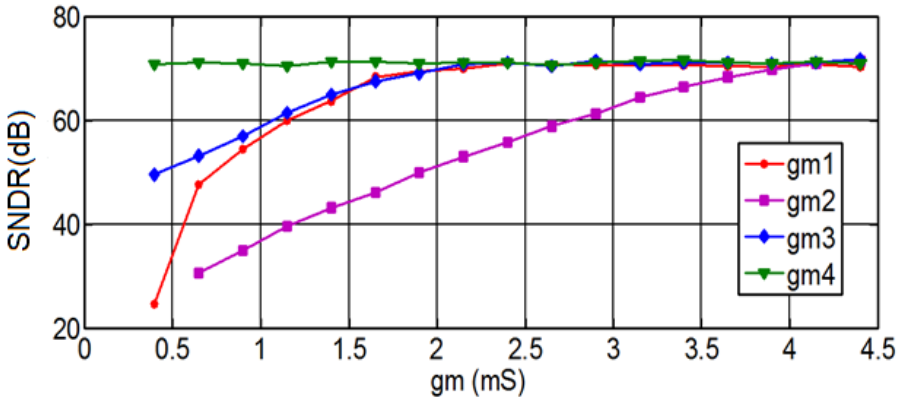


Figure 5.13. SNDR vs. transconductance (f_N = 6 MHz, f_N = 100 MHz).

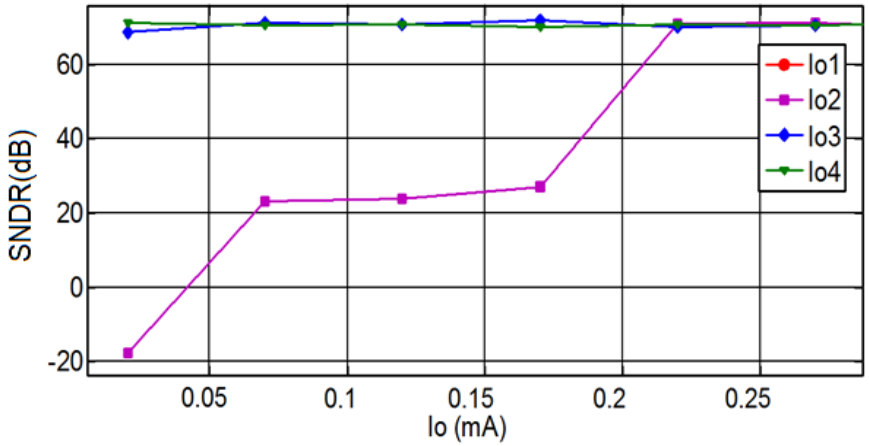


Figure 5.14. SNDR vs. output current (f_N = 6 MHz, f_N = 100 MHz).

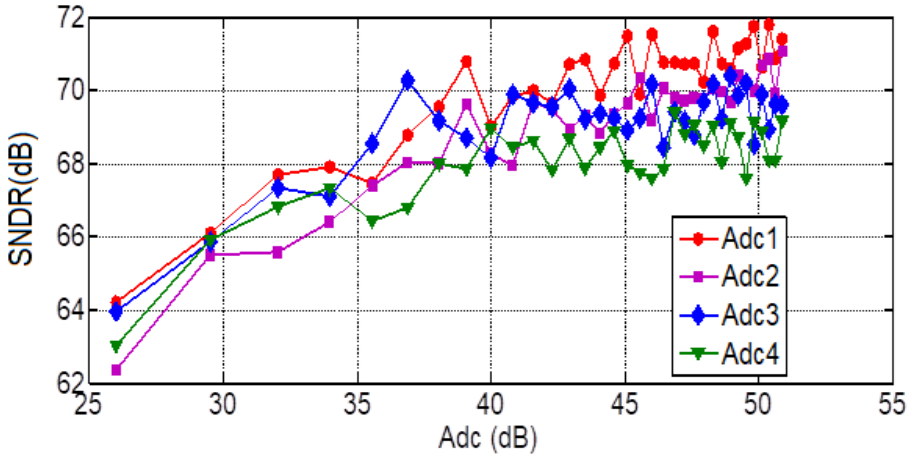


Figure 5.15. SNDR vs. DC gain (f_N = 22 MHz, f_N = 100 MHz).

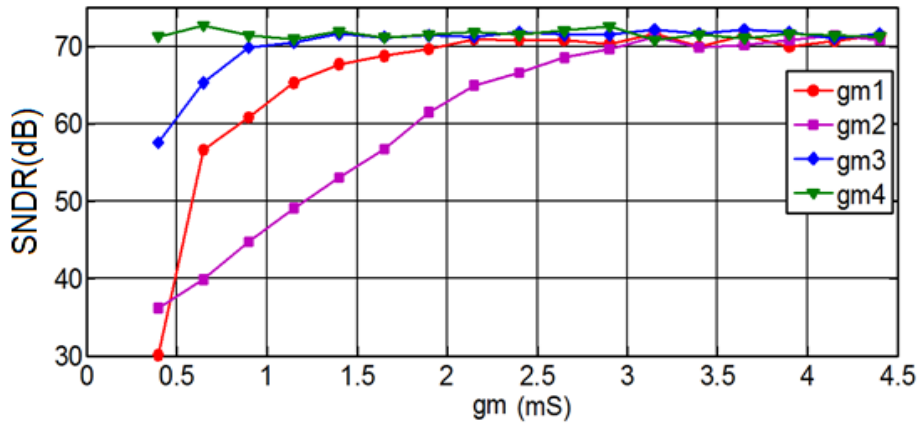


Figure 5.16. SNDR vs. transconductance (f_N = 22 MHz, f_N = 100 MHz).

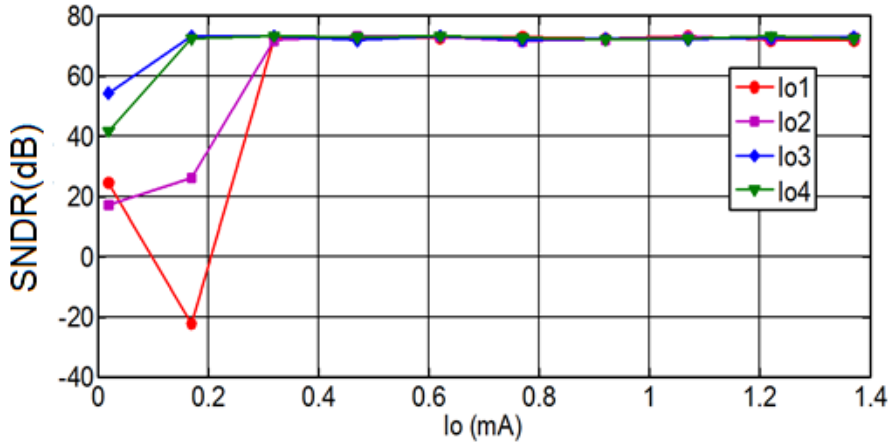


Figure 5.17. SNDR vs. output current (f_N = 22 MHz, f_N = 100 MHz).

Table 5.6. Op-amps specifications (f_s = 100 MHz).

	First op-amp	**Second op-amp**	**Third op-amp**	**Fourth op-amp**
DC Gain (dB)	46.9	46.9	46.5	45.6
g_m (mA/V)	4.2	4.1	3.2	1.5
Io (mA)	0.50	0.90	0.60	0.50
o/p swing for 22MHz (V)	±0.18	±0.13	±0.07	±0.08
o/p swing for 6MHz (V)	±0.26	±0.36	±0.37	±0.25
Input cap. (fF)	72	72	72	72
Output cap. (fF)	32	32	32	32
Eq. input noise ($nV/Hz^{1/2}$)	4	4	5	8

Table 5.7. SNDR for different bandwidths (f_s = 100 MHz).

Notch Frequency (MHz)	Bandwidth (MHz)	SNDR (dB)
6	2.00	59.84
	1.00	70.48
	0.50	81.89
	0.20	85.87
22	2.00	57.64
	1.00	69.12
	0.50	78.40
	0.20	80.20

5.4.2 Sampling Frequency f_S = 200 MHz

Following the same procedure as mentioned in section 5.4.1 , a parametric analysis has been carried out for f_S = 200 MHz. The results for two different notch frequencies of 30 and 36 MHz are illustrated in Figure 5.18 to Figure 5.23

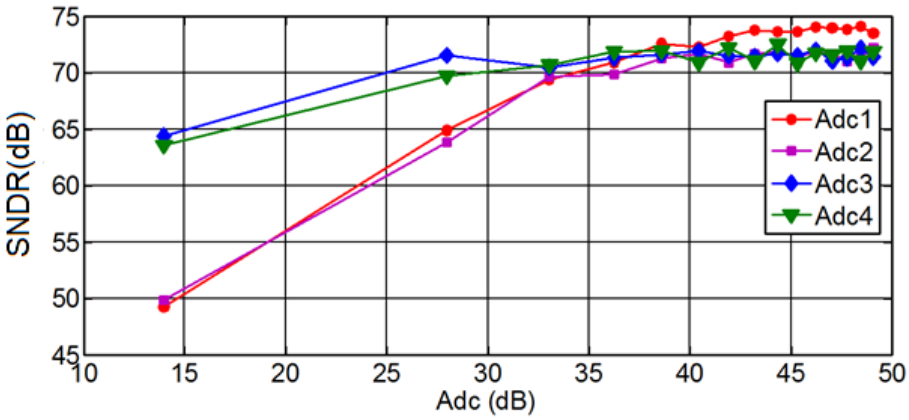


Figure 5.18. SNDR vs. DC gain (f_N = 30 MHz, f_S = 200 MHz).

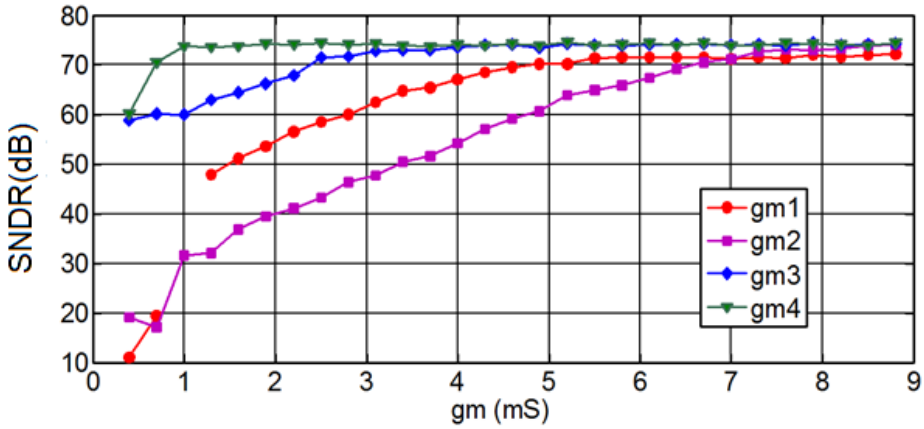


Figure 5.19. SNDR vs. transconductance (f_N = 30 MHz, f_S = 200 MHz).

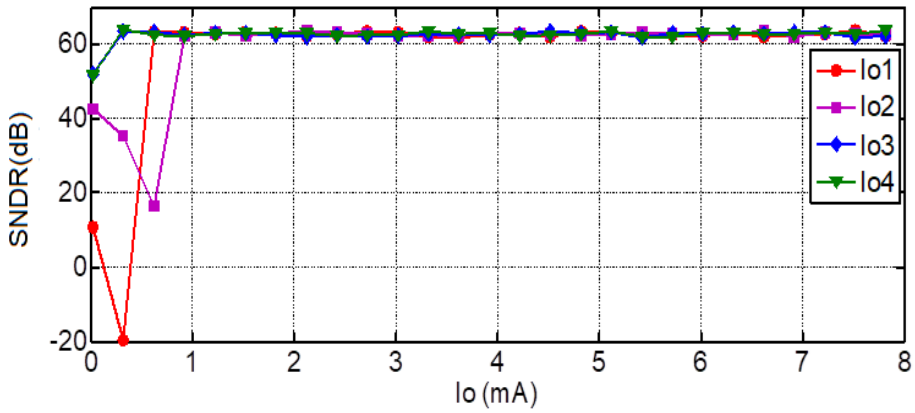


Figure 5.20. SNDR vs. output current (f_N = 30 MHz, f_S = 200 MHz).

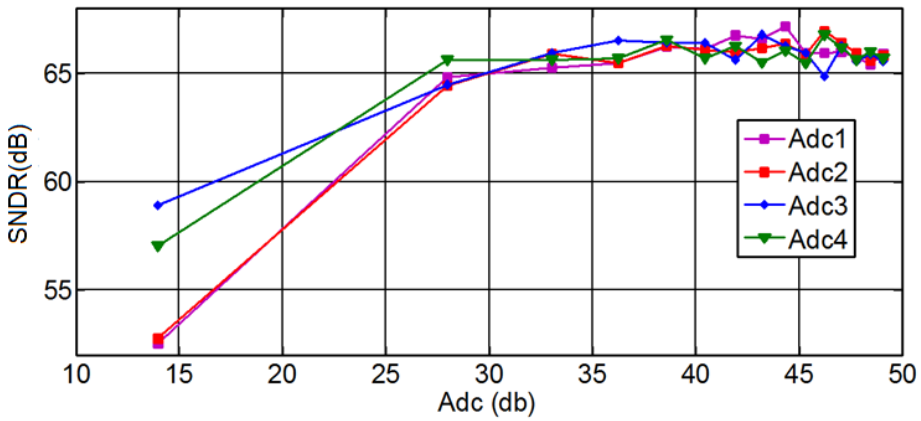


Figure 5.21. SNDR vs. DC gain (f_N = 36 MHz, f_S = 200 MHz).

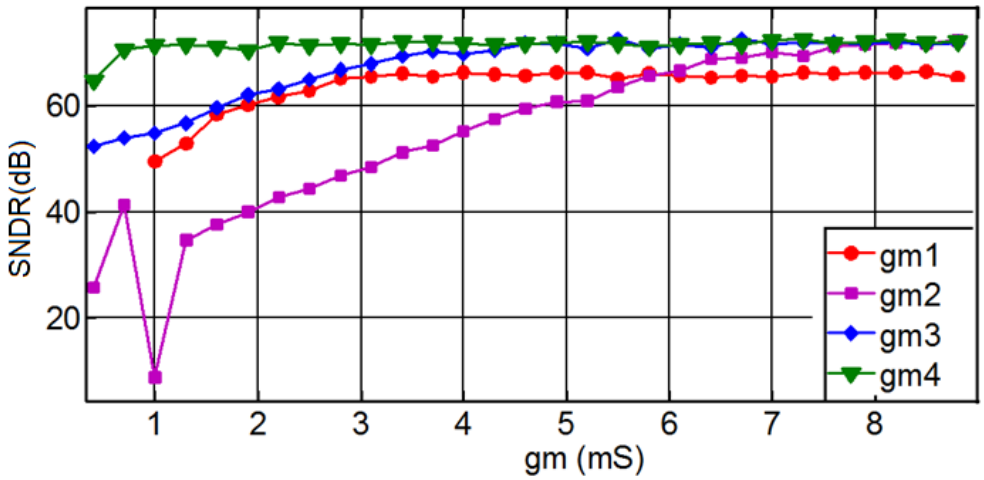


Figure 5.22. SNDR vs. transconductance (f_N = 36 MHz, f_S = 200 MHz).

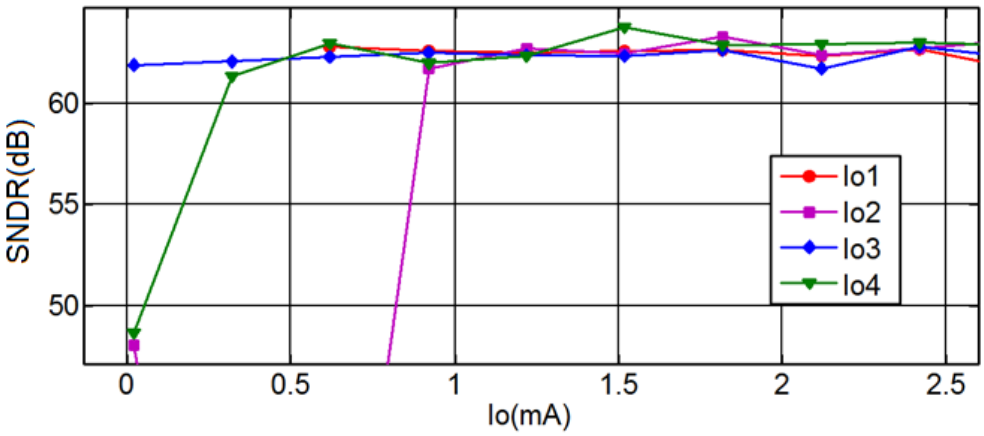


Figure 5.23. SNDR vs. output current (f_N = 36 MHz, f_S = 200 MHz).

Table 5.8 gives the resultant required parameters for op-amps while Table 5.9 shows the SNDR for the different bandwidths and notches for an input of -6 dBFS.

Table 5.8. Op-amp specifications (f_S = 200 MHz).

	First op-amp	Second op-amp	Third op-amp	Fourth op-amp
DC Gain(dB)	46.90	46.90	46.50	45.60
g_m (mA/V)	5.10	4.50	3.20	1.5
Io (mA)	1	1	0.60	0.50
o/p swing for 36MHz(V)	±0.17	±0.18	±0.16	±0.12
o/p swing for 30MHz(V)	±0.18	±0.14	±0.17	±0.14
Input cap. (fF)	72	72	72	72
Output cap. (fF)	32	32	32	32
Eq. input noise ($nV/Hz^{1/2}$)	4	4	5	8

Table 5.9. SNDR for different bandwidths (f_S = 200 MHz).

Notch Frequency (MHz)	Bandwidth (MHz)	SNDR (dB)
30	2.00	56.92
	1.00	61.23
	0.50	65.13
	0.20	74.21
36	2.00	58.3
	1.00	61.4
	0.50	64.76
	0.20	75.35

5.5 Transistor-Level Design

This section describes the details of the transistor-level design of the modulator. Starting with the block-level description of the complete modulator, the subsequent sections give the design and simulation results of different building blocks.

5.5.1 SC Implementation of Modulator

A single-ended SC implementation of the modulator is given in Figure 5.24. This diagram represents the arrangement of 4 integrators, an active adder, quantiser and the feedback DAC. The sampling capacitors in front of each integrator are represented by C_{sb1}, $C_{sc2,}$ C_{sc3} and C_{sc4}. The first sampling capacitor C_{sb1}, has been divided into 4 parts to realise a 5 level feedback [58]. C_{i1} to C_{i4} are the integrating capacitors for the integrators. The sampling capacitors of the adder are represented by C_{sb5}, C_{sa2}, C_{sa2}, C_{sa3} and C_{sa4}. Moreover, C_{sg1} and C_{sg2} are the capacitors to realise the resonance.

All the integrators and adder employ the variable sampling capacitors to realise the desired capacitor ratio listed in Table 5.10.

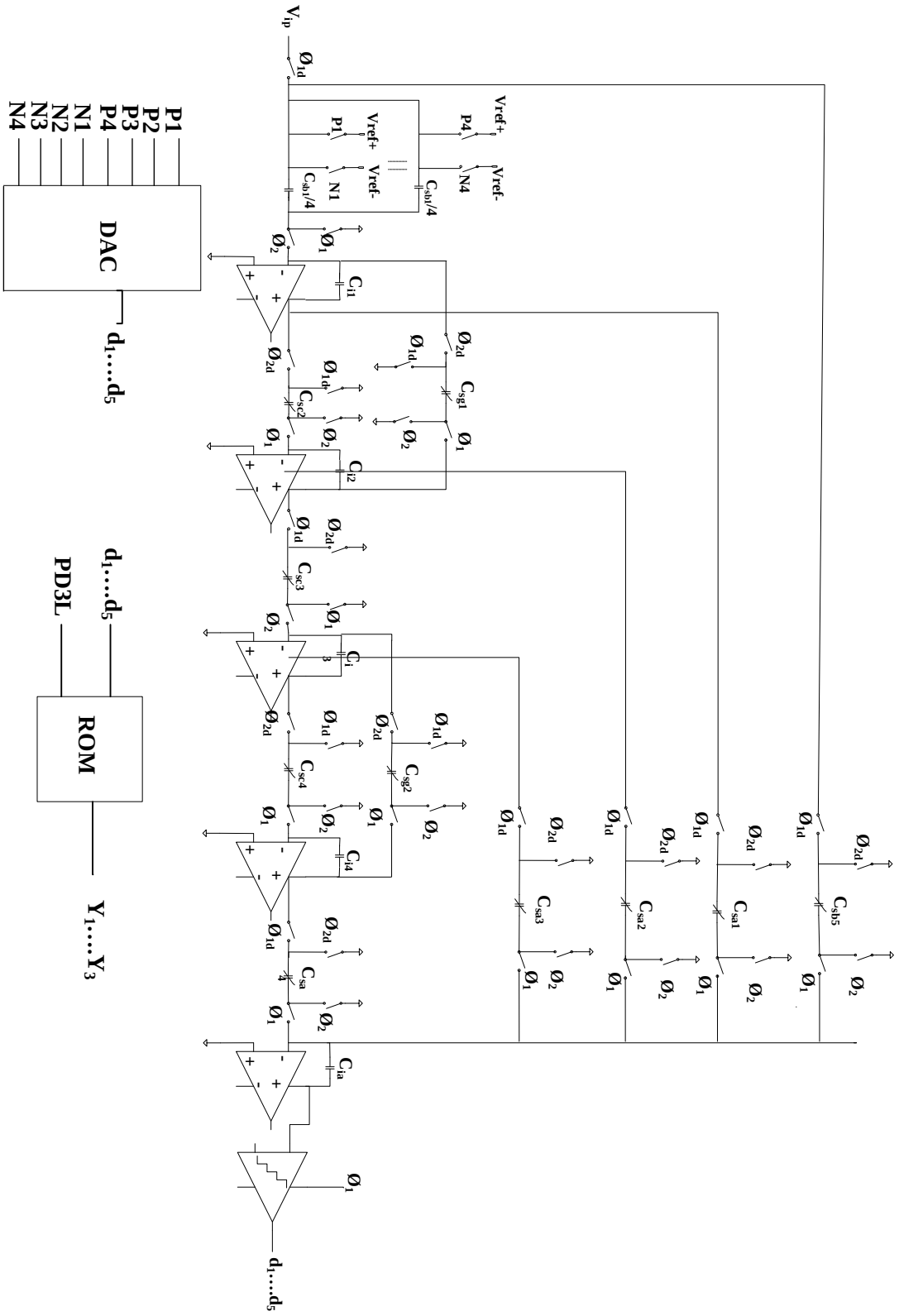


Figure 5.24. Single-ended version of a 4th-order SC ΣΔM.

Table 5.10. Implementation of integrator coefficients.

Coefficient	Capacitor Ratio	Coefficient	Capacitor Ratio
a_1	$\frac{C_{sa1}}{C_{ia}}$	c_1	$\frac{C_{sc1}}{C_{i1}}$
a_2	$\frac{C_{sa2}}{C_{ia}}$	c_2	$\frac{C_{sc2}}{C_{i2}}$
a_3	$\frac{C_{sa3}}{C_{ia}}$	c_3	$\frac{C_{sc3}}{C_{i3}}$
a_4	$\frac{C_{sa4}}{C_{ia}}$	c_4	$\frac{C_{sc4}}{C_{i4}}$
b_1	$\frac{C_{sb1}}{C_{i1}}$	g_1	$\frac{C_{sg1}}{C_{i1}}$
b_5	$\frac{C_{sb5}}{C_{ia}}$	g_2	$\frac{C_{sg2}}{C_{i2}}$

The first integrator coefficient (i.e. b_1) remains the same over the full range of f_N. Therefore, its sampling capacitor is fixed. The remaining integrators and adder employ variable sampling capacitors. As an illustration, Figure 5.25 depicts the single-ended version of the 3rd integrator. Here the integrating capacitor remains fixed while sampling and the resonant capacitors are made up of binary weighted capacitors (C_{sc3} is made up of C_{uc1}, C_{uc2}, C_{uc3} and C_{uc4} while C_{sg2} is made up of C_{ug1}, C_{ug2}, C_{ug3}, C_{ug4} and C_{ug5}). Depending upon the control signal, the binary weighted sampling capacitors can be added or removed from the circuit to realise the desired ratio with integrating capacitor (and hence the coefficient) [123]. With this approach, the capacitor ratio to implement a loop filter coefficient for a specific notch is achieved. The resonance capacitors, C_{sg1} and C_{sg2}, are more sensitive to the parasitic. Therefore, a simpler

configuration has been adopted for their implementation (as shown in Figure 5.26). Here the binary weighted capacitors branches are connected and disconnected using a single switch connected in series.

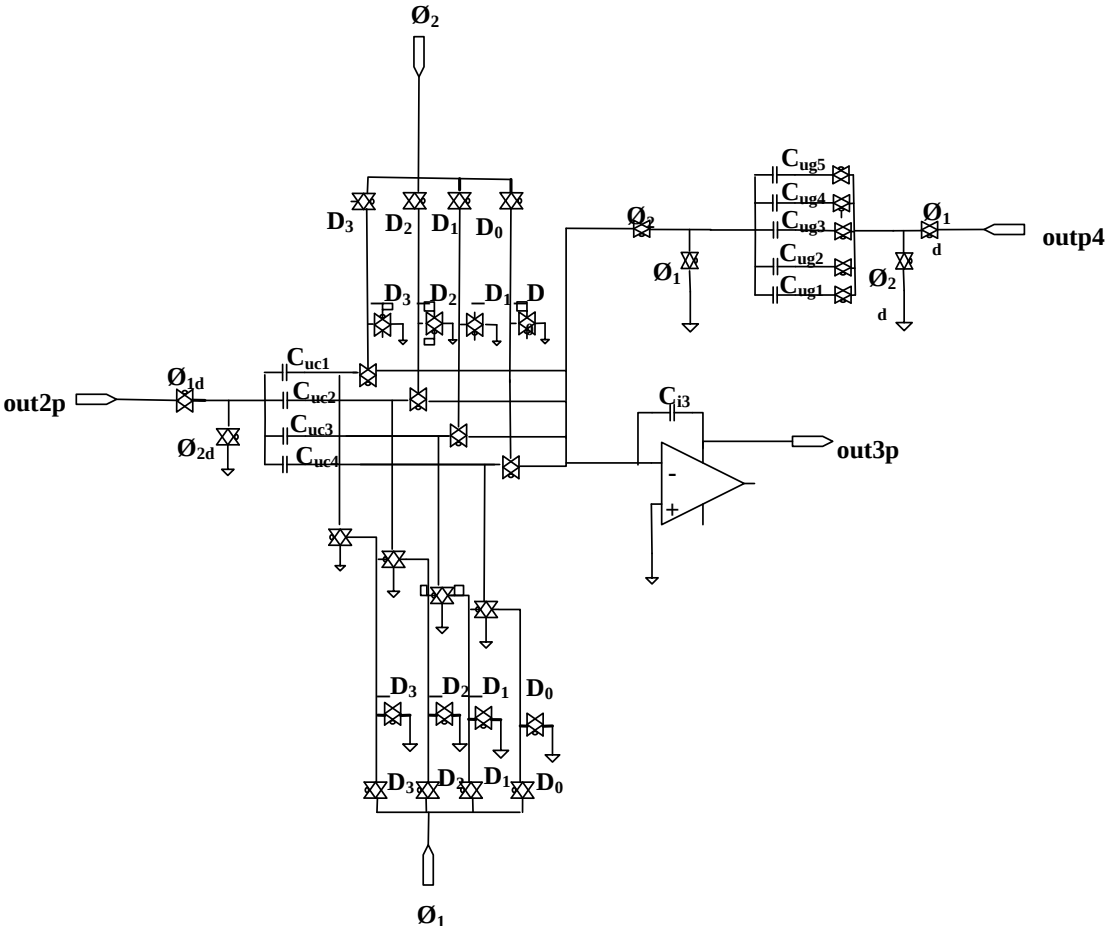


Figure 5.25. Switched capacitor implementation of the third integrator.

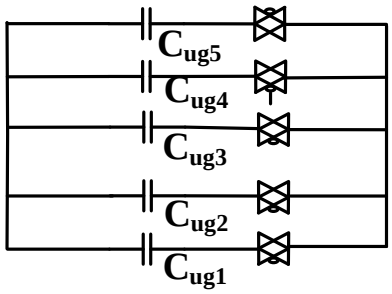
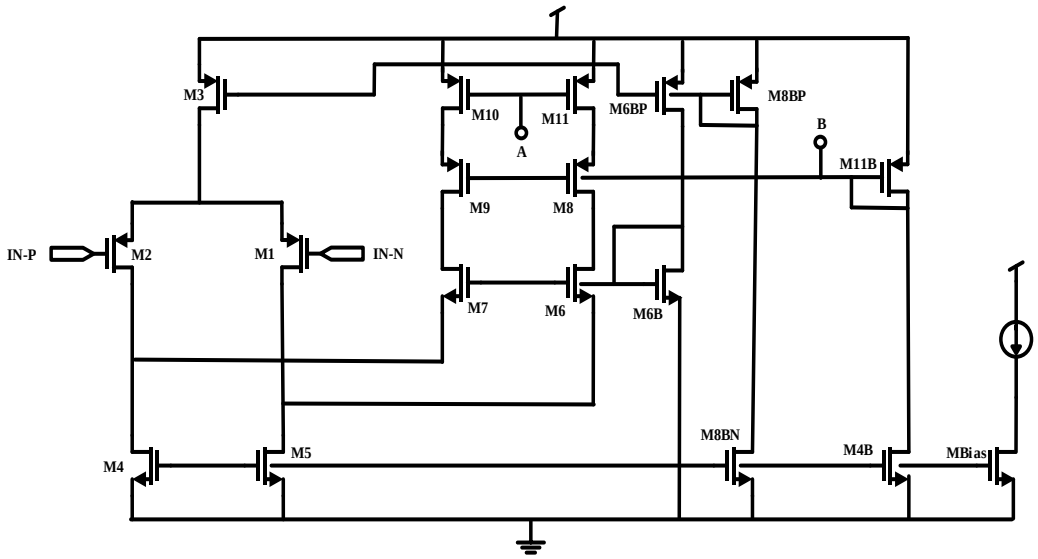


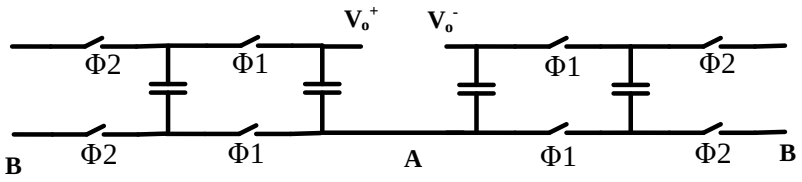
Figure 5.26. Implementation of variable resonance capacitor (C_{sg1} and C_{sg2}).

5.5.2 Op-Amps

Due to the higher output swing, good stability and larger gain, a folded cascode topology has been adopted for all of the op-amps in the modulator [1]. The circuit diagrams of the op-amp and common-mode feedback network employed are shown in Figure 5.27 (a) and (b), respectively. To reduce the substrate noise coupling, the differential input pair uses the PMOS transistors. Minimum-length transistors have been avoided in the input pair and in the current mirrors in order to reduce the 1/*f* noise and mismatch effects. Table 5.11 and Table 5.12 summarise the transistor sizes and achievable performance of the op-amp with the different bias current settings.



(a)



(b)

Figure 5.27. Folded cascode op-amp: (a) Core op-amp (b) SC common-mode feedback network.

Table 5.11. Transistor sizes of op-amp.

	Length (µm)	Width (µm)
M1, M2	0.25	264.08
M3	0.4	276
M4, M5	1	233.8
M6	0.2	23.52
M8BP, M9, M11B	0.2	50
M10, M11	0.4	184
M3B, M6BP	0.4	23
M4B, M8BN	1	16.7
M6B	0.955	1.65
M8B	0.99	3.72

Table 5.12. Op-amp performance summary.

Bias Current (µA)	**10**	**20**	**30**	**40**	**50**	**60**	**65**	**70**
DC gain (dB)	47.33	47.77	47.77	47.45	46.9	46.21	45.7	45.31
g_m (mA/V)	1.56	1.45	2.45	3.60	4.01	4.58	5.20	5.48
Phase margin	62.20	63.30	63.55	64.10	64.20	64.40	64.50	64.60
Io (µA)	87.2	185.70	286.60	389.00	491.00	596.00	647.00	698.00
Output swing (V)	±0.9	±0.8	±0.73	±0.67	±0.61	±0.56	±0.53	±0.50
Input cap. (fF)	322	320	332	343	347	354	359	362
Output cap. (fF)	28	27	23	20	18	17	16	15
Power (mW)	0.64	1.17	1.80	2.03	2.50	2.95	3.14	3.37

5.5.3 Capacitors

Due to the better capacitor density and lower cost, MOM capacitors have been used in all the integrators and adder. These capacitors rely on the coupling capacitance between the interdigitated metal fingers as shown in Figure 5.28. The metal fingers can be stacked to increase the capacitance density. Another benefit associated with MOM capacitors is lower bottom-plate parasitic capacitance (less than 5 %) compared to the standard MIM capacitors.

B=Bottom Plate
T=Top Plate

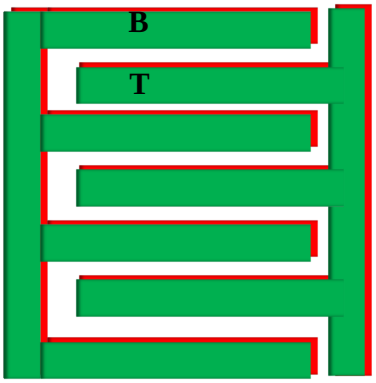


Figure 5.28. Arrangement of top and bottom plates in MOM capacitors.

A complete list of capacitors required for different integrators and adder have been summarised in Table 5.5. The unit MOM capacitor employed is 50 fF. Therefore, the total number of unit elements required for the differential implementation of the modulator (based on the capacitance requirement from Table 5.5, including 4 integrators and an adder) is 2×305. In order to see the impact of mismatches, Monte Carlo simulations were performed with 0.15 % standard deviation of mismatches in coefficients which shows 1.5 dB deviations in achievable SNDR over the whole range of notch frequencies.

A common-centroid technique has been employed for the layout of all the capacitors in the integrators and adder. Dummy capacitors have been extensively used to ensure similar surroundings for each unit capacitor. As an example, Figure 5.29 illustrates the unit capacitor arrangement of the 3rd integrator. In this figure, C_i represents the integrating capacitor while C_{s1} to C_{s4} shows the 4 sampling capacitors. Dummy capacitors are represented by DU.

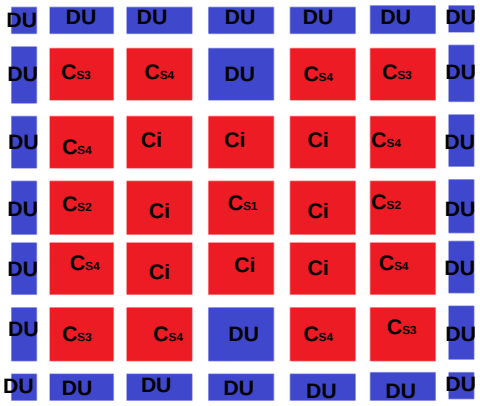


Figure 5.29. Common centroid arrangement of capacitors in 4th integrator.

5.5.4 Switches

Standard CMOS transmission gates have been utilised as switches. Two important factors considered for switch design are the Switch-ON resistance (R_{ON}) and the non-linearity of the input sampling switches. R_{ON} can severely affect the dynamics and transient response of the SC integrators [132][133]. The non-linearity of the input sampling switches may cause the dynamic distortion at the output of the modulator. This impact becomes worse when operating at higher notch frequencies [134].

Behavioural simulations reveal that a switch with an R_{ON} with a mean value of 150 Ω can be tolerated in the first, second and third integrators. The 4th integrator and adder have more relaxed requirements in terms of R_{ON} (i.e. 300 Ω). Also, a ratio of 3.125 between the PMOS and NMOS transistor widths leads to a resistance plot centred on the common-mode voltage 0.6 V. The resulting transistor sizing and the corresponding electrical simulation results are summarised in Table 5.13.

Table 5.13. Transistor sizing of switches of the different integrators and adder.

	First, Second and Third Integrator	4th Integrator	Adder
Width PMOS (μm)	12	6	
Width NMOS (μm)	3.84	1.92	
Length PMOS, NMOS (nm)	80	80	
R_{ON} (Ω)	147	285	
Cdd (fF) Css (fF)	30.63	15.46	

5.5.5 Comparators

Dynamic comparator architecture composed of three blocks, pre-amplifier, regenerative latch and set-reset (SR) latch, has been utilised in the modulator. This comparator presents very appealing features of high-speed, low power consumption and low offset. Figure 5.30 (a) and (b) presents the schematics of the pre-amplifying stage and the regenerative latch of the comparator, respectively.

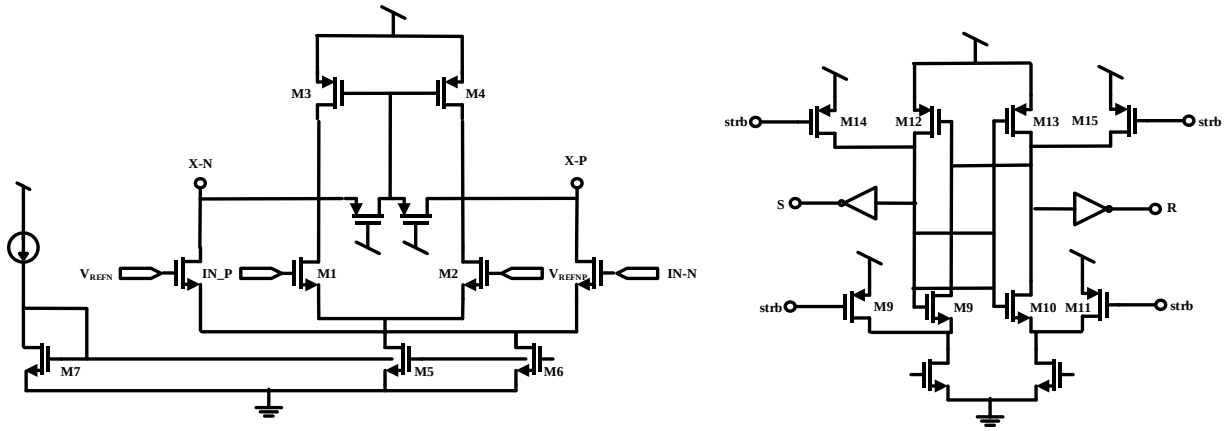


Figure 5.30.Comparator schematic (a) Pre-amplifying stage (b) Regenerative latch.

5.5.6 Quantiser

The quantiser has a differential flash architecture and can be divided into three parts as depicted in Figure 5.31 [135]. First part consists of a resistor ladder generating the voltage references for individual comparators while the second part consists of an array of comparators that compares the adder output with the reference voltages generated in the resistor ladder. The third part of ADC consists of digital logic that translates the thermometer code at the output of comparators. The delays of all the digital paths are balanced with buffers (not shown in the figure).

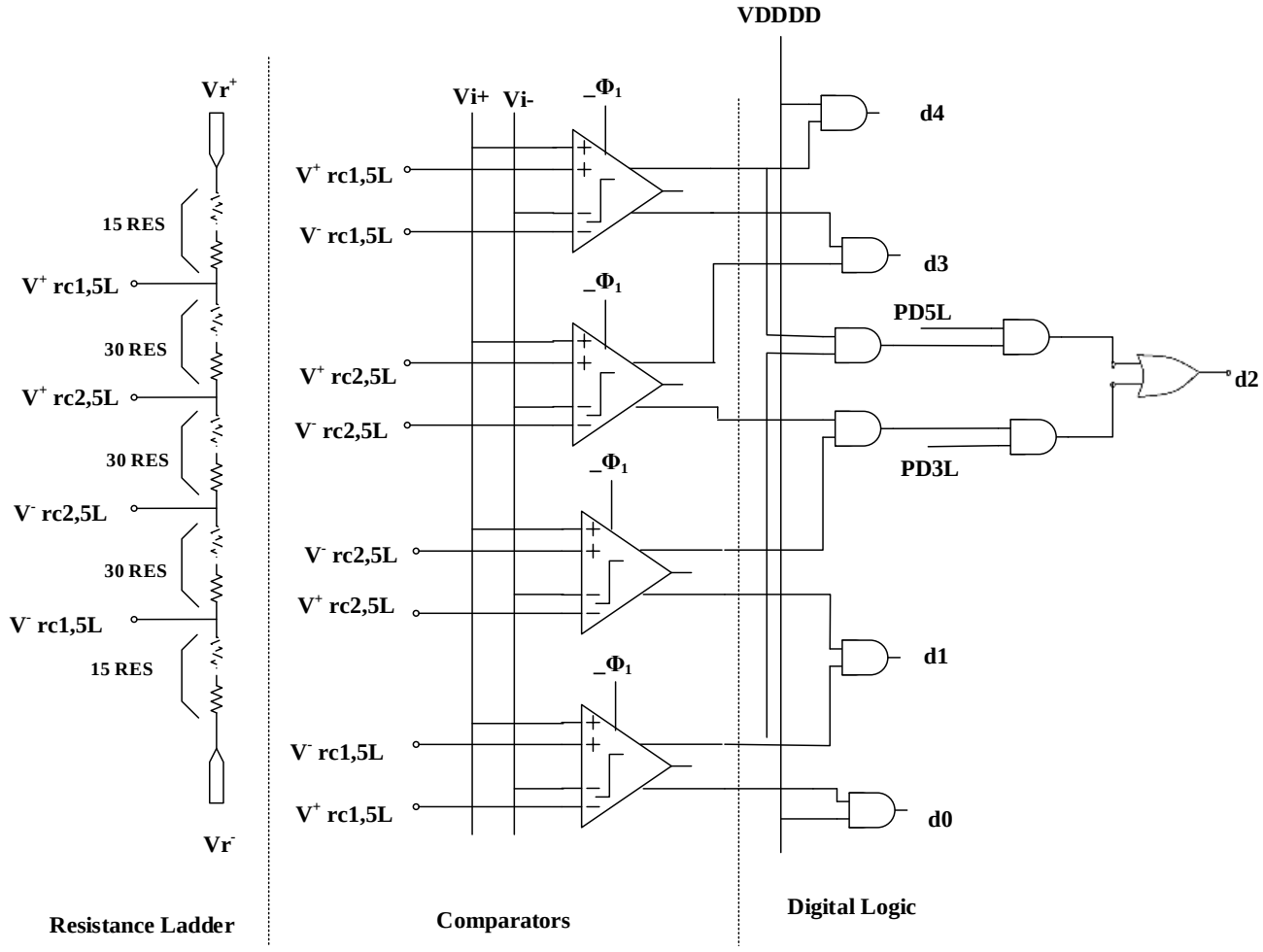


Figure 5.31. Resistance ladder, quantiser and digital logic.

5.5.7 Biasing Circuit

The biasing circuit is composed of two stages. The first stage replicates the externally fed current. The output of the first stage mirror is connected to 9 units of second stage mirrors. Each of these current mirrors consists of four branches which are controlled by an externally provided digital control word. Depending upon the control word, each unit mirror can provide the current in the range of 10 µA to 100 µA. Figure 5.32 shows the schematic of the first and second stage mirrors. The transistor sizing is given in Table 5.14.

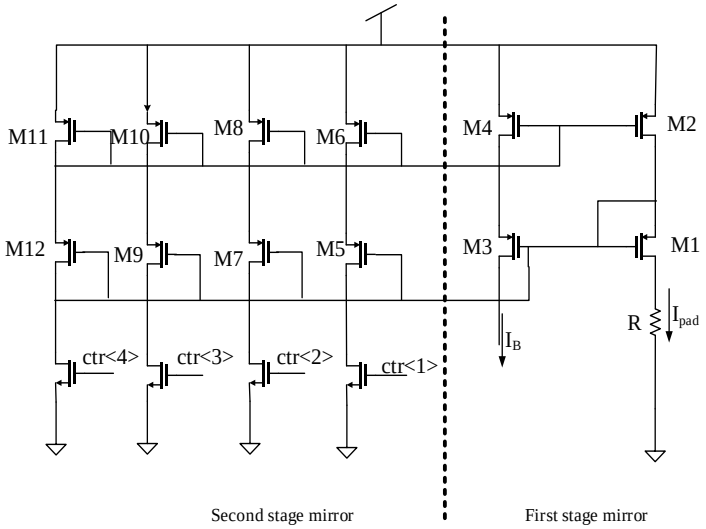


Figure 5.32. Master biasing circuit.

Table 5.14. Transistor sizing of current mirror.

	W (µm)	L(µm)	Number of fingers	W_{Total} (µm)
M1	2.5	0.5	2	5
M2	0.625	0.5	2	1.25
M3	0.625	0.5	8	5
M4	0.625	0.5	2	1.25
M5	5	0.5	1	0.5
M6	1.25	0.5	1	1.25
M7	5	0.5	2	10
M8	1.25	0.5	2	2.5
M9	5	0.5	3	15
M10	1.25	0.5	3	3.75
M11	5	0.5	4	20
M12	1.25	0.5	4	5
MC	1	0.2	1	1

5.5.8 Clock Generator

Figure 5.33 depicts the schematic of the clock phase generator used to generate the non-overlapping clock phases ϕ_1, ϕ_{1d}, ϕ_2, ϕ_{2d} [136][137]. Standard cells from the digital technology library have been used extensively in the design of clock generators. The output of the clock generator is passed through a series of buffers before being fed to other blocks. The integration and sampling operations in the ΣΔM are controlled by these clock phases (and their delayed i.e. ϕ_1, ϕ_{1d}, ϕ_2, ϕ_{2d}).

5.5.9 Auxiliary Blocks

The auxiliary blocks include the DAC and serial-to-parallel register. All these blocks have been designed with the digital cells from the technology libraries.

Figure 5.34 shows the digital gates used to binary encode the quantiser digital outputs Y<1:4> to generate the P<1:4> and the N<1:4> control signals that control the DAC operation through the feedback switches.

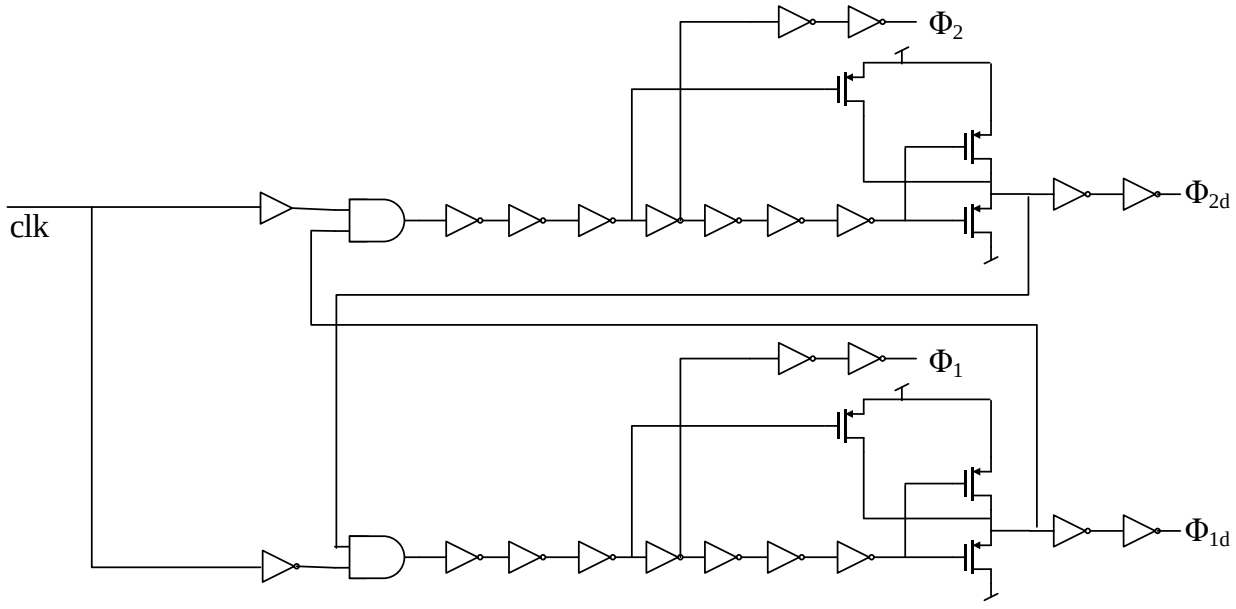


Figure 5.33. Clock phase generator schematic.

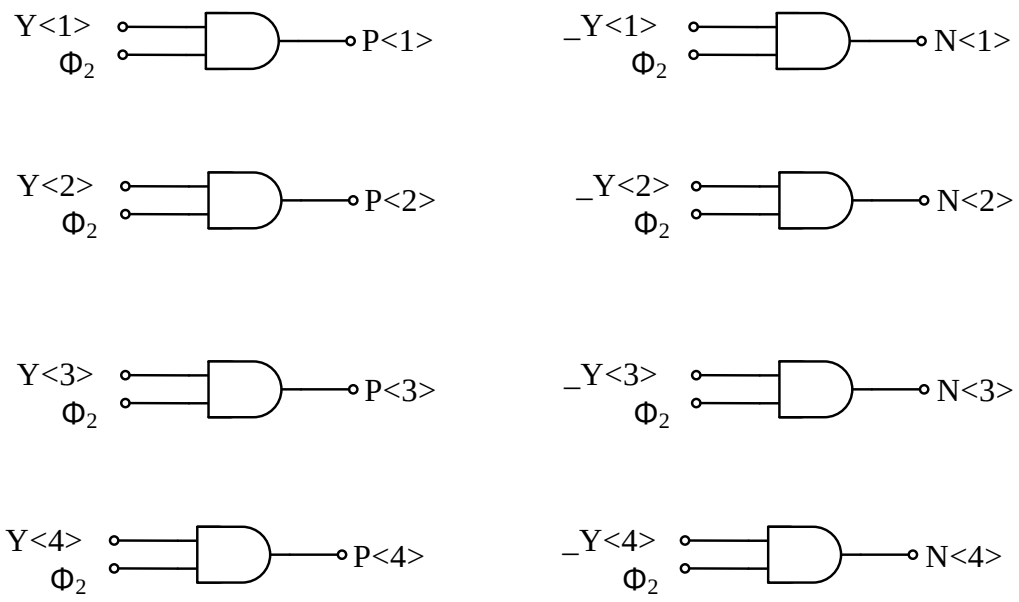


Figure 5.34. DAC control signals configuration.

The reconfiguration of the modulator coefficients and biasing requires a specific combination of control signals. In order to cope with this, a serial-to-parallel register is used [135]. It is designed by connecting several (76) D flip-flops in series, this register can be loaded with a specific control word (used to realise the specific SC ratios and biasing etc.). The block diagram of the register is depicted in Figure 5.35.

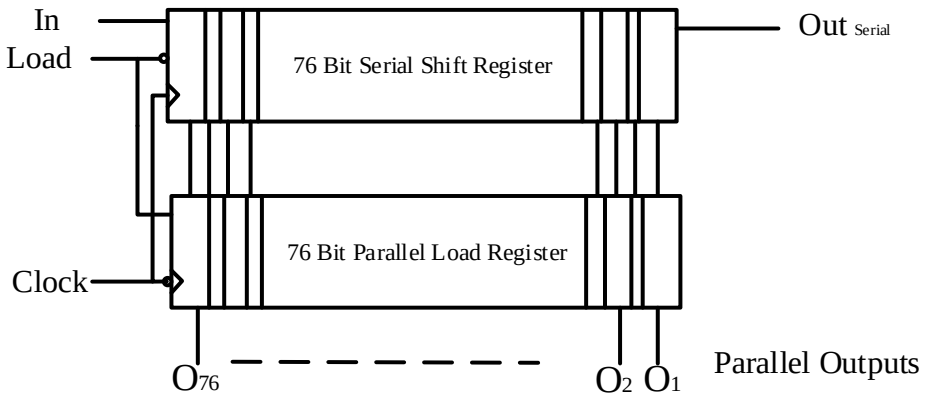


Figure 5.35. Block diagram of the serial-in parallel-out register.

The clock signal, “Clock”, functions as the input clock for the flip-flops of the register in the serial shift register block. While another input signal, “Load”, enables either the shifting operation in the top register or the loading in the bottom register, as illustrated in Figure 5.35. The serial input data, “In”, is collected and transformed into 76 parallel control bits, “O_1-O_{76}”.

Table 5.15. Functionality of control signals.

Index	Signal name	Description
1..4	ctr_biasCM<1:4>	Biasing of CM
5..8	ctr_oa1<1:4>	Biasing of first op-amp
9:12	ctr_oa2<1:4>	Biasing of second op-amp
13..16	ctr_oa3<1:4>	Biasing of third op-amp
17..20	ctr_oa3<1:4>	Biasing of fourth op-amp
21..24	ctr_add<1:4>	Biasing of Adder
25..28	ctr_comp<1:4>	Biasing of comparator
29..32	ctr_test<1:4>	Biasing of test circuit
33	PD3L	3 Level quantiser activation
34	PD5L	5 Level quantiser activation
36	PD_gen	Quantiser master enable
37..41	D_g1<1:5>	First resonance
42..45	D_int2<1:4>	Second integrator sampling
46..50	D_g1<1:5>	Second resonance
51..54	D_int3<1:4>	Third integrator sampling
55..58	D_int4<1:4>	Fourth integrator sampling
59..63	D3<1:5>	Adder control
64..68	D4<1:5>	
69..73	D5<1:5>	
74..76	SIG_CON<3:5>	

5.6 Layout Design

Figure 5.36 illustrates the layout of the ΣΔM where the different blocks are highlighted.

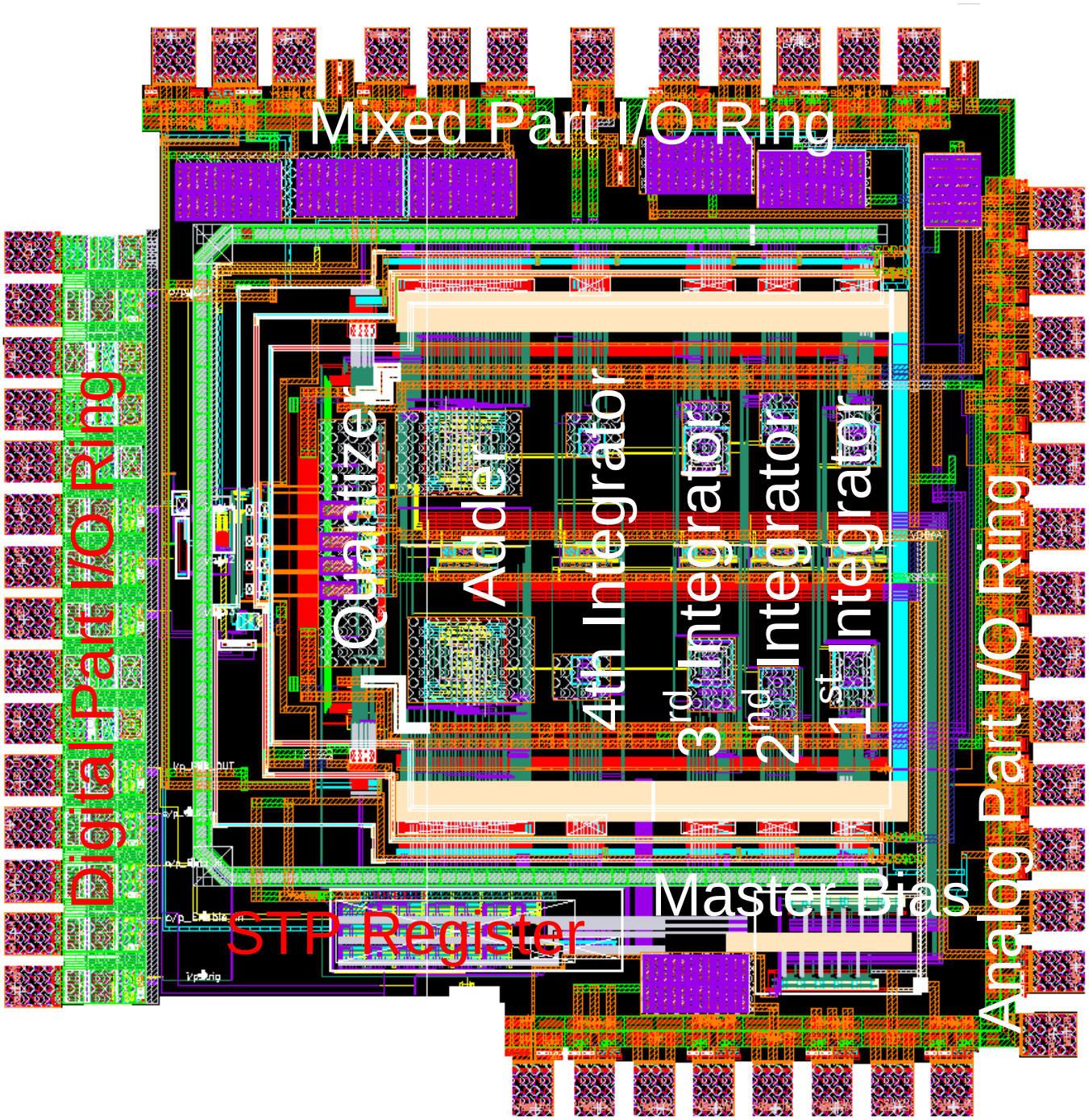


Figure 5.36. Layout of whole ΣΔM ADC with different blocks being highlighted.

Depending upon the switching activity and functionality, the whole modulator can be considered as made up of three different sections. The analog section consists of the op-amps, capacitors, pre-amplifiers of the comparators and the master bias circuitry. The mixed-signal section consists of switches (of the integrators and the analog adders), the regenerative latches of the comparators and the buffers of the clock phases. The digital section consists of the digital gates, ROM, the digital logic of DAC and serial-to-parallel register. All these sections are provided with distinct power and ground supplies from the I/O ring. In order to avoid noise coupling that result from bulk sharing, guard rings have been employed across these three sections.

The I/O ring consists of two types of cells. Full custom cells are used for the analog and mixed signals and power supplies. High speed digital signals e.g. control bits, clocks and digital output bit stream use the I/O cells from the digital library. The fast switching part of the I/O ring is placed as far as possible from the other sections. In order to avoid the switching coupling noise, the analog and the mixed signals part of the ring is physically separated from the digital part of the I/O ring, as shown in Figure 5.36.

5.7 Experimental Characterization

The ADC is fabricated in a 90-nm 1P8M CMOS 1.2 V process and has an area of 3.515 mm^2 (1875μm × 1875μm). A micrograph of ADC is shown in Figure 5.37 .

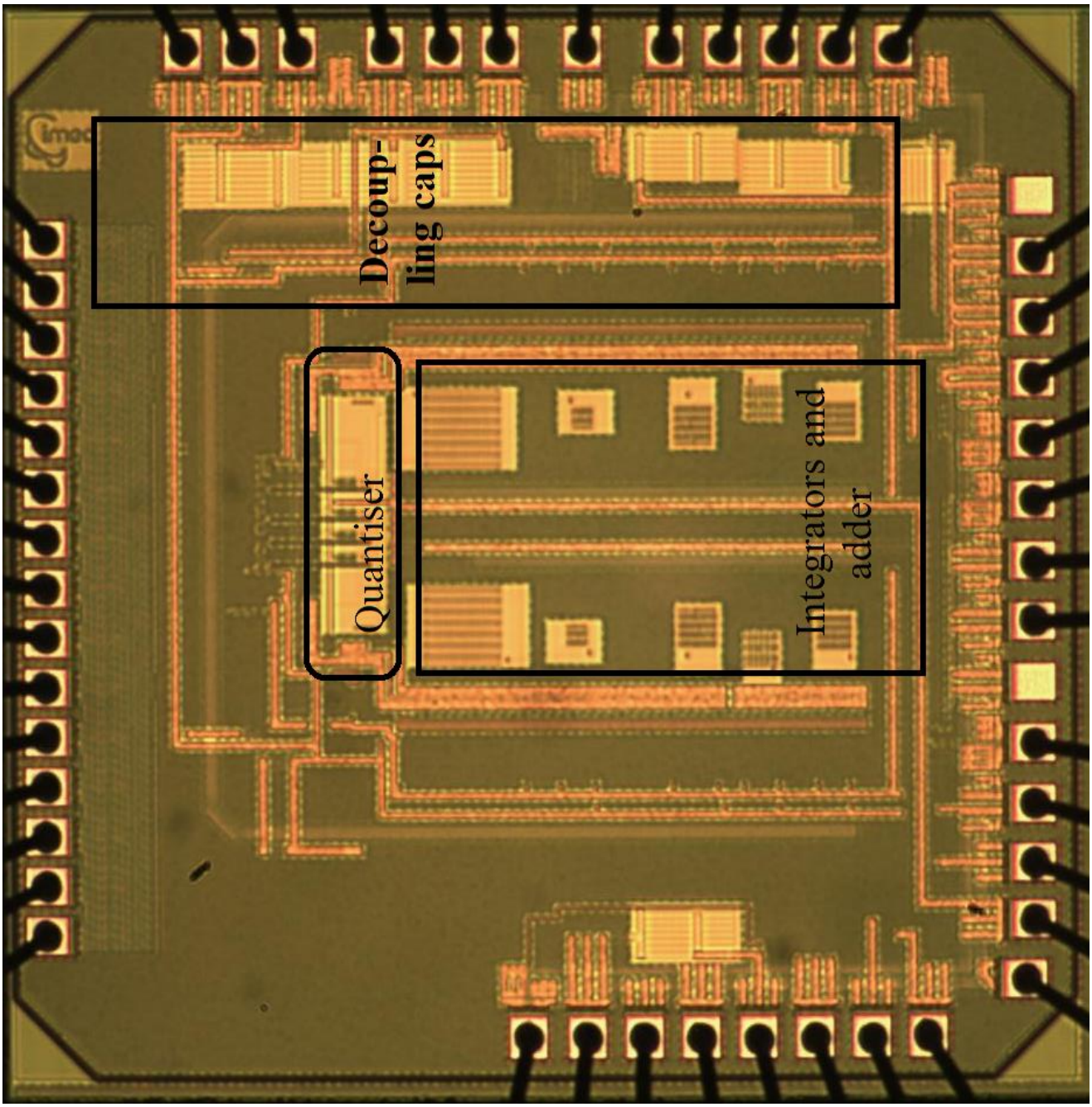


Figure 5.37. Micrograph of the fabricated ADC.

5.7.1 Test PCB

The test printed circuit board (PCB) schematic is shown in Figure 5.38 and a photograph is depicted in Figure 5.39. The following considerations highlight some of the test PCB aspects:

1. The input signal is generated from an external source (fully differential low-distortion external source Tektronix SG5010 audio oscillator) and provided to the PCB via an SMA connector. After being applied, the input signal is filtered by a passive RC antialiasing filter on the PCB. A set of capacitors and 50 Ω resistors are used to realise this filtering function.
2. The PCB applies the external voltage of a 2.5 V supply required for the I/O devices and a 1.2 V supply required for the internal circuitry of the chip.
3. The CM voltage is generated on chip but there is also provision to apply an external CM. To this purpose, a buffer and the footprint of a 0 Ω resistor has been included on the PCB.
4. All the on-chip supplies, references etc. are passed through the passive low-pass π filters mounted on the PCB before their connection with the chip. Each π filter consists of two capacitors and one inductor.
5. Different jumpers, test points and 0 Ω resistors have been extensively mounted over the whole PCB to measure the currents and voltages at different test points.
6. Decoupling capacitors have been used between all the power supplies, references, grounds, and CM etc.
7. There is also a provision for the logic-analyser connection that is used to collect the output bit stream for the processing.
8. The PCB has 4 layers with separate ground and power planes.

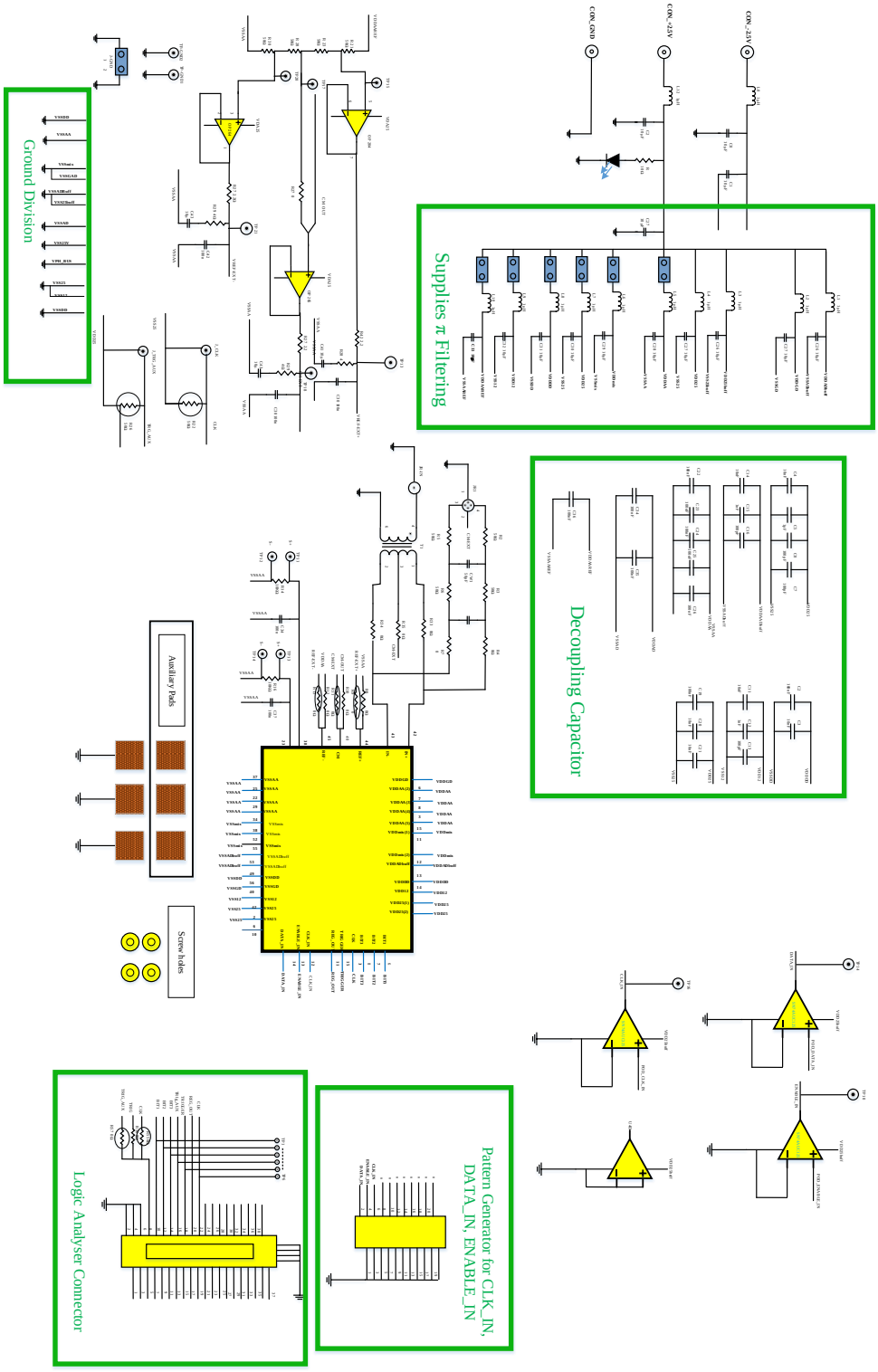


Figure 5.38. Test PCB for the evaluation of the ADC.

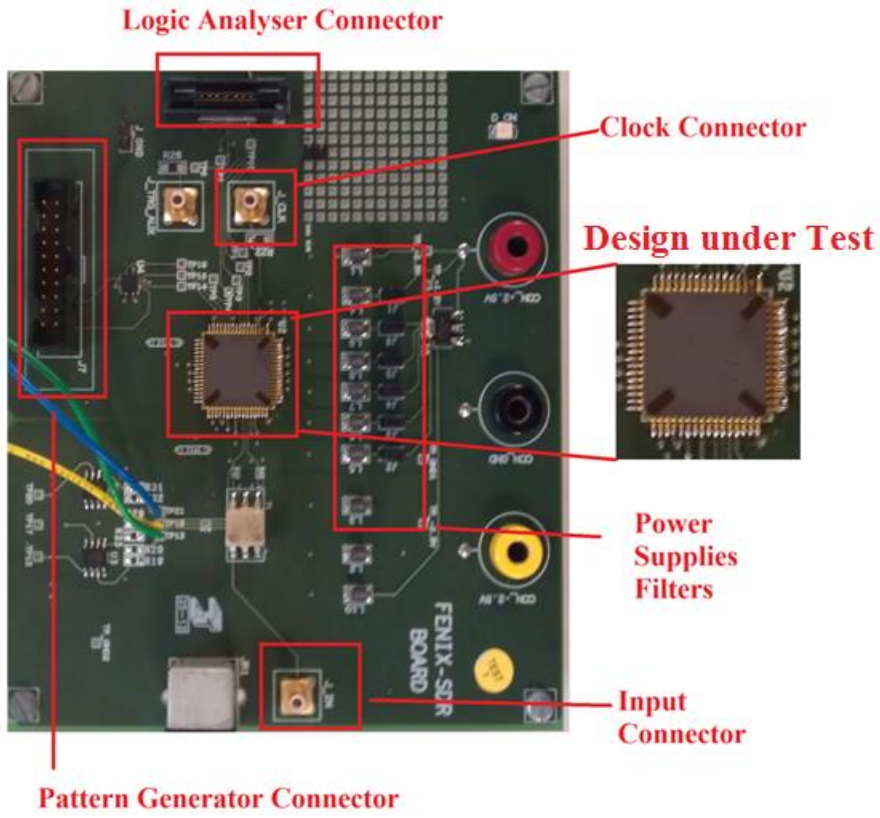


Figure 5.39. Photograph of the test PCB.

5.7.2 Experimental Results

The experimental verification of the 4th-order DT CRFF-based ΣΔM has been carried out over the various notch frequencies. In the first step of the characterization plan, a pre-selected control word (generated by pattern generator) is loaded into the serial-to-parallel register of the ADC. This control word sets the reconfigurable coefficients and biasing of op-amps for a particular notch. The same control word is available at one of the outputs of ΣΔM to verify that it has been loaded accurately. Once the control word is correctly written to the register, an input tone can then be applied. By using single tones of different frequencies and strengths, the modulator performance has been validated. The output of the modulator consists of a 3-bit word that is captured by the logic analyser and subsequently processed in Matlab®.

Using the protocol described above, the modulator has been tested for full range of notch frequencies.

The experimental level characterization revealed the correct operation of the modulator over the f_N range of DC-to-18 MHz while operating at a sampling rate of 100 MHz. Figure 5.40 to Figure 5.46 depict the signal spectrum of the digitized output at the different notch frequencies while operating at a sampling rate of 100 MHz. Figure 5.47 plots the measured SNDR as a function of the input level for different single-tone inputs over the whole tuneable range (DC-to-18 MHz) for a bandwidth of 1 MHz. Table 5.16 summarises the experimental results of the modulator.

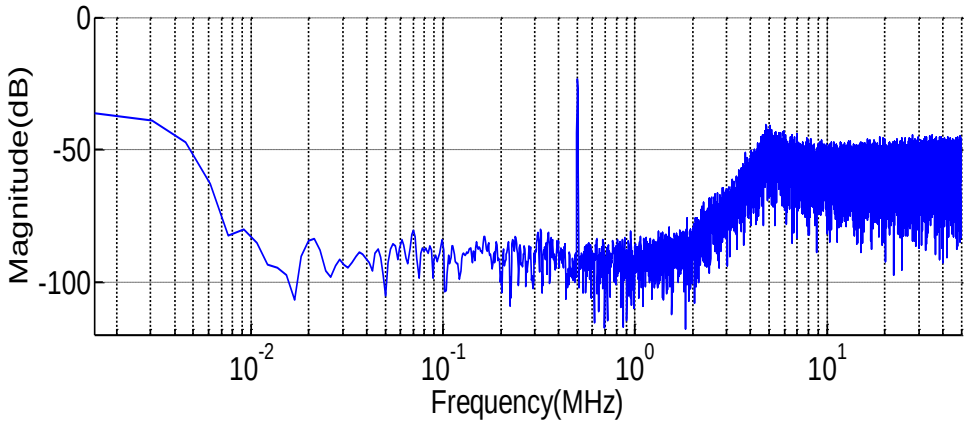


Figure 5.40. Spectrum plot for LP configuration.

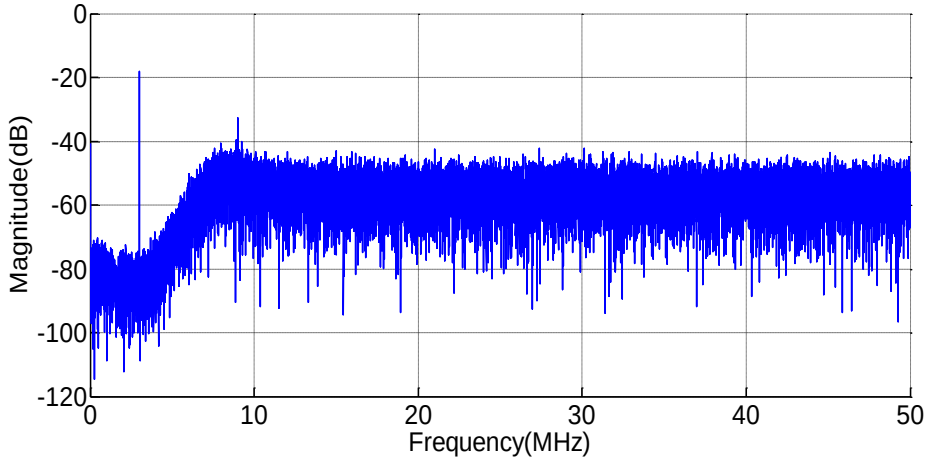


Figure 5.41. Spectrum plot at f_N = 3 MHz.

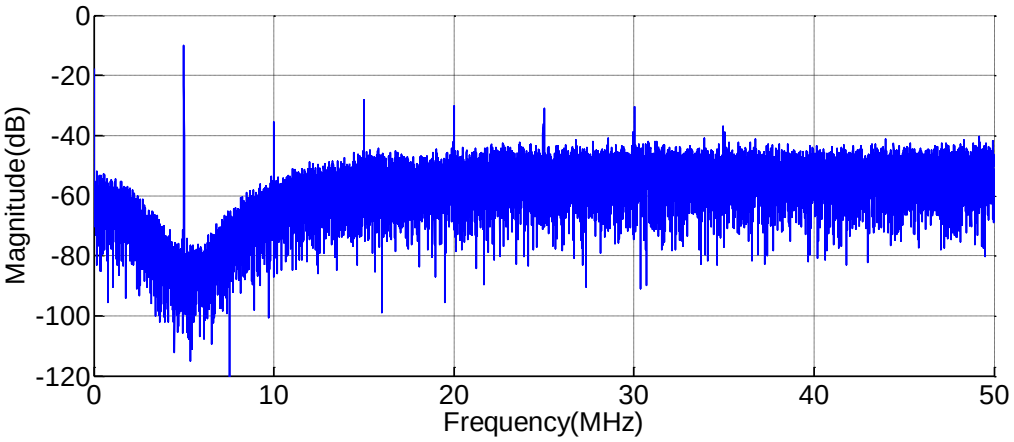


Figure 5.42. Spectrum plot at f_N = 5 MHz.

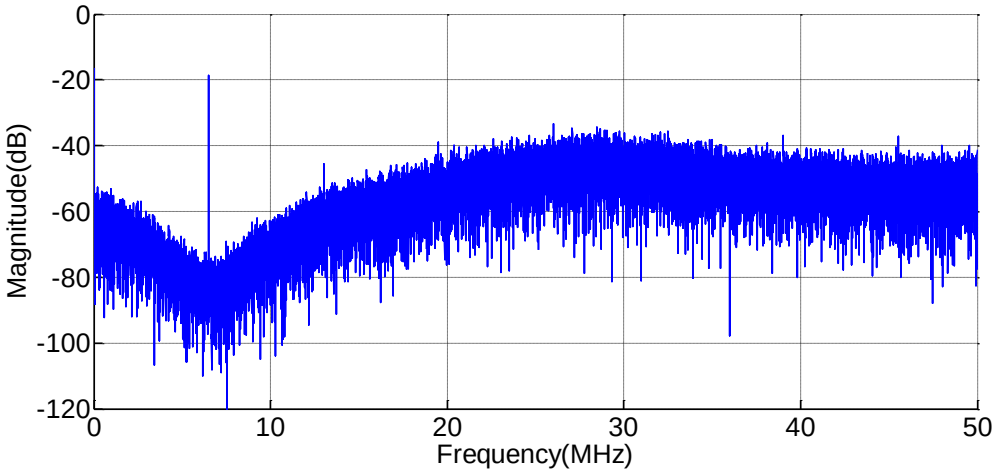


Figure 5.43. Spectrum plot with f_N = 6 MHz.

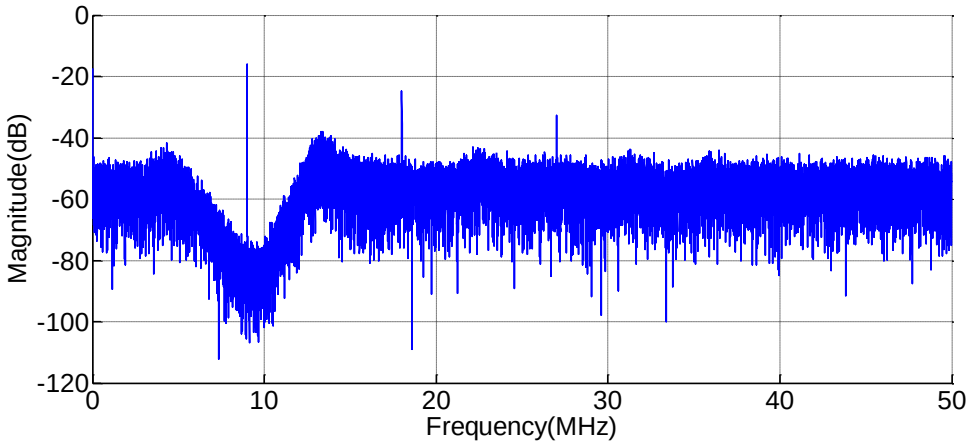


Figure 5.44. Spectrum plot at f_N = 9 MHz.

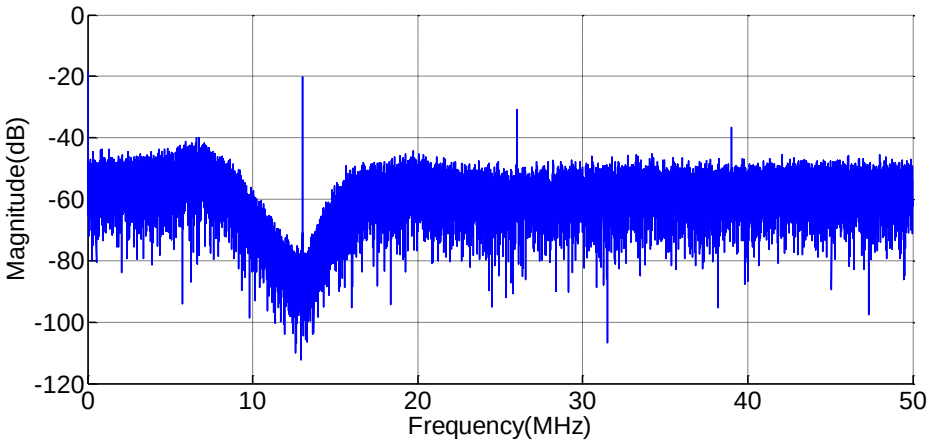


Figure 5.45. Spectrum plot at f_N = 13 MHz.

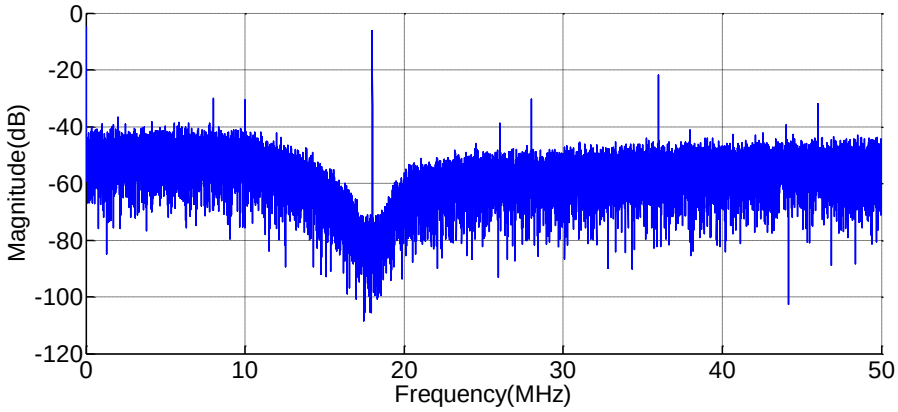


Figure 5.46. Spectrum plot at f_N = 18 MHz.

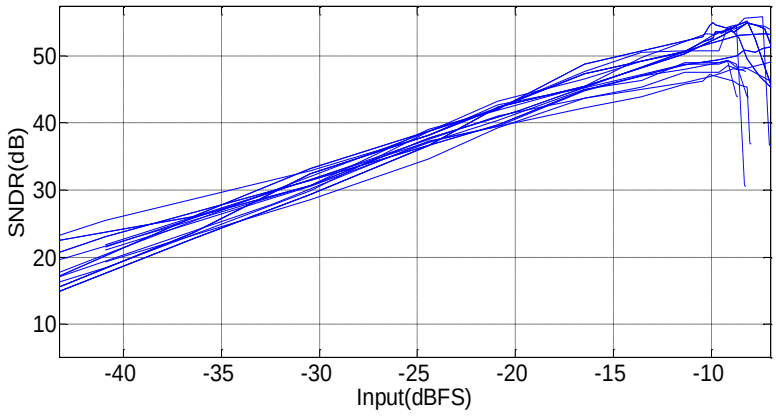


Figure 5.47. SNDR vs. input for a BW of 1MHz at f_N = 100 kHz-to-18 MHz.

Table 5.16. Performance summary of the designed ADC

Process		90-nm
Active Area (mm^2)		2.97
f_S (MHz)		100
BW (MHz)		1
Notch Frequency (MHz)		0-to-18
Supply Voltage (V)		1.2
OSR		50
Peak SNDR (dB)		46-to-55
Power Consumption	Analog	10-13 mA
	Mixed	7-8 mA
	Digital	2-3 mA

Although the circuit level simulations revealed the correct operation of the modulator over the whole range of notch frequencies, experimental level characterization have shown the correct operation of modulator up to a f_N of 18 MHz only while operating over a sampling rate of 100 MHz. Three possible reasons for the performance degradation are summarised in the following.

1. Variable coefficients required for the f_N tuneability, have been implemented with the reconfigurable capacitor ratio, which are realised with the switched capacitor branches. Parasitic capacitances introduced due to the routing and interconnection of the capacitors disturb the capacitors ratio (or coefficients) resulting in the degradation of the NTF. Due to unavailability of the layout-parasitic extractor for the design kit, the parasitic impact was not fully evaluated at the post-layout level during the design phase. Hence the routing and the interconnections were not optimised that led to the degraded performance at experimental level.
2. The post-layout performance of the op-amps was not evaluated during the design phase. Op-amps transconductance, DC gain and slew rate get degraded due to parasitic. Transconductance requirements for the higher notch frequencies are much

higher. Therefore, the experimental level characterization has shown correct results up to 18 MHz only while operating at 100 MHz. Moreover, due to the degraded DC gain, zeros in the NTF are disturbed that causes increased noise in the signal band. As a result, the achievable performance was lower than the expected.

3. No DEM has been implemented for 5 level feedback DAC. One consequence of this can be observed in the simulated spectra (Figure 5.40 to Figure 5.46). The non-linearity in the DAC caused the signal harmonics and higher in-band noise.

Table 5.17 compares the experimental results of the modulator with some other notable examples of BP or reconfigurable LP/BP ΣΔMs. Compared to the previously reported SC-based ΣΔM ADCs ([123][138][139][140]) the designed ADC achieves a higher tuneability range. Over the recent years, there has been a surge in CT implementations with tuneable notch. Three of the notable recent continuous time implementations with a tuneable notch frequency are reported in [96] [142] and [17]. The architecture reported in [96] employs a duty-cycle controlled DAC in the feedback for better reconfiguration of notch frequency that can be varied over a range of 180-to-220 MHz. [142] is a quadrature ΣΔM and can achieve a notch tunability of 0.5-to-12 MHz. The architecture detailed in [17] employs 3rd order CT architecture that can operate in LP or BP mode. Due to CT implementations of these three architectures, power consumption and hence resultant FoMs are much lower. Another important architecture is [15]. This is a reconfigurable architecture that can operate either in LP mode in BP mode. Also, a few reconfigurable receiver architectures operating in GHz range featuring SC-based ΣΔM ADCs have been reported recently [89][145]. These architectures first down-convert the incoming signal using a variable oscillation frequency and then a LP ΣΔM ADC digitizes the baseband signal. The designed ADC employs a single sampling frequency to digitize the range of input frequencies.

Table 5.17. Comparison of the designed ADC with other reported BP or reconfigurable BP ΣΔM ADCs

	Arch.	**f_S (MHz)**	**f_N (MHz)**	**BW (MHz)**	**SNDR (dB)**	**Power (mW)**	**FoM_W (pJ/conv)**	**FoM_S (dB)**
[138]	SC	1	0.1-0.40	0.00781	61	200	13965	106.91
[123]	SC	40	0-12.60	0.31	71-81	115	63-20	135.90-145
[139]	SC	42.8	10.70	0.2	42.3	12	282	114.51
[140]	SC	37.05	10.7	0.2	76	88	42.66	139.52
[141]	SC, TI	200	50	10	45.7	2	0.64	142.68
[96]	CT	800	180-220	25	69	35/36	0.303/312	157.53/157.7
[142]	CT, Quadrature	51.2/120/200	0.5-12	0.27/5/8	81/61.2/60.9	4.8/8.9/12.1	0.99/0.95/0.084	158.50/168.49/169.20
[17]	CT	180/320	0 4–6	5-/10 5-/10	62.9-/64.1 65.1-/62.2	3.1/4.8/4.2/6.3	0.21/0.23/0.36/0.24	165.1/165.1/159.1/166.2
[15]	CT	2000	10, 504	90	54.3/41.4	45	0.058/2.60	147.30/134.25
* [89]	SC	1776	1776+1kHz	10/20/40	45–52	35.5–53.0	--	
** [145]	SC	400-4000	400-4000	4/10	60-68 52-65	17-70.5	--	
This work	SC	100	0-18	0.2/1/2	45-64	22.8-28.8	44.01-49.55	123.41-133.43

* The architecture is a whole receiver chain with channel select SC ΣΔM ADC. Power consumption given in the table is for the whole receiver chain. ** This architecture is a downconversion SC ΣΔM ADC. Power consumption given in table is for the whole receiver chain. *** FoM_W is either taken from the published article or calculated using

5.8 Conclusion

This chapter described the architectural level exploration and the circuit level implementation of a 4th-order CRFF variable f_N low-pass/band-pass ΣΔM ADC. Starting from the coefficient synthesis of the modulator, the circuit level design and the implementation of the modulator were presented. The experimental results proved the correct operation of the

modulator over f_N range of 0-to-18 MHz while operating at 100 MHz sampling rate. The presented chip has been included as a proof of concept of the techniques proposed.

Chapter 6: Design of a 12-Bit SAR ADC with Improved Linearity and Offset for Power Management ICs

6.1 Introduction

PMICs generate, manage, control and distribute stable power supply voltages to other circuits and chips in the electronic systems. Due to the growing complexity of electronic systems, PMICs have evolved into a far more sophisticated system than a simple power supply to support multiple power domains etc. Important features of these ICs are to sense the different voltages and currents and in-built "intelligence" to make functional decisions and interface effectively with other blocks [146]. Furthermore, these ICs need to be integrated within the overall system design for high efficiency [146].

This chapter focuses on the practical design and implementation of a 12-bit SAR ADC in 0.13 μm CMOS 1.2/3.3V technology to enable the digital controller of DC/DC converters in the PMICs. A general description of the ADCs employed in PMICs is presented in section 6.2. The performance specifications and architectural-level exploration of the targeted ADC are also described in the same section. Based on the architectural-level study, a SAR ADC is selected for the final implementation. The basic concepts of SAR ADC and different design considerations are discussed in sections 6.3 and 6.4, respectively. The linearity analysis of SAR ADC is presented in section 6.5. The proposed ADC architecture is detailed in section 6.6. The circuit level design of the switches and custom MOM capacitors are also discussed in the same section while section 6.7 is dedicated to the DAC segmentation explanation. Section 6.8 describes the comparator design and the offset removal techniques. The ADC layout is shown in section 6.9. Finally, section 6.10 describes the test setup and measured results of the fabricated ADC.

6.2 ADCs for Controller of DC/DC Converters of PMICs

With the introduction of more sophisticated electronic systems, the complexity of the PMICs has also increased. Different blocks on a single die require multiple voltages and currents for their proper operation. This trend has put more stringent requirements on the different blocks in the PMIC, specifically, the output power management unit which is responsible for the generation of different voltage levels as shown in Figure 1.3. This unit primarily consists of a DC/DC converter and a controller. In recent years, there has been a surge in digitally controlled DC/DC converters. Digital controllers have more programmability when compared to their analog counterparts, which enables the implementation of more advanced control and calibration algorithms at a system level [19]. Figure 6.1 illustrates a simplified block diagram of a typical digital controlled DC/DC converter. The controller consists of an ADC, a digital subtractor, a digital compensator, and a digital pulse width modulator (DPWM). The ADC digitizes the output voltage (V_{OUT}). Based on the ADC output, $V_{OUT}(n)$, and the reference voltage, V_{REF}, the digital subtractor generates an error signal (e(n)). Subsequently, based on e(n), the digital compensator and the DPWM produce the control signal for the power transistor that can be turned ON or OFF which effectively achieves the voltage regulation.

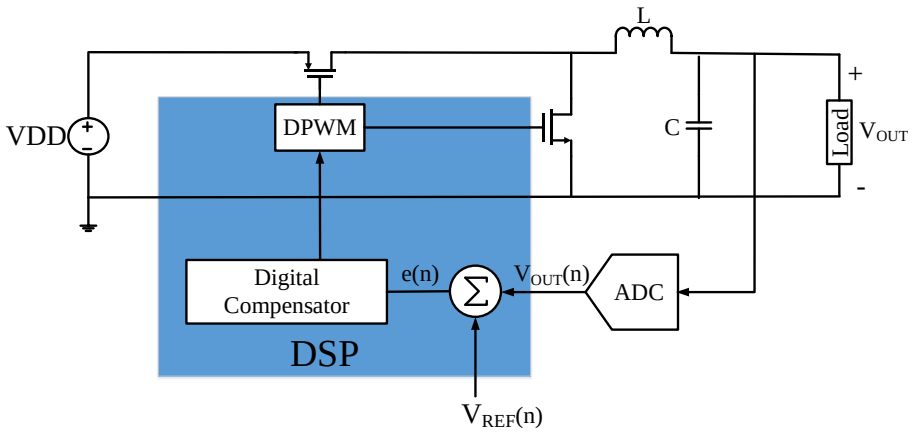


Figure 6.1. A digital controller of DC/DC converter with ADC.

In these controllers, the ADC is a key building block. In addition to the digitization of V_{OUT}, the ADC is also employed for the monitoring of various housekeeping signals e.g. output of temperature sensor etc. [19]. The specifications of such ADCs are different compared to the conventional signal processing ADCs. One important characteristic of such an ADC is to digitize signals which are higher than the core supply voltage. The input signals of the ADC are either error signal i.e. difference of output regulated voltage and reference voltage, or sensors outputs. Therefore, due to the DC nature of these signals, the DC specifications of these ADCs e.g. DNL, INL, gain, offset and monotonicity are of more concern. These ADCs are used in the feedback path of the digital controllers. Hence, latency and monotonicity are the two most important features. Furthermore, these ADCs are required to digitize multiple inputs; therefore, a multiplexer may be needed as well.

6.2.1 Design Goals Overview

The targeted ADC is going to be used as a part of the power management controller. The ADC must provide fast feedback to a closed loop of the current/voltage sensors (multiplexed). Furthermore, the ADC needs to attend to multiple sensors in future up to 8 lines through multiplexed inputs. Also, the ADC will be used to monitor 1.6 V single-ended signals with respect to noisy ground ($3.2V_{pp}$ differential). Therefore, a major design challenge is to reduce the external capacitors employed for the voltage scaling. In the targeted application, the area specified for ADC is 0.25-to-0.5 mm^2, while the power budget for ADC is 2-to-3 mA. Table 6.1 summarises the target specifications of the required ADC.

Table 6.1. Required specifications of the targeted ADC.

Specification	Value	Notes
Resolution	12-bit	ENOB ≈ 11 bits
ADC latency	<1 μs	
Sampling/Throughput rate	1-to-2 MS/s	
Area	0.25-0.5 mm^2	
Current consumption	2-4 mA	
Input voltage range	0V -1.6 V	.
DNL	±1 LSB	At 11-bit
Offset error, Gain error	< 1LSB, <0.5 LSB	
Resolution with respect to input BW	12-bit from DC-1MHz,	Voltage and Current Sense Signals
Power Supply	1.2 V/2.5 V/3.3 V	TSMC 0.13-μm

6.2.2 Implementation Alternatives

In order to achieve the given set of specifications, different ADC architectures have been considered. One of the straight-forward implementations is a flash ADC. However, the most important limitation associated with the flash architectures is the number of comparators required, which increases exponentially with resolution and hence results in excessively large area and power consumption [27]. Pipeline ADCs are a good alternative to achieve higher than 10-bit resolution, but the complexity of the inter-stage amplifier increases with higher resolution [37].

The SAR ADC is one of the energy efficient ADC architectures [34]. These ADCs can achieve resolutions up to 10-to-11 bits without any need for the calibration [148]. Moreover, considering the digitally driven nature of SAR ADCs and the fact that most of the SAR architectures employ switched-capacitor architectures as the underlying DACs, makes its

implementation in modern CMOS technologies much simpler compared to other Nyquist rate ADCs. Other advantages include the scaling of the resolution and reconfigurability of conversion rate [149][150]. Due to all these advantages, SAR architecture has been selected for the final implementation.

6.3 Basic SAR ADC Operation

A simplified schematic of a conventional N-bit SAR ADC is shown in Figure 6.2. It consists of an S/H circuit, DAC, comparator and digital SAR logic [34]. The conversion process starts with the input signal sampling, following which ADC uses binary search algorithm for the digitization of the input signal. An N-bit ADC requires N number of bit trials which are performed in a binary fashion [35]. During the first bit trial, also known as most significant bit (MSB) trial, the input sampled signal (V_{IN}) is compared against the half of the value of reference voltage i.e. $V_{REF}/2$. The comparator then decides the MSB bit and sets the search region for the next bit trial i.e. MSB-1bit trial.

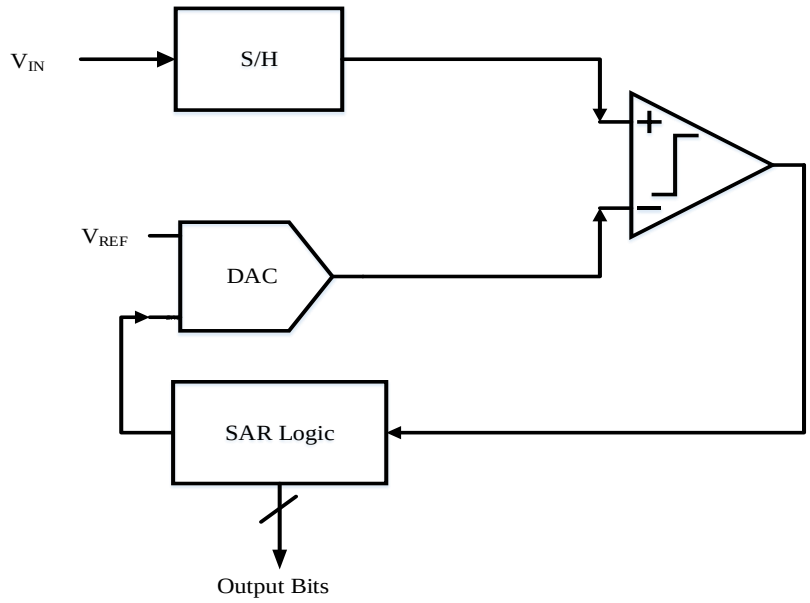


Figure 6.2. Basic SAR ADC.

Based on the MSB result, a quarter of the reference voltage ($V_{REF}/4$) is either added or subtracted from the previously applied reference and is then compared with the sampled input signal. This operation is repeated for the remaining bit trials by adding or subtracting the binary-ratioed reference voltages i.e. $V_{REF}/4$, $V_{REF}/8$ and $V_{REF}/16$ and so on. Let us assume an input of 11.2 V is applied to a 4-bit SAR ADC input having V_{REF} of 16 V. Figure 6.3 explains the above-mentioned search algorithm for this SAR ADC. During the first bit trial, the input is compared against 8 V which is the half of the V_{REF} i.e. $V_{REF}/2$. As the input is larger than this, output of the comparator is 1 and one quarter of full-scale i.e. $V_{REF}/4$ is added to the current value. Hence during the second bit trial, the input is now compared against 12 V i.e. 8+4. As the input is less compared to current approximation, ADC outputs 0 and for the next bit trial $V_{REF}/8$ is subtracted from the current value. Same procedure is repeated for the 4^{th} bit trial. Final digital output from the ADC is 1011 (or 11) that has the quantisation error of 0.2 i.e. 11.2-11=0.2 which is within ±0.5 LSB (LSB = $16/2^4 = 1$).

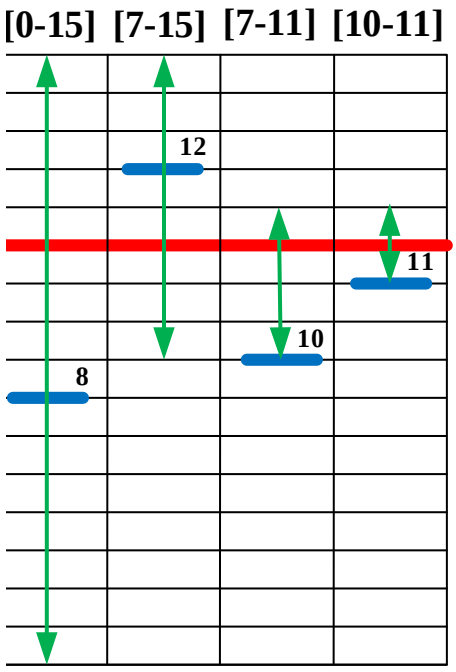


Figure 6.3. 4-bit binary search algorithm in SAR ADC.

6.4 Design Considerations for SAR ADCs

The SAR ADC operation for digitization of the applied input signal comprises three blocks, namely: an S/H, the quantiser or comparator and SAR logic-based DAC. This section examines the different design considerations for these blocks.

6.4.1 S/H Circuit

Figure 6.4 shows a conventional S/H circuit which comprises a switch and a capacitor. During the ON state, known as track mode, the switch is closed, and the input signal gets acquired on the top-plate of the capacitor. During off state, the switch is open, and S/H enters the hold mode. The sampled output voltage on the capacitor undergoes further processing during the bit trial mode.

The S/H circuit design involves some key design considerations which includes thermal noise, sampling period and input signal range. Thermal noise is one of the important factors that can limit the achievable resolution and speed [151]. Typically, the S/H switches are realised using MOSFETs. During the track mode, the MOSFET switch operates in the triode region and behaves like a resistor with a finite ON-resistance (R_{ON}). If the sampling capacitor has a value of C_S, the thermal noise with the MOSFET operating in triode region, is given by [50]:

$$\overline{V}^2_{n,rms} = \frac{kT}{C_S}. \tag{6.1}$$

Where: k= Boltzmann's Constant, and T= Operating Temperature.

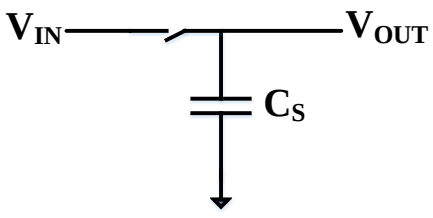


Figure 6.4. A basic S/H circuit.

The quantisation noise is one of the important design parameters of the ADC. For an N-bit ADC with a full-scale voltage of V_{FS}, quantisation noise can be written as:

$$\overline{V}^2_Q = \frac{V_{FS}}{12.2^N}. \tag{6.2}$$

If the thermal noise is considered to be equal to the quantisation noise, the minimum C_S required can be estimated as:

$$C_s = 12kT\frac{12^{2N}}{V_{FS}^{\ 2}}. \tag{6.3}$$

Based on this expression, the C_S required for a specific resolution can be estimated. As an example, for a single standard deviation of noise and a 12-bit ADC with V_{FS} of 1 V, the minimum required C_S is 833 fF.

Another important design consideration is the sampling time. The S/H circuit can be modelled as a simple RC circuit. The resulting required minimum sampling period can be calculated from the time constant of the circuit and LSB of ADC.

For an N-bit ADC, if V_{REF} is equal to V_{FS}, LSB can be written as ([152][153]):

$$LSB = \frac{V_{FS}}{2^N}. \tag{6.4}$$

The time, "t", required for the sampled voltage to settle within a specific fraction (in this case consider 0.25 LSB) of input voltage, can be written as:

$$V(t) = V_{IN}\left[1 - e^{\frac{-t}{\tau}}\right] \tag{6.5}$$

Where τ = Time Constant and V(t) stands for the sampled voltage at a specific time instant "t".

If the input applied voltage is equal to the FS voltage i.e. $V_{IN} = V_{FS}$, the sampled voltage settled within 0.25 LSB of the input voltage for an N-bit ADC can be written as:

$$V(t)_{0.25LSB} = V_{FS}\left[1 - \frac{1}{4\left(2^{N}\right)}\right] \tag{6.6}$$

Substituting $V_{IN} = V_{FS}$ in (6.6), the required time for the settling is:

$$t = \ln\left[\frac{1}{2^{N}4}\right]\tau. \tag{6.7}$$

As an example, for a 12-bit ADC, the number of time constants needed to settle within 0.25 LSB of the input voltage is 9.7. For simplicity it can be approximated as 10. As a summary, for the targeted 12-bit architecture, the sampling window required must be larger than 10 $R_{ON}C_S$ time constants of the sampling network.

The timing jitter in the sampling clock is another important issue that results in aperture error. This error becomes significant as the input frequency increases. The maximum frequency (f_{MAX}) that can be digitized by an N-bit ADC having an aperture error of T_A, is given by [154]:

$$f_{MAX} = \ln\left[\frac{1}{\pi 2^{N+1} T_A}\right] \tag{6.8}$$

As an example, considering 1 ps clock jitter, a 12-bit ADC can digitize up to 388 MHz with full accuracy.

6.4.2 DAC

The DAC is the core building block of SAR ADCs. It generates the various analog levels against which the input signal is compared. From this perspective, the DAC can be thought of as the decisive factor in overall accuracy and linearity of the ADC systems.

Over the years, several DAC architectures have been proposed. Some of the most important architectures include resistive ladder, switched-current and switched-capacitor DACs

[155]-[157]. In modern CMOS processes, the mismatches of resistors are much higher than that of capacitors [158]. Moreover, the area requirement with the SC implementation is drastically reduced compared to the equivalent switched-resistor implementations [158]. Therefore, the majority of SAR ADCs employ capacitive DACs. The most commonly-employed capacitive DAC architectures are conventional binary-weighted (CBW) and binary weighted with attenuated capacitors (BWA) [149][159][160].

6.4.3 Conventional Binary Weighted DAC

Figure 6.5 shows a simplified single-ended schematic of N-bit CBW DAC architecture. The unit capacitors, C_U, here are arranged in a fully binary fashion. Theoretically, capacitance required for an N-bit ADC is $2^N C_U$.

Ideally, the unit capacitor (C_U), must be kept as small as possible to reduce the area and power consumption. However, there are two major factors that determine the size of C_U i.e. thermal noise and static performance.

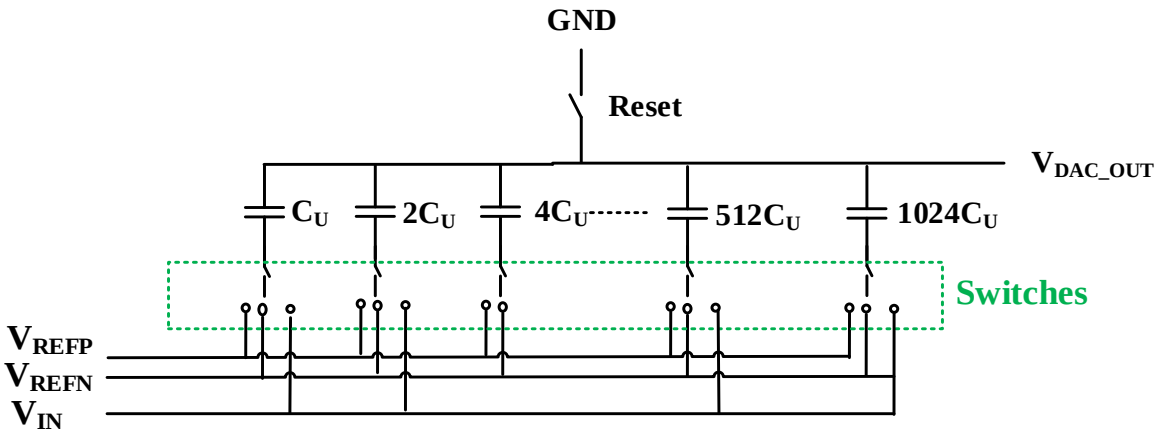


Figure 6.5. A single-ended schematic of CBW DAC.

As an example, the minimum capacitance required to keep thermal noise below 0.5 LSB for a 12-bit ADC can be calculated using (6.3). For a V_{FS} of 1.2V, required capacitance is 833 fF. Therefore, a 12-bit CBW architecture, made up of 4096 C_Us, requires a C_U of 0.2 fF.

The ADC makes the decision based on the reference generated by the DAC. If the capacitors inside DAC are not appropriately ratioed, the static performance of ADC is degraded [161]. The most important factors deteriorating the desired ratio of capacitors and hence the static performance of DAC are the parasitic capacitances and the random variation in the capacitor value caused due to process mismatch [162]. A detailed analysis of the impact of capacitor's mismatches and parasitic is performed in section 6.5.

6.4.4 Binary Weighted with Attenuation Capacitor DAC

A simplified single-ended schematic of an N-bit BWA DAC is shown in Figure 6.6 which consists of an M-bit main-DAC and L-bit sub-DAC, where M + L = N. Both the MSB and the LSB DACs are connected through a bridge capacitor, denoted as C_B.

The value of C_B is selected by the following criterion:

$$C_B = C_U \left[\frac{2^L}{2^M - 1} \right]. \tag{6.9}$$

As an example, consider both M and L to be 6 bits in a 12-bit ADC. Therefore, the resulting C_B required is 32/31 C_U in the absence of top-plate parasitic capacitances.

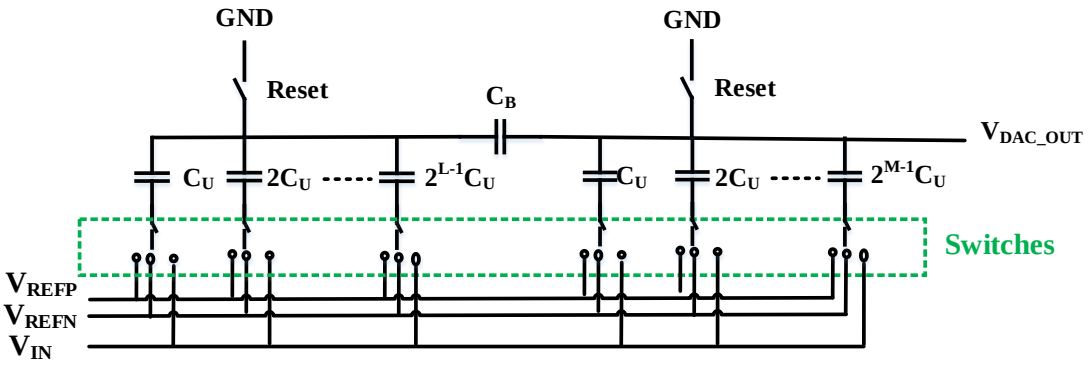


Figure 6.6. A single-ended schematic of BWA DAC.

Although the number of the unit capacitors in BWA DACs are lower than CBW DAC, static (or DC) performance of these architectures suffers more from the capacitor mismatches than their CBW counterparts. Furthermore, the top-plate parasitic of the sub-DAC also degrades the static performance in these architectures [161]. A detailed analysis of the impact of capacitor's mismatches and parasitic are performed in section 6.5.

6.4.5 Comparator

Comparator is a key element in the SAR ADCs. It resolves each bit by comparing the sampled analog input signal to the output of the DAC and generates a digital decision of '0' or '1' for the SAR logic.

Owing to their low power consumption, higher output swing and high speed, latched comparators have become a preferred option in SAR ADCs [34][27]. A latched comparator majorly consists of three building blocks, namely: differential input stage or pre-amplifier, regenerative latch and SR latch as discussed in section 5.5.5.

Major design considerations governing comparator performance are input offset, input referred noise including thermal noise and 1/f noise and metastability etc. The offset in the comparator is a result of the mismatches in transistor drain currents and threshold voltages due to

manufacturing random process variations [1]. The offset limits the minimum achievable resolution of the comparator. It can be partially mitigated by increasing the transistor sizes and careful layout. Metastability in the comparators occurs when the input is near the comparator decision point and as a result the comparator is not able to generate a valid output within designated time. One technique to reduce the probability of metastability is to increase the gain of the pre-amplifier [147]. In addition to above, other important design considerations include the speed, power dissipation, input capacitance and input common mode range of comparator [147].

6.5 Background on Linearity Analysis of SAR ADCs

The targeted ADC is going to be applied in the feedback control loop of the controller of DC/DC converter. Therefore, the ADC is required to have excellent linearity performance. In particular, to achieve the monotonic behaviour the DNL should not exceed beyond -1 LSB.

The linearity of the overall SAR ADC is determined by the linearity of the DAC. This section gives a detailed linearity analysis of BWA and CBW architectures for parasitic capacitances and capacitor mismatches.

6.5.1 Effect of Parasitic Capacitance on Linearity

In order to investigate the effect of parasitic capacitances on the linearity characteristics of capacitive-array DACs, it should be noted that the bottom-plate parasitic do not impact the linearity as output voltage is independent of that. The top-plate parasitic capacitance to the substrate does not impact the linearity performance of the CBW architectures but degrades the performance of BWA architectures [161].

A single-ended simplified version of N-bit CBW DAC array having a unit capacitor C_U and top-plate parasitic of C_{Par} is depicted in Figure 6.7. The binary weighted capacitors inside the capacitor-array are controlled by the control signals which are generated from the SAR-logic. Based on the states of control signals, voltage on the top-plate (i.e. V_{OUT}) is given by:

$$V_{OUT} = V_{REF}\left[\frac{\sum_{i=0}^{N} C_i D_i}{C_{Total} + C_{Par}}\right], \tag{6.10}$$

Where, C_i is the i^{th} capacitor in the DAC array, D_i is the control signal from SAR logic, $2^{(i-1)}C_U$, C_{Total} is the total capacitance in the array while C_{Par} represents the parasitic capacitance connected from the top-plate of capacitor-array to ground. It is apparent from (6.10) that C_{Par} acts as an attenuator that impacts the magnitude of the V_{OUT}, but it does not influence its polarity [161].

A single-ended version of the capacitor array in a BWA DAC is illustrated in Figure 6.8, with MSB-side and LSB-side DACs consisting of M and L bits, respectively with M=L= N/2. The output voltage at the top-plate of MSB-side, which connects to the comparator input, can be written as [161]:

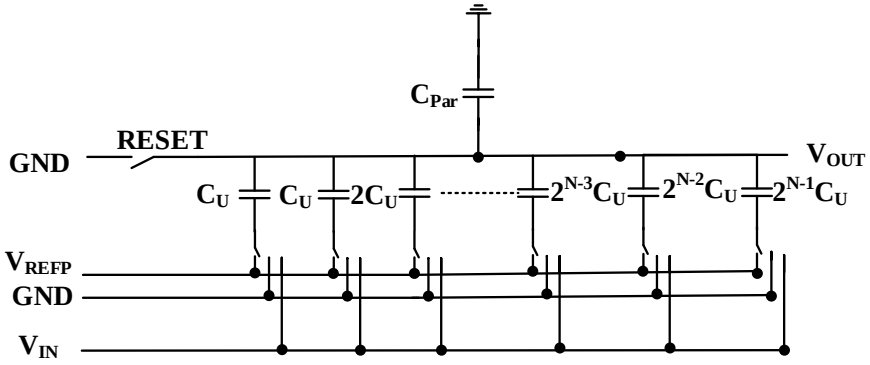


Figure 6.7. Parasitic capacitance in CBW DAC.

$$V_{OUT} \cong V_{REF}\left[\frac{\sum_{i=0}^{L-1} C_i D_i}{C_{Total\_MSB} + C_{Par\_MSB}}\right] + A_{tt}C\left(V_{REF}\left[\frac{\sum_{i=0}^{M-1} C_i D_i}{C_{Total\_LSB} + C_{Par\_LSB}}\right]\right) \quad (6.11)$$

Where C_{Total_MSB} , C_{Par_MSB}, C_{Total_LSB} and C_{Par_LSB} are the total main capacitance on MSB side of array, parasitic capacitances on the MSB side of array, total main capacitance on LSB side of array and parasitic capacitances on the LSB side of array, respectively while $A_{tt}C$ is given as,

$$A_{tt}C = \left[\frac{C_U}{C_{Total\_LSB} + C_{Par\_LSB}}\right]$$

Shown in equation (6.11), is the effect of the top-plate parasitic at the LSB-side (i.e. C_{Par_LSB}) on output voltage of DAC i.e. V_{OUT}, which is not constant with changing input digital code and hence can results in significant linearity degradation. On the other hand, the effect of top-plate parasitic capacitances on the MSB-side (i.e. C_{Par_MSB}) impacts the magnitude only. For the case M=L= N/2, the maximum DNL occurs every $2^{N/2}$ code and is given as [161][167]:

$$DNL \cong V_{REF}\left[\frac{2^N C_{Par\_LSB} + 2^{\frac{3N}{2}}(C_U + C_B)}{2^{N+1} C_U}\right] \quad (6.12)$$

Equation (6.12) shows that in order to keep the DNL within ±1 LSB, C_{Par_LSB} should be smaller than C_U.

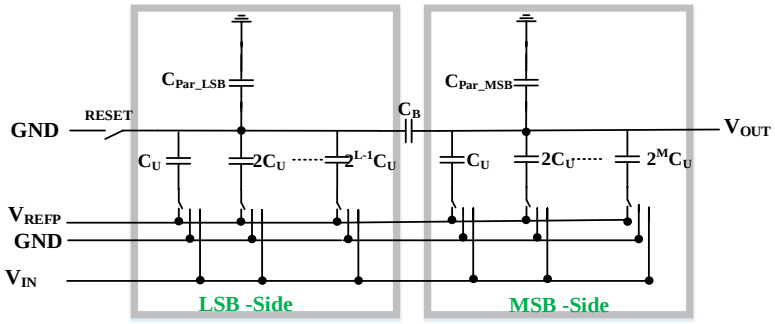


Figure 6.8. Parasitic capacitance in BWA DAC.

Usually the MOM capacitors available in 0.13-μm CMOS design kit feature a top-plate parasitic in the range of 5-to-7%. Exact value of parasitic depends upon the unit capacitor value. In that sense, as an example, for a 6-6 BWA DAC based ADC with unit capacitor of 20 fF, resultant C_{Par_LSB} could be in the range of 64 fF-to-89.6 fF. In order to keep C_{Par_LSB} lower than C_U, the maximum allowable top-plate parasitic capacitance for a single C_U should not exceed 1.5%. Therefore, a custom MOM capacitor having lower top-plate parasitic (< 0.25%), has been designed for this ADC. A detailed discussion about custom MOM capacitor architecture is given in section 6.6.2.

6.5.2 Impact of Capacitor Mismatches on Linearity

In addition to parasitic capacitance, capacitor mismatch is another limitation in realising higher resolution SAR ADCs. The ccapacitor mismatch can be modelled assuming a Gaussian probability distribution of the unit capacitor value with a mean equal to the nominal capacitance C_U and a standard deviation of ΔC is given as [167]:

$$[\Delta C] = \frac{K_C C_U}{2A} = K_C \sqrt{\frac{C_{Sperc} C_U}{2}} \qquad (6.13)$$

Where K_C, A and C_{Spec} are the Pelgrom mismatch coefficient [168], the area and the specific capacitance i.e. capacitance/area, respectively. This expression is a good starting point for the evaluation of different trade-offs associated with the mismatches. For the larger surface areas, the effects associated with area dominate, and equation (6.13) is reduced to Pelgrom's mismatch coefficient and $1/\sqrt{A}$. However, for lower areas, the mismatches increase at a higher rate as the edge effects start to dominate. The exact dependence of area and the edge effects depend upon the CMOS process technology and capacitor type [168].

Due to capacitor mismatch, the DAC output voltage deviates from nominal values resulting in degradation of the linearity. In the CBW based architectures illustrated in Figure 6.7, the impact of capacitor mismatch is worst at the mid code transition, as the number of capacitors changing their states are maximum during this transition. Theoretically, the variance of the maximum DNL and INL during this bit trial is given as [167]:

$$\sigma(\mathrm{DNL})_{\mathrm{CBW,MAX}} = 2^{\frac{N}{2}}\left(\Delta C / C_U\right), \tag{6.14}$$

$$\sigma(\mathrm{DNL})_{\mathrm{CBW,MAX}} = 2^{\frac{N}{2}}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right). \tag{6.15}$$

Also,
$$\sigma(\mathrm{INL})_{\mathrm{CBW,MAX}} = \sigma(\mathrm{DNL})_{\mathrm{CBW,MAX}} = 2^{\frac{N}{2}-1}\left(\Delta C / C_U\right) \tag{6.16}$$

And,

$$\sigma(\mathrm{INL})_{\mathrm{CBW,MAX}} = 2^{\frac{N}{2}-1}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right). \tag{6.17}$$

In the case of a differential implementation, the number of capacitors is doubled. Therefore, the variance of maximum DNL and INL is scaled by √2.

For a BWA architecture illustrated in Figure 6.8, the worst case standard deviation of the INL and DNL also occurs at mid code transition. For an N-bit BWA-DAC with MSB and LSB-DACs, both having N/2 bits, the variance of maximum DNL and INL can be written as [167]:

$$\sigma(\mathrm{DNL})_{\mathrm{BWAMAX}} = 2^{\frac{3N}{4}}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right), \tag{6.18}$$

and

$$\sigma(\mathrm{INL})_{\mathrm{BWA,MAX}} = 2^{\frac{3N}{4}-1}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right). \tag{6.19}$$

Random capacitor mismatch is a major source of linearity errors in SAR ADCs targeting resolution greater than 10-bit. Due to their lower cost, MOM capacitors have become a preferred option for the DAC implementation in SAR ADCs. Therefore, an accurate estimation of the mismatch in the MOM capacitor is of prime importance. Table 6.2 summarises mismatch data from two other CMOS processes. Based upon the literature and design kit data, the MOM capacitor mismatch is approximately three times that of MIM capacitors [170]. For the current design kit, a MIM capacitor of 16fF has a mismatch coefficient of 0.85% μm. Therefore, a MOM capacitor having the same capacitance (i.e. 16 fF), as a rough estimate, the K_C can be taken as 2.55% μm i.e. 3 × 0.85. For high level analysis, 3 % μm is a good conservative approximation.

As discussed previously, the impact of capacitor mismatch is most pronounced at MSB-1 transition resulting in maximum INL and DNL occurring during this bit trial [27][161]. By employing the expressions (6.18) and (6.19), with a K_C of 3 %μm, the value of standard variance of the maximum DNL for a 6-6 BWA architecture is calculated for different values of C_U and C_{Spec}. The resulting 3σ DNL_{MAX} (LSB) and 3σ INL_{MAX} (LSB) over a wider range of C_U and C_{Spec} are illustrated in Figure 6.9 and Figure 6.10, respectively. These figures show that for a given C_U lower values of C_{Spec} or higher area, results in better linearity performance. As an example, a C_U of 20 fF having a C_{spec} below 0.2 fF/μm^2 or an area of 100 μm^2, can achieve the required linearity performance (DNL < ±1LSB). In order to obtain the desired linearity performance with a higher C_{Spec} or smaller C_U either analog or digital calibration is required.

Table 6.2. Capacitors mismatch data from different design kits.

Technology (nm)	**Cap Type**	**Cap. Mismatch (Std. dev %)**	**K_C (%μm)**
UMC 130	MIM	1	0.95
ST 65	MIM	5	0.5
ST 65	MOM	1	1.5

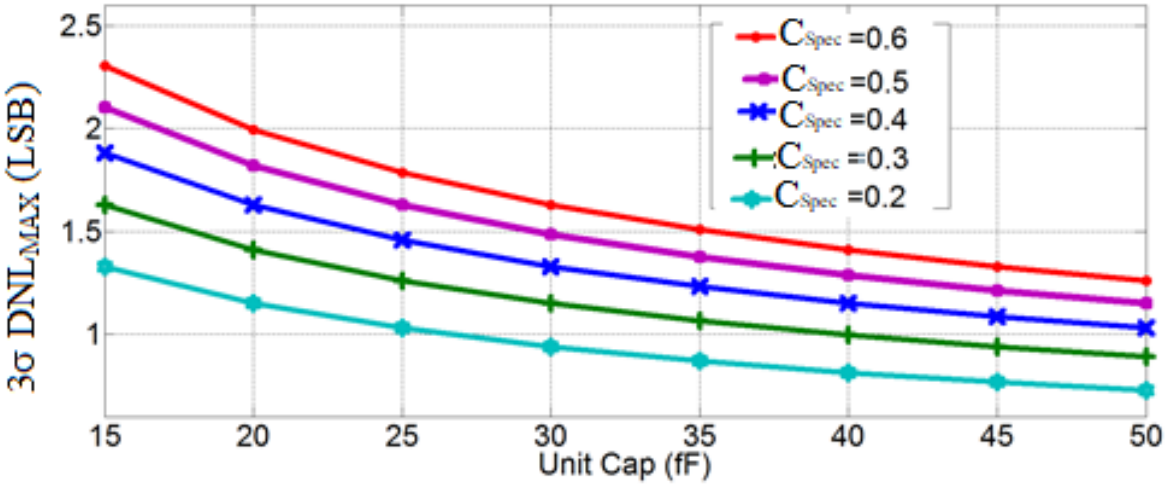


Figure 6.9. 3σ DNL_{MAX} incurred for BWA DAC based SAR ADC over a range of C_U and C_{spec}.

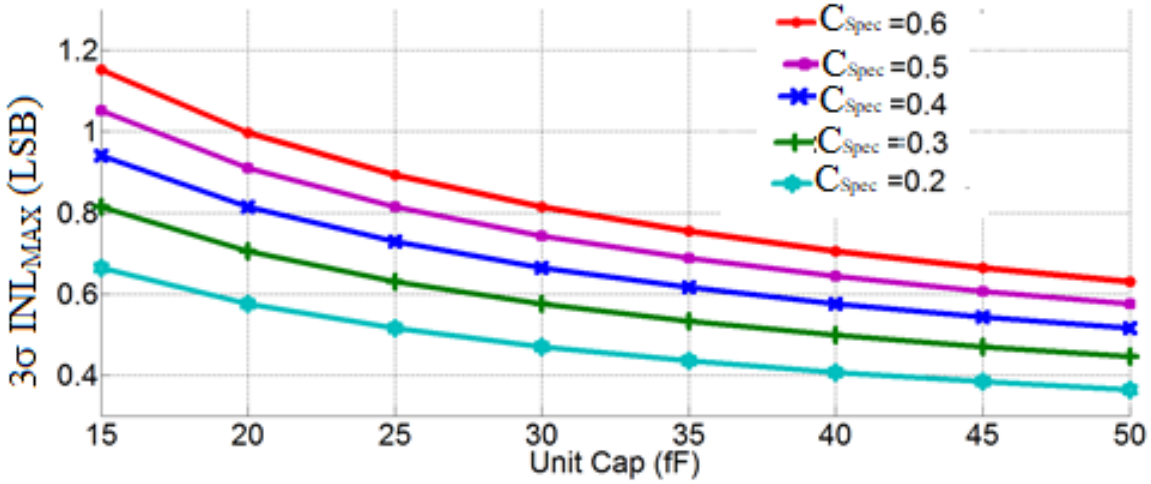


Figure 6.10. 3σ INL_{MAX} incurred for BWA DAC based SAR ADC over a range of C_U and C_{spec}.

6.6 ADC Architecture and Input Scaling

The capacitance required for an N-bit SAR ADC with CBW and BWA DAC architectures are given by,

$$C_{Total,CBW} = 2^N C_U \tag{6.20}$$

$$C_{Total,BWA} = \left(2^M + 2^L\right) C_U \tag{6.21}$$

Where, M and L are the number of capacitors on MSB and LSB sides, respectively in the BWA architecture. Although BWA architectures suffer more from the parasitic capacitances and capacitor mismatches, the number of the unit capacitors and hence circuit complexity is much lower [149][161]. The proposed ADC employs a 6-6 BWA architecture with bottom-plate sampling as illustrated in Figure 6.11. This sampling technique is more favourable for applications requiring higher linearity as the non-linearity associated with the junction capacitance of the top-plate switch is almost zero [22] . One problem associated with the bottom-plate sampling is that the voltage on the top of LSB-DAC could exceed the power rails i.e. 0 or 1.2 V during the bit trials. As a result, the parasitic diode of the top-plate switches can turn ON and cause leakage current and, hence corrupting the sampled signal.

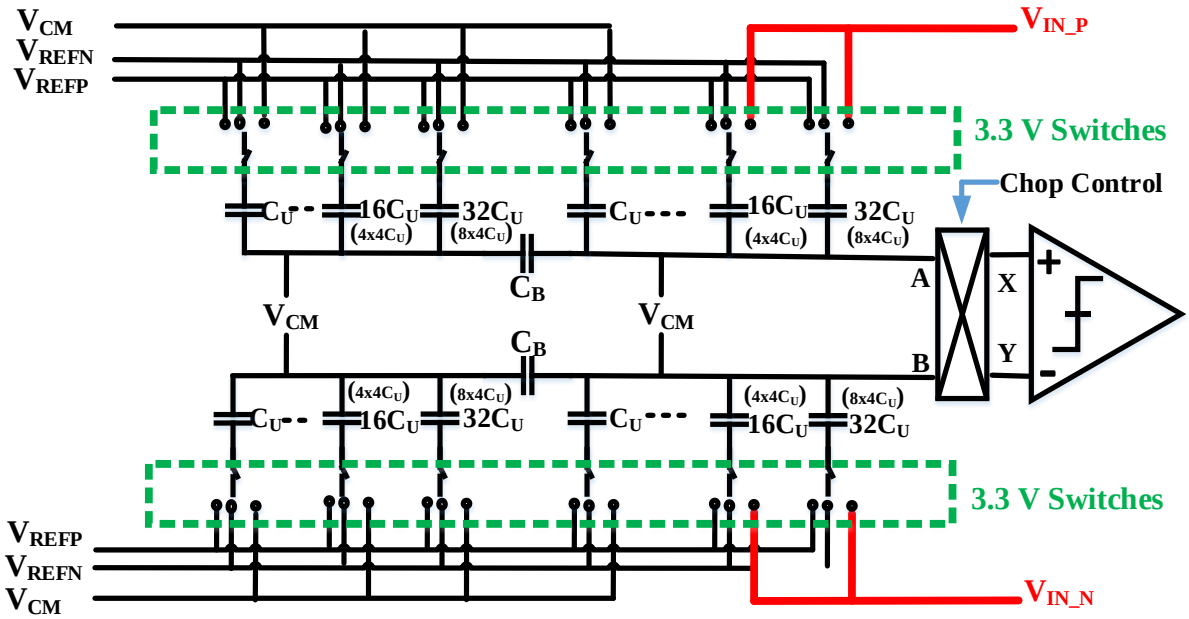


Figure 6.11. Proposed 6-6 BWA 12-bit SAR ADC architecture with input scaling.

In this architecture, input sampling scaling is realised by only sampling the input signal onto the bottom plates of the MSB and MSB-1 capacitors while the common mode voltage (V_{CM}) is sampled onto the bottom-plate of all the remaining capacitors as shown in Figure 6.12. This has the effect of scaling the input signal by a factor of three quarters of the initial input voltage. By employing a different number of input capacitors during sampling phase, this technique can be further extended to realise different input scaling ratios to enable larger input ranges.

6.6.1 Switches

NMOS are used to connect the capacitors of the DAC to the reference voltages (V_{REFP} and V_{REFN}), the input signal (V_{IN}) and the common mode voltage (V_{CM}). In order to balance the parasitic capacitance and to facilitate the capacitor segmentation, a modular design approach has been used when designing and completing the capacitor array.

The capacitors in the DAC are arranged in the columns of 4 unit capacitors (i.e. C_Us). An equivalent single-ended DAC schematic is shown in Figure 6.13.

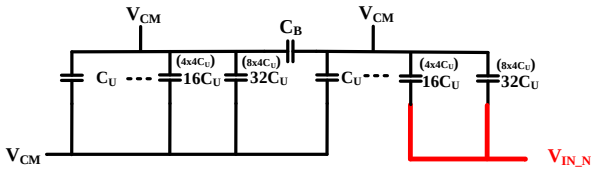


Figure 6.12. Sampling of the input voltage.

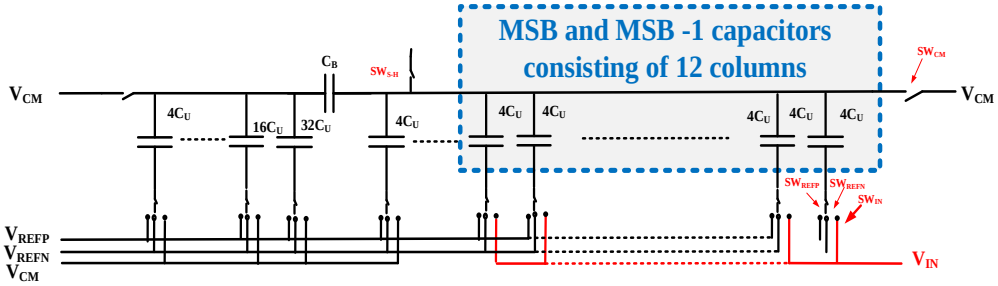


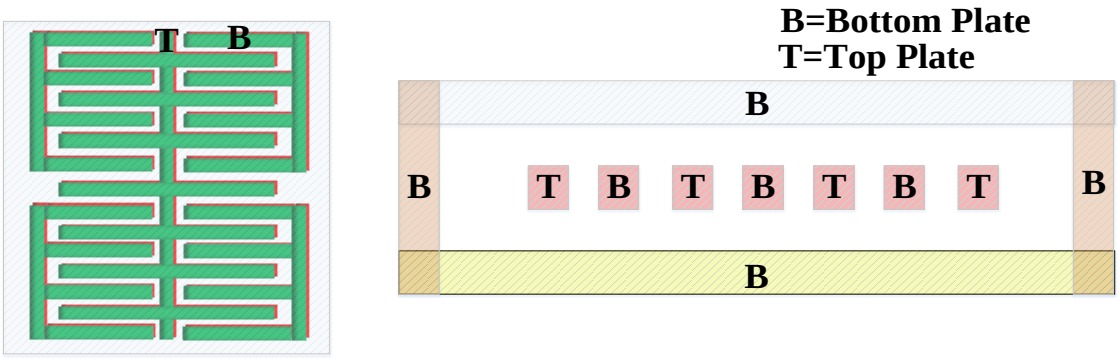
Figure 6.13. Simplified schematic of SE DAC of the SAR ADC.

Hence, the MSB capacitor consists of 8 columns; the MSB-1 capacitor consists of 4 columns and so on. Each capacitor column is controlled by an independent set of three switches (SW_{REFP}, SW_{REFN} and $SW_{IN.}$). The top plates of all the columns either MSB-DAC or LSB-DAC are shorted together and connected to V_{CM} using the SW_{CM} switch. The reference switches (SW_{REFP} and SW_{REFN}) are activated during various bit trials to connect the bottom plates of the capacitors to V_{REFP} and V_{REFN}, respectively.

The ADC employs 3.3 V NMOS IO devices for the input (V_{IN}, 0-to-3.2 V_{pp_d}), V_{REFP} (1.2 V), V_{REFN} (0 V) and V_{CM} (0.8 V) switches.

6.6.2 Custom MOM Capacitors

As discussed in section 6.5.1, in terms of parasitic, a DNL of ±1 LSB requires the capacitors with a top-plate parasitic less than 1.5 %. Therefore, a custom MOM capacitor having top-plate parasitic lower than 0.25 % has been designed. The top and cross-sectional views of the designed custom MOM capacitor are depicted in Figure 6.14 (a) and (b), respectively.



(a) (b)

Figure 6.14. MOM Capacitor (a) Top view (b) Cross-sectional view.

The top and bottom plates of the capacitor consist of metal 3 and 4, with each plate consisting of 8 interdigitated fingers. The capacitor top-plate is also shielded with metal 2 and metal 5, which are connected to the bottom plate of the capacitor. As bottom-plate surrounds the top-plate in all directions, therefore, any parasitic capacitance from the top-plate is to the bottom plate, where it adds to the core capacitance only (main capacitance between top and bottom plates), and not to ground where it would impact on the resultant DAC linearity. The entire structure of the capacitor array is placed in N-well to further isolate it from the P-substrate. This creates a repeatable architecture minimizing systematic offset.

The size of a single C_U is 8 µm ×8 µm. The extracted capacitance between top and bottom plates is 20 fF. The top and bottom-plate to substrate parasitic capacitances are 40 aF (0.2%) and 1.2 fF (6.2%), respectively.

6.7 DAC Segmentation for Improved Linearity

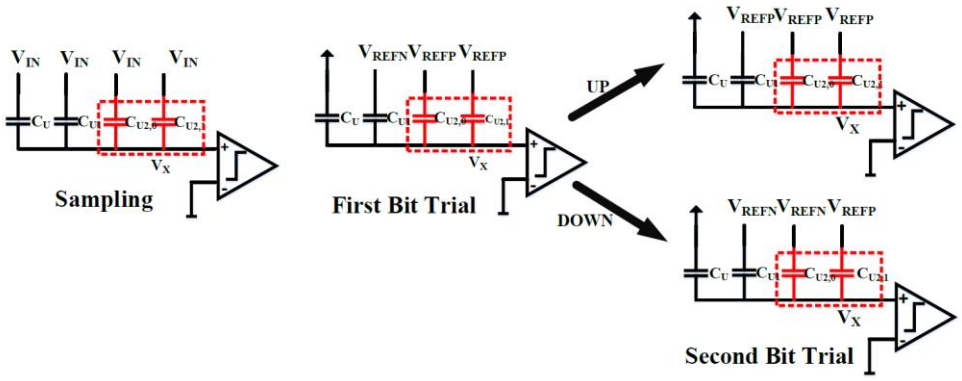
The DAC is used for sampling the input signal and reference generation. It was shown in section 6.5.2 that capacitor mismatch limits the achievable linearity in the DAC. As this ADC is going to be used in a feedback control loop, high linearity especially DNL is very important for the monotonicity. Capacitor segmentation has already been used to improve the DNL of an ADC [175]. This ADC employs 4-level segmentation to achieve better linearity. This section explains the segmentation algorithm for a 2-bit SAR ADC, followed by a qualitative analysis of a 4-bit segmented DAC and its associated achievable performance.

6.7.1 DAC Segmentation

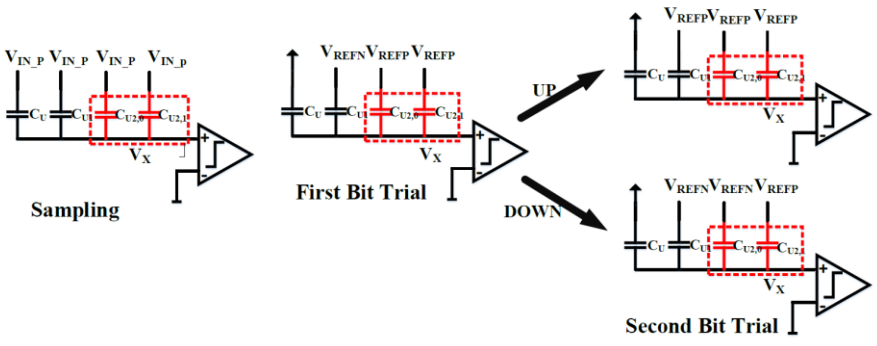
A detailed analysis of DAC segmentation is given in [175]-[177]. For the purpose of this analysis, a 2-bit binary CBW-DAC consisting of two capacitors has been chosen as illustrated in

Figure 6.15. Here C_{U1} represents the LSB-capacitor while the MSB-capacitor is split into two equal parts; $C_{U2,0}$ and $C_{U2,1}$. All of these unit capacitors have equal capacitances i.e. $C_{U2,1}$= $C_{U2,0}$= C_{U1}= $C_{U.}$ Figure 6.15 (a) and (b) shows the switching of the capacitor array in conventional and segmented DACs, respectively.

The conversion process starts by sampling the input signal onto the bottom plates of all capacitors. During the sampling phase, the connections of all the capacitors are the same in both types of DAC i.e. conventional and segmented DACs. After sampling the input signal, during the first bit trial, all MSB capacitors (i.e. $C_{U2,0}$ and $C_{U2,1}$) are connected to V_{REFP} i.e. positive reference, while the LSB-capacitor C_{U1} is connected to V_{REFN} i.e. negative reference.



(a)



(b)

Figure 6.15. 2-bit SAR ADC operation with (a) Normal DAC (b) Segmentation DAC.

Resultantly, voltage at the comparator's input becomes $V_X = -V_{IN} + V_{REFP}/2$. If $V_{IN} > V_{REFP}/2$ then $V_X < 0$ and the comparator output is "1". Therefore, during the next bit trial, an "up" transition is to be performed. Due to "up" transition, during the second bit trial, the number of capacitors connected to V_{REFP} need to be increased. For this transition, the capacitors in the both DACs change their states in the same way. All capacitors in the MSB-capacitor i.e. $C_{U2,0}$ and $C_{U2,1}$ remain connected to the V_{REFP} while the LSB capacitor (i.e. C_{U1}) is also connected to V_{REFP} (as depicted by the "up" transition part of the second bit trial of Figure 6.15 (a) and (b)). Therefore, the comparator input now becomes $V_X = -V_{IN} + 3V_{REFP}/4$. Based upon this input, second output bit is obtained. On the other hand, if during the first bit trial, $V_{IN} < V_{REFP}/2$ then $V_X > 0$ and the comparator output is "0". Therefore, during the next trial, a "down" transition is to be performed. Hence, the number of capacitors connected to V_{REFN} need to be increased. For this transition, conventional DAC and segmented DAC behave differently. In the conventional DAC, (as depicted by the "down" transition part of the second bit trial of Figure 6.15 (a)), the MSB capacitors ($C_{U2,0}$ and $C_{U2,1}$) change their state from V_{REFP} to V_{REFN} while the LSB capacitor C_{U1} changes its state from V_{REFN} to V_{REFP}. During this bit trial, the maximum number of capacitors changes their states in conventional DAC i.e. 3 capacitors. In contrast to this, in a segmented DAC, only half of the MSB-array capacitors i.e. $C_{U2,1}$ change their state to V_{REFN} while the other half i.e. $C_{U2,0}$ is connected to V_{REFP} as depicted by the "down" transition part of the second bit trial of Figure 6.15 (b). The LSB capacitor C_{U1} remains connected to V_{REFN}. Therefore, only one capacitor changes its state i.e. $C_{U2,1}$ compared to three in a conventional DAC and hence results in lower differential non-linearity i.e. DNL. The same concept can be extended to a multibit implementation as stated in the next section.

6.7.2 Linearity Analysis of Segmented DAC Array

DAC segmentation can significantly improve the resultant DNL. This can be explained with an example from [175]. A BWA DAC having M and L number of bits in the MSB and LSB-DACs, respectively, is shown in Figure 6.16. In this architecture, the capacitance seen from node B towards the left, can be represented as C_S and can be written as:

$$C_S = \frac{(2^L - 1)C_U{}^2}{(2^L - 1)C_U + C_U} \approx C_U . \tag{6.22}$$

The maximum error due to capacitor mismatch occurs at the $(MSB-1)^{th}$ bit transition as the maximum number of capacitors change their state during this bit trial. In order to calculate the error due to capacitor mismatch, we assume V_X as the voltage at top-plate of the MSB-DAC during MSB-trial and V_X' is the voltage after the transition i.e. during $(MSB-1)^{th}$ trial.

During the MSB-bit trial, the MSB capacitor i.e. $2^{M-1}C_U$ in the MSB-DAC are connected to $V_{REFN,}$ while all the remaining capacitors in the MSB-DAC i.e. C_U-to-$2^{M-2}C_U$ and all the capacitors in LSB-DAC i.e. C_U-to-$2^{L-1}C_U$ are connected to the V_{REFP} as shown in Figure 6.17 (a). (Same analysis can be carried out for the opposite case i.e. MSB capacitor in the MSB-DAC being connected to V_{REFP} and remaining capacitors to V_{REFN}.)

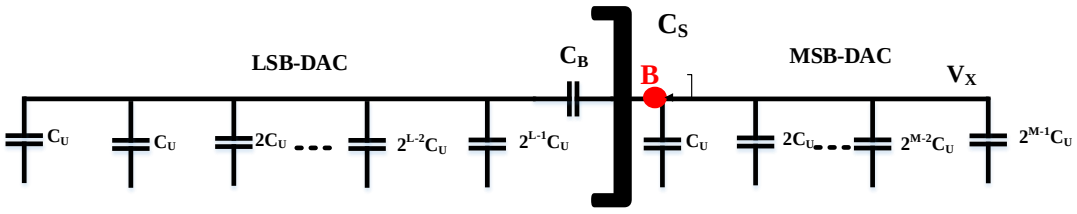


Figure 6.16. BWA DAC consisting of M and L numbers of bits in the MSB and LSB-DACs.

The voltage at the top-plate on the MSB-DAC is given by:

$$V_X \cong V_{REFP}\left[\frac{\sum_{i=0}^{L-1} C_i D_i}{C_{Total\_MSB}}\right] + \left[\frac{C_U}{C_{Total\_LSB}}\right]\left(V_{REFP}\left[\frac{\sum_{i=0}^{M-1} C_i D_i}{C_{Total\_LSB}}\right]\right). \tag{6.23}$$

During the MSB-bit trial,

$$V_X \approx \frac{(2^{M-1}-1)C_U}{2^M(1-2^{-N})C_U} V_{REFP} \tag{6.24}$$

$$V_X \approx \frac{(2^{M-1}-1)C_U}{2^M C_U} V_{REFP} \tag{6.25}$$

Now consider the MSB-1 bit trial as shown in Figure 6.17 (b). All of the unit capacitors in the MSB capacitor are connected to V_{REFP} while all the remaining capacitors switch their state to V_{REFN}, as shown in Figure 6.17 (b).

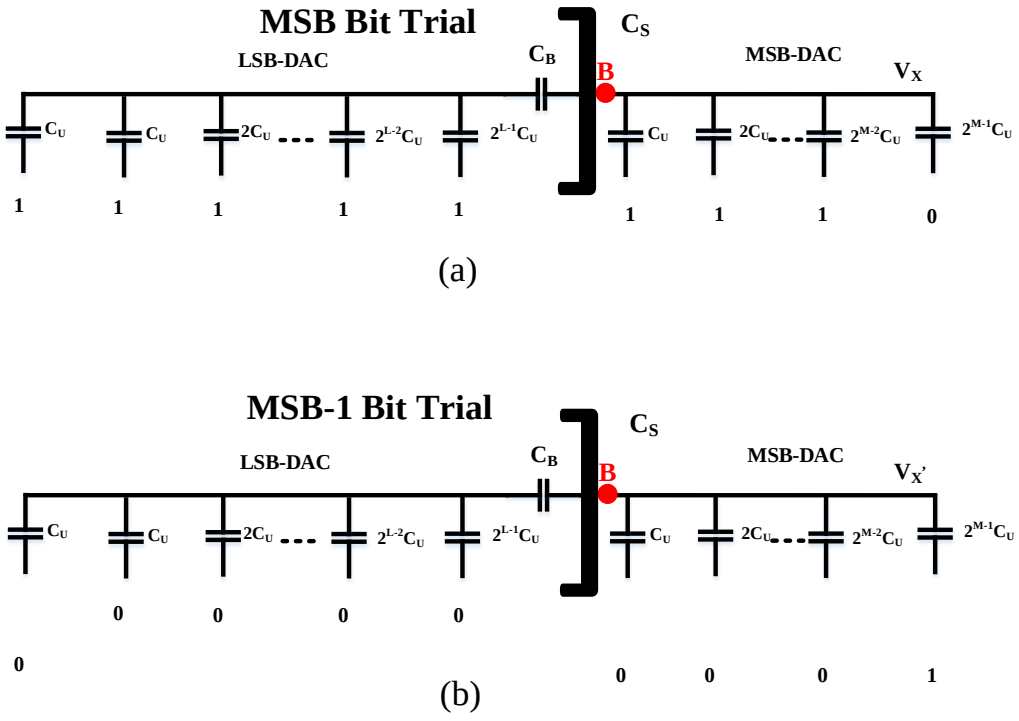


Figure 6.17. Capacitor states during (a) MSB-bit trial (b) MSB-1 bit trial.

The voltage at the top-plate V_X' is now given by:

$$V_X' \approx \frac{2^{M-1}C_U}{2^M(1-2^{-N})C_U} V_{REFP} \approx \frac{2^{M-1}C_U}{2^M C_U} V_{REFP}. \quad (6.26)$$

Ideally, the difference of V_X to V_X' equals to $V_{REFP}/2^M$. It can be written as follows:

$$V_X - V_X' \approx \frac{2^{M-1}C_U - (2^{M-1}-1)2^{M-1}}{2^M C_U} V_{REFP} \approx \frac{V_{REFP}}{2^M} \quad (6.27)$$

If the standard deviation for the capacitor mismatch in C_U is ΔC_U, the real value of the unit-capacitor C can be written as:

$$C = C_U + \Delta C_U. \quad (6.28)$$

Therefore, equitation (6.27) can be written as:

$$V_X - V_X' \approx \frac{2^{M-1}C - (2^{M-1}-1)2^{M-1}}{2^M C} V_{REFP}. \quad (6.29)$$

All unit capacitors are connected in parallel with each other in the DAC. If the total number of capacitors connected in parallel is N, the standard deviation of the total capacitance in the capacitor array is $\sqrt{N}\,\Delta C_U$. Therefore, the standard deviation of V_X - V_X' can be calculated as:

$$\sigma(V_X - V_X') = \frac{2^{M-1}C_U + \sqrt{2^{M-1}}\Delta C_U - (2^{M-1}-1)C_U - \sqrt{2^{M-1}-1}\Delta C_U}{2^M C_U + \sqrt{2^M} C_U} V_{REFP}, \quad (6.30)$$

$$\sigma(V_X - V_X') \approx \frac{C_U + \sqrt{2^{M-1}}\Delta C_U - \sqrt{2^{M-1}-1}\Delta C_U}{2^M C_U} V_{REFP}. \quad (6.31)$$

Therefore, the variance of maximum DNL incurred during this code transition is given by:

$$\sigma(DNL)_{Maximum,Normal} = (V_X - V_X')_{std} - (V_X - V_X')_{Ideal}, \quad (6.32)$$

$$\sigma(DNL)_{Maximum,Normal} \approx \frac{\sqrt{2^{M-1}}}{2^M}\left(\frac{\Delta C_U}{C_U}\right) V_{REFP}. \quad (6.33)$$

Now consider the DAC where upper "K" bits out of the "M" bits are segmented as illustrated in Figure 6.18. Here the upper "K" bits of MSB-DAC are rearranged in multiple columns to ease the segmentation. In this configuration, the maximum number of switching occurs during the bit trial when all the capacitors in the $(M-K)^{th}$ binary weighted capacitors change their state from V_{REFN} to V_{REFP}. The capacitor array before and after the code transition is shown in Figure 6.19 (a) and (b), respectively.

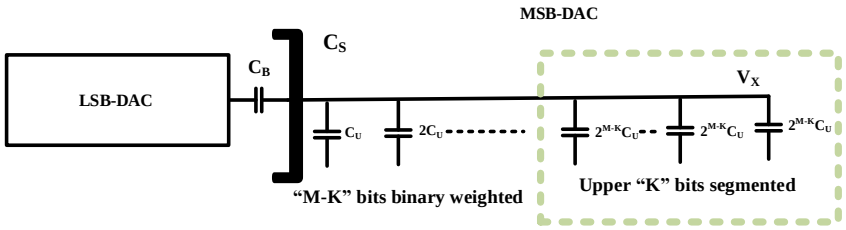


Figure 6.18. Segmented MSB-DAC where upper K bits in MSB-DAC are segmented.

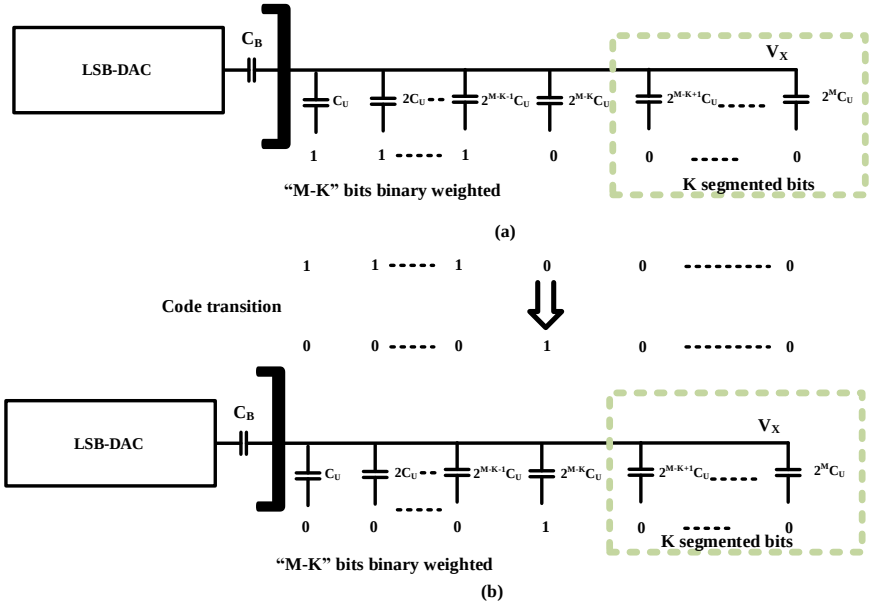


Figure 6.19. Code transition where maximum number of capacitors in segmentation DAC change their state (a) Before transition (b) After transition.

The maximum DNL and INL occur during this bit trial. The voltage at the top-plate of the MSB-DAC before and after the code transition as depicted in Figure 6.19(a) and (b) i.e. V_X and V_X'are given by (6.34) and (6.35), respectively:

$$V_X \approx \frac{(2^{M-K}-1)C}{2^M C} V_{REFP}, \tag{6.34}$$

$$V_{X'} \approx \frac{2^{M-K} C}{2^M C} V_{RREFP}, \tag{6.35}$$

Using the same procedure as explained before, the variance of maximum DNL can now be written as follows:

$$\sigma(DNL)_{MaximumSegmented} = (V_X - V_{X'})_{std} - (V_X - V_{X'})_{Ideal}, \tag{6.36}$$

$$\sigma(DNL)_{MaximumSegmented} = \frac{\sqrt{2^{M-K}}\Delta C_U - \sqrt{2^{M-K}-1}\Delta C_U}{2^M C_U} V_{REFP}. \tag{6.37}$$

Which simplifies to:

$$\sigma(DNL)_{MaximumSegmented} = \frac{\sqrt{2^{M-K+1}-1}}{2^M} \frac{\Delta C_U}{C_U} V_{RREFP} \tag{6.38}$$

Comparison of equations (6.33) and (6.38) shows that the maximum standard deviation of the DNL in the segmented DAC is reduced by a factor of $\sqrt{2^{K-1}}$.

In the proposed architecture, the upper 4 bits of the MSB-DAC are segmented. 4-bit segmentation ideally reduces the variance of maximum DNL by a factor of $\sqrt{8}$ (or 2.82). In order to facilitate this segmentation, the capacitors in the DAC are arranged in columns where each column consists of 4 C_Us as depicted Figure 6.20, with two dummy rows above and below. Each of these columns is controlled by an independent set of 3 switches i.e. V_{IN}, V_{REFP} and V_{REFN}, which are driven by the control signals generated by SAR logic. For 4-level capacitor segmentation, 17 additional signals are generated from the SAR logic. In order to validate the

capacitor segmentation algorithm, a set of Monte Carlo runs with Gaussian distributed mismatch errors $\sigma C_U / C_U$=0.5-to-3% were performed at the behavioural level of the circuit, that validated the DNL improvement. As an example, Figure 6.21 shows the DNL plot of the 12-bit SAR ADC with conventional and segmented DACs while having 0.81 % mismatch in the MSB and the MSB-1 capacitors.

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	32	32	32	32	16	16	8	8	4	D	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	D	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	D	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	D	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	2	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	2	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	2	1	1	16	16	32	32	32	32	B	32	32	32	32	16	16	8	8	4	2	1	16	16	32	32	32	32	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Figure 6.20. Layout of 12-bit DAC to facilitate the segmentation.

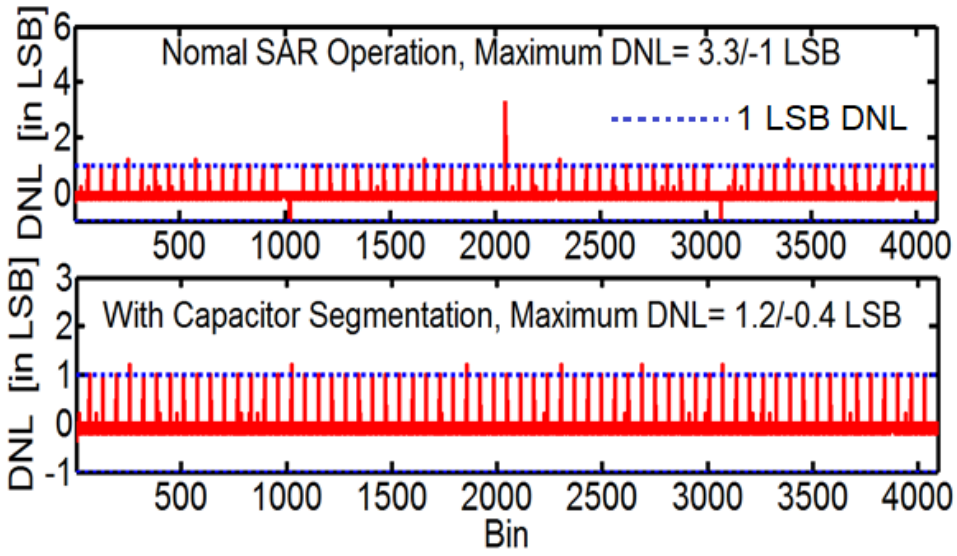


Figure 6.21. DNL plots of 12 SAR ADC, 0.81% mismatch in MSB and MSB-1 in 6-6 BWA based SAR ADC with conventional and segmented DACs.

6.8 Comparator

The designed 12-bit SAR ADC employs a double tail latch comparator as shown in Figure 6.22 [178]. This architecture is more suited to lower-supply voltages as the number of stacked transistors are lower compared to a conventional dynamic comparator. These comparators do not dissipate any static power. Furthermore, these comparators allow larger currents in the latching stage for higher speed while maintaining lower current in the input stage for lower offset.

During the reset phase i.e. CLK = 0, the transistors M4 and M5 charge the two nodes "P" and "N" to supply voltage, VDD. As a result, transistors M9 and M10 turn ON and discharge the output nodes, OUT-P and OUT-N, to ground. During the ON phase, CLK =VDD, the transistors M4 and M5 turn off and an input-dependent differential voltage ΔV_{PN} is formed between the nodes, "P" and "N". This voltage is then transferred to the regenerative latch, consisting of M6, M7, M8 and M9, which generates the outputs, OUT-P and OUT-N, that are then passed to the SR-Latch. Table 6.3 and Table 6.4 present the transistor sizes and the simulation results of the comparator, respectively.

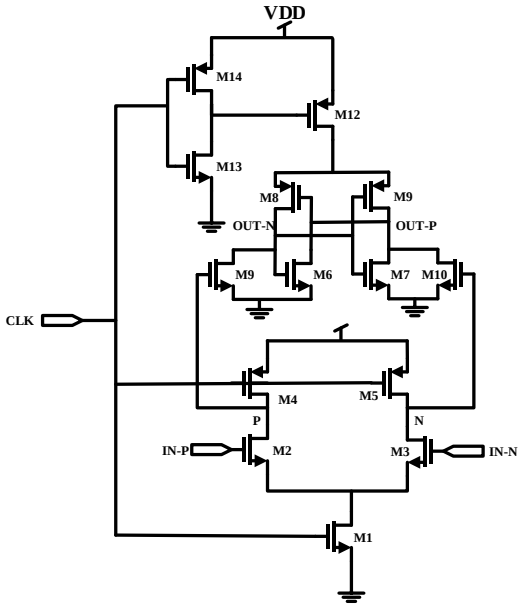


Figure 6.22. Double-tail latch comparator.

Table 6.3. Transistor sizes in double tail latch comparator.

Devices	Type	Size(μm)
M1	NMOS	4/0.26
M2, M3	NMOS	24/0.26
M4, M5	PMOS	4/0.26
M6, M7	NMOS	8/0.26
M8, M9	PMOS	24/0.26
M10, M11	NMOS	16/0.26
M12	PMOS	4/0.26

Table 6.4. Simulation results of comparator.

Specification	Value
Offset (std. dev, mV)	1.59
RMS Noise (μV)	88
Current (μA)	90

6.8.1 Comparator Offset Removal

The comparator offset can vary with time due to temperature and aging effects and is the primary source of offset within the ADC. The proposed ADC is going to be incorporated in a system that will have a life span of several years (5-to-10) and hence requires an accurate and dynamic estimation of the ADC offset during its lifespan. A chopping circuit is placed at the comparator's differential inputs shown in Figure 6.23. The SAR ADC operation sequence for the ADC during the offset-calculation mode is depicted in Figure 6.24. As a first step, the nodes A and B are initially connected to nodes X and Y, respectively as shown in Figure 6.23. After the reset and sampling phase, the SAR algorithm goes through a regular bit-trial sequence. However, instead of progressing to the next sample, the comparator inputs are then switched, thus connecting nodes A and B with Y and X, respectively and a second sequence of bit trials is performed. The two respective digital outputs are then processed to determine the offset.

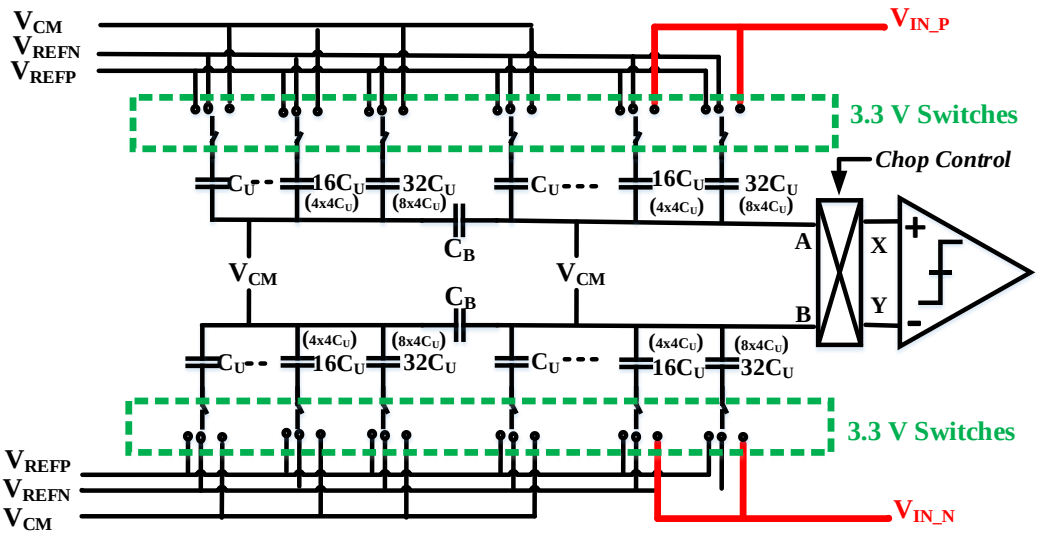


Figure 6.23. Full schematic of ADC with chopping in front of comparator.

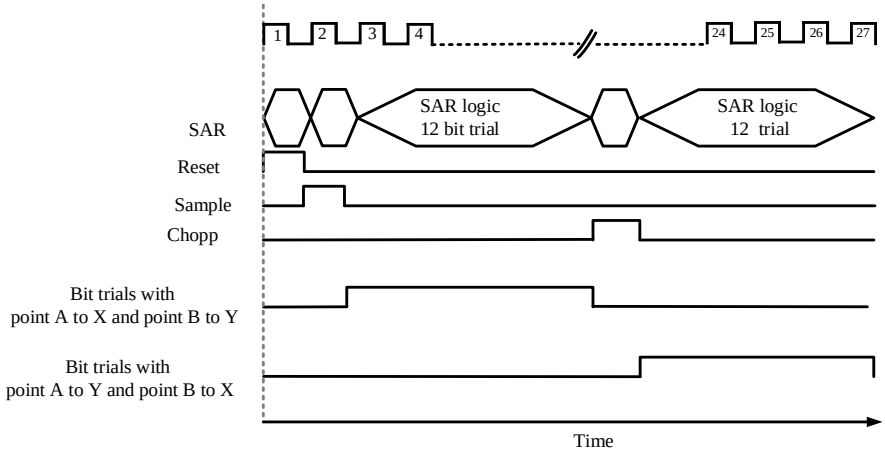


Figure 6.24. ADC operation sequence in offset-calculation.

The offset-calculation can be performed for any input level. When run in offset-calculation mode, the two output codes obtained are subsequently averaged and the comparator offset is determined. Based upon the requirement of offset-calculation frequency, the ADC can be run in this mode. The ADC has a conversion time of 0.5 μs when the output rate = 2 MS/s and requires 1 μs in offset-calculation mode. As an example, the ADC can be run in normal mode for a longer time (let's say 1 ms) and then in the offset-calculation mode for a single time (i.e. 1 μs). In this sense, the impact of offset-calculation upon the throughput of ADC is not significant. Offset-

calculation mode is activated using a control signal of SAR logic that can be controlled from outside. The offset calculation mode can also be used to reduce the comparator's 1/f noise.

6.9 ADC Layout

The 12-bit SAR ADC is fabricated in a 0.13-μm 1P6M CMOS process. For better noise isolation, all NMOS devices are placed in a deep-n-well (DNW). The following subsections briefly explain the layout of the different circuit blocks.

6.9.1 DAC

The unit capacitors in the DAC are arranged in columns with each column consisting of 4 C_Us, with additional dummy capacitors added for matching purposes. All the capacitor columns in the array are arranged in pseudo common centroid fashion to facilitate the routing and at the same time improve the relative matching as depicted in Figure 6.25. Here 32, 16, 8 represent MSB, MSB-1 and MSB-2 capacitors, respectively and so on. The complete capacitor array is surrounded by two rows, above and below, and two columns at either ends of dummy capacitors. It was stated in section 6.6.1 that the switches employed in DAC are 3.3 V NMOS while the SAR logic employs 1.2 V devices. Therefore, level shifters are required between SAR logic and DAC switches. Moreover, to make the complementary references (V_{REFP}, V_{REFN}) going to single capacitor columns non-overlapping, a break-before-make (BBM) circuit has been employed. Each capacitor column is controlled by a single set of switches along with corresponding level shifters and BBM. The arrangement of capacitor array column, BBM, level shifter and SAR logic is shown in Figure 6.26. A complete layout of the DAC is shown in Figure 6.27.

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	32	32	32	32	16	16	8	8	4	D	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	D	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	D	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	D	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	2	D	D	16	16	32	32	32	32	D	32	32	32	32	16	16	8	8	4	2	D	16	16	32	32	32	32	D	D
D	D	32	32	32	32	16	16	8	8	4	2	1	1	16	16	32	32	32	32	B	32	32	32	32	16	16	8	8	4	2	1	16	16	32	32	32	32	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Figure 6.25. Pseudo-random arrangement of capacitors.

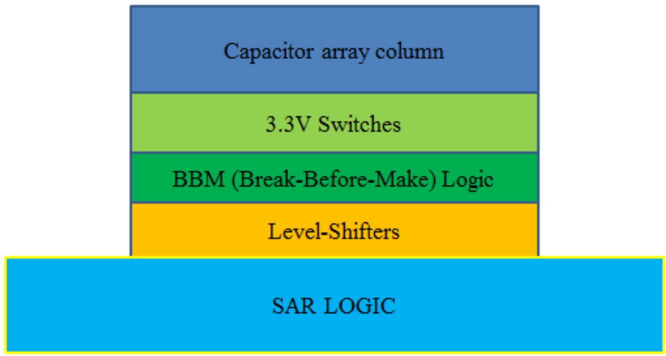


Figure 6.26. Arrangement of SAR logic, level shifters, BBM and capacitor array.

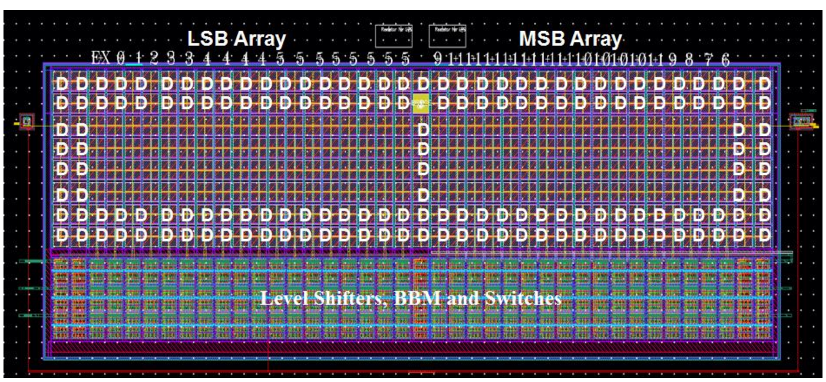


Figure 6.27. Complete DAC layout with capacitor array, switches, BBM and level shifters.

6.9.2 IO Pad Ring

Figure 6.28 shows IO ring arrangement. It consists of 64 bond-pads. The pitch between two adjacent bond-pads is 100 μm. Two bond-pads are double-bonded for the supply (VDD) and the ground (VSS). The parallel digital outputs from SAR ADC and all digital IO pads are placed on the left-hand side of the die. The said arrangement takes up an area of 2230 μm × 2230 μm.

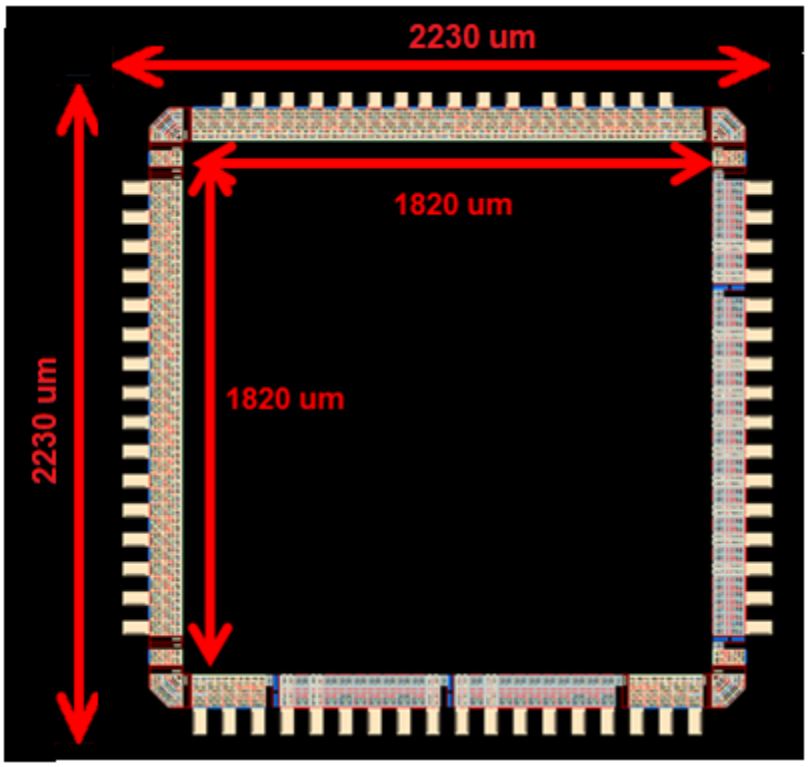


Figure 6.28. IO ring layout.

6.9.3 Full Chip Layout

The ADC layout along with the IO ring is shown in Figure 6.29. The dimensions of the core ADC are 640 μm × 370 μm. The vacant regions of the chip are filled with decoupling capacitors to provide on-chip decoupling for the supplies, references and VCM. A detailed version of the core ADC layout with individual blocks is shown in Figure 6.30.

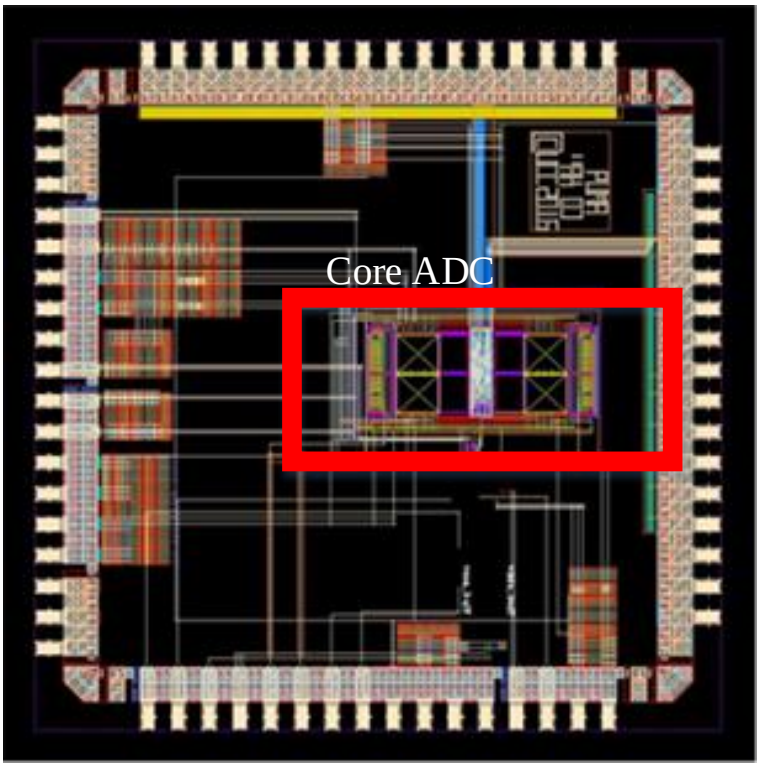


Figure 6.29. Core ADC and IO ring.

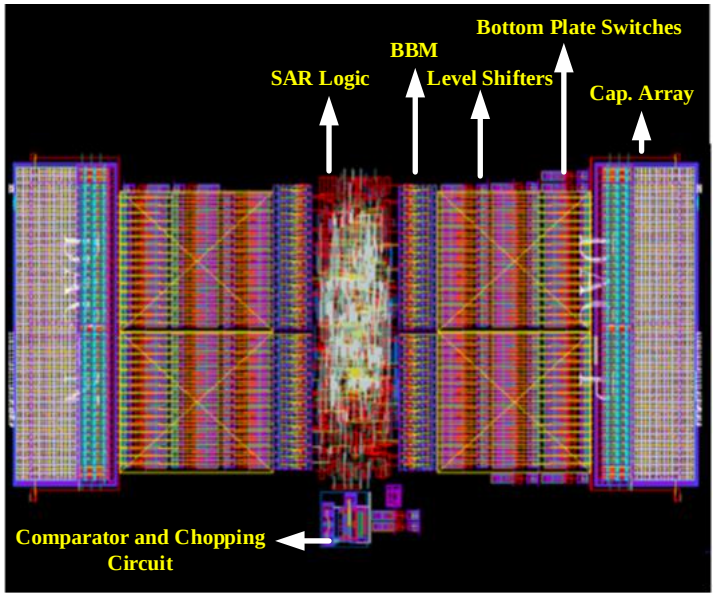


Figure 6.30. Core ADC sub-blocks.

6.10 Experimental Characterization

The chip micrograph of ADC is shown in Figure 6.31 which shows the SAR logic, level shifters, switches and capacitor array.

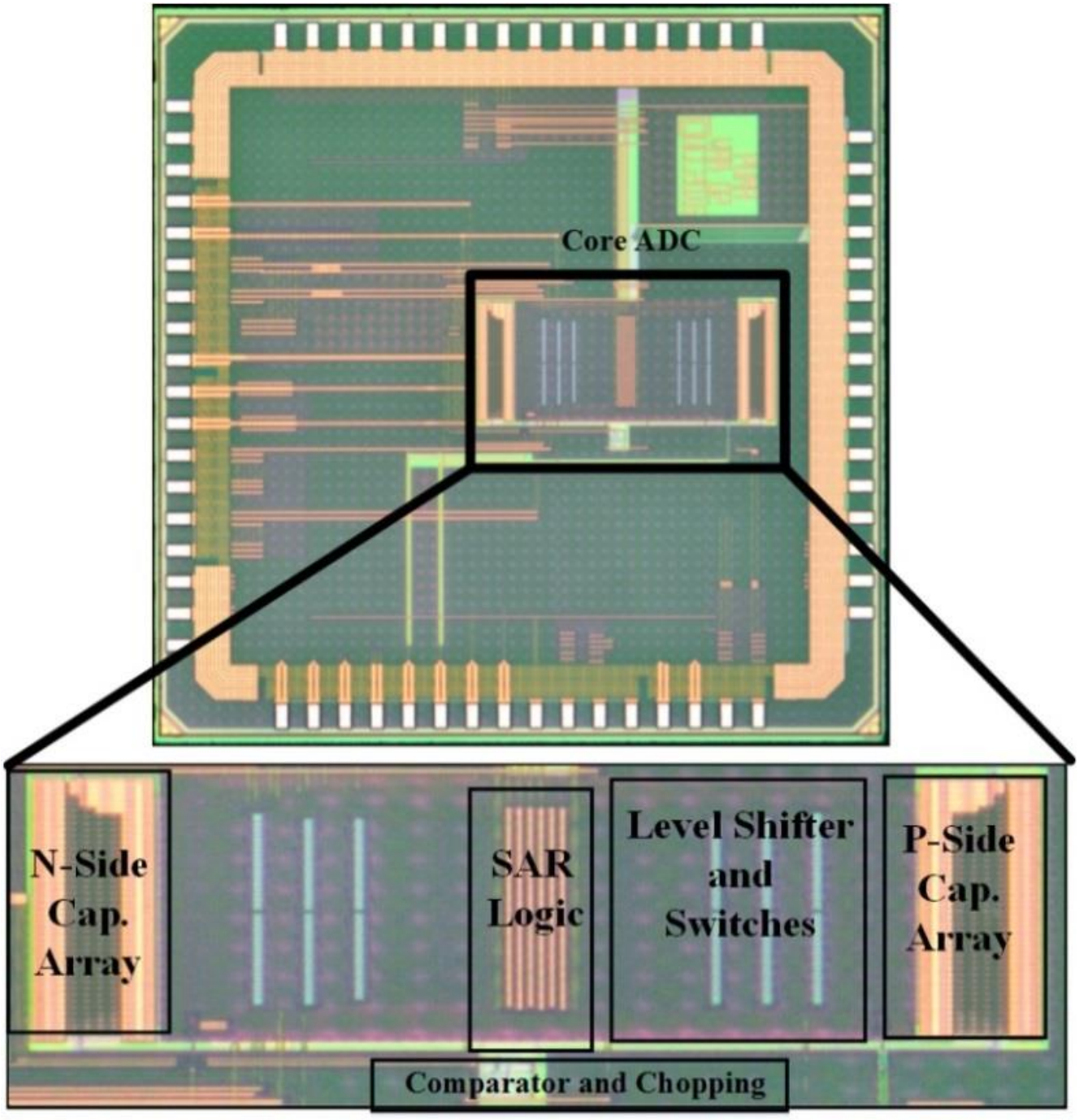


Figure 6.31. Chip micrograph and core ADC.

6.10.1 Test PCB

The test PCB schematic is shown in Figure 6.32 and a photograph of the resultant PCB is shown in Figure 6.33. In order to make the PCB debugging and operation easier, a simple schematic was employed for the test PCB. The following considerations highlight some of the test PCB aspects:

1. To minimise the bond-wire inductance caused due to lengthy bond wires of the package, the chip is directly wire bonded on the PCB.
2. The differential input signal is provided to the design-under-test (DUT) from an external signal generator. No AAFs were placed on the PCB. Filtering and common-mode of the differential signal can be generated from an external board e.g. breadboard.
3. All the power supply voltages (3.3 V, 1.2 V, 0 V,) common mode voltage (0.8 V), along with reference voltages (1.2 V and 0 V) are supplied externally without using any regulator on the PCB. Each of the supplies has a dedicated connector on the PCB. This results in more area consumption on the PCB but provides flexibility and ease of control. Anti-aliasing filtering of the input signal is provided using external capacitors and resistors.
4. Decoupling capacitors have been extensively used between all the power supplies, common mode, references (1.2 V) and grounds.
5. The PCB has 4 layers with separate ground and power planes.

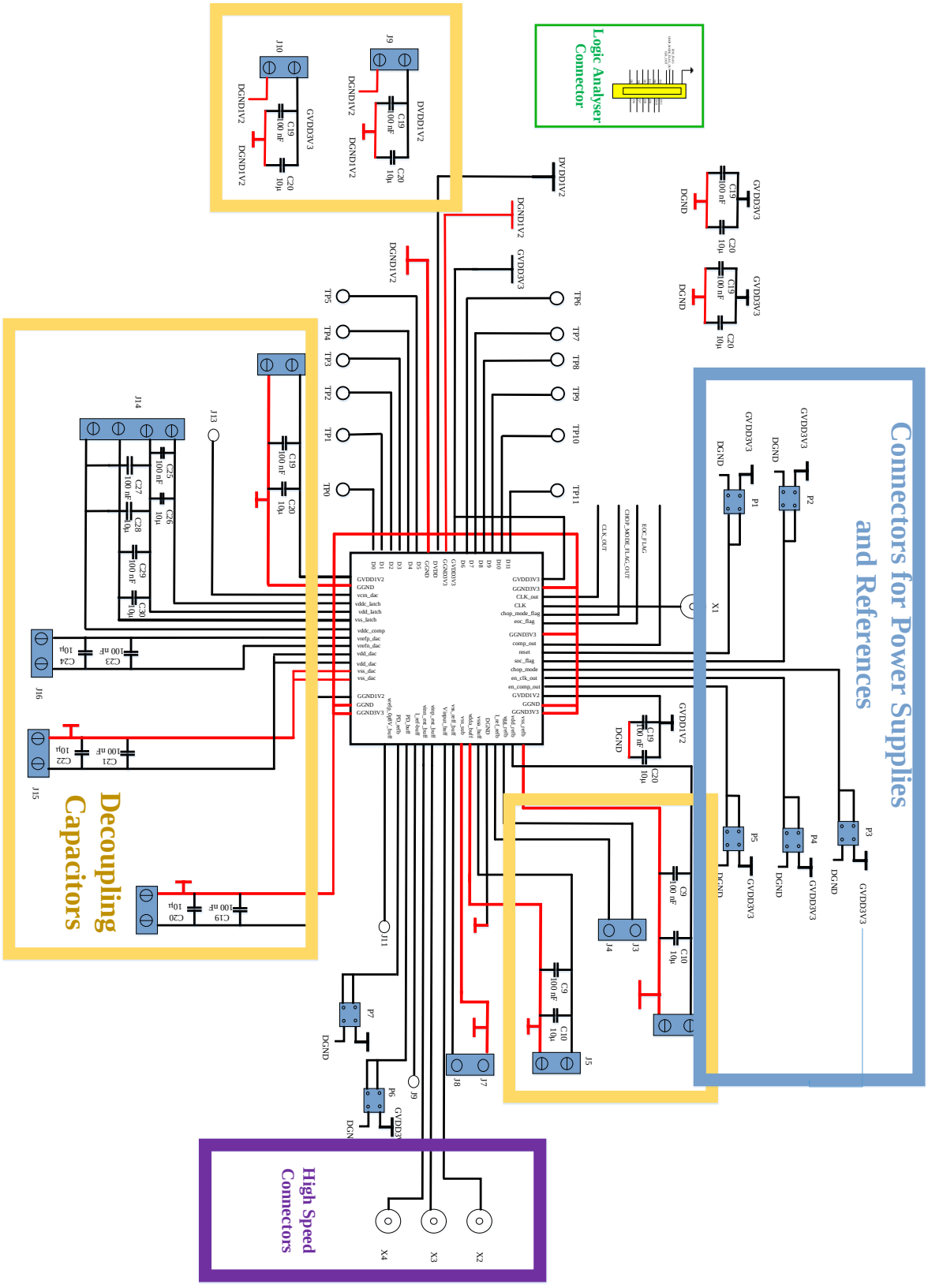


Figure 6.32. Test PCB schematic

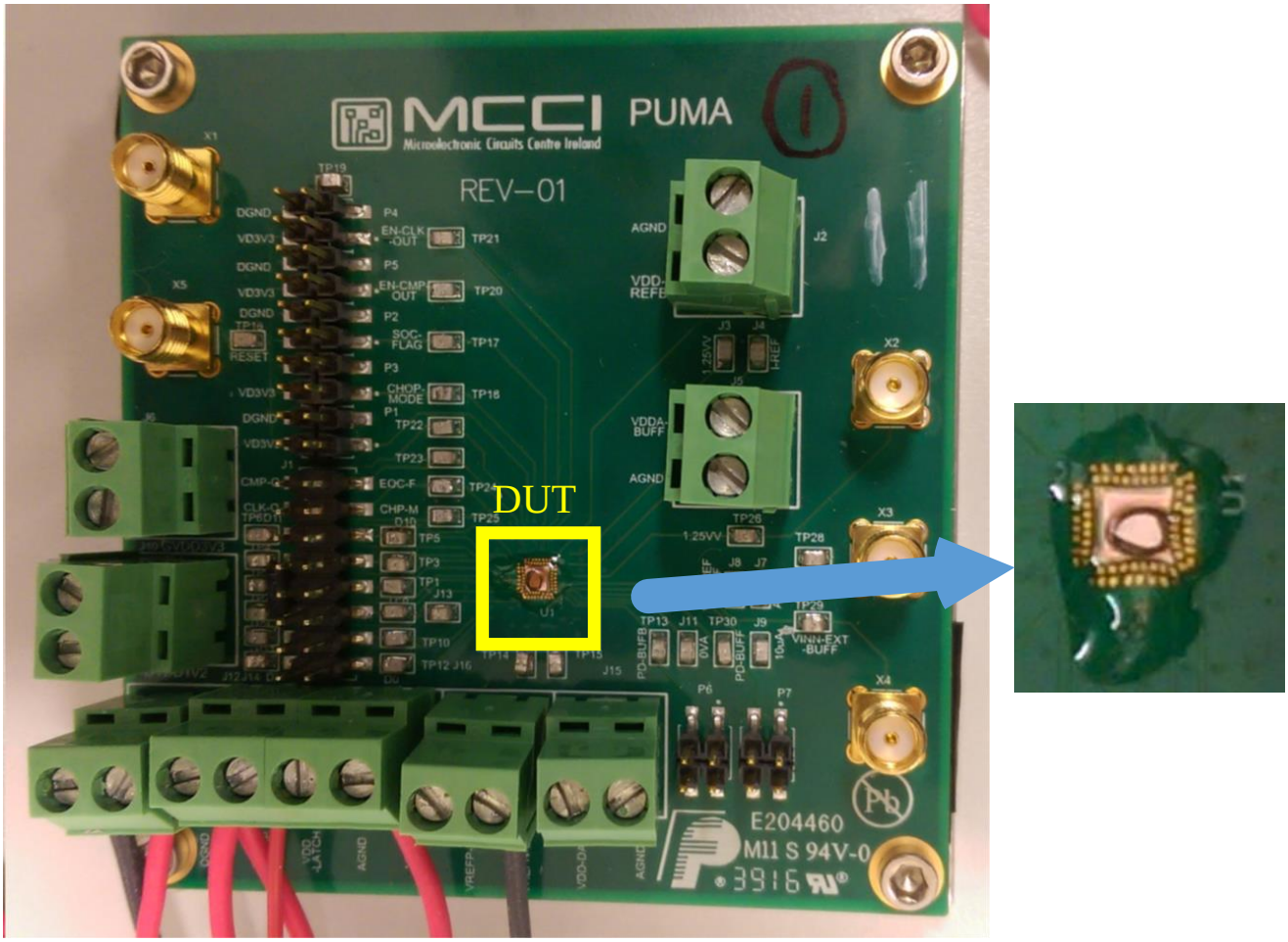


Figure 6.33. Photograph of the test-PCB with a close up of DUT

6.10.2 Test Setup

A block diagram of test setup is shown in Figure 6.34. A differential input or sinusoid signal is provided using an arbitrary function generator (Tektronix 3022C). A highly precise DC voltage source capable of providing the voltages with nV accuracy (Keithley 2602A) has been utilised for the reference and common mode voltage generation. The master clock is generated by an Agilent 33250A signal source. The digital output bit streams are captured by the oscilloscope (MSO 4104). A Labview® project on the workstation controls all the equipment and stores the data which is later processed in Matlab®.

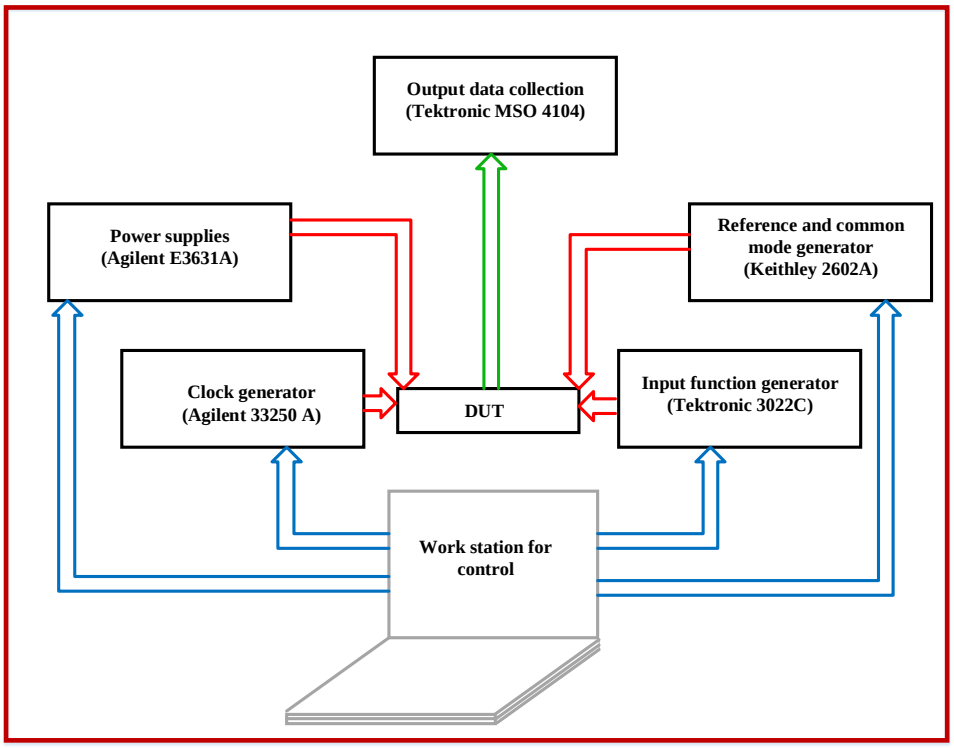


Figure 6.34. Block diagram of test setup

6.10.3 Measurement Results

The ADC has been characterised at an output data rate of 2 MS/s. The comparator, SAR logic and BBM circuit all operate at 1.2 V. The input and reference switches and level shifters operate from a 3.3 V supply.

At first, the ADC was run in the offset-calculation mode. To this end, ADC was characterised with differential DC inputs with different inputs i.e. 0-to-1.6 V as described in section. 6.8.1. The measured comparator offset is 340 μV.

The dynamic performance of the ADC is also characterised by means of applying a sinusoid signal to the input over the range of input frequencies 100 kHz-to-1 MHz i.e. Nyquist frequency. The oscilloscope collects 64 k points for each of the input tones applied. The output spectrum plots of 3 different frequencies are shown in Figure 6.35. The SNDR and the SFDR at

the Nyquist frequency are 69.3 dB and 79 dB, respectively, with no capacitor mismatch calibration. Figure 6.36 shows the SNDR and SFDR versus input frequency plot. The ADC achieves an ENOB of 11.22 without any capacitor mismatch calibration.

The linearity performance of the ADC can be extracted using a variety of tests. The code density test has been employed for the linearity performance characterization. This test involves deriving the digital output code histogram with a slowly varying input ramp. The test was conducted using a FS (0-to-1.6 V), differential ramp. The reconstructed ramp has a voltage range of 0-to-1.2 V, before digital scaling is applied, that validates the accuracy of the input signal scaling. The measured DNL and INL at 2 MS/s are shown in Figure 6.37, and are within 1.2/-1.0 LSB and 2.3/-2.2 LSB at 12 bits, respectively. The INL plot shows a saw-tooth characteristic at a code spacing of 128 (7 bits). As the ADC has a 6-6 BWA architecture, this characteristic manifests that top-plate parasitic on the MSB-DAC and LSB-DAC are not quite balanced. Nonetheless, considering the 11-bit performance, the measured DNL and INL are 0.6/-0.5 LSB and 1.15/-1.1 LSB, respectively. The DNL performance at 11 bits clearly demonstrates the required monotonic behaviour.

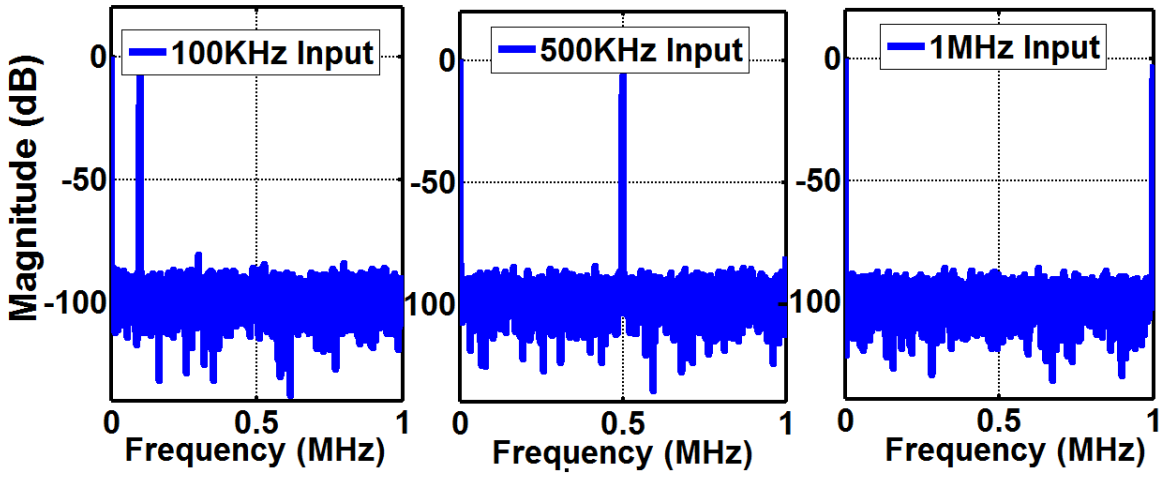


Figure 6.35. Measured FFT spectrum of 3 different input frequencies, 100 kHz, 500 kHz and 1 MHz

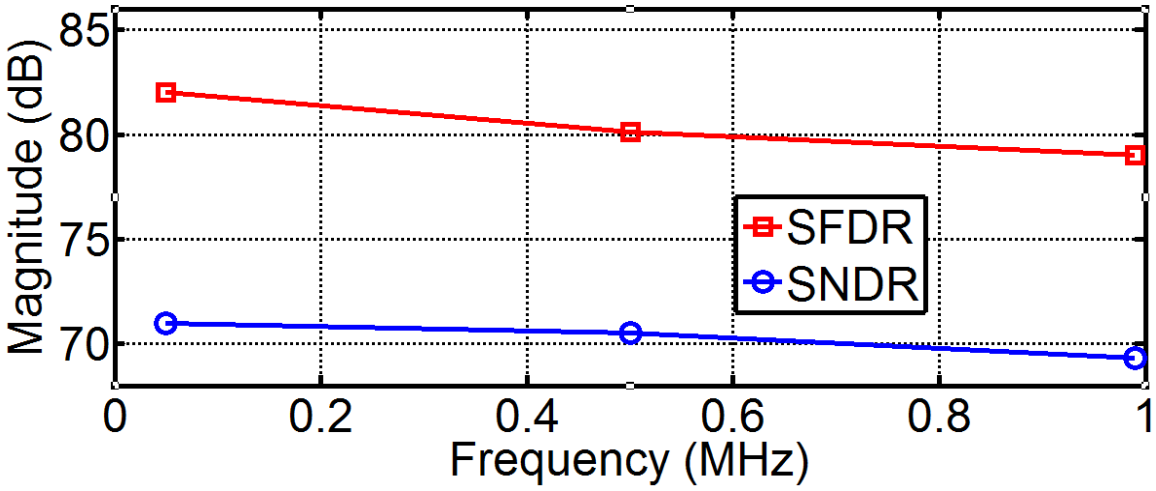


Figure 6.36. SNDR and SFDR vs. input frequency

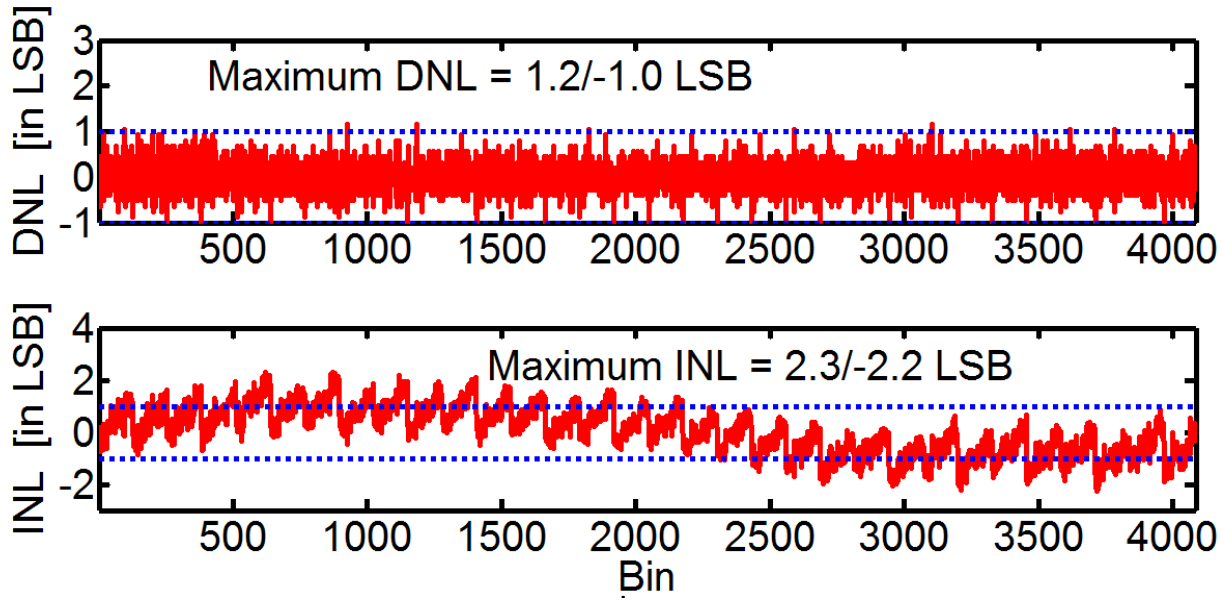


Figure 6.37. Measured INL and DNL at 2MS/s

The prototype consumes a total power of 0.82 mW. The comparator and the BBM circuit consume 0.13 mW, while the SAR logic takes 0.23 mW, all operating from a 1.2 V supply. The level shifters consume an additional 0.46 mW. Table 6.5 summarises the measured performance of the ADC. A comparison of the measured results with different state-of-art designs is presented in Table 6.6.

Table 6.5. Measured performance of SAR ADC

Process		0.13 μm
Active Area (mm^2)		0.24 (0.35 mm X 0.657 mm)
Supply Voltage		1.2/3
f_S (MHz)		2
Peak SFDR (dB) at 1 MHz		79
Peak SNDR (dB) at 1 MHz		69.3
Comparator Offset (LSB)		< 0.5
Power Consumption (mW)	Comparator and BBM	0.13
	SAR Logic	0.23
	Level Shifters	0.46

Table 6.6. Comparison of the measured performance with different state of the art designs

Specification	Technology (μm)	Supply Voltage VDD, (V)	Data Rate (MS/s)	Input Signal Swing(V)	DNL (LSB)	INL (LSB)	Resolution	ENOB	Power (mW)	FoM_W (fJ/conv.step)	FoM_S (dB)
[148]	0.18	1	0.1	1 **(V_{REF})**	[b.] ±2 .4	[b] ±2.8	12	9.4	0.0038	56	159.53
[179]	0.13	1.2	50	2 **($\pm V_{REF}$)**	0.91/-0.63	1.27/-1.36	10	9.18	0.82	29	161.86
[180]	0.13	1	11		±0.8	±3.0	12	10.1	3.57	311	154.43
[182]	0.065	0.7	1.00E-03	0.7 (V_{REF})	0.48/-0.55	0.52/-0.61	10	9.1	3.00E-06	5.5	161.86
[183]	0.04	0.45	0.2	0.9	0.44	0.45	10	8.95	8.40E-05	0.85	154.43
[184]	0.18	0.45	0.2	0.9	<0.5	<1	9	8.27	9.40E-04	22	159.53
[185]	0.04	1	6.4		1.08/-1	3.79	13	10.35	0.046	5.5	168.76
[186]	0.065	1.2	50	2.4 ($\pm V_{REF}$)	0.5/-0.7	1.0/-0.9	12	10.9	2.09	21.9	176.39
[187]	0.13	1.2	[a.] 0.25				10	12	0.061	59.5	161.81
[188]	0.35	3.3	0.25	50	0.55	1.81	14	13.03	4.29	2050	172.49
[189]	0.18	0.75	0.01	0.75	0.6/-0.37	0.94/-0.89	11	9.76	250E-6	28.8	168.15
[190]	0.065	1.2	1.25		0.74/-0.53	0.74/-0.80	12	11.25	44.1E-3	14.4	167.11
[191]	0.18	1.8	1.07		0.6/-0.6	1.2/-1.2	10	8.8	63.6E-3	130.8	154.8
This Work	**0.13**	**1.2/3.3**	**2**	**3.2 ($\pm 1.33 V_{REF}$)**	**1.2/-1.0**	**2.3/-2.2**	**12**	**11.22**	**0.9** [c.] **0.44**	**189** [c.] **93**	**159.76** [c.] **162.86**

[a] Sampling Rate is 2 MS/s with an oversampling ratio of 8. [b] Extrapolated to 12 bits [c] Without level shifters

One of the salient features of the proposed ADC compared to the similar architectures designed in the same process nodes, ([179] and [180]), is the embedded input scaling. The chip is can digitize an extended input range of 3.2 V_{pp-d}, compared to 2 V_{pp-d} and 2.4 V_{pp-d} in previous publications art i.e. [179] and [186] which corresponds to ±1.33 times the reference voltage. By employing the reduced number of capacitors during the sampling phase, other different scaling factors can be easily achieved. This makes it an attractive option for the sensor-based systems. The designed ADC has also shown comparable performance in terms of linearity. The architecture reported in [185] achieves a DNL of 1.08/-1 LSB and INL of 3.79 LSB but at the cost of background calibration for capacitor mismatch and comparator offset. Similarly, the architecture reported in [186] also used a background calibration for capacitor mismatch. The designed ADC does not require any capacitor calibration and can achieve a monotonic behaviour at 11-bits. Other competitive SAR ADCs are the ones reported in [187] and [188]. The former includes noise-shaping while the later uses a higher supply voltage. [190] and [191] are two other recent examples of SAR ADCs. The architecture reported in [190] is a 12-bit 8-4 BWA DAC neural-network-based SAR ADC. [191] is also a Secure SAR ADC architecture.

Overall, it can be concluded that the input scaling technique presented in this design can be easily embedded in a SAR ADCs, while achieving a performance competitive with the state of the art. The presented chip does not achieve the lowest FoM, although that was not the main design goal of this design. Instead, the main design objective and an attractive feature of the ADC circuit is the offset calculation mechanism. This technique enables a dynamic control of offset calculation over the whole operational life of the chip. All these features, together with the measured performance metrics, make the proposed ADC a suitable option for integration in a digital controller of DC/DC converters.

6.11 Conclusion

This chapter described the details of a 12-bit SAR ADC for a digital controller in a DC/DC converter. Starting from the brief introduction of PMICs, a detailed analysis of ADCs for DC/DC converters was presented. Based upon the architectural level exploration of the different ADC architectures, a SAR ADC was selected for the target application. Finally, the circuit level design, layout and experimental characterisation of the proposed 12-bit SAR ADC capable of digitizing an extended input range of 3.2 $V_{pp\text{-}d}$ which is ±1.33 times the reference voltage, having improved linearity and offset correction, was presented.

Chapter 7: Conclusions and Future Work

7.1 Conclusions

The research work carried out in this thesis has focused on the design of high-performance ADCs considering two different architectures which dominate the current state of the art: ΣΔMs and SAR. ΣΔMs can achieve higher resolution while the SAR ADCs are better suited for the low power applications with low to medium resolution.

In that scenario, the thesis has discussed the architectural level exploration, circuit level design, implementation and characterization of these ADCs for two different types of applications namely: SDR and PMICs.

In the context of SDR, in addition to the existing communications standards, a modern radio receiver would need to support today's evolving systems such as IoTs, video-on-demand and machine-to-machine communications etc. The ADC is a mandatory component required to interface between the analog and digital world in a receiver. An ideal ADC for such receivers should be capable of directly digitizing the input RF signals just after the antenna thus transferring the entire signal processing to the digital domain. BPΣΔMs are an attractive option for such applications because these can be used to digitize the signals located at higher input frequencies while achieving higher resolutions. The first part of the thesis has described the details of two such modulators. Initially, the synthesis methodology for the implementation of a sub-sampling continuous time BP-ΣΔM ADC with raised-cosine FIR feedback DAC has been developed. Based upon this methodology, a 4^{th}-order continuous time BP-ΣΔM ADC with reduced number of loop-filter coefficients with respect to previous approach has been described. The proposed modulator can achieve an efficient and robust digitization of 0.455-to-5 GHz

signals with a scalable 8-to-15 bit effective resolution within a 0.2-to-30 MHz signal bandwidth, with a reconfigurable 1-to-4 GHz sampling rate. These advantages make the proposed modulator very suited for RF digitization in the next generation of SDR mobile systems. To contribute to the same topic, the design and implementation of a 4^{th}-order reconfigurable SC single-loop CRFF discrete time low-pass/band-pass ΣΔM ADC in 90-nm 1.2V CMOS has been presented. Both the architecture and circuit-level reconfiguration strategies are combined to achieve a competitive performance. The experimental results have validated the correct operation of the modulator over an input tuning range of 0-to-18 MHz while operating at 100 MHz sampling rate. The ADC achieves a peak resolution of 8-to-9 bits while consuming 16 mW.

PMICs are another important part of modern electronic systems that generate, manage, control and distribute stable voltages to other circuits and blocks. These ICs have become an integral part of electronic systems including automotive, healthcare, computing, artificial intelligence, neural networks, IoTs etc. to optimise energy management, efficiency and sustainability. One of the important sub-blocks of a PMIC is the output power management unit which largely consists of different DC/DC converters. In recent years, there has been a surge in digitally controlled DC/DC converters. The ADC is a key part of digitally controlled DC/DC converters which is used to digitize the sensed voltages and currents. Unlike the signal processing counterparts, these ADCs require an excellent DC performance. In that context, owing to their lower power consumption, simpler architecture and other advantages, SAR ADCs are better suited for such applications. In the second part of the thesis, the design and implementation of a 12-bit SAR ADC for such applications has been presented. Two important features of the presented SAR ADC are the input sampling scaling technique and the comparator offset removal. Using an input sampling scaling technique an extended input range of 3.2 V_{pp-d}

(±1.33 V_{REF}) can be digitized. The same sampling scaling technique can be easily extended to obtain other scaling factors of the input signal. The SAR ADC can be run in offset-calculation mode and the comparator offset can be obtained dynamically. Also, to achieve a lower DNL, a 4-level segmentation has been used. The ADC is implemented in a 0.13-µm 1.2V/3.3V CMOS and achieves an SNDR of 69.3 dB and an SFDR of 79 dB without calibration, while consuming 0.82 mW. The ADC has a measured DNL of 1.2/-1.0 LSB and INL of 2.3/-2.2 LSB at 12-bit making it an attractive option for the targeted application.

7.2 Future Work

In terms of the ΣΔM ADC for SDR applications, one area of potential work is the circuit level implementation of the proposed 4th-order continuous time BP-ΣΔM ADC. The advent of the latest CMOS technologies (28nm, 7nm, 5nm, 4nm) have paved the way for the design of different analog and mixed signal blocks operating in multi-GHz regions. These deep sub-micron CMOS technologies enable the migration of the ADC closer to the antenna, to enable the deployment of the SDR architecture.

The 4th-order SC-ΣΔ ADC with a tuneable notch, has been described in the thesis. One possible extension to the described work is the CT implementation that can operate at higher sampling rates. The loop filter coefficients in the CT-implementation can be realised with the current sources which can be used to reduce the f_N tuning steps.

The second section of the thesis presented the design of a 12-bit SAR ADC. The DAC inside the DAC employs the custom MOM capacitors. The size of these capacitors can be further reduced for lower power consumption while keeping the linearity in view. The SAR ADC has employed a 4-level capacitor segmentation that can be further extended to 5 or 6-level. The

capacitor segmentation algorithm applied has reduced the DNL but the INL remains the same. INL improvement of the ADC is another potential area of research. The capacitor-swapping technique proposed in [192] improves the capacitor-DAC middle-code transition error that results in improved linearity. The same technique can be extended to multi-level and combined with the capacitor segmentation to obtain better INL and DNL.

List of Publications Derived from this PhD Dissertation.

1. **S. Asghar,** S. S. Afridi, A. Pillai, A. Schuler, J. M. de la Rosa and I. O'Connell, "A 2-MS/s, 11.22 ENOB, extended input range SAR ADC with improved DNL and Offset calculation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 11, pp. 3628-3638, Nov. 2018.

2. **S. Asghar,** S. Afridi, A. Pillai, A. Schuler, J. M. de la Rosa and I. O'Connell, "A 2MS/s, 11.22 ENOB, 3.2 Vpp-d SAR ADC with improved DNL and offset calculation," in Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, May 2018.

3. **S. Asghar**, R. del Río and J.M. de la Rosa, "Undersampling RF-to-Digital CT sigma-delta modulator with tunable notch frequency and simplified Raised-Cosine FIR feedback DAC", in Proceedings of the 2013 International Symposium on Circuits and Systems (ISCAS), Beijing, China, May 2013

4. **S. Asghar**, R. del Río and J.M. de la Rosa, "A 0.2-to-2MHz BW, 50-to-86dB SNDR, 16-to-22mW flexible 4th-order sigma- delta modulator with DC-to-44MHz tunable center frequency in 1.2-V 90-nm CMOS", in Proceedings of the 2012 IEEE/IFIP 20th International on VLSI and System-on-Chip, Santa Cruz, USA, 2012

Other Related Publications

1. A.Morgado, J.G. García-Sánchez, **S. Asghar**, L.I. Guerrero, R. del Río and J.M. de la Rosa, "A power-scalable concurrent cascade 2-2-2 SC sigma-delta modulator for software defined radio", in Proc. of the International Symposium on Circuits and Systems(ISCAS), pp. 516-519, Seoul, Korea, May 2012.

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Appendices

APPENDIX A

Mathematica Code for Coefficients of 4th-order CT BP-ΣΔM

```
(*CT Modulator consists of 4 feedback paths. This script shows the \
script for half delayed path and having one resonator path*)

num = 1/(2*0.076)

(*here num is calculated for each of notch frequency. e.g. \
0.25*fs means pi/2, therefore  in this case
 num=1/(0.25*2 )=2
 Therefore pi/num=pi/2*)



m = 0.5 (*m=1-td/Ts while td=delay time*)

(*As mentioned in the pdf to calculate the modified z-transform, we \
need to calculate the values of expression at each poles*)

(*for 1st pole*)
Clear[p1, wo, wdac, v1, dv1, v1]  (*  p1=1st poles, wo=resonant \
frequency, wdac=DAC frequency, *)
v1 = (s -     p1) (wo   Exp[      m*s] wdac^2)/(((s^2 + wo^2) (s^2 + wdac^2)
(z - Exp[s])))
wo = Pi/num
wdac = 2*Pi
T = 1

p1 = -I Pi/num

frac1 = Limit[v1, s -> p1]
(*for 2nd pole*)
```

```
Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -     p1) (wo   Exp[
      m*s] wdac^2)/(((s^2 + wo^2) (s^2 + wdac^2) (z - Exp[s])))
wo = Pi/num
wdac = 2*Pi
T = 1


p1 = I Pi/num


frac2 = Limit[v1, s -> p1]


(*for 3rd pole*)


Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -      p1)   (wo^2    Exp[       m*s]  wdac^2)/(((s^2  +  wo^2)  (s^2  +
wdac^2) (z - Exp[s])))
wo = Pi/num
wdac = 2*Pi
T = 1


p1 = -I Pi*2


frac3 = Limit[v1, s -> p1]



(*for 4th pole*)


Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -      p1)  (wo^2    Exp[       m*s]  wdac^2)/(((s^2  +  wo^2)  (s^2  +
wdac^2) (z - Exp[s])))
wo = Pi/num
wdac = 2*Pi
T = 1
```

```
p1 = I Pi*2

frac4 = Limit[v1, s -> p1]


gh = Numerator[Together[frac1 + frac2]]

 ij = Expand[(gh *  (z - 1))/z^2]

(*it is multiplied with (z-1)/z  which is z-transform of [1-e(-Ts)], \
while unit delay in feedback path is also taken into account*)

Apart[(ij)/(z^2 - 1.776 z + 1)]

(*It is partially fractionated and resulting terms have two types of \
terms. 1st one is (0.21123118065653965`-0.1093843189227223` \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)+(0.21123118065653965`+0.10938431892272218` \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \[ImaginaryI])+z) which \
have the poles at pi/6.57894736   0.1520fs.Other terms are \
-(0.23787295118979684`-1.1102230246251565`*^-16 \
\[ImaginaryI])/z^2-(0.4224623613130793`-1.1102230246251565`*^-16 \
\[ImaginaryI])/z which need to be compensated *)

Numerator[ Together[(   0.21123118065653965` -      0.1093843189227223` I)/((-
0.888`   -   0.4598434516223972`   I)   +   z)   +   (     0.21123118065653965`
+     0.10938431892272218` I)/((-0.888` + 0.4598434516223972` I) + z)]]


Expand[%*(z^2 - 1.776 z + 1)]

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
(*CT Modulator consists of 4 feedback paths. This script shows the \
script for zero delayed path and having one resonator path*)

num = 1/(2*0.076)

(*Overhere num is calculated for each of notch frequency. e.g. \
0.25*fs means pi/2, therefore  in this case
 num=1/(0.25*2 )=2
 Therefore pi/num=pi/2*)


m = 1   (*m=1-td/Ts while td=delay time*)

(*As mentioned in the pdf to calculate the modified z-transform, we \
need to calculate the values of expression at each poles*)

(*for 1st pole*)
Clear[p1, wo, wdac, v1, dv1, v1]  (*  p1=1st poles, wo=resonant \
frequency, wdac=DAC frequency, *)
v1 = (s -
    p1) (wo   Exp[
      m*s] wdac^2)/(((s^2 + wo^2) (s^2 + wdac^2) (z - Exp[s])))
wo = Pi/num
wdac = 2*Pi
T = 1

p1 = -I Pi/num

frac1 = Limit[v1, s -> p1]
(*for 2nd pole*)
Clear[p1, wo, wdac, v1, dv1, v1]
```

```
v1 = (s -     p1) (wo   Exp[      m*s] wdac^2)/(((s^2 + wo^2) (s^2 + wdac^2)
(z - Exp[s])))

wo = Pi/num

wdac = 2*Pi

T = 1


p1 = I Pi/num


frac2 = Limit[v1, s -> p1]


(*for 3rd pole*)


Clear[p1, wo, wdac, v1, dv1, v1]

v1 = (s -     p1)   (wo^2    Exp[       m*s] wdac^2)/(((s^2 + wo^2) (s^2 +
wdac^2) (z - Exp[s])))

wo = Pi/num

wdac = 2*Pi

T = 1


p1 = -I Pi*2


frac3 = Limit[v1, s -> p1]




(*for 4th pole*)


Clear[p1, wo, wdac, v1, dv1, v1]

v1 = (s -     p1) (wo^2    Exp[       m*s] wdac^2)/(((s^2 + wo^2) (s^2 +
wdac^2) (z - Exp[s])))

wo = Pi/num

wdac = 2*Pi

T = 1
```

```
p1 = I Pi*2

frac4 = Limit[v1, s -> p1]


gh = Numerator[Together[frac1 + frac2]]

 ij = Expand[(gh *  (z - 1))/z^2]

(*it is multiplied with (z-1)/z  which is z-transform of [1-e(-Ts)], \
while unit delay in feedback path is also taken into account*)

Apart[(ij)/(z^2 - 1.776 z + 1)]

(*It is partially fractionated and resulting terms have two types of \
terms. 1st one is (0.23112490777807002`-0.056293048383779576` \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)+(0.23112490777807002`+0.056293048383779576` \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \[ImaginaryI])+z) which \
have the poles at pi/6.57894736   0.1520fs.Other terms are \
0.46224981555614003`/z which need to be compensated *)

Numerator[
 Together[(   0.23112490777807002` -     0.056293048383779576` I)/((-0.888` -
0.4598434516223972`     I)     +             z)     +     (0.23112490777807002`
+     0.056293048383779576` I)/((-0.888` + 0.4598434516223972` I) + z)]]


Expand[%*(z^2 - 1.776 z + 1)]


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
(*CT Modulator consists of 4 feedback paths. This script shows the \
script for half delayed path and having two resonators path*)

num = 1/(0.076*2)
(*Overhere num is calculated for each of notch frequency. e.g. \
0.25*fs means pi/2, therefore  in this case
 num=1/(0.25*2 )=2
 Therefore pi/num=pi/2*)


m = 0.5       (*m=1-td/Ts while td=delay time*)

(*As mentioned in the pdf to calculate the modified z-transform, we \
need to calculate the values of expression at each poles*)



(*for 1st pole*)
Clear[p1, wo, wdac, v1, dv1, v1]  (*  p1=1st poles, wo=resonant \
frequency, wdac=DAC frequency, *)

mul = m*s
v1 = (s -      p1)^2 (wo^2 s  Exp[      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 +
wdac^2) (z - Exp[s])))
wo = 3.14/num
wdac = 2*3.14
T = 1     (* Sampling Time is normalized to 1*)

p1 = -I 3.14/num  (*1st pole*)
dv1 = D[v1, s]            (*Derivative of v1*)
frac1 = Limit[dv1, s -> p1] (* Evaluating dv1 when s\[Rule]pole1*)
```

```
(*for 2nd pole*)

Clear[p1, wo, wdac, v1, dv1, v1]

v1 = (s -      p1)^2 (wo^2 s  Exp[      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 +
wdac^2) (z - Exp[s])))

wo = 3.14/num

wdac = 2*3.14

T = 1


p1 = I 3.14/num

dv1 = D[v1, s]

frac2 = Limit[dv1, s -> p1]




(*for 3rd pole*)


Clear[p1, wo, wdac, v1, dv1, v1]

v1 = (s -      p1) (wo^2 s Exp[       mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 +
wdac^2) (z - Exp[s])))

wo = 3.14/num

wdac = 2*3.14

T = 1


p1 = -I 3.14*2


frac3 = Limit[v1, s -> p1]

(*for 4th pole*)

Clear[p1, wo, wdac, v1, dv1, v1]

v1 = (s -

    p1) (wo^2 s Exp[       mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 + wdac^2) (z -
Exp[s])))

wo = 3.14/num

wdac = 2*3.14
```

```
T = 1

p1 = I 3.14*2

frac4 = Limit[v1, s -> p1]



gh34 = Numerator[  Together[frac3 +      frac4]]            (* Numerator of
combination of 3rd and 4th \

fractions *)


gh = Numerator[  Together[frac1 +     frac2]]                    (* Numerator
of combination of 1st and \

2nd fractions *)


den = Denominator[  Together[frac1 +     frac2]]              (* Denominator
of combination of 1st and 2nd \

fractions *)


(*Numerator of 3rd and 4th fractions is (0.005843299525388367`+0.` \

\[ImaginaryI])-(0.005843299525388367`+0.` \[ImaginaryI]) z it may be \

written as -0.005843299525388367*(z-1)*)



ij34 = (-0.005843306936293634*(z^2 - 1.776 z + 1)^2)/z^2



(*As frac1+frac2 =(-0.005843299525388367*(z-1))/((-1+z) ((-1+z) we \

multiply it (z-1)/z which is z-transform of [1-e(-Ts)], while unit \

delay in feedback path is also taken into account here.Moreover it \

is multiplied and divided with (z^2-1.776z+1)^2. Resultant is ij34*)

 ij = Expand[(gh *  (z - 1))/z^2]



(*frac3+frac4 is combined and then multiplied with (z-1)/z which is \
```

```
z-transform of [1-e(-Ts)],*)


afo = Apart[(ij34 + ij)/(z^2 - 1.776 z + 1)^2]


(*All of the fractions are combined and then partially fractionated. \
Resultant terms consist of two types of terms. One

is [(0.05674223809011536`+6.106226635438361`*^-16 \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)^2-(0.10458793378536996`+0.07857423430477051` \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)+(0.05674223809011464`+1.1102230246251565`*^-16 \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \
\[ImaginaryI])+z)^2-(0.10458793378536854`-0.0785742343047709` \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \[ImaginaryI])+z)],

that only shows the fractions having poles at \
pi/6.57894736   0.1520fs. Other terms are \
0.01684786921342306`/z^2+0.2091758675707385`/z which need to be \
compensated*)


Together[(  0.05674223809011536` +    6.106226635438361`*^-16  I)/((-0.888` -
0.4598434516223972` I) +     z)^2 - (0.10458793378536996` +
   0.07857423430477051` I)/((-0.888` - 0.4598434516223972` I) + z) + (
    0.05674223809011464`   +      1.1102230246251565`*^-16   I)/((-0.888`   +
0.4598434516223972` I) +     z)^2 - (  0.10458793378536854` -
   0.0785742343047709` I)/((-0.888` + 0.4598434516223972` I) + z)]
6.57895


0.5
```

```
0.5 s

(E^(0.5 s) s (-p1 + s)^2 wdac^2 wo^2)/((s^2 + wdac^2) (s^2 +
   wo^2)^2 (-E^s + z))

0.47728

6.28

1

-0.47728 I

(8.98392 E^(1.5 s)
   s (0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s +
    z)^2) - (
 17.9678 E^(0.5 s)
   s^2 (0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 +
    s^2)^2 (-E^s + z)) - (
 35.9357 E^(0.5 s)
   s^2 (0.47728 I + s)^2)/((0.227796 + s^2)^3 (39.4384 + s^2) (-E^s +
    z)) + (17.9678 E^(0.5 s)
   s (0.47728 I + s))/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s +
    z)) + (8.98392 E^(
  0.5 s) (0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 +
    s^2) (-E^s + z)) + (
 4.49196 E^(0.5 s)
   s (0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s + z))

(0.0415874 + I (0.0433568 + 0.0589967 z) +
 0.0113456 z)/((-0.888248 + 0.459365 I) + z)^2
```

```
(E^(0.5 s) s (-p1 + s)^2 wdac^2 wo^2)/((s^2 + wdac^2) (s^2 +
   wo^2)^2 (-E^s + z))

0.47728

6.28

1

0.47728 I

(8.98392 E^(1.5 s)
   s (-0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s +
    z)^2) - (
 17.9678 E^(0.5 s)
   s^2 (-0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 +
    s^2)^2 (-E^s + z)) - (
 35.9357 E^(0.5 s)
   s^2 (-0.47728 I + s)^2)/((0.227796 + s^2)^3 (39.4384 + s^2) (-E^s +
     z)) + (17.9678 E^(0.5 s)
   s (-0.47728 I + s))/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s +
    z)) + (8.98392 E^(
  0.5 s) (-0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 +
    s^2) (-E^s + z)) + (
 4.49196 E^(0.5 s)
   s (-0.47728 I + s)^2)/((0.227796 + s^2)^2 (39.4384 + s^2) (-E^s +
    z))

(0.0415874 + I (-0.0433568 - 0.0589967 z) +
 0.0113456 z)/((-0.888248 - 0.459365 I) + z)^2
```

```
(E^(0.5 s) s (-p1 + s) wdac^2 wo^2)/((s^2 + wdac^2) (s^2 +
   wo^2)^2 (-E^s + z))

0.47728

6.28

1

-6.28 I

-((0.00292165 + 4.65318*10^-6 I)/((-0.999995 - 0.0031853 I) + z))

(E^(0.5 s) s (-p1 + s) wdac^2 wo^2)/((s^2 + wdac^2) (s^2 +
   wo^2)^2 (-E^s + z))

0.47728

6.28

1

6.28 I

-((0.00292165 - 4.65318*10^-6 I)/((-0.999995 + 0.0031853 I) + z))

(0.0058433 + 0. I) - (0.0058433 + 0. I) z

(-0.0226912 +
   0. I) - (0.151268 + 0. I) z + (0.151268 + 0. I) z^2 + (0.0226912 +
    0. I) z^3
```

```
((-0.888248 - 0.459365 I) + z)^2 ((-0.888248 + 0.459365 I) + z)^2

-((0.00584331 (1 - 1.776 z + z^2)^2)/z^2)

(-0.302536 + 0. I) + (0.0226912 + 0. I)/z^2 + (
 0.128577 + 0. I)/z + (0.128577 + 0. I) z + (0.0226912 + 0. I) z^2

(0.0567422 + 6.10623*10^-16 I)/((-0.888 - 0.459843 I) + z)^2 - (
 0.104588 + 0.0785742 I)/((-0.888 - 0.459843 I) + z) + (
 0.0567422 + 1.11022*10^-16 I)/((-0.888 + 0.459843 I) + z)^2 - (
 0.104588 - 0.0785742 I)/((-0.888 + 0.459843 I) + z) + (
 0.0168479 - 6.93889*10^-17 I)/z^2 + (0.209176 - 3.88578*10^-16 I)/z

((0.323502 -
   1.17961*10^-15 I) - (0.868953 - 1.56819*10^-15 I) z + (0.742993 -
    9.99201*10^-16 I) z^2 - (0.209176 -
    3.88578*10^-16 I) z^3)/(((-0.888 - 0.459843 I) +
   z)^2 ((-0.888 + 0.459843 I) + z)^2)

afo

(0.0567422 + 6.10623*10^-16 I)/((-0.888 - 0.459843 I) + z)^2 - (
 0.104588 + 0.0785742 I)/((-0.888 - 0.459843 I) + z) + (
 0.0567422 + 1.11022*10^-16 I)/((-0.888 + 0.459843 I) + z)^2 - (
 0.104588 - 0.0785742 I)/((-0.888 + 0.459843 I) + z) + (
 0.0168479 - 6.93889*10^-17 I)/z^2 + (0.209176 - 3.88578*10^-16 I)/z

Chop[%]

0.0567422/((-0.888 - 0.459843 I) + z)^2 - (
 0.104588 + 0.0785742 I)/((-0.888 - 0.459843 I) +
  z) + 0.0567422/((-0.888 + 0.459843 I) + z)^2 - (
```

```
 0.104588 - 0.0785742 I)/((-0.888 + 0.459843 I) +

  z) + 0.0168479/z^2 + 0.209176/z


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


(*CT Modulator consists of 4 feedback paths. This script shows the \
script for zero delayed path and having two resonators path*)

num = 1/(0.076*2)
(*Overhere num is calculated for each of notch frequency. e.g. \
0.25*fs means pi/2, therefore  in this case
 num=1/(0.25*2 )=2
 Therefore pi/num=pi/2*)


m = 1     (*m=1-td/Ts while td=delay time*)

(*As mentioned in the pdf to calculate the modified z-transform, we \
need to calculate the values of expression at each poles*)



(*for 1st pole*)
Clear[p1, wo, wdac, v1, dv1, v1]  (*  p1=1st poles, wo=resonant \
frequency, wdac=DAC frequency, *)

mul = m*s
v1 = (s -
     p1)^2 (wo^2 s  Exp[
      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 + wdac^2) (z - Exp[s])))
wo = 3.14/num
wdac = 2*3.14
T = 1     (* Sampling Time is normalized to 1*)

p1 = -I 3.14/num  (*1st pole*)
dv1 = D[v1, s]            (*Derivative of v1*)
frac1 = Limit[dv1, s -> p1] (* Evaluating dv1 when s\[Rule]pole1*)



(*for 2nd pole*)
Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -
     p1)^2 (wo^2 s  Exp[
      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 + wdac^2) (z - Exp[s])))
wo = 3.14/num
wdac = 2*3.14
T = 1

p1 = I 3.14/num
dv1 = D[v1, s]
frac2 = Limit[dv1, s -> p1]
```

```
(*for 3rd pole*)

Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -
    p1) (wo^2 s Exp[
      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 + wdac^2) (z - Exp[s])))
wo = 3.14/num
wdac = 2*3.14
T = 1

p1 = -I 3.14*2

frac3 = Limit[v1, s -> p1]



(*for 4th pole*)

Clear[p1, wo, wdac, v1, dv1, v1]
v1 = (s -
    p1) (wo^2 s Exp[
      mul] wdac^2)/(((s^2 + wo^2)^2 (s^2 + wdac^2) (z - Exp[s])))
wo = 3.14/num
wdac = 2*3.14
T = 1
p1 = I 3.14*2
frac4 = Limit[v1, s -> p1]



gh34 = Numerator[
  Together[frac3 +
    frac4]]          (* Numerator of combination of 3rd and 4th \
fractions *)

gh = Numerator[
  Together[frac1 +
    frac2]]                  (* Numerator of combination of 1st and \
2nd fractions *)

den = Denominator[
  Together[frac1 +
    frac2]]             (* Denominator of combination of 1st and 2nd \
fractions *)

(*Numerator of 3rd and 4th fractions is (0.005843299525388367`+0.` \
\[ImaginaryI])-(0.005843299525388367`+0.` \[ImaginaryI]) z it may be \
written as -0.005843299525388367*(z-1)*)


ij34 = (0.005843306936293634*(z^2 - 1.776 z + 1)^2)/z^2


(*As frac1+frac2 =(-0.005843299525388367*(z-1))/((-1+z) ((-1+z) we \
```

```
multiply it (z-1)/z which is z-transform of [1-e(-Ts)], while unit \
delay in feedback path is also taken into account here. Moreover it \
is multiplied and divided with (z^2-1.776z+1)^2. Resultant is ij34*)


ij = Expand[(gh *  (z - 1))/z^2]


(*frac3+frac4 is combined and then multiplied with (z-1)/z which is \
z-transform of [1-e(-Ts)],*)


afo = Apart[(ij34 + ij)/(z^2 - 1.776 z + 1)^2]


(*All of the fractions are combined and then partially fractionated. \
Resultant terms consist of two types of terms. One

is [(0.05674223809011536`+6.106226635438361`*^-16 \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)^2-(0.10458793378536996`+0.07857423430477051` \
\[ImaginaryI])/((-0.888`-0.4598434516223972` \
\[ImaginaryI])+z)+(0.05674223809011464`+1.1102230246251565`*^-16 \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \
\[ImaginaryI])+z)^2-(0.10458793378536854`-0.0785742343047709` \
\[ImaginaryI])/((-0.888`+0.4598434516223972` \[ImaginaryI])+z)],

that only shows the fractions having poles at \
pi/6.57894736   0.1520fs. Other terms are \
(0.01684786921342306`-6.938893903907228`*^-17 \
\[ImaginaryI])/z^2+(0.2091758675707385`-3.885780586188048`*^-16 \
\[ImaginaryI])/z which need to be compensated*)



Together[(
  0.05513056690221478` +
   0.01342766387430719` I)/((-0.888` - 0.4598434516223972` I) +
    z)^2 - (0.055459239262580104` +
   0.10780534574735412` I)/((-0.888` - 0.4598434516223972` I) + z) + (
  0.05513056690221432` -
   0.013427663874306857` I)/((-0.888` + 0.4598434516223972` I) +
    z)^2 - (0.05545923926257927` -
   0.10780534574735401` I)/((-0.888` + 0.4598434516223972` I) + z)]
```

APPENDIX B

Matlab Code for 4th-Order Variable Notch Frequency CRFF ΣΔM ADC

```
close all
mex 'simulateDSM.c'
OSR=50;                          % Oversampling Ratio
N = 4;                           % Order of Modulator
H_inf=1.912;                     % Out of band gain
opt =1;                          % Zero Optimization
Nlev =4;                         % No of Levels =4 when used it relaxes the
                                 % swing requirement


tun=0;
for (i=1:48)%%%% getting 100 NTF for 100 notch frequencies with step of
.0025*fs OSR = 40e6/(2*50e3); % OSR = 80
H(i) = synthesizeNTF(N,OSR,opt,H_inf,0.01*tun);


stf(i)=H(i); %copy the ntf to stf, so that they will have the same poles.
stf(i).z=[]; %setting the numerator of stf to 1
  tun=i;
end
p=13;
H=H(p);
form = 'CRFF';
% Plot the response with chosen coefficients
[a,g,b,c] = realizeNTF(H,'CRFF')
ABCD = stuffABCD(a,g,b,c,form);
[ntf, stf] = calculateTF(ABCD);
f = linspace(0,0.24,1000);
z = exp(2i*pi*f);
magNTF = dbv(evalTF(ntf,z));
magSTF = dbv(evalTF(stf,z));
```

```
subplot(224)
figure
plot(f,magNTF,'b',f,magSTF,'m','LineWidth',1)
xlabel('Normalized Frequency');
ylabel('Magnitude');
legend('Noise Transfer Function','Signal TransferFunction')



%%%%%%%%%%%%%% Part 2 -- Perform Dynamic Range Scaling %%%%%%%%%%%%%%
 u = linspace(0,(Nlev-1),100);
Np = 1e4; % Number of same input points to test at time
T = ones(1,Np); %Normalized input signal = 5 (Nlev)
maxima = zeros(N,length(u));
for i = 1:length(u)
ui = u(i);
[v,xn,xmax] = simulateDSM( ui(T), ABCD, Nlev );
% Get Values for the max of each output node
maxima(:,i) = xmax(:);
if any(xmax>1e2) % Why100 ???
umax = ui % MaxStable input (Only stable to 2.88)
u = u(1:i);
maxima = maxima(:,1:i);
break;
end
end
figure; clf
for i = 1:N
  plot(u,maxima(i,:),'o');
if i==1
hold on;
end
plot(u,maxima(i,:),'g-','linewidth',2);
```

```
end
axis([0 3 0 10])
xlabel('Input Amplitude (Max = 5)')
ylabel('State Amplitude (Max = 5)')
x = [0.84 0.77 1.01 1.24]
[ABCDs,umax] = scaleABCD(ABCD,Nlev,0.01*(p-1),x,Nlev+5,[],Np)
[as,gs,bs,cs] = mapABCD(ABCDs,form)
u = linspace(0,umax,100);
for i = 1:length(u)
ui = u(i);
[v,xn,xmax] = simulateDSM( ui(T), ABCDs,Nlev );
maxima(:,i) = xmax(:);
if any(xmax>1e2)
umax = ui;
u = u(1:i);
maxima = maxima(:,1:i);
break;
end
end
%figure; clf
for i = 1:N
%plot(u,maxima(i,:),'ro');
if i==1
hold on;
end
plot(u,maxima(i,:),'k-','linewidth',3);
axis([0 3 0 5])
xlabel('Input Amplitude (Max = 5)')
ylabel('State Amplitude (Max = 5)')
%legend('Pre-Dynamic Range Scaling','','','Post-Dynamic Range Scaling')
end
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%% Part 7 - "Quantise" The Cap Values%%%%%%%%%%


R = 100; % Rounding Factor
a2 = round([as].*R)./R
%gsn = gs;
g2 = round([gs].*R)./R
b2 = round([bs].*R)./R
c2 = round([cs].*R)./R


asn_f(p,:)=a2
gsn_f(p,:)= g2
bsn_f(p,:)=b2
csn_f(p,:)=c2

fs=100e6;fi=0.01*(p-1)*fs;A=1;ts=1/fs;Ts=1/fs;N=65536   ;i=1   %   Simulation Parameters
sigma=0.05    % Coefficients Uncertainty
sim('wbbpsdm_old.mdl')
```