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Neuromorphic Low-Power Inference on Memristive Crossbars With On-Chip Offset Calibration

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ABSTRACT Monolithic integration of silicon with nano-sized Redox-based resistive Random-Access Memory (ReRAM) devices opened the door to the creation of dense synaptic connections for bio-inspired neuromorphic circuits. One drawback of OxRAM based neuromorphic systems is the relatively low ON resistance of OxRAM synapses (in the range of just a few kilo-ohms). This requires relatively large currents (many micro amperes per synapse), and therefore imposes strong driving capability demands on peripheral circuitry, limiting scalability and low power operation. After learning, however, a read inference can be made low-power by applying very small amplitude read pulses, which require much smaller driving currents per synapse. Here we propose and experimentally demonstrate a technique to reduce the amplitude of read inference pulses in monolithic neuromorphic CMOS OxRAM-synaptic crossbar systems. Unfortunately, applying tiny read pulses is non-trivial due to the presence of random DC offset voltages. To overcome this, we propose finely calibrating DC offset voltages using a bulk-based three-stage on-chip calibration technique. In this work, we demonstrate spiking pattern recognition using STDP learning on a small 4×4 proof-of-concept memristive crossbar, where on-chip offset calibration is implemented and inference pulse amplitude could be made as small as 2mV. A chip with pre-synaptic calibrated input neuron drivers and a 4×4 1T1R synapse crossbar was designed and fabricated in the CEA-LETI MAD200 technology, which uses monolithic integration of OxRAMs above ST130nm CMOS. Custom-made PCBs hosting the post-synaptic circuits and control FPGAs were used to test the chip in different experiments, including synapse characterization, template matching, and pattern recognition using STDP learning, and to demonstrate the use of on-chip offset-calibrated low-power amplifiers. According to our experiments, the minimum possible inference pulse amplitude is limited by offset voltage drifts and noise. We conclude the paper with some suggestions for future work in this direction.

INDEX TERMS Neuromorphic, low-power inference, pattern recognition, template matching, offset calibration, memristive crossbar, nano-synapse.

I. INTRODUCTION

Neuromorphic computing has recently attracted more attention. It all started in the late 1980s, when Caver Mead first coined the term 'neuromorphic' and proposed the concept of morphing the biological brain on a chip [1]. Like the biological brain, the main components in neuromorphic computing are neurons interconnected by synapses. The main idea of silicon neurons is to use sub-threshold transistor currents (in the order of nA) to mimic the biophysical properties of neurons. Such brain-inspired neuromorphic computing systems have been attractive because their co-location of memory

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and processing units offers an alternative to classical von Neumann architectures [2].

Some of the best-known neuromorphic chips over the last few decades have been Neurogrid [3], [4], BrainScaleS [5], [6], TrueNorth [7], SpiNNaker [8] and Loihi [9], to mention just a few. Other chips of this type include Darwin [10], ROLLS [11], ODIN [12], and DYNAPs [13]. Comparisons of these chips based on specifications like technology, feature size, number of transistors, number of neurons, number of synapses, energy, etc. can be found in literature [14], [15]. There are also low-cost user-friendly boards like NeuroShield, featuring the NM500 neuromorphic chip, which can be driven by Raspberry Pi or Arduino [16].

A. THE MEMRISTOR AS A FAVORABLE SYNAPSE

When Chua first coined the term 'memristor' in the early 70s, nobody even knew the device existed [17]. Later in 2008, when HP labs demonstrated the physical existence of memristors, several memristor models were proposed to study and explore their potential applications [18]–[22]. These sustained the neuromorphic community's enthusiasm about creating and using memristors as favorable synapses for neuromorphic circuits. The non-volatile nature, analog behavior, nano-scale size, and monolithic CMOS compatibility of a memristor make it the candidate of choice for use as a synaptic element in neuromorphic circuits. Moreover, its nano-size existence aids its monolithic integration with silicon layers to build ultra-dense synaptic connections along with its CMOS counterpart. Research has been carried out into different memristor switching mechanisms, such as redox-based, phase-change, magnetic junction-based, and ferroelectric mechanisms, and into different physical models, such as conductive filaments, the Schottky barrier, charge trapping, and the electrochemical migration of point defects, in order better to understand the working physics behind the device and its switching phenomena [23]–[31].

ReRAMs are based on establishing a conductive filament during switching and have transpired as a promising artificial synaptic device for high-density synaptic crossbars mainly because of their robustness and their integration capability [32]. ReRAM technology combines the features of high-speed Static Random-Access Memory (SRAM) performance with the non-volatile properties of flash memories by implementing them at low power consumption. Metal oxide-based ReRAM comprises a transition-metal-oxide layer sandwiched between two metal electrodes so that when voltage pulses are applied to the electrodes the device shows a change in resistance.

Of all the different transition materials (HfO_2, NiO, Al_2O_3, Nb_2O_5, $SrTiO_3$, $Pr_{0.7}Ca_{0.3}MnO_3$, CuO_2, Ag_2S, $AgGeSe$, etc.), HfO_2-based devices are known for their high endurance, high switching speed, and low-switching energy [33]–[38]. In this work, OxRAM devices (the TiN-Ti-HfO_2-TiN structure) with a series-connected MOSFET selector (creating the so-called '1T1R' structure), are used as synapses, as

illustrated in Fig. 1(a). By applying a controlled voltage through the terminals of the 1T1R structure, the resistance of the device can be dynamically switched between Low Resistive State (LRS) and High Resistive State (HRS) [39], [40]. LRS is typically in the order of $k\Omega$, and HRS is in the order of hundreds of $k\Omega$ to $M\Omega$. Fig. 1(b) shows a layout view of the 1T1R synapse in the MAD200 technology The MAD200 hybrid fab-process involves: 1) a 130nm CMOS Standard Foundry Wafer with four Cu Metal layers M1, M2, M3, and M4, 2) TiN bottom electrode definition, 3) memory stack (HfO_2 10nm/Ti 10nm/TiN) deposition, 4) ϕ 300 nm MESA[1] patterning, 5) placing of vias and 6) M5 layer deposition. Fig. 1(c) shows a microscopic cross-section view of the monolithically integrated hybrid CMOS and OxRAM MAD200 technology used here [41].

A thick oxide NMOS with W = 6.7μ m and L = 0.5μ m was used as the MOSFET selector. The OxRAMs were initially in a Pristine Resistive State (PRS) and their filaments were formed by applying a bias $V_{TS} = 4V$ with 10μ s pulse width and a gate bias $V_{GS} = 1V$, to limit the current to a recommended compliance of about 30μ A. For a RESET (Erase) operation, a bias of $V_{ST} = 3V$ with 100ns pulse duration was applied by keeping the gate fully ON ($V_{GT} = V_{DD} = 4.8V$). For a SET (Write) operation, a bias of $V_{TS} = 2.4V$ with 100ns pulse duration was applied along with the gate bias of $V_{GS} = 1.5V$. For a read operation, a read voltage of $V_{TS} = V_{Read} = 0.3V$ was applied with a gate bias of $V_{GS} = 4.8V$. Table 1 shows the bias conditions for the different OxRAM operations. Since here the maximum voltage required for proper memristor operation was 4.8V, for convenience we used thick-oxide transistors for all our CMOS circuits with a common power supply of $V_{DD} = 4.8V$.

TABLE 1. Bias conditions for different OxRAM operations.

OxRAM operation	V_{TS}	V_{GS}	Pulse-width
Form	4V	1V	10µs
Erase	-3V	4.8V	100ns
Write	2.4V	1.5V	100ns
Read	0.3V	4.8V	variable

B. MEMRISTIVE CROSSBAR AND SNEAK-PATH CURRENTS

The term 'crossbar switch' dates from 1913, when J. N. Reynolds from Western Electric thought of using a cross-point or a coordinate array to operate a large number of relay contacts with only a small number of magnets [42]. In the early 2000s, many crossbar-based architectures were proposed, using two-terminal devices for memory, logic, and neuromorphic applications [43]–[48]. The crossbar-based neuromorphic circuits shown in Fig. 2 (a) comprise two layers of parallel lines that are perpendicular to each other and which act as word-lines ($W_{1,2,3,4}$) and bit-lines ($B_{1,2,3,4}$). They are

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[1]Manufacturing Execution System Application (MESA) patterning is using a thick photoresist pattern. In a MESA-process, it is done after doping of impurities and before etching polysilicon.
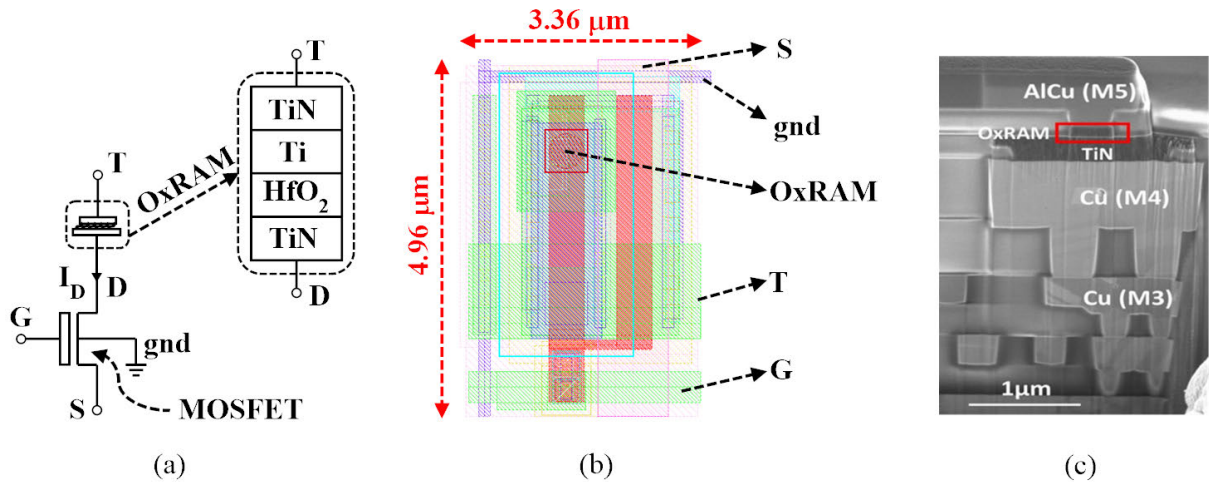
FIGURE 1. (a) 1T1R structure, (b) Layout preview of 1T1R in MAD200 PDK, (c) Microscopic view of the monolithic integrated hybrid CMOS and OxRAM [41].
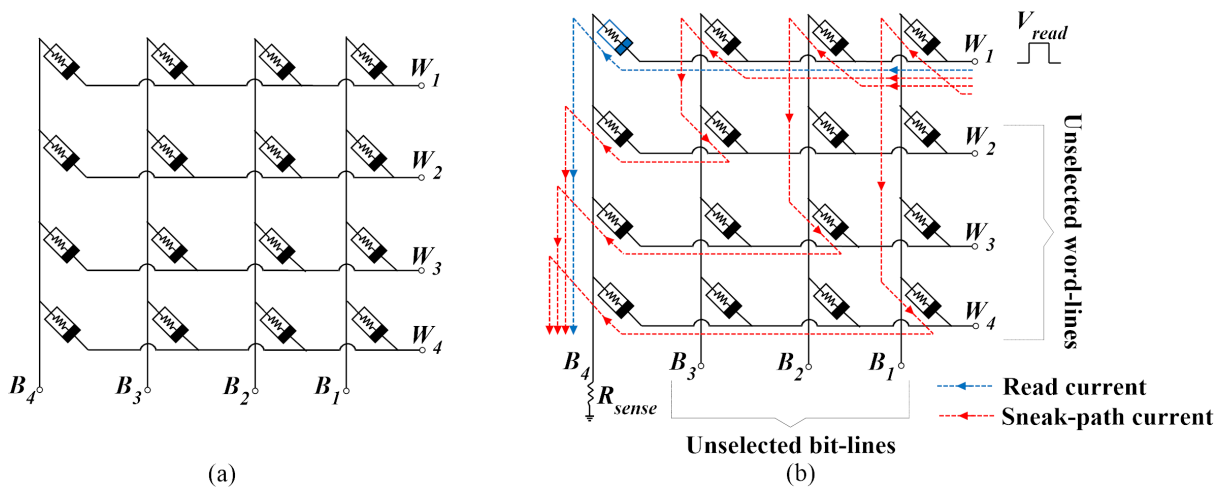

FIGURE 2. (a) A 4 × 4 memristive crossbar, (b) Read current and sneak-path current in a 4 × 4 memristive crossbar.

arranged in a two-dimensional array with a synaptic element at each intersection or cross-point. The synaptic elements can be programmed to 'LRS' or 'HRS', representing logic '1' or '0', respectively, when appropriate voltages are applied to the word-lines and bit-lines.

One big drawback of selector-less memristive crossbars is the sneak-path current. Sneak-path currents are currents which pass through the unselected path of word-lines and bit-lines and which may aggravate the crossbar's read and write operation performance, thereby limiting its scalability [49]. When a particular synaptic device is targeted in a crossbar and its current is read by applying a read voltage V_{read}, along with the desired read current, sneak-path currents also appear across the inference bit-line, as shown in Fig. 2 (b). Sneak paths can cause the state of the synaptic device to be misread or unintentionally changed. They are relevant when crossbars are used as digital memories, but are not critical when crossbars are used for analog vector-matrix multiplications.

Several architectures, synaptic devices and read/write procedures have been proposed to mitigate the effect of sneak path currents in crossbars. Synaptic devices like two anti-serial memristors [50] and architectures like unfolded crossbars with 1D1M devices [51] have been researched with the same objective. Studies have also been carried out into read techniques such as multiport read-out with mathematical cancellation of sneak-path currents [52], a threshold-based read-out system [53], a two-step read process based on "open-column" semantics [54], and a three-step read (or multistage read) process for determining the state of the memristor in the presence of sneak paths [55]. Write bias schemes with V/2 and V/3 have shown low write energy and high read margins, thereby minimizing the effect of sneak-path currents [56]–[58]. Another interesting approach for eliminating sneak-path currents is to use demultiplexer circuits based on encoded nanowire doping [59]. Sneak-path currents also can be avoided using 1T1R synapses [60]. This can limit scalability, but greater crossbar density and smaller area overhead

can be achieved by fabricating the memristor fabric on top of the CMOS layer using sub-CMOS-feature-size nanowires with different fabrication processes. This can be done using spatially-distributed interface pins to connect the top-level CMOS metal layer to the nanowire crossbars [61], [62]. In the MAD200 technology used in this work, 1T1R synapses are mandatory because the 1T MOSFET selector is required to impose proper compliance currents for 'form' and 'write' operations. This way, if the calibrated crossbar is used as plain memory, there will be no issue with sneak-paths.

C. STDP LEARNING RULE AND ITS APPLICATIONS

STDP (Spike Timing Dependent Plasticity) is a family of computational neuroscience learning rules for spike-based neural systems. STDP dates back to 1993, when Gerstner first reported a simple variant [63]. Surprisingly, many neuroscience researchers only observed its experimental existence in biology later [64]–[71], and its underlying molecular and electrochemical principles are still under debate [72].

Fig. 3 shows a preview of a synaptic junction, where pre-synaptic and post-synaptic neurons connect. The pre-synaptic neuron sends an action potential $V_{mem-pre}$ to the synapse, which cumulatively generates a post-synaptic action potential $V_{mem-pos}$ at the membrane of the post-synaptic neuron. t_{pre} is the time at which the pre-synaptic spike occurs and t_{pos} is the time at which the post-synaptic spike occurs. The pre-synaptic action potential causes neurotransmitters to be released into the synaptic cleft. Each synapse or synaptic junction is characterized by synaptic weight (or strength) w, which determines the efficacy of the pre-synaptic spike in contributing to the cumulative action in post-synaptic neurons. According to STDP, the change in synaptic weight is a function of the time difference between the pre-synaptic spike and the post-synaptic spike. A causal relationship (pre- spike shortly before the post- spike) produces a weight increase, while an anti-causal relationship (post- spike shortly after the pre- spike) produces a weight decrease. Hence the change in

FIGURE 3. A synaptic junction that connecting a pre-synaptic and a post-synaptic neuron.

synaptic weight $\triangle w = \xi(\triangle T)$, where $\triangle T = t_{pos} - t_{pre}$. For positive $\triangle T$, synaptic weight is potentiated (i.e. $\triangle w > 0$) and for negative $\triangle T$, synaptic weight is depressed (i.e. $\triangle w < 0$). STDP takes into account the spikes' relative time [73]. The machine learning and computational neuroscience community have been using STDP for applications like pattern learning and object or pattern recognition since the early 2000s [74]–[82].

D. LOW-POWER INFERENCE WITH OFFSET CALIBRATED OPAMPS

The objective of our work was to use tiny read pulses for functional applications such as pattern recognition to make the system low-power during inference. Typically, such read pulses have amplitudes of 100mV, 50mV, or even less, but they are further limited by DC offset voltages and noise. The amplitudes of the read pulses determine the maximum current the crossbar line drivers need to provide. This driving capability scales with crossbar size. Consequently, reducing the maximum driving currents can reduce the overall operation current (and power consumption) by over one order of magnitude. Experimental results of the bulk-based, three-stage calibration approach to calibrate the DC offset voltages of opamps have already been reported [83]. Our proposal in this work was to experimentally demonstrate template matching and more sophisticated pattern recognition through STDP learning using the tiniest possible read inference pulses with opamps with calibrated offset voltages. Before presenting these results, we also present the results of the synapse characterization and simple template matching.

II. A 4 × 4 MEMRISTIVE CROSSBAR SYSTEM WITH ON-CHIP OFFSET CALIBRATION

This section describes the demonstration system setup used in our study, which included a 4 × 4 memristive crossbar for pattern recognition. Fig. 4 shows a conceptual diagram mainly comprising pre-synaptic drivers, post-synaptic drivers, synapses ($W_{11,12,13,14,21,...44}$), and the three-stage calibration scheme. $V_{pre\{1,2,3,4\}}$ are the pre-synaptic lines, $V_{post\{1,2,3,4\}}$ are the post-synaptic lines and $V_{g\{1,2,3,4\}}$ are the gate lines. A dedicated PCB was designed that facilitated testing of the chip in different experiments, such as OxRAM characterization, template matching, and pattern recognition using STDP learning.

The access principle of the 4 × 4 memristive crossbar system was to apply 'active' biases to one pre-synaptic line, one gate line, and one post-synaptic line. The rest of the pre-synaptic lines, gate lines, and post-synaptic lines were applied with 'default' biases. In this way, we could target one specific synaptic device in the crossbar and execute a desired OxRAM operation such as 'form', 'erase', 'write', or 'read'. The other synapses in the crossbar were undisturbed by applying 'default' biases across their terminals. We also used an 'idle' state in which all terminals were connected to 0V. Table 2 shows the 'active' and 'default' biases used for the different OxRAM operations when synapse W_{ij} was targeted
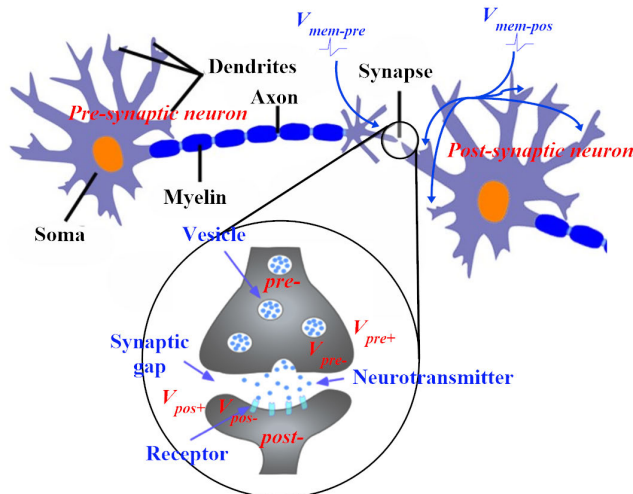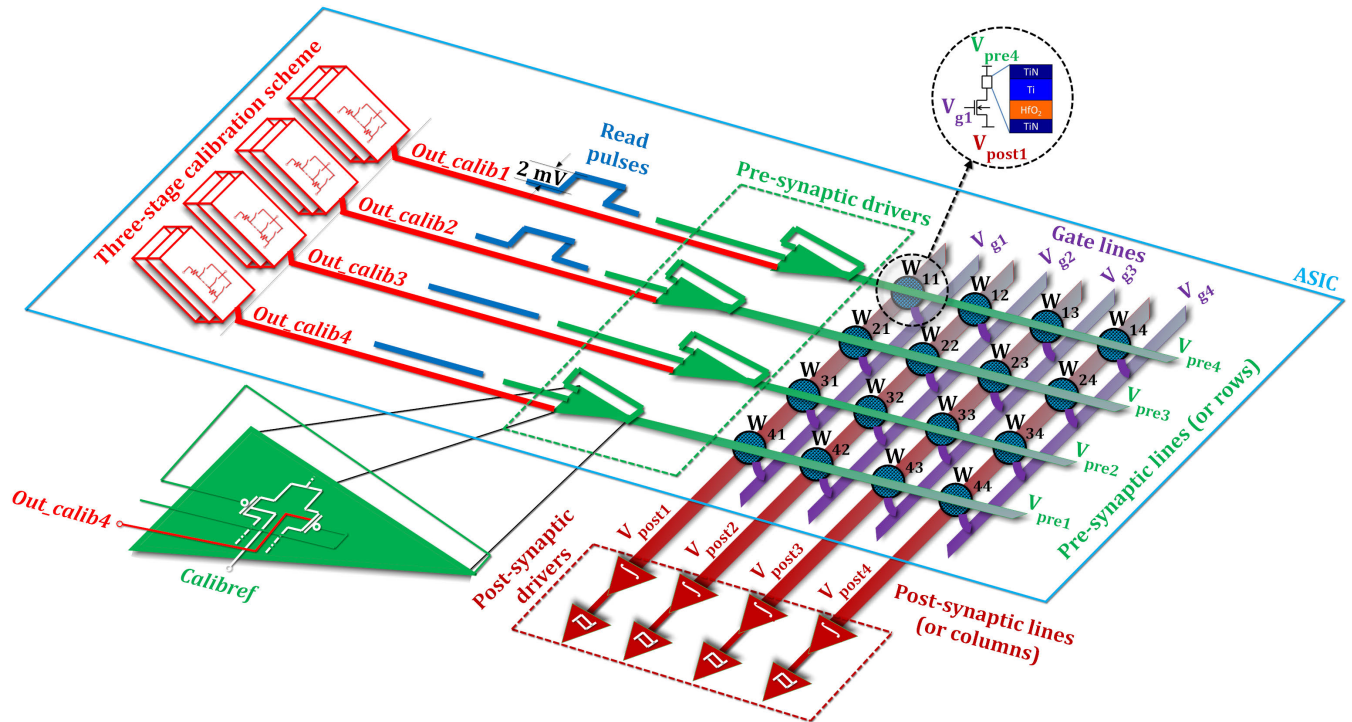
FIGURE 4. Conceptual diagram of the 4 × 4 memristive crossbar with on-chip calibration and read pulses applied across pre-synaptic lines during inference.

TABLE 2. 'Active' and 'default' biases applied across crossbar terminals for different OxRAM operations when synapse, W_{ij} is targeted in the crossbar shown in Fig. 4.

OxRAM Operation	Active biases			Default biases		
	V_{prei}	V_{postj}	V_{gj}	$V_{pre\{k \neq i\}}$	$V_{post\{l \neq j\}}$	$V_{g\{l \neq j\}}$
Form	4V	0V	1V	0V	4V	0V
Erase	0V	3V	4.8V	3V	0V	0V
Write	2.4V	0V	1.5V	0V	2.4V	0V
Read	2.4V	2.27V	4.8V	2.27V	2.27V	0V
Idle	0V					

FIGURE 5. Schematic view of the pre-synaptic driver across a pre-synaptic line, V_{prei}.

(see Fig. 4). During inference operation in template matching or pattern recognition tasks, a sequence of read pulses were applied in parallel to all pre-synaptic lines (rows), according to the corresponding input pattern.

A. PRE-SYNAPTIC DRIVERS

Each pre-synaptic driver was made up of a digital pulse shaping block and an offset calibrated opamp, as show in Fig. 5. This gave three possible analog values to be applied to each pre-synaptic line of the crossbar for different OxRAM operations. The opamps' DC offset voltages were calibrated before setting a low-amplitude inference pulse in the read-out pre-synaptic line path and the opamps were biased with independent digitally-controlled current bias circuits, which we call I-pots, each providing an individual i_{bias} current [84]. Each pre-synaptic driver had its own calibration circuit. One of the bulk terminals of the differential pair of MOSFETs of
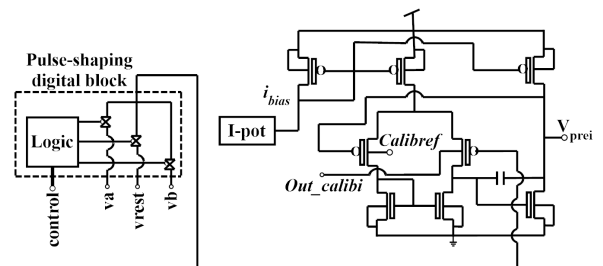
the opamp, 'Out_calibi', was driven by the calibration circuit for offset calibration. Bias 'Calibref' was common for all opamps, while 'Out_calibi' was provided by the calibration circuit of each opamp.

A three-stage bulk-based calibration scheme was implemented to finely tune the bulk voltage 'Out_calibi' of each opamp, as shown in Fig. 6 [83]. It consisted of cascaded resistor ladders of high ohmic unsalicided N+ polysilicon resistors with 16 levels in each stage. As we planned to calibrate DC offset via bulk of PMOS differential pairs, the reference voltage V_{ref} was set near to the supply voltage (4.8 - 0.3 = 4.5V). The first stack of resistors was connected to reference voltages $V_{ref} + V_d$ and $V_{ref} - V_d$, which were set to choose a coarse (stage 1) voltage range, which was in turn used to pick finer (stage 2 and stage 3) ranges in the next stacks. Here, V_d is half the tuning voltage range, and V_{ref} is the reference voltage. The output of the calibration scheme 'Out_calibi' connected to one of the opamp differential pair
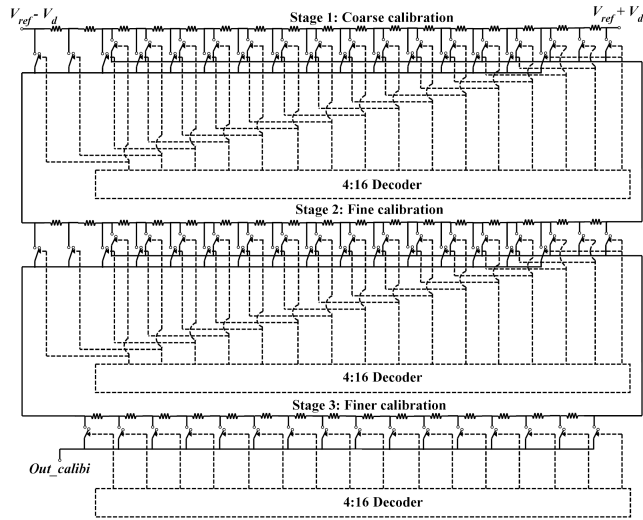
FIGURE 6. Schematic view of the three-stage calibration scheme with decoders to control the switches.

FIGURE 7. Scheme of a post-synaptic driver coupled to a post-synaptic line of the crossbar.

transistor bulk terminals (shown in Fig. 5), while the other bulk terminal (*Calibref*) was biased at $V_{ref} = 4.5V$.

B. POST-SYNAPTIC DRIVERS

Each post-synaptic line was followed by a post-synaptic driver. The scheme, shown in Fig. 7, mainly comprised opamps, switches, and decoders. Control lines $B_{1,2}$ selected the different feedback elements of read opamp A_{j1} for different operations—'form', 'erase', 'write', 'read'—by keeping appropriate biases across all the V_{postj} lines. The objective was to keep the required virtual ground voltage of the inverting terminal of opamp A_{j1} or the V_{postj} line for the different OxRAM operations. During inference, opamp A_{j1} was used as an integrator, the output of which was compared with a reference V_{comp} by a comparator (using opamp A_{j2}). Here, the R_{read} feedback path was selected during synapse characterization and the C_{integ} feedback path was selected during inference for integration. The values of R_{read} and C_{integ} were tunable, depending on the resistance range of interest, the inference pulse amplitude, and the pulse-width. S_j was chosen by a decoder (not shown in Fig. 7). When line V_{postj} was chosen as the active post-synaptic line, signal S_j was kept 'ON'. This connected line V_{postj} to 'active column bias'. Alternatively, when line V_{postj} was chosen as a default post-synaptic line, signal S_j was kept 'OFF'. This connected the post-synaptic line V_{postj} to 'default column bias'. Both 'active column bias' and 'default column bias' for different OxRAM operations were established through switches and decoders in such a way that at any given instant one of the post-synaptic lines was kept as active while the others were left to default.

C. DIGITAL CONTROL AND AUXILIARY CIRCUITRY

An on-chip, edge-triggered D flip-flop-based 104-bit shift register was used to load the control-bits for the input of the I-pots' and opamps' input offset calibration circuits. A PCB
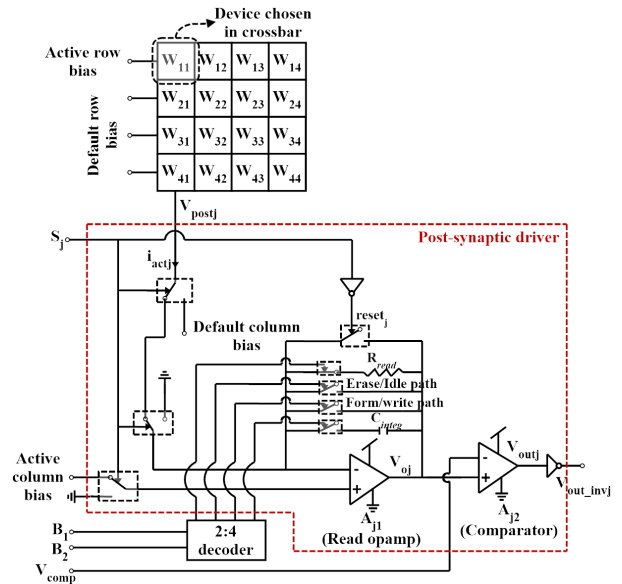
was designed to facilitate the testing of the memristive crossbar in different experiments, such as synapse characterization, learning patterns, etc. Fig. 8 shows a functional block diagram of the test platform, including the ASIC (Application Specific Integrated Circuit). The main functional blocks in the platform were the opamps, switches, level-shifters, decoders, and a custom SPARTAN®-6 FPGA board, also known as an AER-node[2] board [85]. The nomenclatures used for the functional blocks were 'OA' for Operational Amplifiers' and 'Sw' for switches. The pre-synaptic drivers were embedded within the chip, while the post-synaptic drivers were made available on the PCB.

Line *data_in* is a simple serial line for loading the 104-bit control-word used for programming the digital inputs to the calibration schemes and I-pots in all the pre-synaptic drivers. It was initially loaded into the on-chip shift-register using the *clock* signal. Once *data_in* had been fed in, *clock* was stopped, and the *latch* signal was turned 'ON' to hold the digital inputs. Opamps were used to keep the desired biases for $V_{ref} + V_d$, V_{ref} - V_d, va, vrest, vb, V_{comp}, and *Calibref*. Opamps were also used to set optimal values of 'active' and 'default' biases for the gate lines and post-synaptic lines for the different OxRAM operations. The pre-synaptic line biases for different OxRAM operations were directly applied across terminals va, vrest and vb (see Fig. 5), which were digitally controlled through the 'control' bus. For gate lines ($V_{g\{1,2,3,4\}}$) and post-synaptic lines ($V_{post\{1,2,3,4\}}$), the biases for different OxRAM operations were applied via switches that were selectively chosen using decoders (see around Fig. 7 for $V_{post\{1,2,3,4\}}$). Fig. 9 shows the scheme for digitally setting 'default' and 'active' biases across gate line terminals in the 4×4 memristive crossbar for different OxRAM operations. Here, 'F_act', 'E_act', 'W_act', 'I_act',

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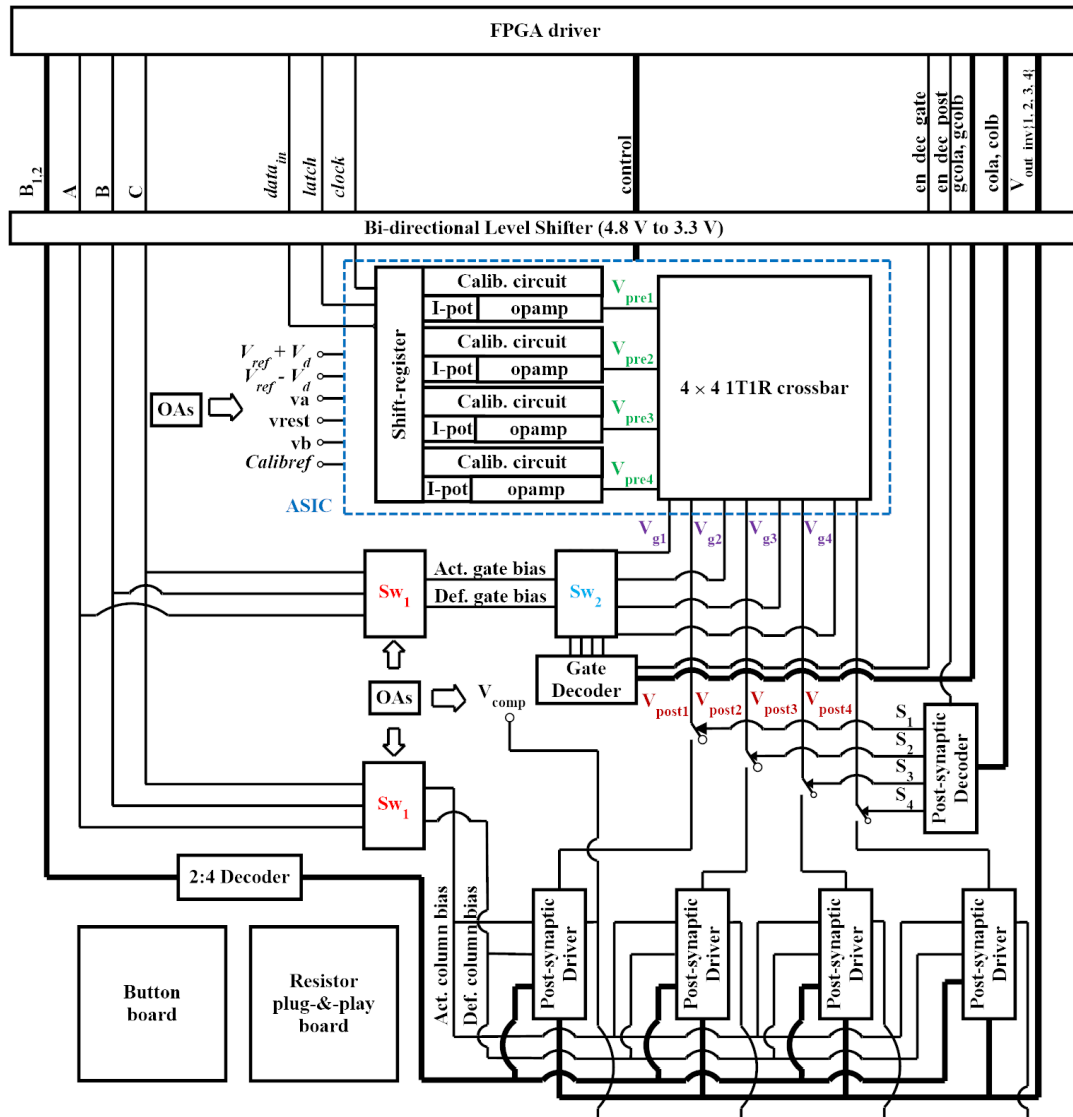[2]AER stands for Address Event Representation.

FIGURE 8. Functional block diagram of the test platform used to test the chip.

and 'R_act' are the 'active' biases for different OxRAM operations such as 'Form', 'Erase', 'Write', 'Idle' and 'Read'. Similarly, 'F_def', 'E_def', 'W_def', 'I_def', and 'R_def' are the 'default' biases for different OxRAM operations.

Two different arrangements of switches 'Sw$_{\{1,2\}}$' were used. A dedicated 3-bit line (A, B, C) was used to control the switches in 'Sw$_1$', which targeted different OxRAM operations. The values for this 3-bit control line are shown in Table 3. Here, 'ON' indicates 4.8V (V$_{DD}$ or Supply voltage), and 'OFF' indicates 0 V. Another 3-bit group (gcola, gcolb and en_dec_gate) was used to control the switches in 'Sw$_2$', which selected the 'active' and 'default' gate lines. A 6-bit control bus was used for the gate terminals, for targeting a synapse and providing the gate biases required for the desired OxRAM operation. Post-synaptic lines were also controlled by the 6-bit (A, B, C, cola, colb and en_dec_post) control bus, while a 2-bit control line, B$_{1,2}$, was used to

choose the feedback path in opamp A$_{j1}$ (shown in Fig. 7) for different OxRAM operations. A 7-bit control line was used for the post-synaptic terminals, for targeting a synapse and providing the post-synaptic line biases required for the desired OxRAM operation.

A bi-directional voltage level conversion between 4.8V and 3.3V was used for the FPGA driver to control the overall testing of the chip. A Spartan®-6 FPGA board was used to program and digitally control the PCB (with the test-circuits) and the ASIC part. The outputs of the post-synaptic drivers, Vout{1,2,3,4}, were fed to the driver by algorithms like pattern recognition. In addition to the PCB, two auxiliary boards—a button board and a resistor plug-&-play board—were also made. The button-board provided additional push-buttons, since this was one of the limitations in the SPARTAN®-6 driver board [85]. The button-board also had additional digital nodes with control-bits that could be
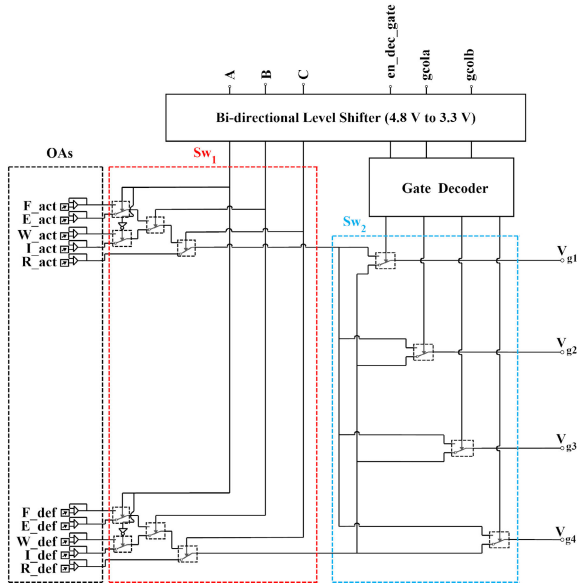
FIGURE 9. Scheme for digitally setting 'default' and 'active' biases across gate line terminals in the 4 × 4 memristive crossbar for different OxRAM operations.

TABLE 3. Control-bit for performing different OxRAM operations in the targeted 1T1R device in the crossbar, with pre-synaptic lines calibrated for DC offset voltage.

OxRAM operation	A	B	C
'Form'	ON	ON	ON
'Erase'	OFF	ON	ON
'Write'	OFF	OFF	ON
'Read'	OFF	OFF	OFF
'Idle'	ON	OFF	ON

set manually. The resistor plug-&-play board helped test the PCB before moving on with the chip and also facilitated the testing of the crossbar terminals.

III. EXPERIMENTAL RESULTS

Fig. 10 shows the experimental setup of the memristive cross-bar for pattern recognition using offset calibrated low-power amplifiers. It mainly comprises the test-PCB incorporating the chip under test, a SPARTAN®-6 driver board, the auxiliary boards (a button-board and a resistor plug-and-play board), a Mixed Signal Oscilloscope (MSO), and its digital pod. The chip, designed using MAD200 technology (CEA-LETI OxRAM ST130nm CMOS), was assembled into a PGA100 package, different previews of which are shown in Fig. 11. The 4 × 4 1T1R crossbar circuit with on-chip offset calibration is highlighted in these figures with dashed red lines. The test-PCB was controlled through the SPARTAN®-6 driver board. The button-board had dedicated buttons to perform OxRAM operations like 'Form_Idle_Read', 'Weight update', 'Erase_Idle_Read', 'Write_Idle_Read', and 'Read' in sequence. The buttons on the button-board corresponding to these tasks or operations are highlighted in Fig. 10. The chip, the PCB, the SPARTAN®-6 driver board, the auxiliary boards, and the MSO facilitated the following experiments:

(i) Synapse characterization, (ii) DC offset voltage calibration, (iii) Template matching, and (iv) Pattern recognition by STDP learning.

A Finite State Machine (FSM) was programmed in the FPGA to define the functions of each button on the button-board. Different states were made in the FSM in such a way that the push-buttons on the button-board were programmed to establish different OxRAM operations in a sequence on the targeted 1T1R device. One of the push-buttons was programmed to carry out the 'Form_Idle_Read' tasks, while another was programmed for the 'Erase_Idle_Read' tasks. Other buttons were programmed exclusively to carry out 'Write_Idle_Read' tasks and a separate 'Read' operation, and to perform offset calibration during that 'Read' operation. A push-button was also programmed for the 'Weight update' task, which was later used in the template matching and pattern recognition experiments.

A. OPERATION AND CHARACTERIZATION OF INDIVIDUAL 1T1R SYNAPSES

The main idea used to characterize a 1T1R synapse in a crossbar was to target a device by picking the corresponding active pre-synaptic line, post-synaptic line, and gate. 'Active' biases for these pre-synaptic lines, post-synaptic lines, and gate terminals were applied for different OxRAM operations, as discussed in Section I-A. The rest of the pre-synaptic lines, post-synaptic lines, and gates were connected to 'default biases' (as shown in Table 2), where the biases across the top and bottom terminals of the device were similar and the gate biases were set at 0V. In this way, the states of the other devices remained unchanged. Read opamp, A_{j1} (as shown in Fig. 7) with $R_{read} = 26.71k\Omega$ was used to find the state of the synapse during 'read'. Synapses were characterised in the following three steps: (a) set active and default voltages using opamps for different OxRAM operations, (b) target a synaptic 1T1R device in the crossbar, (c) load the control-word using the shift register to perform the required OxRAM operation through a 3-bit control signal, F(A, B, C), as shown in Table 3.

All OxRAMs were carefully formed and switched between LRS and HRS for characterization. Fig. 12(a) shows the active pre-synaptic i=2 line (V_{pre2}) bias, the post-synaptic j=3 line (V_{post3}) bias, the gate line (V_{g3}) biases, the output voltage V_{out3} of read opamp A_{31}, and the digital signals when the 'ERASE_IDLE_READ' operation was carried out (see Fig. 7). Fig. 12(b) shows the active pre-synaptic line (V_{pre2}) bias, the post-synaptic line (V_{post3}) bias, the gate line (V_{g3}) biases, the output voltage V_{out3} of read opamp A_{31}, and the digital signals when the 'WRITE_IDLE_READ' operation was carried out.

The 'data-loading' part was originally programmed for 52.5ms. This is the control-word that was loaded to the on-chip shift register. Only the last region of the 'data-loading' part is shown in Fig. 12. This was followed by 'Idle', 'Erase', 'Idle', 'read', and 'Idle'. During 'Idle', both the top and bottom terminals of the targeted 1T1R device were biased at 0V and the gate was turned 'OFF'. During
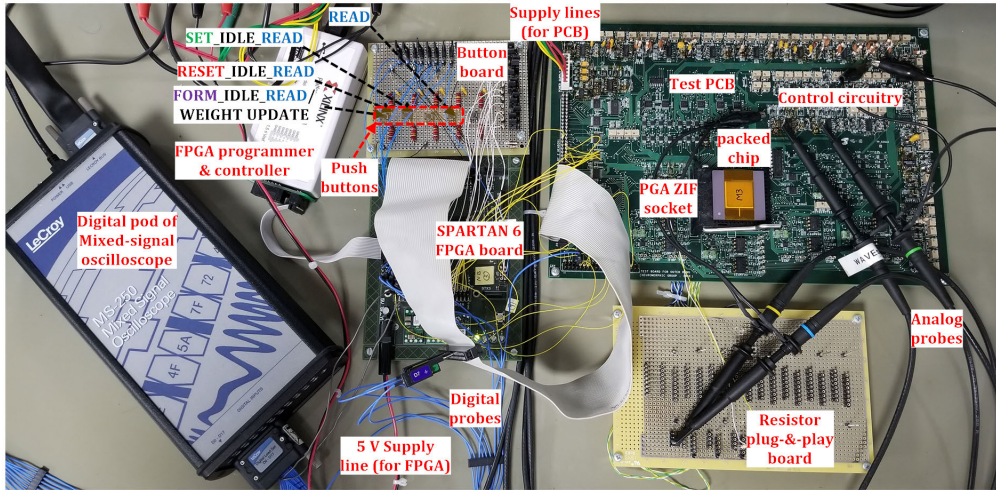
FIGURE 10. Experimental set-up of the memristive crossbar for pattern recognition using offset calibrated low-power amplifiers.
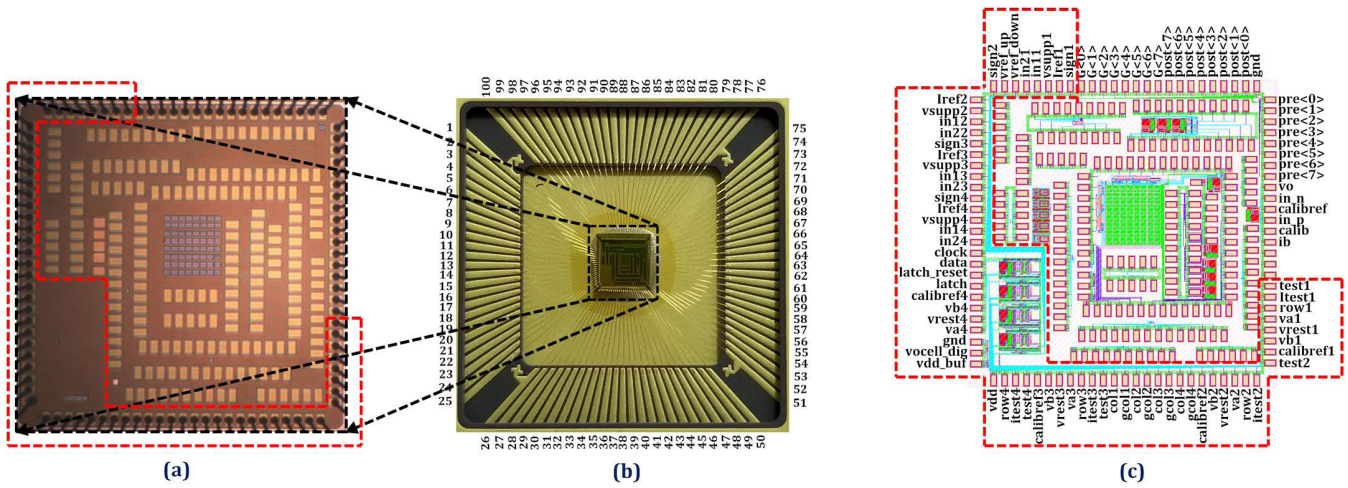

FIGURE 11. (a) Zoom preview of the top of the chip, (b) Top view of the chip packed in the PGA100 package, (c) Layout view of the chip in MAD200 PDK with labelled pads.

'read', the active pre-synaptic line and post-synaptic line were initially switched to the required 'read' biases and the active gate line was turned 'ON' once 15ms had elapsed. The values of control signals A, B, and C for different OxRAM operations were digitally set based on Table 3. The LRS and HRS resistance values of the OxRAM were calculated from Fig. 12. A feedback resistor with a resistance value of 26.71kΩ was used at the read opamp A_{31}. The 'Read' voltage was 2.4V - 2.27V = 0.13V. The output of the read opamp A_{31} went to 2.246V during a 'Read' after 'Erase' when the active gate was turned 'ON'. Similarly, the output of the inference opamp went to 0.436V during a 'Read' after 'Write' when the active gate was turned 'ON'. The LRS and HRS values were calculated as follows

$$\text{LRS} = \left(\frac{26.71\text{k}\Omega}{2.27\text{V} - 0.436\text{V}}\right) \times 0.13\text{V} = 1.89\text{k}\Omega \quad (1)$$

$$\text{HRS} = \left(\frac{26.71\text{k}\Omega}{2.27\text{V} - 2.246\text{V}}\right) \times 0.13\text{V} = 144.68\text{k}\Omega \quad (2)$$

Fig. 13 shows the measured LRS and HRS OxRAM values of synapses in the 4 × 4 crossbar. Here, the maximum and minimum HRS values were 315.28kΩ and 16.5kΩ, respectively. The maximum and minimum LRS values were 2.92kΩ and 1.66kΩ, respectively. Fig. 14 shows the LRS and HRS values for 10 switching cycles of an OxRAM in the 4 × 4 memristive crossbar. Here, the maximum HRS was 385.8kΩ and the minimum HRS was 120kΩ. The maximum LRS was 1.95kΩ and the minimum LRS was 1.87kΩ. Fig. 15 shows the LRS and HRS values for 400 switching cycles of an OxRAM of a synapse. The plot shows high variability in the distribution of HRS. Here, the maximum HRS was 1.19MΩ and the minimum HRS was 5.9kΩ. The maximum LRS was 3.82kΩ and the minimum LRS was 2.53kΩ.

B. CALIBRATION OF DC OFFSET IN OPAMPS

DC offset voltages need to be calibrated when minimum read pulses are used for inference. Calibration of DC offset during
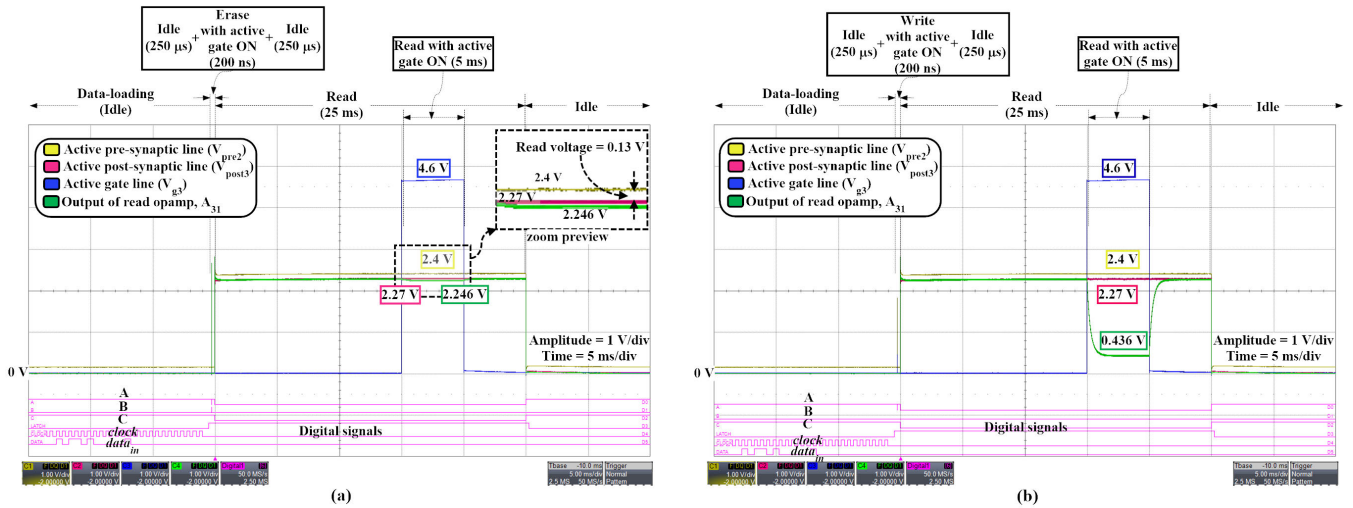
FIGURE 12. Active pre-synaptic line i=2 (V$_{pre2}$) bias, post-synaptic j=3 line (V$_{post3}$) bias, gate line (V$_{g3}$) biases, output voltage V$_{o3}$ of read opamp A$_{31}$ and, digital signals applied in the form of pulses, (a) showing a read operation after an erase operation, (b) showing a read operation after a write operation.
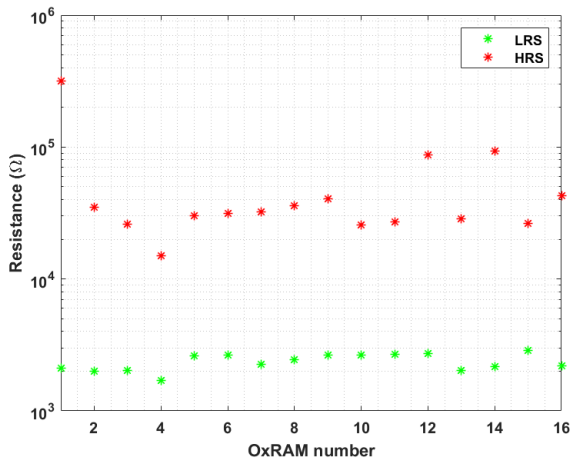

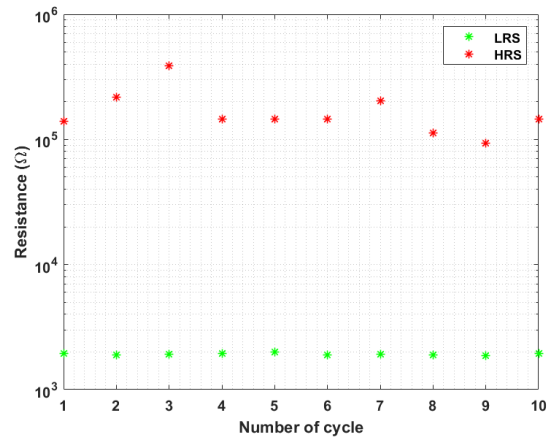**FIGURE 13.** LRS and HRS OxRAM values of all 16 synapses in the 4 × 4 crossbar.

inference involves the following steps: (a) set active and default voltages for OxRAM operations, such as 'read' and 'idle' or 'global', (b) set *Calibref* = 4.5V, V_{ref} = 4.5V and V_d = 15mV, (c) set the 12-bit control input for the calibration scheme, (d) target a synaptic 1T1R device by selecting its active pre-synaptic line as the active line in the crossbar, and (e) load the control-word using the shift register and then hold it with the *latch* signal to calibrate the DC offset during a 'read' operation. The residual DC offset is determined by observing the difference between the input and the output of the corresponding pre-synaptic driver.

Fig. 16(a) compares the experimental and simulation results when pre-synaptic line V_{pre1} of the crossbar was calibrated for DC offset voltage during coarse (or stage 1) calibration. The zero-crossing region in Fig. 16 (a) was targeted and DC offset voltages were calibrated during fine (or stage 2) and finer (or stage 3) calibration, the results of which are shown in Fig. 16 (b) and Fig. 16 (c). These results were obtained by averaging 100 million samples in order to filter

FIGURE 14. LRS and HRS values for 10 switching cycles of an OxRAM of the 4 × 4 memristive crossbar.
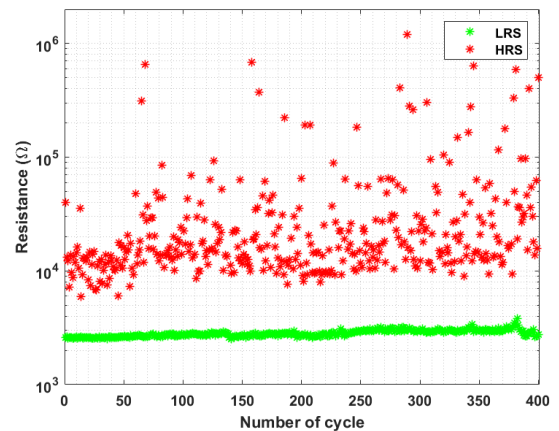

FIGURE 15. Switching of a synapse's OxRAM resistance between HRS and LRS for 400 cycles.

out noise, with standard deviation of about 200μ V. Experimental results of the three-stage calibration scheme have been discussed in detail elsewhere [83]. The pre-synaptic lines
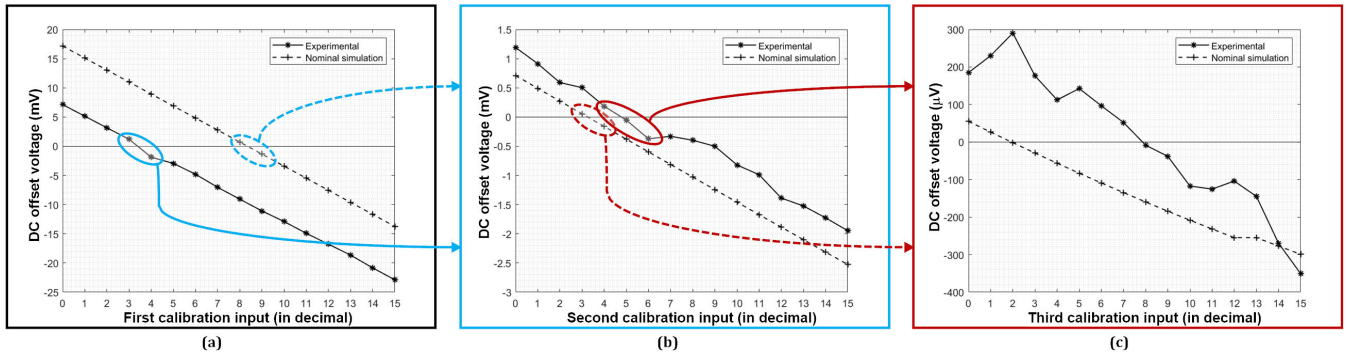
FIGURE 16. Comparison of experimental and simulation results of DC offset voltage calibration across one pre-synaptic line. (a) For coarse (or stage 1) calibration, (b) for fine (or stage 2) calibration, and (c) for finer (or stage 3) calibration.
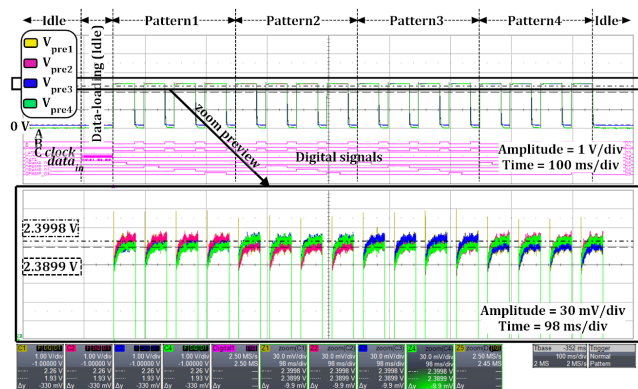

FIGURE 17. Calibrated pre-synaptic lines ($V_{pre\{1,2,3,4\}}$) and digital signals (A, B, C, *clock* and *data$_{in}$*) during an inference.

FIGURE 18. Measured drift of DC offset with time over a 50-minute period. One thousand offset measurements were taken during this time. The running average over 100 consecutive measurements is shown as a thick continuous line.

were calibrated in such a manner that they aligned in the same level with the lowest possible mismatch. Fig. 17 shows the calibrated pre-synaptic lines ($V_{pre\{1,2,3,4\}}$), together with digital signals (A, B, C, *clock* and *data$_{in}$*) during inferences. Pattern$\{1,2,3,4\}$ are the input pulses fed across the pre-synaptic lines of the crossbar. These details are discussed briefly in Section III-C. Here, the 'active' pre-synaptic lines were biased with 2.3998V and the 'default' pre-synaptic lines were biased with 2.3899V (9.9mV difference). We can therefore appreciate the alignment of calibrated pre-synaptic lines when the difference between the 'active' and 'default' biases is kept at around 10mV.

To determine how the DC offset voltage drifts, calibration was performed every 3 secs for 50 minutes (1000 measurements). Fig. 18 shows the offset variation with respect to time. Here, both the observed and the moving average offset (mean recorded offset in 5 minutes) values were recorded. We can see how the offset voltage (which was initially calibrated at around 1mV) drifted slowly and crossed 'zero' after 30 mins. Later, the offset moved towards negative values. We see a noise envelope of about 4mV around the mean value. The difference between the maximum and minimum peaks was about 8mV during this time frame. Due to this drifting of the offset, attempts were made after calibration to finish the experiments (as described in Section III-C and Section III-D)

FIGURE 19. Patterns used for recognition-task using 4 × 4 crossbar: (a) Pattern1, (b) Pattern2, (c) Pattern3, (d) Pattern4.

in a short period of time. In practical applications with minimum read pulses down to just a few mV, re-calibration should be performed frequently.

C. TEMPLATE MATCHING USING MINIMUM INFERENCE PULSES ON OFFSET CALIBRATED MEMRISTIVE CROSSBAR

Our goal was to use the minimum possible 'inference' pulses after offset-calibration of the opamps for inference computations. To do this, we initially considered a template matching

FIGURE 20. Conceptual block diagram showing patterns fed as read pulses across the pre-synaptic lines (or rows) of the calibrated crossbar with synaptic weights switched to learned values.

FIGURE 21. Output ($V_{o\{1,2,3,4\}}$) of opamp ($A_{\{1,2,3,4\}1}$) and digital signals (A, B, C, *clock*, *data_{in}* and $V_{out\_inv\{1,2,3,4\}}$) for template-matching using read voltage of 14mV.

experiment in which we programmed the crossbar with given weights and then performed inference. The patterns (Pattern1, Pattern2, Pattern3, and Pattern4) in our experiment are shown in Fig. 19. Fig. 20 shows a conceptual block diagram of how patterns were fed in as 'input' pulses across the pre-synaptic lines of the cro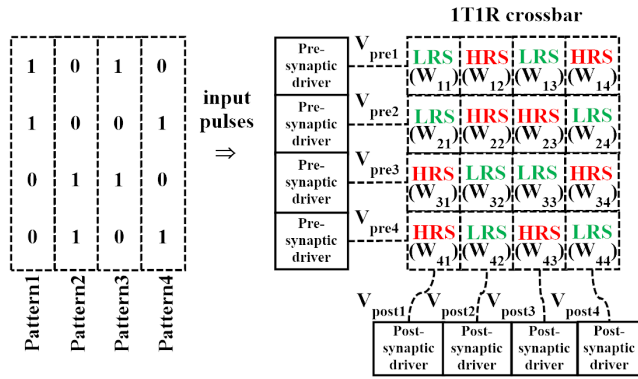ssbar, the synapses of which were programmed with patterns 1 to 4 in Fig. 19. The FPGA was programmed in such a way that clicking the 'Weight update' push-button would update all weights and this would be followed by inference. The weights were updated to set the synapses to the desired weights, as shown in Fig. 20.

Initially, the OxRAMs in the 4×4.1T1R crossbar were formed one-by-one and set to weights as shown in the crossbar of Fig. 20. The pre-synaptic opamps were then calibrated for DC offset compensation as explained in Section III-B. Following this, an inference was carried out for the patterns (shown in Fig. 19) in the sequence: Pattern1, Pattern2, Pattern3, Pattern4. This was done by applying input pulses at the pre-synaptic lines in the sequences needed for the planned patterns.

Let us first consider Pattern1. This pattern had binary inputs in the sequence '1', '1', '0', '0', so two minimum 'inference' pulses were applied during its inference: one at V_{pre1} and another at V_{pre2}. The remaining pre-synaptic lines, $V_{pre\{3,4\}}$, remained fixed at their reference levels. With reference to Fig. 7, for the applied inference pulses there would be current flowing through the post-synaptic lines V_{postj}, which would be integrated at opamps A_{j1} (with $C_{integ} = 908nF$), resulting in corresponding voltage decrements at nodes V_{oj}. These output voltages were then compared with the reference voltage $V_{comp} = 1.7V$ using opamp A_{j2}, resulting in output voltage V_{outj} (or its digital inverted version V_{out_invj}). For Pattern1, as the contributing synapses $W_{\{11,21\}}$ of post-synaptic line V_{post1} had net strong weights (LRS) in comparison with synapses $W_{\{12,22\}}$, which contributed to V_{post2}, with synapses $W_{\{13,23\}}$, which contributed to V_{post3}, or with synapses $W_{\{14,24\}}$, which contributed to V_{post4}, the output of the comparator opamp (A_{12}) V_{out1} ramped down faster and spiked earlier than the rest. Consequently, V_{out_inv1} would result
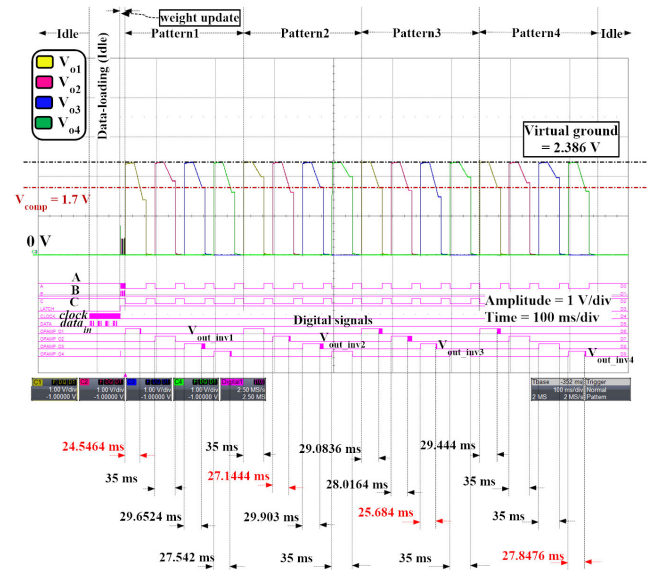
in the shortest pulse-width in comparison with the others. Inference for the other patterns occurred in a similar way.

Fig. 21 shows the outputs V_{oj} of integrating opamps $A_{\{1,2,3,4\}1}$ for each of the four applied input patterns. For visualization purposes, each input pattern is applied four times in sequence, with only one V_{oj} being displayed each time. Between each input pattern application, all four integrators were reset. The output voltage V_{oj} that reached comparison level $V_{comp} = 1.7V$ the fastest indicated that post-synaptic node j was the closest match to the applied input pattern. The slopes at nodes V_{oj} ramped down for 15ms, which is the time interval the gate lines were activated. Fig. 21 also shows digital control signals A, B, C, clock, and data$_{in}$, which loaded the calibration and configuration bits and set the signal sequence for input pattern application. Also shown in Fig. 21 are the digital post-synaptic outputs V_{out_invj}. The duration of each of these is annotated for each input pattern. The shortest duration is marked in red, indicating it was the best match to the applied input pattern: for Pattern1, output V_{out_inv1} provided the shortest duration of 24.55ms; for Pattern2, output V_{out_inv2} provided the shortest duration of 27.14ms; for Pattern3, output V_{out_inv3} provided the shortest duration of 25.68ms; and for Pattern4, output V_{out_inv4} provided the shortest duration of 27.85ms, as expected according to the synaptic values stored.

In order to find the smallest read pulses for inference, the 'read' amplitude was reduced in steps, starting from 0.13V, by increasing the 'virtual ground' (the lower-level voltage of the read pulses). The initial value of this 'virtual ground' or active post-synaptic line voltage during 'read' was 2.27V and is shown in Fig. 12 in Section III-A. Fig. 22 shows the results when the read voltages were reduced to the smallest values we could adjust them to while still operating properly (down to around 2 mV). The same figure shows
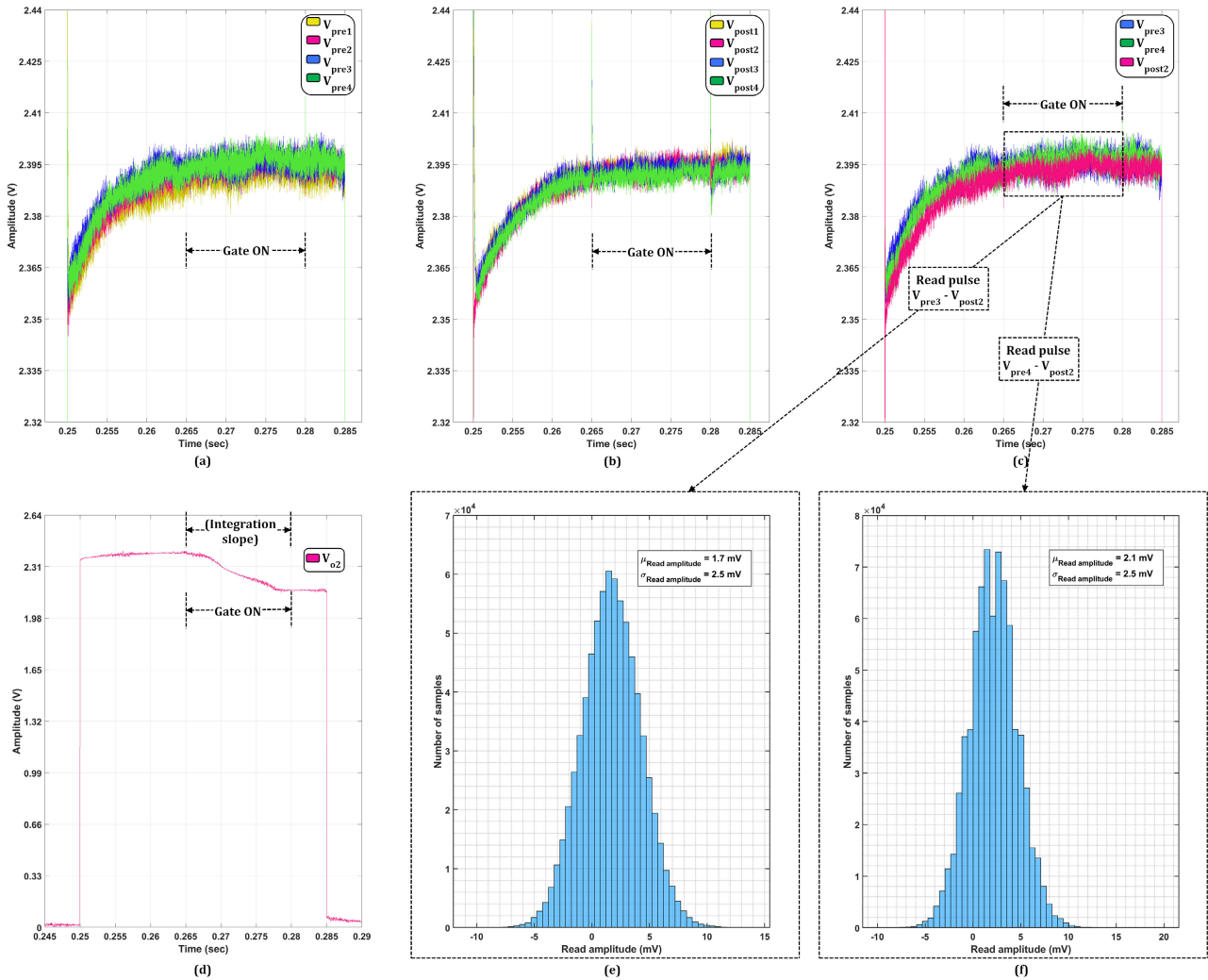
FIGURE 22. Applying tiny input pulses (for Pattern2) across calibrated pre-synaptic lines. (a) Zoom preview of the pre-synaptic lines, ($V_{pre\{1,2,3,4\}}$), (b) Zoom preview of the post-synaptic lines ($V_{post\{1,2,3,4\}}$). (c) Zoom preview of the pre-synaptic and post-synaptic lines that constitute the two read pulses (V_{pre3} - V_{post2}) and (V_{pre4} - V_{post2}). (d) Output (V_{o2}) of opamp (A_{21}) during inference. (e) Statistical spread of read voltage for read pulse (V_{pre3} - V_{post2}) when gate is 'ON'. (f) Statistical spread of read voltage for read pulse (V_{pre4} - V_{post2}) when gate is 'ON'.

the input pulses applied for 'Pattern2' and the inference output for V_{post2}. Here, $C_{integ} = 104nF$ was used. Fig. 22(a, b) show the details of all pre-synaptic and post-synaptic lines during inference. Fig. 22(c) shows the pre-synaptic and post-synaptic lines that constituted the two active read pulses for Pattern2 (V_{pre3} - V_{post2}) and (V_{pre4} - V_{post2}). Fig. 22(d) shows the output (V_{o2}) of opamp (A_{21}) during inference. As can be seen, significant noise was present at the read pulses. Fig. 22(e, f) show the noise data histograms of read amplitudes for the two read pulses (V_{pre3} - V_{post2}) and (V_{pre4} - V_{post2}) during the time the gate was 'ON'. The first read pulse had a mean value of 1.7mV, while the standard deviation of the measured data points was 2.5mV, meaning that the instantaneous measured read amplitude became negative for a considerable part of the total time. The mean amplitude for the second read pulse was 2.1mV, while noise standard deviation was also 2.5mV, again resulting in

some negative instantaneous read pulse amplitudes. However, as the read pulses were integrated over a much longer period, only their average values contributed to the final integral, while the high frequency voltage noise (of $\sigma = 2.5mV$ or amplitude $\approx 6\sigma = 15mV$) passed through. This can be seen in Fig. 22(d), where the integration slope is shown with a superimposed noise in the range of about $\sqrt{2} \times 15mV = 20mV$ amplitude.

The question remains of whether the noise we measured came mainly from the chip or from the experimental setup and oscilloscope, and what ratio each element was contributing. From our noise transient simulations of the in-chip circuitry, we obtained intrinsic noise histograms with standard deviations of about $120\ \mu V$. We therefore suspect that the dominant noise we measured was produced by off-chip elements, such as PCB components or the instruments.
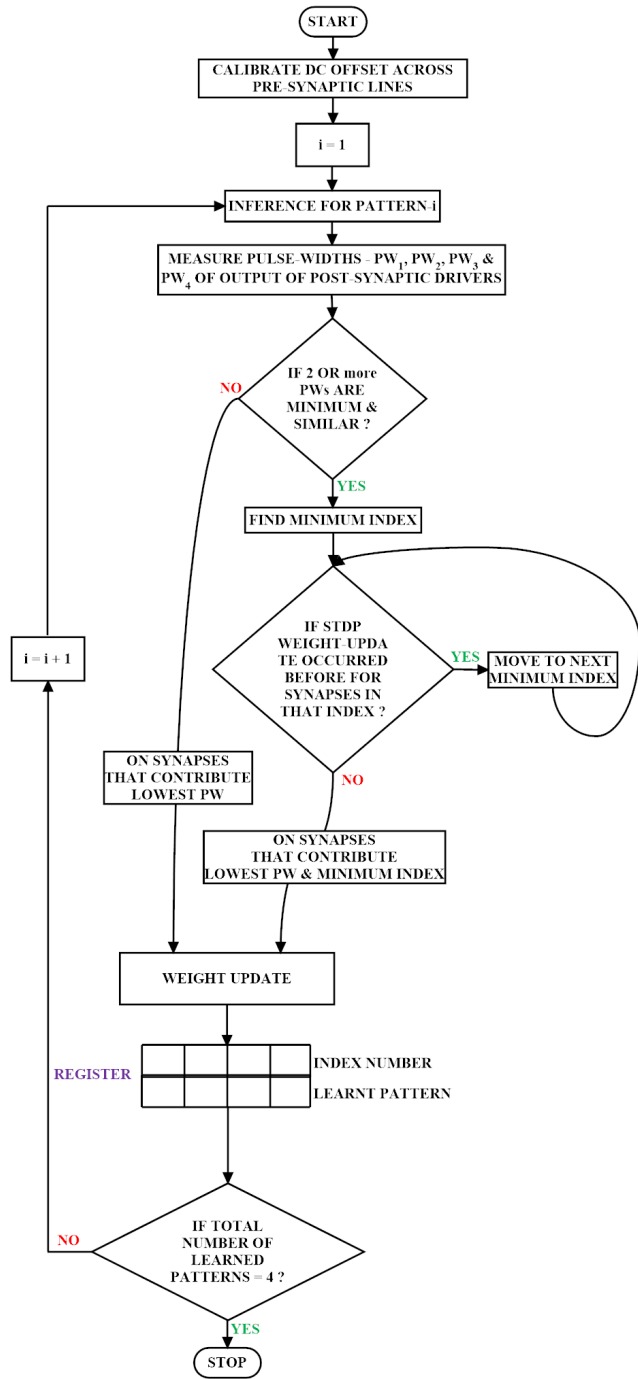
FIGURE 23. Flowchart for inference and STDP learning on offset calibrated 4 × 4 1T1R crossbar for pattern recognition.

FIGURE 24. Output ($V_{o\{1,2,3,4\}}$) of opamp ($A_{\{1,2,3,4\}1}$) and digital signals (A, B, C, *clock*, *data$_{in}$* and $V_{out\_inv\{1,2,3,4\}}$) during 1st weight-update.

FIGURE 25. Output ($V_{o\{1,2,3,4\}}$) of opamp ($A_{\{1,2,3,4\}1}$) and digital signals (A, B, C, *clock*, *data$_{in}$* and $V_{out\_inv\{1,2,3,4\}}$) during 2nd weight-update.

D. PATTERN RECOGNITION BY STDP LEARNING

The second experiment we considered was pattern recognition using STDP learning. Here, weight updates were performed based on the time of occurrence of pre-synaptic and post-synaptic pulses. When the post-synaptic pulse spiked after the pre-synaptic pulse, the weight of the corresponding synapse was strengthened by decreasing the resistance. In contrast, when the pre-synaptic pulse spiked after the post-synaptic pulse or when there was no pre-synaptic pulse,

the weight of the corresponding synapse was weakened by increasing the resistance. A condition (prioritisation of the minimum index of the post-synaptic line with contributed synapses that had not previously been subject to weight updates) was used when two or more post-synaptic pulses spiked at the same time. Initially, the weights were kept random.

The FPGA driver board was programmed in such a way that the user could initially calibrate DC offset as explained in Section III-B and then proceed to the pattern recognition task. Achieving minimum pulse-width at the output of a post-synaptic driver during inference for an input pattern is an indication of minimum distance or maximum similarity between that driver's applied and stored patterns. In this case the contributing weights were strengthened (resistance was lowered).

Fig. 23 shows the flowchart used for inference and STDP learning. The procedure was as follows: (a) DC offset
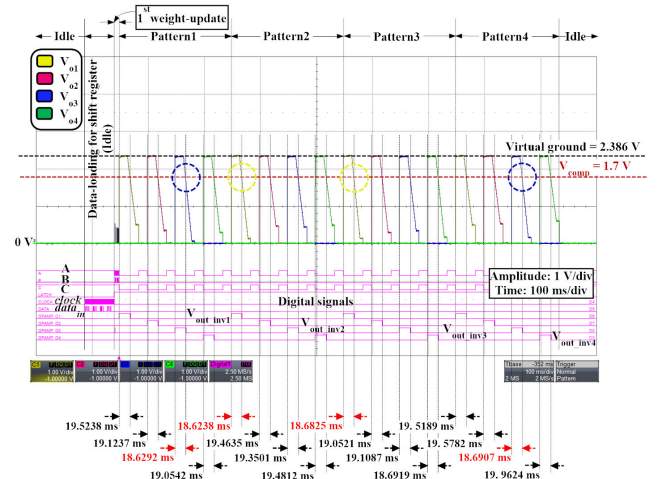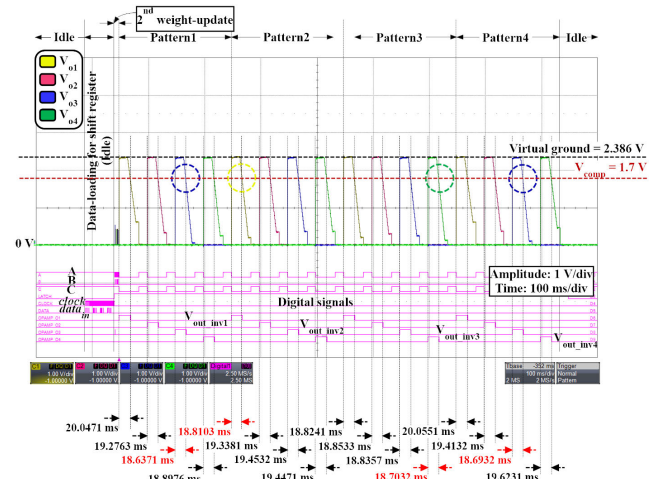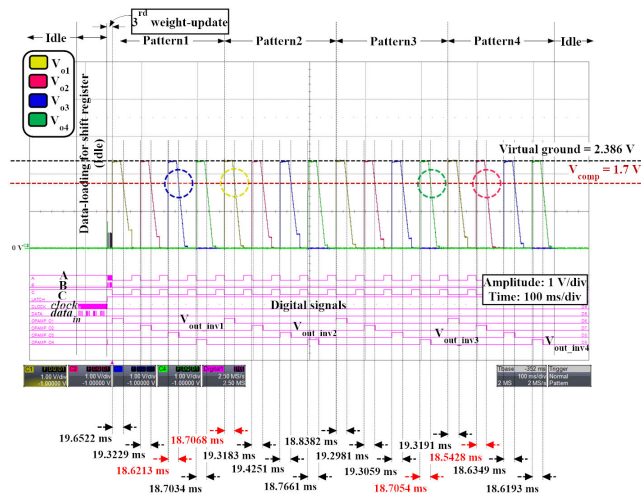
FIGURE 26. Output ($V_{o\{1,2,3,4\}}$) of opamp ($A_{\{1,2,3,4\}1}$) and digital signals (A, B, C, *clock*, *data$_{in}$* and $V_{out\_inv\{1,2,3,4\}}$) during 3rd weight-update.

calibration of pre-synaptic line amplifiers as explained in Section III-B. (b) An inference was then performed for the first Pattern. The resulting pulse-widths of the outputs (V_{out_invj}) of the post-synaptic drivers were measured. (c) The STDP weight update was performed on the synapses that contributed minimum pulse-width at the output of the post-synaptic driver, whereas the rest of the weights were kept untouched. When two or more pulse-widths were similar and minimum, priority was given to the one that had the minimum index number and to those contributing synapses that had not undergone weight updates earlier. (d) The trained patterns and their index numbers were both stored in a register, which was later used to learn future patterns for checking whether synapses had undergone weight updates earlier when two or more pulse-widths became minimum and similar. (e) The process was iterated for all patterns one-by-one and ended when all patterns had been learned.

Fig. 24 shows the outputs (V_{oj}) of opamps (A_{j1}) and digital signals (A, B, C, *clock*, *data$_{in}$* and V_{out_invj}) during 1st weight-update, where V_{out_inv3} resulted in the least pulse-width for 'Pattern1' and 'Patterns4'. This is indicated by two blue dashed circles. V_{out_inv1} resulted in the least pulse-width for 'Pattern2' and 'Patterns3'. This is indicated by two yellow dashed circles. Fig. 25 shows the output (V_{oj}) of opamp (A_{j1}) and digital signals (A, B, C, *clock*, *data$_{in}$* and V_{out_invj}) during 2nd weight-update, where V_{out_inv3} resulted in the least pulse-width for 'Pattern1' and 'Pattern4'. Here, V_{out_inv1} resulted in the least pulse-width for 'Pattern2' and V_{out_inv4} resulted in the least pulse-width for 'Pattern3'. These are indicated by yellow and green dashed circles, respectively. Fig. 26 shows the output (V_{oj}) of opamp (A_{j1}) and digital signals (A, B, C, *clock*, *data$_{in}$* and V_{out_invj}) during 3rd weight-update, where the synapses had almost learned the weights. Here, V_{out_inv1} resulted in the least pulse-width for 'Pattern2', V_{out_inv2} resulted in the least pulse-width for 'Pattern4', V_{out_inv3} resulted in the least pulse-width for

'Pattern1', and V_{out_inv4} resulted in the least pulse-width for 'Pattern3'. Fig. 26 is the only one to have four different colors of dashed circles, indicating the occurrence of learning.

IV. CONCLUSION AND FUTURE OUTLOOK

Present day OxRAM devices present resistance values as low as just a few kiloohms. Instantaneous read and inference currents through each device can therefore be in the range of many micro-amps or even mili-amps, thus hindering the implementation of large-scale crossbars for vector-matrix multiplication in typical neural computing applications due to excessive power dissipation. Here we explored the viability of using minimum amplitude inference stimulation pulses, as low as a few mV, to reduce power dissipation at the crossbar as much as possible, while at the same time relaxing the driving capability of the stimulation and integration circuits. One limitation in reducing input stimuli voltage amplitudes is the offset voltage mismatch of the driver circuits. To overcome this, in this work we explored the viability of using bulk-based calibration of differential pairs to minimize their input offset voltages. This was done by using minimum amplitude inference pulses for applications such as template matching and pattern recognition with STDP learning. Demonstrating these applications on a small-scale memristor crossbar, we verified satisfactory inference with minimum read pulses of about 2mV. This paves the way for low-power inference to increase scalability.

In the presented setup, post-synaptic drivers were implemented off-chip with commercial ultra-low offset voltages. This was required here as we wanted to be able to use memristor currents in the range of up to hundreds of μA (for non-minimum inference pulses). Consequently, integrating capacitors in the range of hundreds of nF were required, making the implementation of on-chip post-synaptic drivers inviable. In order to make it possible to implement the post-synaptic drivers on-chip, one solution is to downscale the memristor currents by several orders of magnitude before integrating them. This can be done by using multi-decade current down-scaling circuits, which we have investigated before [86]. In that case, offset voltage calibration should be applied both at the pre-synaptic lines and at the post-synaptic lines of the memristor crossbar. Another alternative, which avoids multi-decade current down-scaling, is to perform ultra-fast inference through stimulation pulses in the range of nano-seconds. However, this imposes the careful design of very high speed pre- and post-synaptic drivers, which would again require high power consumption. In the long term, the best solution would most probably be the combination of low amplitude and fast inference pulses together with new memristor devices with much larger ON resistance values. Another factor worthy of careful consideration is the impact of noise, which will limit very high-speed integration, as one requires to average it out. Finally, offset drift is also relevant when it becomes comparable to the read amplitude and should be taken into account, for example through frequent re-calibration.

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