A Modular Current-Mode High-Precision Winner-Take-All Circuit

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Abstract

In this paper we present a Winner-Take-All (WTA) circuit realized using current-mode circuit design techniques. The operation of the WTA is based on current comparators and current mirrors. Speed and precision is determined primarily by the characteristics of the current mirror used. Using special current mirrors, resolutions below 1% and settling times below 100ns were simulated. The circuit remains operative with reasonable speed and precision for an input signal range wider than two decades. It requires current input signals and provides voltage output signals.

I. Introduction

In the last years the field of current-mode signal processing has been receiving considerable attention, and more circuit designers are using current-mode circuit design techniques to develop compact and fast A/D converters [1], filters [2], neural networks [3], and fuzzy operators [4]. In the area of neural networks and fuzzy signal processing a very common building block is the Winner-Take-All (WTA) circuit (also called *Max-operator*). Several WTA circuit topologies have been reported in the literature. Some of them operate with voltage signals [5], and others operate with current input signals [6]. However, all of them rely on the good matching of the V_T of an array of transistors. The number of transistors in this array is equal to the number of inputs. This fact imposes that all transistors of a WTA have to be inside the same chip (or, at least, the same wafer). If there is a need to assemble a large neural net composed of several chips and with a WTA circuit distributed among these chips, the performance in precision of the WTA may become drastically degraded. In this paper we present a current-mode WTA circuit which requires current input signals, and is therefore suitable for a current signal processing environment. The circuit can be extended between several chips, without loss of precision for the overall system performance. In the present paper we will first describe the mathematical principle of operation of the WTA. Afterwards, we will study the stability of the equilibrium point, followed by the verification of the global stability of the circuit. Then we will consider several current mirror topologies to be used in the circuit. Finally we will present Hspice simulation results that characterize the operation of the current-mode WTA circuit.

II. Description of WTA Operation

Analytically, the problem of finding the maximum value among a set of input values $\{x_i\}$ can be stated as the solution y of the following nonlinear algebraic equation

$$y = \sum_{i=1}^{N} \alpha_i U(x_i - y) \tag{1}$$

where α_i are positive parameters that need to meet some conditions, and $U(\cdot)$ is the step function

$$U(x) = \begin{cases} 1 & if \quad x > 0 \\ \in (0,1) & if \quad x = 0 \\ 0 & if \quad x < 0 \end{cases} \tag{2}$$

For example, consider the special case for eq.(1) in which $N=4$, as shown in Fig. 1. In this case, the solution of eq.(1) is given by the intersection of the curves $f_1(y) = \sum \alpha_i U(x_i - y)$ and $f_2(y) = y$, which is point A. At point A we have

$$y = x_4 = max\{x_i\} \tag{3}$$

which is the maximum of the input set values. Looking at Fig. 1 we can see that if we impose the condition

$$\alpha_i \geq x_i \qquad \forall i \tag{4}$$

then the curves $f_1(y)$ and $f_2(y)$ will intersect at the point that defines the maximum of the set $\{x_i\}$. In order to implement eq.(1) in an electronic circuit, some dynamics need to be added. Practical circuits are described by time-domain differential equations, therefore we need a differential equation whose solution is eq.(1). Consider, for example, the following time-domain first order differential equation,

$$\tau \dot{y} = -y + \sum_{i=1}^{N} \alpha_i U(x_i - y) \tag{5}$$

The steady-state solution of this equation is precisely eq.(1). For this solution to be stable, it is required that

$$\left.\frac{d\dot{y}}{dy}\right|_{Solution} < 0 \tag{6}$$

This means that the stability condition for eq.(5) is

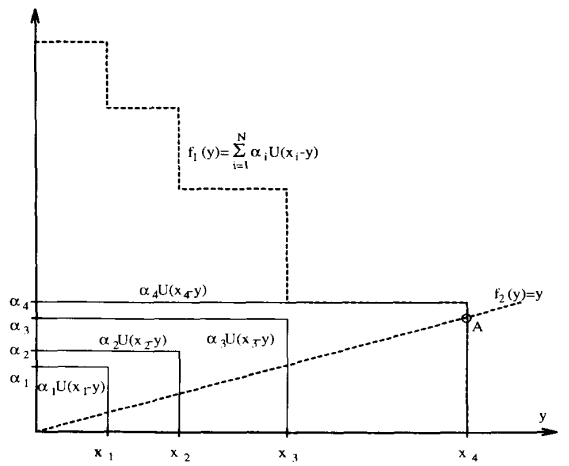

Fig. 1: Graphical representation of a particular case of eq.(1)

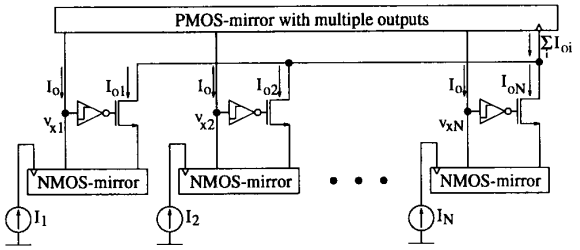

Fig. 2: Circuit diagram of complete current-mode WTA

$$-1-\sum_{x_i \geq y} \alpha_i \delta(x_i - y) < 0 \qquad (7)$$

$\delta(\cdot)$ being the derivative of the step function. This condition is always fulfilled.

III. Current-Mode Circuit Implementation

The circuit implementation that follows implements the mathematical model of eq.(1) with the coefficients $\{\alpha_i\}$ defined as

$$\alpha_i = x_i \qquad \forall i \qquad (8)$$

The circuit that implements each of the terms $\alpha_i U(x_i\text{-}y)$ of eq.(1) can be seen in Fig. 2. The equivalences between this circuit parameters and the parameters in eq.(1) are as follow:

$$y \equiv I_o \qquad x_i \equiv I_i \qquad \alpha_i \equiv I_i$$
$$\alpha_i U(x_i - y) \equiv I_{oi} \qquad (9)$$

In its steady state, the WTA circuit (see Fig. 2) solves the following equation,

$$I_o = \sum_{i=1}^{N} I_{oi} \qquad with \qquad I_{oi} = I_i U(I_i - I_o) \qquad (10)$$

For the current comparator a simple inverter can be used, or a high performance comparator [7]. The precision of the WTA circuit of Fig. 2 is limited by the current mirrors mismatch errors. Current replication through current mirrors is subject to errors produced by the mismatch between transistors inside the same current mirrors. Therefore, if it is needed to extend the WTA among several chips, the precision can be made insensitive to inter-chip electrical parameters spread by keeping all the transistors of the same current mirror inside the same chip. This can be achieved by using the assembling technique depicted in Fig. 3, which requires the addition of only one extra current mirror. By this approach, the precision of the overall WTA circuit is insensitive to electrical parameters spread between different chips.

IV. Stability Considerations

In this Section we will first study the conditions to make stable the unique steady-state equilibrium point, followed by a global stability study of the complete system. The stability of the equilibrium point is based on local considerations and is therefore performed through a small signal linear circuit analysis. The global stability, however, needs nonlinear large signal considerations, and is based on Liapunov's stability theory [8].

A. Local Stability of the Equilibrium Point

If the operation of the WTA circuit of Fig. 2 is stable, there should be a unique steady state in which all N-mirror cells, except one, are OFF (I_{oi}=0), and I_o=I_i^{max}. In this case, the active part of the circuit is given by the diagram shown in Fig. 4(a), where transistor *M1* is in its ON state and driving

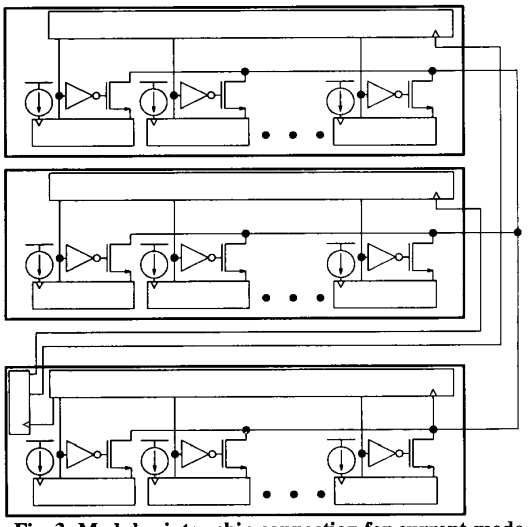

Fig. 3: Modular inter-chip connection for current-mode WTA

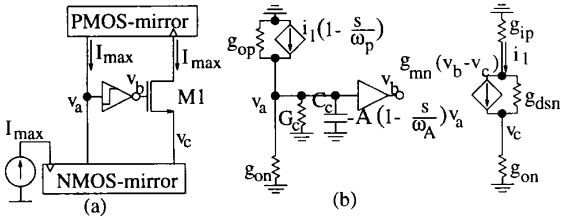

Fig. 4: Steady state representation of WTA current-mode circuit. (a) Circuit diagram, (b) small signal equivalent circuit

the complete I_{max} current. Fig. 4(b) represents the corresponding small signal equivalent circuit, where the main delay elements have been included. Elements C_c and G_c represent the input impedance of the current comparator, A its voltage gain, and ω_A accounts for its internal delay. Conductances g_{on} represent the output impedance of the NMOS current mirror, and for the PMOS current mirror g_{ip} is its input impedance, g_{op} its output impedance, and ω_p defines its delay. For transistor *M1*, only the static parameters g_{mn} and g_{dsn} are considered. Its delay has been included in parameter ω_A. Analysis of this small signal equivalent circuit yields the following second order characteristics equation,

$$s^2 + s\left(\frac{\omega_A \omega_p}{A}\frac{C_c(g_{mn}+g_{on})}{g_{mn}g_{on}} - \omega_A - \omega_p\right) + \omega_A\omega_p = 0 \qquad (11)$$

which is stable if

$$\frac{C_c(g_{mn}+g_{on})/A}{g_{mn}g_{on}} > \frac{1}{\omega_A} + \frac{1}{\omega_p} \qquad (12)$$

Therefore, stable steady-state WTA operation requires fast current mirrors and comparators, but dominating input comparator dynamics and small comparator voltage gain.

B. Global Stability of the System

Note however, that now there are N dominant dynamic elements in the complete WTA during the transient regimes: capacitors C_c at the input of each current comparator. Therefore, the dynamics of the system is not a first order one as was supposed in eq.(5), but it is of order N. Nevertheless,

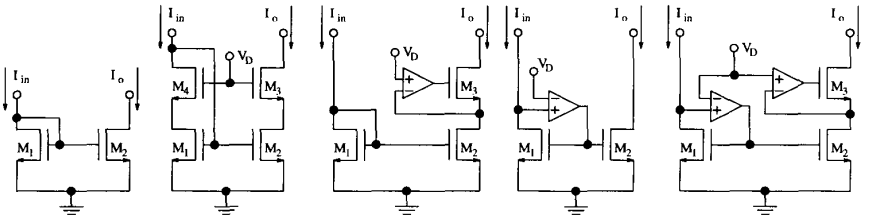

Fig. 5: Current mirror topologies: (a) simple, (b) cascode, (c) regulated cascode [10], (d) active-input [1], (e) active-input regulated cascode [12]

stability analysis can be performed through the use of *Liapunov's* stability theorems [8]. The dynamics of the WTA, assuming capacitors C_c are the dominant dynamic elements, are described by the following set of N first order nonlinear differential equations,

$$C_c \dot{v}_{xi} = -G_c(v_{xi} - v_M) - I_i + \sum_{j=1}^{N} I_j U(v_M - v_{xj}) \tag{13}$$

where v_M is the voltage trip point at the comparators input, and the cell current I_{oi} is described now by,

$$I_{oi} = I_i U(v_M - v_{xi}) \tag{14}$$

Note that, since

$$I_o - I_i = G_c(v_{xi} - v_M) + C_c \frac{d}{dt}(v_{xi} - v_M) \tag{15}$$

there still exists the unique steady-state solution of eq.(10). Under these circumstances, the following scalar function[1],

$$E = \frac{1}{2}\sum_{ij} I_j U(v_{xi} - v_M)\, U(v_{xj} - v_M) + \\ + G_c \sum_i \int_0^{U(v_{xi} - v_M)} U^{-1}(\vartheta)\, d\vartheta + \sum_i (I_i - \sum_j I_j)\, U(v_{xi} - v_M) \tag{16}$$

is a Liapunov function of the *Nth* order WTA system. Computing the time derivative of this function yields,

$$\dot{E} = \sum_{i=1}^{N} U'(v_{xi} - v_M)\, \dot{v}_{xi} p_i \\ p_i = \left[\sum_{j=1}^{N} I_j (1 - U(v_{xj} - v_M))\right] - G_c(v_{xi} - v_M) - I_i \tag{17}$$

where p_i is, by eq.(13), equal to $C_c \dot{v}_{xi}$, thus

$$\dot{E} = -C_c \sum_{i=1}^{N} U'(v_{xi} - v_M)\, \dot{v}_{xi}^2 \le 0 \tag{18}$$

Since $U(\cdot)$ is monotonically increasing ($U'(x) \ge 0,\ \forall x$), it then results that our WTA circuit will make decrease in time the Liapunov function E. Since E is bounded from below the circuit described by eq.(13) will have a steady state ($\dot{v}_{xi} = 0$) which is a minimum of the Liapunov function E. By Liapunov's theorems [8] this means that eq.(13) describes a stable system that converges asymptotically to its unique solution given by (see eq.(3)),

$$I_o = max\{I_i\} \tag{19}$$

1. In order to apply Liapunov's theorems let us approximate the step function $U(\cdot)$ by the following continuous and differentiable function with $\varepsilon > 0$ but close to zero, $U(z) = \dfrac{1}{1 + e^{-z/\varepsilon}}$

V. Election of Current Mirrors

The precision of the overall WTA current mode circuit is determined by the election of the kind of current mirrors used. Since a current comparator has virtually no offset [7], the current error at the input of each current comparator is determined by mirror mismatches. The error at the positive current I_o available at the input of each current comparator results from one p-mirror reflection, preceded by an n-mirror reflection of the winning cell,

$$\sigma^2(I_o) = \sigma_N^2 + \sigma_P^2 \tag{20}$$

while the error of the negative current I_i at the current comparators inputs results from a single n-mirror reflection,

$$\sigma^2(I_i) = \sigma_N^2 \tag{21}$$

The total current error at the input of each current comparator is therefore given by,

$$\sigma_{Total}^2 = \sigma^2(I_o) + \sigma^2(I_{oi}) = 2\sigma_N^2 + \sigma_P^2 \tag{22}$$

However, the error introduced by a current mirror is not only the random mismatch contribution, as considered by eqs.(20)-(22), but also its *systematic* error contribution, which results from different drain-to-source voltages at the reflecting transistors, poor impedance coupling, and inherent nonlinear MOS transistor operation. The random mismatch error contribution of a current mirror is almost topology independent and is determined primarily by the area of the reflecting transistors [9]. However, the systematic error contributed by a current mirror is highly topology dependent. Consider, for example, the five current mirror topologies of Fig. 5. If they all have the same reflecting transistors (*M1* and *M2*) sizes ($W=100\mu m$ and $L=20\mu m$), $V_D=1.5V$, and they are loaded by their complementary PMOS current mirrors with equivalent input impedance, their total current error defined as

$$\Delta I_{Total} = \Delta I_{systematic} + \sigma_I \tag{23}$$

is shown in Fig. 6. This error is expressed in bits, and is a function of the input current I_{in}, which in this case varies from $10\mu A$ to $800\mu A$. For the active-input regulated cascode current mirror, two curves are given: one with $A=100$ and the other with $A=1000$, where A is the voltage gain of the differential voltage amplifiers. Also shown in Fig. 6 is the random mismatch error contribution (σ_I in eq.(23)) which is approximately the same for all the topologies. According to our precision requirements, Fig. 6 can help us to select the most appropriate current mirror topology for our application. In our case we would like to maintain a good accuracy over a very wide signal range. Therefore, we will choose the active-input regulated cascode current mirror.

VI. Simulation Results

A current-mode WTA prototype has been designed for the digital $1.5\mu m$ single-poly CMOS process provided by ES2

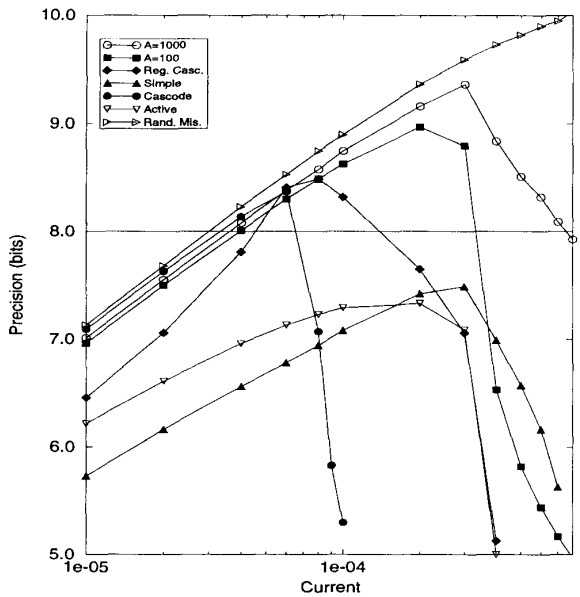

Fig. 6: Resolution (in bits) as a function of working current for different current mirror topologies: simple, cascode, regulated cascode, active-input, and active-input regulated-cascode with voltage gains *A=100* and *A=1000*

through the EUROCHIP service. The main specification for this design was to achieve a precision around *1%* for an input signal range of over 2 decades. According to this requirement, and with Fig. 6 in mind, the only possible current mirror that could achieve this is the active-input regulated-cascode one. Designing current mirrors with active input [1] is not a trivial task. They need to be compensated, and it is difficult to make them fast and stable. Things get even harder when they have to operate with a 2 decades variation in input current. We were able to obtain an acceptable design for our application with the aid of an optimization tool for circuit designers [11]. In a WTA, when maintaining an input at a maximum fixed value and sweeping the second maximum input around this point, let us define *trip-point* as the value of the second input at which this second input becomes the *winner*. Ideally the *trip-point* occurs when the two inputs are equal, however in practice this *trip-point* is characterized by a random variation. Table I shows the standard deviation, obtained through Hspice Monte Carlo simulations, of this *trip-point* for different operating point currents. Simulated speed characterizations are provided inTable II. Here a two input WTA has one of them at a constant value I_i while the other changes in a step fashion between $1/2I_i$ and $2/3\,I_i$. Time t_1 is the time required during a high-to-low transition of the output current I_{oi} to reach the final state with *1%* error. Time t_2 is the same, but for a low-to-high transition.Times t_3 and t_4 are the same simulated measurements than t_1 and t_2, respectively, but for an error of *10%*.

I_i	10μA	50μA	100μA	500μA	1.0mA	2.0mA
absolute	272nA	640nA	977nA	3.21μA	5.93μA	11.6μA
relative	2.72%	1.28%	0.98%	0.64%	0.58%	0.55%

Table I

I_i	t_1	t_2	t_3	t_4
10μA	676ns	1.69μs	653ns	680ns
50μA	328ns	404ns	321ns	331ns
100μA	309ns	363ns	301ns	314ns
500μA	79.9ns	109ns	78.6ns	78.0ns
1.00mA	47.0ns	50.1ns	45.3ns	49.0ns

Table II

VII. Conclusions

We have presented a current-mode WTA circuit that can be extended by inter-chip modular connections without loss of precision in its operation. Stability of the circuit has been studied theoretically and verified through Hspice simulations. A design has been performed and characterized through extensive simulations. Precision values below *1%* have been obtained.

VIII. References

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