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A Methodology for MOS Transistor Mismatch Parameter Extraction and Mismatch Simulation

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Abstract

This paper presents a methodology for mismatch parameter extraction and mismatch simulation using conventional electrical simulators, like HSpice. A measurement and extraction procedure has been carefully designed to be able to obtain reliable measurements of the mismatch parameters of a given technology. The correctness of this extraction procedure method has been checked through three different validation methods. We also present two methods for performing mismatch simulation with conventional circuit simulators (like HSpice) using the extracted parameters.

I. Introduction

Precise analog CMOS circuit design requires availability of confident transistor mismatch models during the design and simulation stages. During the design phase of an analog VLSI circuit, designers face many constraints imposed by the design specifications, such as speed, bandwidth, noise, precision, power consumption, area consumption, which need to be traded off for optimum overall performance. Designers must rely on accurate simulation tools in order to achieve a well optimized final design. Simulation tools are reliable as long as they are based on good models obtained through confident characterization techniques. Often it is not possible to simulate properly the precision limits that can be achieved by a certain circuit topology in a given fabrication process because VLSI circuit manufacturers rarely provide transistor mismatch information. Transistor mismatch affects offset voltage of differential pairs, errors in current mirrors, errors in arrays of identical current sources, ...

Elsewhere [1],[2], we have presented a very simple and cheap methodology to characterize transistor mismatch as a function of transistor width and length plus a new five parameters mismatch model that achieves better results than other mismatch models previously reported in literature [3],[4]. In this paper, we verify the correctness of this new mismatch model and the measurement/extraction procedure through three different validation methods. Also, we present two different methods of using the experimentally extracted mismatch transistor parameters in a conventional electrical simulator, like HSpice, to predict the offset voltage of differential pairs (or whatever circuit specification we may be interested at). The simulated offset is compared versus the experimentally measured one, showing a good agreement between both.

For mismatch characterization of a given technology we fabricate a special purpose chip in the corresponding technology[1]. Our chip consists of a matrix of 8×8 cells. Each cell contains NMOS and PMOS transistors of 30 different sizes. Since, some transistors in the periphery present large systematic deviations with respect to those in the inner cells, only the latter transistors where considered[5]. Transistor parameter mismatches are obtained by measuring pairs of identical transistors located in adjacent cells. Since in the chip there are 6×6 effective cells, there are 6 rows, each of which provides 5 pairs of adjacent cells. This results in 30 adjacent transistor pairs (for each transistor size and type).

For each transistor pair, four curves were measured. Two of them while operating in the ohmic region and the other two for saturation (always in strong inversion). These curves are

$$\textbf{Curve 1: } I_{DS}(V_{GS}),\ V_{SB} = 0V, V_{DS} = 0.1,\ V_{GS} \in [1.5, 5.0] \quad (1)$$

$$\textbf{Curve 2: } I_{DS}(V_{SB}), V_{GS} = 3.0V, V_{DS} = 0.1V, V_{SB} \in [0, 2.0] \quad (2)$$

$$\textbf{Curve 3: } I_{DS}(V_{GS}), V_{SB} = 0V, V_{DS} = 4.0V, V_{GS} \in [1.5, 5.0] \quad (3)$$

$$\textbf{Curve 4: } I_{DS}(V_{SB}), V_{GS} = 3.0V, V_{DS} = 4.0V, V_{SB} \in [0, 2.0] \quad (4)$$

The following strong inversion large signal transistor model is assumed [1]-[2],

$$I_{DS} = \beta \frac{V_{GS} - V_T(V_{SB}) - \frac{1}{2} V_{DS_{eff}}}{1 + \theta_o (V_{GS} - V_T(V_{SB})) + \theta_e V_{DS_{eff}}} \quad (5)$$

where,

$$V_T(V_{SB}) = V_{T0} + \gamma \left[\sqrt{\phi + V_{SB}} - \sqrt{\phi} \right] \quad (6)$$

and $V_{DS_{eff}}$ is defined as,

$$V_{DS_{eff}} = \begin{cases} V_{DS} & \text{for ohmic region} \\ V_{GS} - V_T(V_{SB}) & \text{for saturation} \end{cases} \quad (7)$$

These curves depend nonlinearly on the *large signal parameters* to be extracted (β, V_{T0}, θ_o, θ_e and γ) as well as on the measured data points $\{V_{GS}\}$ and $\{V_{SB}\}$. Therefore, these *large-signal parameters* should be extracted using nonlinear multi-parameters curve fitting techniques. For a given transistor pair, the mismatch in the extracted *large-signal parameters* is obtained by fitting the current mismatch data $\Delta I_{DS}/I_{DS}$ to its theoretical equation [1]-[2],

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_T} \left(\Delta V_{T0} + \frac{\partial V_T}{\partial \gamma} \Delta \gamma \right) + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta_o} \Delta \theta_o + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta_e} \Delta \theta_e \quad (8)$$

and extract from it the *mismatch parameters* ($\Delta\beta/\beta$, ΔV_{T0}, $\Delta\theta_o$, $\Delta\theta_e$, $\Delta\gamma$) simultaneously for curves 1 to 4.

This measurement/extraction procedure is repeated for the $N_T = 30$ transistor pairs. For each extracted *mismatch parameter* ΔP, its standard deviation $\sigma_{(\Delta P)}$ is computed, as well as all correlations between pairs of *mismatch parameters* $r_{(\Delta P_1, \Delta P_2)}$.

II. Validation of the Mismatch Model

In this section, we describe a few tests that we have performed to verify the correctness of our mismatch model and measurement/extraction procedure. The chip we have used for our measurements is fabricated in a standard $1.0\mu m$ double-metal single-poly CMOS technology.

A. Precision Test

A first test to validate our measurement procedure was to measure, repeatedly the same transistor 30 times and follow the same parameter extraction and statistical characterization

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procedure. We obtain a set of standard deviations that give us an indication of the error of our instruments and mathematical algorithms.

When measuring the parameter P mismatch between two transistors the resulting measured ΔP value has two components,

$$\Delta P = \Delta P_{Real} + \Delta P_{meas} \tag{9}$$

where ΔP_{Real} is the real mismatch in parameter P between both transistors and ΔP_{meas} is an error component introduced by the measurement set-up and parameter extraction procedure. By repeating many measurements we obtain the quadratic deviation

$$\sigma^2_{(\Delta P)} = \sigma^2_{(\Delta P_{Real})} + \sigma^2_{(\Delta P_{meas})} \tag{10}$$

because the random transistor mismatch and the measurement errors are supposed to be uncorrelated. By repeating the same measurement over the same transistor, we measure $\sigma_{(\Delta P_{meas})}$. The values of $\sigma_{(\Delta P_{meas})}$ resulted to be less than 1/3 of those of $\sigma_{(\Delta P)}$ in the worst case, and were normally below 1/10.

If N_T is the number of measurements of a normally distributed random variable, and these measurements are used to compute a standard deviation for this variable, $\sigma_{computed}$, then there is a confidence interval for the real standard deviation σ_{Real} [6]

$$r_L(N_T) \times \sigma_{computed} \le \sigma_{Real} \le r_H(N_T) \times \sigma_{computed}. \tag{11}$$

When $N_T = 30$ the 95% confidence interval is $r_L \cong 0.8$, $r_H \cong 1.3$. In our case $\sigma_{(\Delta P)}$ and $\sigma_{(\Delta P_{meas})}$ have been obtained by $N_T = 30$ measurements. On the other hand, we can define a (conservative) confidence interval for $\sigma_{(\Delta P_{Real})}$

$$\begin{aligned} (r_H^*)^2 \times \sigma^2_{(\Delta P_{Real})} &= max[\sigma^2_{(\Delta P_{Real})}] = r_H^2 \times \sigma^2_{(\Delta P)} - r_L^2 \times \sigma^2_{(\Delta P_{meas})} \\ (r_L^*)^2 \times \sigma^2_{(\Delta P_{Real})} &= min[\sigma^2_{(\Delta P_{Real})}] = r_L^2 \times \sigma^2_{(\Delta P)} - r_H^2 \times \sigma^2_{(\Delta P_{meas})} \end{aligned} \tag{12}$$

By defining

$$\alpha = \sigma_{(\Delta P_{meas})} / \sigma_{(\Delta P)} \tag{13}$$

it follows that

$$\begin{aligned} r_H^*(N_T) &= \sqrt{\frac{r_H^2(N_T) - \alpha^2 r_L^2(N_T)}{1-\alpha^2}} \\ r_L^*(N_T) &= \sqrt{\frac{r_L^2(N_T) - \alpha^2 r_H^2(N_T)}{1-\alpha^2}} \end{aligned} \tag{14}$$

Fig. 1 depicts the values of r_H^* and r_L^* as a function of α when $N_T = 30$. Note that even for values of α as high as 0.5 there is still a reasonable confidence interval for $\sigma_{(\Delta P_{Real})}$ (approximately $\pm$ 50%). Since, in our case, the worst case α is less than 1/3, by Fig. 1 we can see that for this worst case, the confidence interval is not significantly degraded. This kind of precision test is also called in the literature *repeatability study* [4]. However, with this *repeatability study*, the only thing we can conclude is that whatever has been measured, it has been measured with acceptable precision. But that does not assure that the obtained statistical mismatch parameters are a good measurement of the physical quantities $\sigma_{(\Delta P)}$ and their respective correlations $r_{(\Delta P_1, \Delta P_2)}$. To verify this, other tests have to be performed.

B. Predicting $\sigma_{(\Delta I_{DS}/I_{DS})}$ of the Measured Curves

If we compute the standard deviation of $\sigma_{(\Delta I_{DS}/I_{DS})}$ in eq.(8), the following expression is obtained,

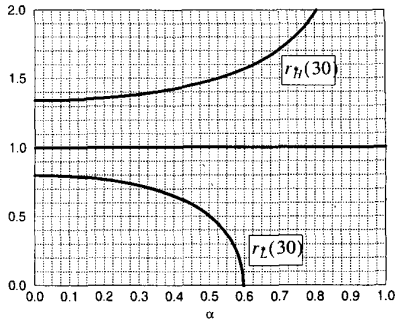

Fig. 1: Plot of r_H and r_L as a function of α

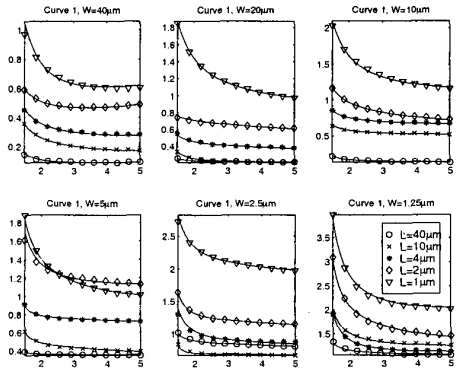

Fig. 2: Simulated (solid lines) and measured values (marked symbols) of $\sigma_{(\Delta I_{DS}/I_{DS})}$ for curve 1 for all transistor geometries

$$\begin{aligned} \sigma^2_{(\Delta I_{DS}/I_{DS})} &= \sigma^2_{(\Delta\beta/\beta)} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_T}\right)^2 \left(\sigma^2_{(\Delta V_{T0})} + \left(\frac{\partial V_T}{\partial \gamma}\right)^2 \sigma^2_{(\Delta\gamma)}\right) \\ &+ \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_o}\right)^2 \sigma^2_{(\Delta\theta_o)} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_e}\right)^2 \sigma^2_{(\Delta\theta_e)} + correlation\ terms \end{aligned} \tag{15}$$

Thus, using the extracted mismatch parameters, $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$, $\sigma_{(\Delta\gamma)}$, $\sigma_{(\Delta\theta_o)}$, $\sigma_{(\Delta\theta_e)}$ and their corresponding correlation coefficients, we can compute the expected current mismatch curves $\sigma_{(\Delta I_{DS}/I_{DS})}$. Fig. 2 shows for the 30 geometries of NMOS type transistors a comparison between the measured $\sigma_{(\Delta I_{DS}/I_{DS})}$ (marked with symbols) versus the computed ones (solid lines) for curve 1. An excellent agreement is observed for all curves 1 to 4 [2].

This is already a very good indication that we are extracting correct enough mismatch parameters. Although we are predicting the same curves we have used to extract the mismatch parameters, the set of mismatch parameters we are extracting is unique, valid for all 4 curves.

However, a more severe test would be to predict other curves, obtained under different bias conditions. This is the test described next.

C. Predicting Differential Pairs Offset Voltage

In this section, we use the extracted statistical mismatch parameters to predict the offset voltage of differential pairs. To obtain direct measurements of differential pairs input voltage offset, for each pair of transistors in our mismatch characterization chip we measure the following curve

$$I_{DS}(V_{GS}),\ V_{SB} = cte, V_{DS} = 3.0V, V_{GS} \in [2.99V, 3.01V], \tag{16}$$

once for each transistor of the pair. The measured transistor are placed in adjacent cells located $363\mu m$ apart. Fig. 3 shows the

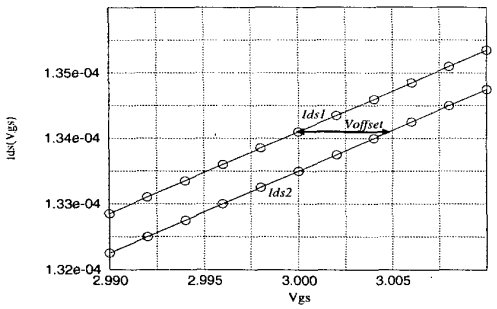

Fig. 3: Measured offset voltages for one pair of NMOS transistors

sizes	MEASURED		COMPUTED		SIMULATED (method1)		SIMULATED (method2)	
	$\sigma_{(V_{off})}$ (mV) (V_{SB}=0V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=1V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=0V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=1V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=0V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=1V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=0V)	$\sigma_{(V_{off})}$ (mV) (V_{SB}=1V)
40/40	1.3041	1.2369	1.281	1.235	1.90	1.69	1.4077	1.3548
40/10	3.1648	2.9778	3.128	2.984	2.67	2.33	3.2888	3.2454
40/4	4.4083	4.0222	4.296	4.036	4.41	3.90	4.4711	4.4122
40/2	5.7135	5.3017	5.575	5.401	7.80	6.99	5.4023	5.7256
40/1	12.1122	13.5417	12.575	14.079	17.29	15.68	14.0158	15.6491
20/40	2.5320	2.2303	2.528	2.265	2.20	1.91	2.5584	2.1511
20/10	2.9655	2.7695	2.931	2.763	3.29	2.84	3.1032	3.0614
20/4	5.2575	4.7859	5.194	4.817	5.44	4.77	5.2443	5.2064
20/2	8.3418	7.2832	8.279	7.407	9.41	8.39	7.8699	7.6360
20/1	20.8098	21.4372	21.110	22.027	20.20	18.28	23.1603	24.8110
10/40	1.8492	1.7251	1.830	1.712	2.87	2.46	1.8822	1.7797
10/10	6.6207	5.7666	6.504	5.829	4.31	3.70	6.6108	5.6031
10/4	8.8444	7.5801	8.744	7.698	7.02	6.12	9.0321	8.3982
10/2	10.7789	9.9204	10.442	9.896	11.87	10.52	10.3967	11.0116
10/1	24.4874	25.9678	24.572	26.831	24.77	22.37	27.1192	31.2029
5/40	3.9449	3.4340	3.921	3.481	4.32	3.66	4.1702	3.7580
5/10	5.4351	4.7066	5.328	4.715	6.01	5.10	5.5696	5.0075
5/4	8.7256	7.6528	8.694	7.695	9.29	8.02	8.6510	7.5812
5/2	17.7500	16.1167	17.645	16.218	15.29	13.45	18.7622	18.7392
5/1	18.2999	18.6891	18.319	18.818	31.19	27.97	20.4303	23.7233
2.5/40	9.3857	8.0999	9.400	8.243	7.33	6.09	9.9110	9.0891
2.5/10	7.6850	6.9679	7.640	6.967	8.83	7.37	8.3719	7.9461
2.5/4	13.8047	12.0785	13.218	11.907	12.29	10.47	14.7429	13.5792
2.5/2	15.6288	14.2745	15.825	14.497	19.30	16.84	16.1576	15.2941
2.5/1	30.0931	29.0792	30.247	29.488	38.67	34.35	32.7123	37.8362
1.25/40	11.6955	9.9583	11.749	10.190	13.28	10.66	12.8067	11.9650
1.25/10	16.4827	15.4563	16.428	15.305	13.68	11.07	19.3184	18.9713
1.25/4	14.9078	13.7128	14.526	13.417	15.61	13.04	16.4553	16.6279
1.25/2	22.2949	20.6132	21.782	20.573	21.83	19.02	24.1983	26.0047
1.25/1	33.3080	34.2983	34.300	34.713	42.60	37.61	40.0272	44.3559

Table 1

measured points for one pair of NMOS transistors of size $40\mu m \times 40\mu m$. Also shown in Fig. 3 are the corresponding interpolated lines of the measurements

$$I_{DS1}(V_{GS}) = m_1 V_{GS} + n_1$$
$$I_{DS2}(V_{GS}) = m_2 V_{GS} + n_2 \qquad (17)$$

Consequently, the offset voltage for this differential pair is given by

$$V_{off} = \frac{m_1 - m_2}{m_2}\ 3.0V + \frac{n_1 - n_2}{m_2}\ . \qquad (18)$$

For each pair of transistors the curves of eq.(16) were measured for two different values of V_{SB}. First for $V_{SB} = 0V$ (no substrate effect), and second for $V_{SB} = 1V$ (with substrate effect: $\Delta\gamma$ is affecting the offset voltage). The standard deviation for these offset voltages was computed for each transistor size and type. Table 1, under the columns named "MEASURED", indicates the measured values for $\sigma_{(V_{off})}$ as a function of transistor size and type.

In order to predict the standard deviation of this offset voltage using our extracted mismatch data, note that (see Fig. 3)

$$V_{off} = \frac{\Delta I_{DS}}{g_m} \quad \Rightarrow \quad \sigma_{(V_{off})} = \frac{I_{DS}}{g_m}\sigma_{(\Delta I_{DS}/I_{DS})}\ , \qquad (19)$$

where $\sigma_{(\Delta I_{DS}/I_{DS})}$ can be computed by evaluating eq.(15) in saturation, and I_{DS}/g_m can be calculated using the mean extracted large signal parameters ($\bar{\beta}$, $\overline{V_{T0}}$, $\bar{\theta}$, and $\bar{\gamma}$). The values of $\sigma_{(V_{off})}$ computed this way are also shown in Table 1 under the columns named "COMPUTED". Note that the computed values stay within the confidence intervals of the measured values.

III. Mismatch Simulations

The extracted mismatch parameters can be used in a conventional electrical circuit simulator, like HSpice, to predict circuit specifications such as offset voltages, error in the output current of a current mirror, etc. This can be a very valuable tool to design high performance circuits. HSpice simulations have been performed in order to predict the measured differential pairs input offset voltages of Table 1. We describe two simulation methods, both based on Monte Carlo simulations.

A. Method 1:

In this method the idea is to use the transistor model provided by the manufacturer and introduce into it random variations for some of the most mismatch sensitive parameters. In our case, the manufacturer model is a Level 6 Hspice model. Obviously the physical meaning of the large signal parameters (such as β, V_{T0}, θ and γ) is different than for the simple model we assumed during our mismatch characterizations (eqs. (5)-(6)). Besides this, and in our particular case, the manufacturer model does not include explicitly the mobility degradation parameter "θ". Consequently, we will use only $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$ and $\sigma_{(\Delta\gamma)}$ and ignore all correlations. The way to use this mismatch model in (H)Spice is as follows.

Each transistor in the netlist is substituted by a subcircuit call which includes a MOS transistor of the specified size and whose β, V_{T0}, and γ are recomputed by adding noise to them. If $\sigma_{(\Delta\beta/\beta)}$, $\sigma_{(\Delta V_{T0})}$, and $\sigma_{(\Delta\gamma)}$ are the extracted mismatch parameters then the recomputed values for β, V_{T0}, and γ are,

$$\beta^{new} = \beta^{nom} + \Delta\beta\ ,\ \Delta\beta = \beta^{nom} GAUS\left(mean{=}0, sigma{=}\frac{\sigma_{(\Delta\beta/\beta)}}{\sqrt{2}}\right)$$
$$V_{T0}^{new} = V_{T0}^{nom} + \Delta V_{T0}\ ,\ \Delta V_{T0} = GAUS\left(mean{=}0, sigma{=}\frac{\sigma_{(\Delta V_{T0})}}{\sqrt{2}}\right) \qquad (20)$$
$$\gamma^{new} = \gamma^{nom} + \Delta\gamma\ ,\ \Delta\gamma = GAUS\left(mean{=}0, sigma{=}\frac{\sigma_{(\Delta\gamma)}}{\sqrt{2}}\right)$$

where $GAUS(\cdot)$ is a normally distributed random number generation routine whose "*mean*" and "*sigma*" values have to be provided. Note that each deviation is divided by "$\sqrt{2}$". This is because the transistor defined by eq. (20) is deviated with respect to a nominal one. The HSpice input file section that performs what describes eq. (20) is:

```
.subckt nmod_typ Drain Gate Source Bulk width=w
length=l
m_nmod Drain Gate Source Bulk nmos w=w l=l
.MODEL NMOS NMOS
 + LEVEL   = 6.0        UPDATE = xxx
 + XL      = xxx        WDEL   = xxx   LATD   = xxx
 + VTO     = vto_n      TOX    = xxx   BETA   = beta_n
 + GAMMA   = gamma_n    VBO    = xxx   LGAMMA = xxx
 + NWE     = xxx        NWM    = xxx   SCM    = xxx
 + XXX
.param beta_n_global_typ=xxxx
.param vto_n_global_typ=xxxx
.param gamma_n_global_typ=xxxx
.param delta_beta  = agauss(0,sigma_beta,1)
```

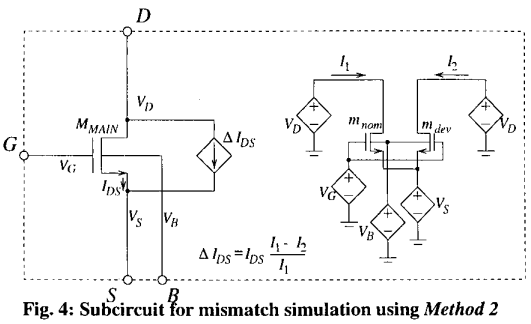

Fig. 4: Subcircuit for mismatch simulation using *Method 2*

```
.param delta_vto   = agauss(0,sigma_vto,1)
.param delta_gamma = agauss(0,sigma_gamma,1)
.param beta_n = 'beta_n_global_typ*(1+delta_beta)'
.param vto_n   = 'vto_n_global_typ+delta_vto'
.param gamma_n = 'gamma_n_global_typ+delta_gamma'
.ends
```

Using this procedure the differential pairs input offset voltages described in the previous section were simulated for all transistor sizes, with and without substrate effect. The results are given in Table 1 under the columns named "SIMULATED (method1)".

B.Method 2:

The previous method has two problems:

- The MOS transistor model provided by the manufacturer might not include some of the large signal parameters we have used, like β, V_{T0}, θ or γ.
- The physical meaning of parameters β, V_{T0}, θ or γ in the MOS model provided by the manufacturer (if they are present) is probably different to the one in the model we have assumed (eqs. (5)-(6)). Therefore, *Method* 1 is only an approximate procedure for predicting transistor mismatch, and the success of this method depends on how much the transistor model provided by the manufacturer differs from the one we have assumed.

A possible alternative to overcome these problems would be to substitute each transistor in the netlist by the subcircuit depicted in Fig. 4. The subcircuit includes 3 MOS transistors and a set of controlled sources. Transistor M_{MAIN} is a nominal transistor (without deviations) using the model provided by the manufacturer. Transistors m_{nom} and m_{dev} are modeled using the transistor model we have assumed (eqs. (5)-(6)). Transistor m_{nom} is a nominal transistor and transistor m_{dev} is such that its β, V_{T0}, θ and γ values are modified by adding random deviations. The voltage controlled voltage sources that bias transistors m_{nom} and m_{dev} do the function of copying the terminal voltages present at transistor M_{MAIN}. The currents flowing through each transistor are sensed: I_{DS} for M_{MAIN}, I_1 for m_{nom}, and I_2 for m_{dev}. Transistor M_{MAIN} has a current source in parallel ΔI_{DS} whose value at each instant is given by

$$\Delta I_{DS} = I_{DS} \frac{I_1 - I_2}{I_1}. \tag{21}$$

Note that now we can use our five *mismatch parameter* $\{\Delta\beta/\beta, \Delta V_{T0}, \Delta\theta_o, \Delta\theta_e, \Delta\gamma\}$ model[1] to define the *large signal parameters* for m_{dev}. The goal is to be able to generate for each m_{dev} these 5 *mismatch parameters* by knowing their standard deviations and respective correlation coefficients. This can be done in (H)Spice as follows. Suppose that for each m_{dev} transistor we know its *statistical mismatch parameters*. Suppose also, that for each m_{dev} we can generate 5 random numbers $\{x_1, x_2, x_3, x_4, x_5\}$ which are uncorrelated, have zero mean, and their standard deviation is $\sigma(x_i) = 1/\sqrt{2}$. Using these five uncorrelated random numbers we can obtain five correlated mismatch parameters for m_{dev} as follows,

$$\begin{aligned}
\Delta\beta/\beta &= c_{11}x_1 \\
\Delta V_{T0} &= c_{21}x_1 + c_{22}x_2 \\
\Delta\theta_o &= c_{31}x_1 + c_{32}x_2 + c_{33}x_3 \\
\Delta\theta_e &= c_{41}x_1 + c_{42}x_2 + c_{43}x_3 + c_{44}x_4 \\
\Delta\gamma &= c_{51}x_1 + c_{52}x_2 + c_{53}x_3 + c_{54}x_4 + c_{55}x_5
\end{aligned} \tag{22}$$

Where coefficients c_{ij} can be obtained by computing the standard deviations of the right and left hand side of eq. (22) [2]. The advantage of this method is that there is complete independence between the simulator model parameters that define the current through transistor M_{MAIN} and our model parameters (appearing in equations (5)-(6) and that we extract experimentally for each technology) that define the currents through transistors m_{nom} and m_{dev}. The effect of the additional transistors m_{nom} and m_{dev} is just to add a deviation ΔI_{DS} in the current passing through the basic transistor M_{MAIN} that depends on the operating point and the transistor geometry.

Using this set-up, and performing Monte Carlo simulations to predict the differential pair input offset voltages for each transistor size, with and without substrate effect, results in the values shown in Table 1 under the columns named "SIMULATED (method2)". Note that these values are more similar to those shown in Table 1 under columns named "COMPUTED" than the ones obtained with the first method of simulation. However, the values under "SIMULATED (method2)" and "COMPUTED" are not identical. The reason is that the coefficient I_{DS}/g_m of eq. (19) is computed by the simulator using the manufacturer transistor model (through transistor M_{MAIN}), instead of the one we have assumed (i.e., eqs. (5)-(6)).

IV. Conclusions

We have designed a new five parameters mismatch model and a method to extract and statistically characterize the mismatch parameters of a given technology. We have developed three different tests in order to validate our mismatch model and measurement/extraction procedure. The first test, previously reported in literature, assures that the measurement and mathematical computations have been done with good precision. The two other designed tests verify the correctness of the mismatch model itself. In these tests, we have achieved an agreement with the experimental results that can not be obtained with the other mismatch models previously reported in literature. Finally, we have proposed two different methods to use our mismatch model as a design tool in a conventional electrical simulator. We have simulated the offset voltage of a differential pair with our two methods and compared it versus the experimentally measured one. A very good agreement between simulations and measurements have been obtained.

V. References

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