

# A CONTINUOUS-TIME CELLULAR NEURAL NETWORK CHIP FOR DIRECTION-SELECTABLE CONNECTED COMPONENT DETECTION WITH OPTICAL IMAGE ACQUISITION

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**Abstract:** This paper presents a continuous-time Cellular Neural Network (CNN) chip [1] for the application of Connected Component Detection (CCDet) [2]. Projection direction can be selected among four different possibilities. Every cell (or pixel) in the 32 x 32 array includes a photosensor circuitry and an automatic tuning circuitry to adapt to average environmental illumination. Electrical image uploading is possible as well. Input pixel-values are stored on local memories (one per cell), allowing sequential processing of the acquired image in different directions.

The prototype has been designed and fabricated on a standard digital CMOS technology: 1.6 $\mu\text{m}$ , n-well, single-poly, double-metal. Circuit implementation is based on current-mode techniques and uses a systematic approach valid for any CNN application [3]. Cell dimensions, including the CNN processing circuitry, the photosensor and the adaptive circuitry are 145 x 150  $\mu\text{m}^2$ , of which the sensor and adaptive circuitry amounts to ~15% of the total pixel area and the wiring and multiplexing (required for direction selectability) to about 40%. The remaining 45% corresponds to the CNN processing circuitry. Pixel density is ~46 cells/ $\text{mm}^2$ , and power dissipation is 0.33mW/cell. These area and power figures forecast single-die CMOS chips with 100 x 100 complexity and about 3W power consumption.

## I. INTRODUCTION

In image-processing systems, the incorporation of preprocessing circuitry at the sensory plane enables the reduction of the amount of output data from the sensor array, and hence, increases the throughput rate in those applications limited by data-transmission rate. In particular, *smart-pixel* chips incorporate an analog computing cell at each sensory point, achieving high speed and low area occupation in the combined sensing/processing functions by exploiting *parallelism*. Fig.1 illustrates the architecture of these chips: each unit (smart-pixel) *senses* a point of the input image and *interacts* with other units in the neighborhood to perform parallel-processing tasks on the input image. In this manner, the transmission path between the sensing and preprocessing areas is eliminated, and in those applications requiring a subsequent high-level processing, the amount of data transmitted to the external processor is significantly reduced.

Smart-pixel chips are of strong practical interest in pattern recognition problems, where features detection in the input image are crucial. For instance, Fig.2 illustrates the task of connected component detection [2] (CCDet), which consists of counting the number of connected pieces encountered by scanning an input image in a given direction. Pattern recognition can be realized by processing the data obtained after performing this task in the directions shown in Fig.2, which involves only a few rows and columns at the image borders [4]. In addition to their usage in preprocessing tasks, smart-pixel chips are also useful as stand-alone units for non-intensive computation applications such as halftoning, motion detection, range-finding, etc.

The paradigm of Cellular Neural Networks (CNN) [1] is a very suitable framework for the *systematic* design of smart-pixel chips. On one hand, CNNs consist of regular arrangements of cells -- topologically identical to a sensor array. On the other, their cells are only locally connected, and thus, require simple routing. Also, the vast body of literature on CNN theory and applications demonstrates outstanding features of this paradigm for array-processing [5]. In particular, resistive grids have recently been demonstrated as a particular CNN class [6].

The chip reported in this paper uses a modified CNN model [7], [3] which results in improved speed/power and area figures as compared to previous CNN implementations [8], [9].

## II. THE CNN PARALLEL PROCESSING PARADIGM

CNN chips transform an input image  $[i_c]$  into an output matrix array  $[y_c]$  via a *dynamic* process of interactions among the computing cells associated to the pixels. The distinctive feature of the CNN paradigm is that these interactions are *local*, limited for each cell to a reduced set of neighbors located within a distance  $r$  in the grid. In particular, there is a wide catalog of image processing tasks available for networks where parameter  $r$  (called *neighborhood radius*) is unity -- very appealing for VLSI implementations because connection among units is made by abutment, requiring no extra routing.

Processing is governed by a set of nonlinear differential equations, one per cell. In particular, we use equations that differ from that originally proposed by Chua-Yang [1], which result in improved speed/power ratio and area occupation in VLSI implementations. The proposed cell equation is given by [7], [3],

$$\tau \frac{dx_c}{dt} = -g[x_c(t)] + D_c + \sum_{d \in N_r(c)} \{A_{cd}y_d(t) + B_{cd}u_d\} \quad (1)$$

and involves two nonlinearities, graphically shown in Fig.3. Summations in (1) extend over the *neighborhood* of the  $c$ -th cell, denoted by  $N_r(c)$ , which contains every cell  $d$  located within a distance  $r$  in the grid, and includes cell  $c$  itself.

Processing tasks performed by CNNs are determined by the *convergence* of (1) to binary equilibrium states following the transient initialized by  $[x_c(0)]$ , driven by  $[u_c]$  and under the boundary conditions imposed by cells at the net border. The outcome of the task depends on parameters  $B_{cd}$ ,  $A_{cd}$ , and  $D_c$  of (1), called *control*, *feedback*, and *offset* parameters, respectively. For uniform networks, the control and feedback parameters can be arranged into matrices which are invariant throughout the grid domain -- they are *templates*. Templates for many different processing tasks can be found elsewhere [5].

## III. PROCESSING CIRCUITRY

### A. Basic Circuit Building Blocks

Fig.4 is a block diagram for the processing circuitry of the  $c$ -th unit in a smart-pixel-CNN chip, according to (1). This figure shows a core integrator with nonlinear losses which is driven by weighted replicas of the input and output signals of the cells in the neighborhood  $N_r(c)$ , plus an offset term. In addition to this core integrator, Fig.4 includes an output structure to generate weighted replicas of the  $c$ -th input  $u_c$  and output  $y_c$ , for transmission to the neighboring units. In the mathematical model used in this prototype, the slope of the outer pieces of Fig.3(b) is close to  $\infty$ . It can be shown [7] that, under this assumption, the nonlinear dissipative term forces the state variable  $x_c$  to remain within the interval  $[-1, 1]$ ; consequently, this state variable can also be used as output variable  $y_c$ , avoiding the hardware implementation of the nonlinearity depicted in Fig.3(a).

Fig.5(a) illustrates the core integrator realization. The parallel combination of the diode-connected input transistor,  $M_1$ , and capacitor  $C$  yields a time constant  $\tau = g_m/C$ , where  $g_m$  is the transconductance parameter of  $M_1$ . On the other hand, note that current  $x_c$  cannot swing beyond the values of the current sources which drive the common output node of transistors  $M_2$  and  $M_3$  -- meaning that  $|x_c| < I_Q$ . A more detailed analysis of this circuit results in,

$$\tau \frac{dx_c}{dt} = J_c - I_Q g\left(\frac{x_c}{I_Q}\right) \quad (2)$$

as required to realize (1). In practice  $\tau$  does not remain constant, but varies with the input current level. However, most processing tasks tolerate this variation with no degradation of the network functionality [7].

Fig.5(b) shows a circuit to realize the output structure of Fig.4 from voltage level  $V_R$  in Fig.5(a), and using the basic current mirror principle of weighted replication [10]. Note that Fig.5(b) contains two different substructures to cover each possible sign of the weight  $A_{cd}$ . Positive weights are obtained using an output transistor whose geometry factor is  $A_{cd}$  times that of transistor  $M_1$ . In this form, a current  $A_{cd}x_c$  is sourced to the output node. Negative weights require an additional current mirror with unity weight for sign inversion.

## B. Some Circuit Design Issues

For area efficiency, transistor dimensions must be as small as possible. However, small-size transistors result in a number of disadvantages which must be carefully evaluated in the design process.

A major error source is the finite  $R_o/R_{in}$  ratio of the mirrors, which causes current-gain error due to spurious current division. Improved  $R_o/R_{in}$  figures can be obtained, with short channel devices, using cascode mirrors, regulated mirrors, or a combination of both [10]. In particular, analysis shows that cascode mirrors result in  $R_o/R_{in}$  values which are several orders of magnitude above that obtained from single mirrors, with smaller area occupation. The CNN prototype reported in this paper uses cascode mirrors sized to handle the whole input current range with minimum distortion and smallest possible devices. The required transistor dimensions, the static gain error due to finite  $R_o/R_{in}$ , and the power dissipation increase with the unitary bias current  $I_Q$  (see equation (2) and Fig.5). Hence, a bias current as small as possible must be chosen. A lower limit is certainly established by leakage-currents (in the range or below a few pA). However, a more restrictive bound exists due to MOS transistor mismatch and Early voltage ( $V_A$ ) degradation with channel length.

Mismatch is produced mainly by variations of  $V_T$  and  $\beta = \mu C_{ox} W/L$ , whose standard deviations  $\sigma(V_T)$  and  $\sigma(\beta)/\beta$  for devices with equal layout show a component which is inversely proportional to the square root of the channel area, and another which is proportional to the distance between devices [11]. However, the distance-dependent component can be neglected (assuming typical distances) for devices with channel area of less than about  $100\mu\text{m}^2$  [11] -- larger than the values used in this prototype. Another important consideration is that for a given  $\sigma(V_T)$  and  $\sigma(\beta)/\beta$ , the ratio  $\sigma(I)/I$  in MOS transistors is inversely proportional to  $v_{gs} - V_T$ . This means that, for some given geometries, bias current can not be decreased too far, since this would produce a low  $v_{gs}$  voltage at the bias point, with the corresponding large  $\sigma(I)/I$ . Hence, mismatch considerations establish bounds for both minimum area and power trends.

## IV. SENSORY CIRCUITRY

### A. Photosensors

The simplest CMOS n-well photosensitive devices are reverse-biased *photodiodes*, formed either directly between  $n_+$ -diffusion and substrate [12] or between well and substrate [13]. The light-induced current in either device is an increasing function of the junction area. This current level increases significantly using a vertical CMOS-BJT as photosensor. Fig.6(a) shows a conceptual layout and cross-section for this device, whose current is approximately proportional to the area of the well-substrate junction  $A_w$ . Current generated by this device is  $\beta+1$  times larger than for a photodiode of the same well area,

$$I_T \sim (\beta + 1)I_W \propto A_w \quad (3)$$

where  $I_T$  denotes the phototransistor current,  $I_W$  is the corresponding current for the well-diode, and  $\beta$  is the transistor current-gain -- around 40 in the technology used, and basically independent of transistor geometry [14].

For some critical tasks [5] currents provided by minimum size photosensors may not be large enough to guarantee the matching level required by the signal processing circuitry. Simplest amplification strategies use either larger wells or cascaded current amplifiers -- very costly in terms of area occupation and, for the latter, inaccurate. Instead, our prototype uses an additional vertical BJT device in a Darlington configuration, achieving an amplification factor of  $\beta+1$ , with practically no area overhead. Fig.6(b) shows the conceptual layout and cross-section for this Darlington phototransistor. Current for this device is,

$$I_D \sim (\beta + 1)I_T \sim (\beta + 1)^2 I_W \quad (4)$$

while its area occupation is scarcely increased by that of a minimum-size vertical BJT.

Fig.7 further illustrates the operation of the Darlington phototransistor. Both characteristics have been measured from a device with a sensitive area  $A_w = 60 \times 60\mu\text{m}^2$ . Fig.7(a) shows the *output* characteristic measured under constant environmental illumination (bright-current), while Fig.7(b) illustrates the effect of a gradual reduction of illumination to complete darkness. Dark-current is  $215 \pm 10\text{pA}$ , which means that the bright-to-dark current-ratio is close to 100dB for environmental laboratory illumination. The same ratio is observed from phototransistors, while

photodiodes yield about 80dB. Although these results are optimistic in the sense that in real images there will be no completely dark areas, the bright-to-dark current-ratios measured provide a wide enough range for data acquisition.

In the prototype described in this paper, the photo-sensitive area in each cell was reduced to that of a minimum-size well region ( $13.6 \times 13.6 \mu\text{m}^2$ ), resulting in a bright-current level of about  $1.5 \mu\text{A}$ .

### B. Auto-zero Strategy

Photosensors produce unidirectional current flow. However, double-rail signals are easily obtained by bias-shifting, as shown in Fig.8. The current  $I_{TH}$  through transistor  $M_{TH}$  sets the zero-level of the double-rail signal, which must be set somewhere between the maximum and the minimum light-induced currents among all photosensors to guarantee good contrast. If the illumination conditions of all possible input scenes were known a priori,  $I_{TH}$  could be set to a fixed value. However, in a more general case, the chip must be able to handle scenes with different lighting conditions, and hence, some kind of auto-zero strategy must be devised to automatically set  $I_{TH}$  to the average of the photosensor currents over the whole array. Fig.8 illustrates the schematic of a sensor and the auto-zero circuitry used for this purpose. The low-impedance node labelled SUM is a global node, common to all pixels. Note that the current  $I_c$  at the  $c$ -th photosensor is replicated twice. One of the replicas interfaces the processing circuitry, while the other is aggregated, through the global-node SUM, to the remaining sensor currents. A detailed calculation of the current through the transistor  $M_{TH}$  results in the following,

$$I_{TH} = \frac{Ng_{mn}}{Ng_{op} + Ng_{mn}} \frac{1}{N} \sum_{c \in GD} I_c \quad (5)$$

where  $g_{op}$  is the output conductance of the p-channel transistor,  $g_{mn}$  is the transconductance of the n-channel transistor, and  $N$  the number of pixels. Assuming  $g_{mn} \gg g_{op}$ , (5) gives  $I_{TH}$  equal to the average of the photosensor currents, and the light-threshold is automatically adjusted to the average illumination. Note that the number of cells in the network does not affect the accuracy of the adaptation circuitry.

## V. PROTOTYPE DESCRIPTION AND RESULTS

The prototype reported in this paper is a continuous time, full-signal-range model [3], CNN system, designed for connected component detection of binary images. The system contains 1024 identical cells, arranged on a square grid with 32 rows and 32 columns. This array constitutes the nucleus of the system, which can be initialized either in electrical or optical form. The direction in which the CCD operation is performed can be externally selected among four different choices. Fig.2 illustrates the four directions implemented. Opposite directions are not required, since the results of the CCD operation would be symmetrical. Every cell incorporates a one-bit memory, which allows the input image to be stored in binary form. In this manner, the same optically- or electrically-acquired image can be processed in each of the four directions, and the results downloaded, without need for repeated image acquisition (optically), or uploading (electrically). The functionality of this prototype responds to operations performed in character recognition applications [15], [16], [17], [18], [19], [20]. The electrical *input* and *output* procedures are performed on a row by row schedule, at a clock frequency of 10MHz. Input and output processes share the same bidirectional bus, and only 32 bonding pads are required for the two tasks.

Cell circuitry, illustrated in Fig.9, follows the general implementation technique described previously. Saturation current level is  $I_Q = 5\mu\text{A}$ , and current mirror and sources has been designed to optimize robustness against mismatch. Transistors sizes are  $W = 4.8\mu\text{m}$  and  $L = 4.8\mu\text{m}$  for mismatch relevant transistors, and  $W = 4.8\mu\text{m}$  and  $L = 3.2\mu\text{m}$  for “cascode” transistors.

Every cell includes, in addition to the processing circuitry, a photosensor and automatic threshold-adjustment circuitry for optical initialization. As mentioned earlier, a one-bit memory is also included in every cell. Either input-procedure results in storing the input image in the image-memory compound of the individual pixel-memories at each cell. After the image has been loaded in this memory, it can be processed in any of the four directions, and the result downloaded, any number of times. Finally, a substantial amount of the cell area (40%) is dedicated to neighbors interconnections, which in this case must be provided for the nine neighbors of every cell, and for signal multiplexing, required to perform the CCD task in the particular direction selected.

In addition to the central cell array, the system contains a number of array-periphery circuitry used for biasing, control, and input and output procedures. Fig.10 shows the layout of the prototype and an expanded cell view. Table 1 contains miscellaneous figures regarding the area consumption, power dissipation and speed of the prototype. The total number of bonding pads is 49, although only 44 external pins are strictly required. The functionality of these pads is described in Table 2.

CHARACTERISTIC	VALUE
Cell dimensions	143.6 $\mu\text{m}$ $\times$ 151.6 $\mu\text{m}$
Cell array dimensions	4598.4 $\mu\text{m}$ $\times$ 4894.8 $\mu\text{m}$
System dimensions	4797.6 $\mu\text{m}$ $\times$ 5140.4 $\mu\text{m}$
Total chip dimensions	5021.6 $\mu\text{m}$ $\times$ 5799.2 $\mu\text{m}$
Cell dissipation	330 $\mu\text{W}$ <sup>a</sup>
Cell array dissipation	338mW
System dissipation	380mW
Maximum master-clock frequency	10MHz
Image processing time	8 $\mu\text{s}$
Total processing time per image	11.2 $\mu\text{s}$ or 14.4 $\mu\text{s}$ <sup>b</sup>

**Table 1: Miscellaneous characteristics of the prototype.**

- a. Power dissipation depends on illumination, since this changes the light-induced currents. This values correspond to laboratory illumination. An increase of about 30% can result under strong illumination conditions.
- b. Optical and electrical input mode, respectively. The time required for a complete electrical up-loading or down-loading of one image is 3.2 $\mu\text{s}$ .

The chip has been tested with a number of different input images, of which Fig.2 is an example, using an automatic digital testing equipment and an optical device for image projection over the surface of the chip. The experimental setup is illustrated in Fig. 11. System behavior was the expected one in every case. The threshold adjustment circuitry in the optical interface behaved as expected as well.

## VI. CONCLUSIONS

As compared to previous CNN implementations, this prototype makes the required synergy between sensing and processing, and significantly improves area and speed/power figures. In particular, when compared to previous chips for the same application [8], [9], this prototype, apart from including sensors at the cells with the adaptation circuitry and direction programmability, reduces the area consumption by a factor of two, and the speed/power figure by more than one order of magnitude.

## VII. REFERENCES

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Name	Pad count	Type	Description
VDDA	1	POWER	Analog power supply. Nominally 5 volts.
GNDA	1	GROUND	Analog ground connection.
VPBL	1	BIAS	Unitary bias current control. Internally connected to ground through a resistor, which yields $I_Q = 5\mu\text{A}$ . Can be used to increase or decrease $I_Q$ .
VCP	1	BIAS	Internally generated reference voltage.
VCN	1	BIAS	Internally generated reference voltage.
VDDD	1	BIAS	Digital power supply. Nominally 5 volts. Can be shorted with VDDA.
GNDD	1	GROUND	Digital ground connection. Can be shorted with GNDA
FOT	1	IN	Input-mode control signal. Must be permanently high for optical-input operation, and low for electrical-input.
WRT	1	IN	Enables internal memory writing. Used for optical image acquisition and for electrical image uploading. It also configures the I/O lines IO[0-31] either as input or output bus.
LOAD	1	IN	Used to initialize every CNN cell with the content of its local cell memory.
S[0-1]	2	IN	Control the direction of the CCD operation. Each of the four possibilities corresponds to one direction.
B[4-0]	5	IN	Row selection control. Used to connect the I/O lines to the cells of a particular row.
IO[0-31]	32	IN/OUT	Input/output bus. During electrical initialization, the memories of the cells in the row selected by B[4-0] is written with the content of this bus. During output image downloading, the bus is connected to the output of the cells in the selected row. Its configuration as input or output bus is controlled by signal WRT.

**Table 2: Pinage description.**

- crete-Time Cellular Neural Networks". *IEEE Trans. Circuits and Systems*, Vol. 40, pp. 132-146, 1993.
- [4] H. Suzuki et al.: "A CNN Handwritten Character Recognition". *Int. Journal of Circuit Theory and Applications*, Vol. 20, pp. 601-612, 1992.
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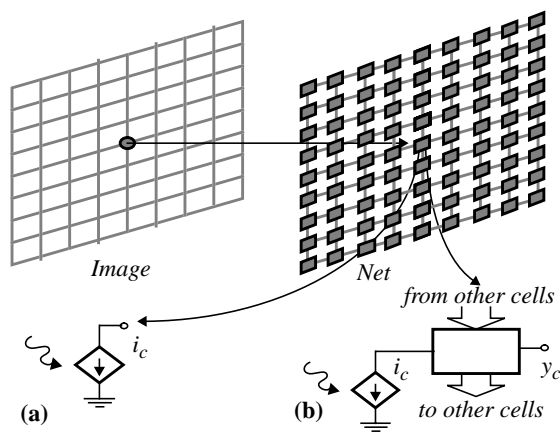


Fig.1: Illustrating the Architecture of Smart Pixel Chips: (a) Sensory-Only Units; (b) Concurrent Sensory + Processing Units (smart-pixel).

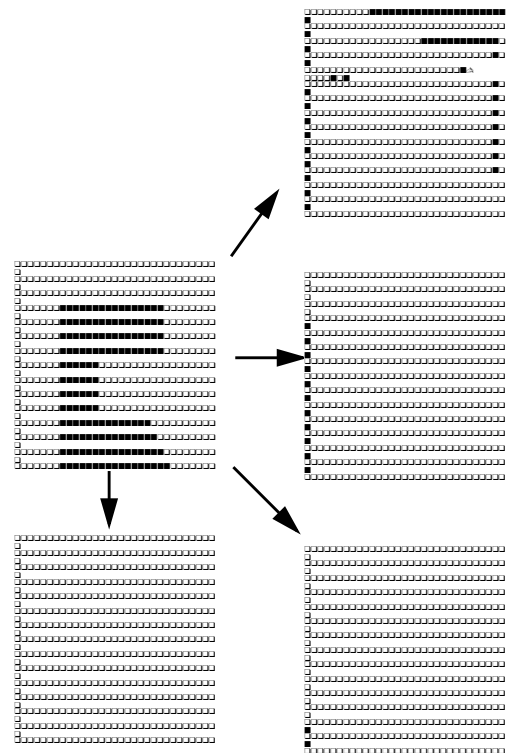


Fig.2: Connected Component Detection Four Different Directions.

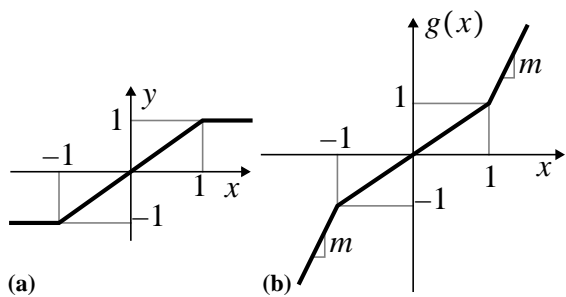


Fig.3: CNN Cell Nonlinearities (a) Output Nonlinearity; (b) Dissipative Term.

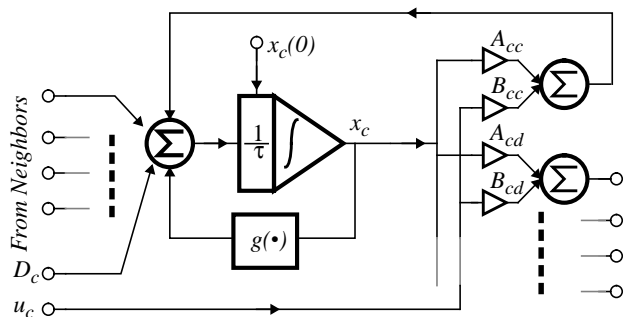


Fig.4: Conceptual Block Diagram for the Processing Circuitry of a CNN Smart pixel.

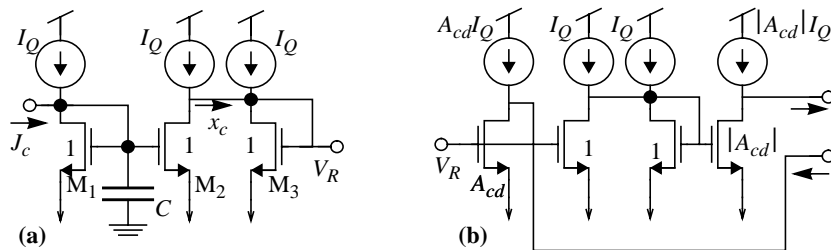


Fig.5: Current-Mode Circuit Blocks for the Processing Circuitry of CNN Smart Pixels: (a) Core Integrator; (b) Output Structure.

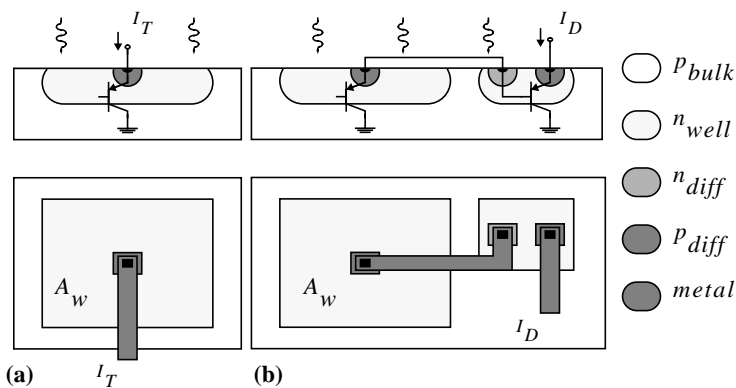
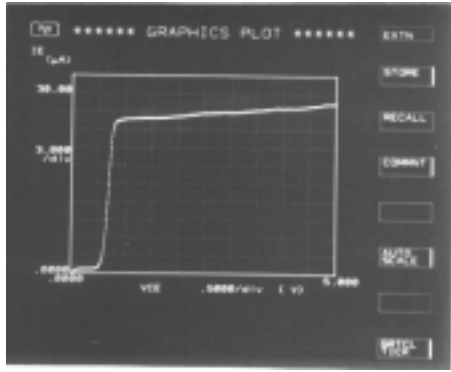
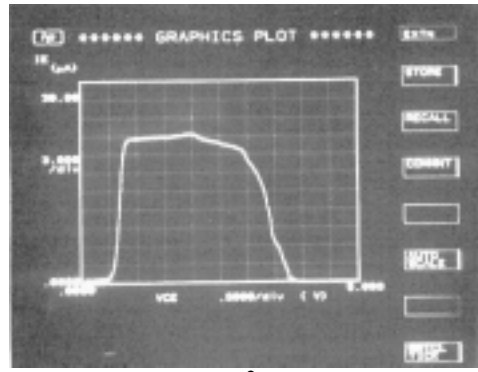


Fig.6: (a) CMOS compatible vertical p-n-p transistor. (b) Darlington configuration of two vertical p-n-p transistors.





(a)



(b)

Fig.7: Measured Output Characteristics of a Phototransistor with  $A_W = 60 \times 60 \mu\text{m}^2$ : (a) Under Constant Environment Illumination; (b) For Gradual Reduction of Illumination.

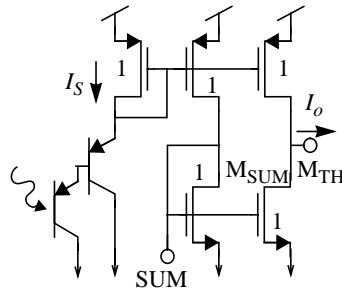


Fig.8: Sensor with auto-Zero Circuitry.

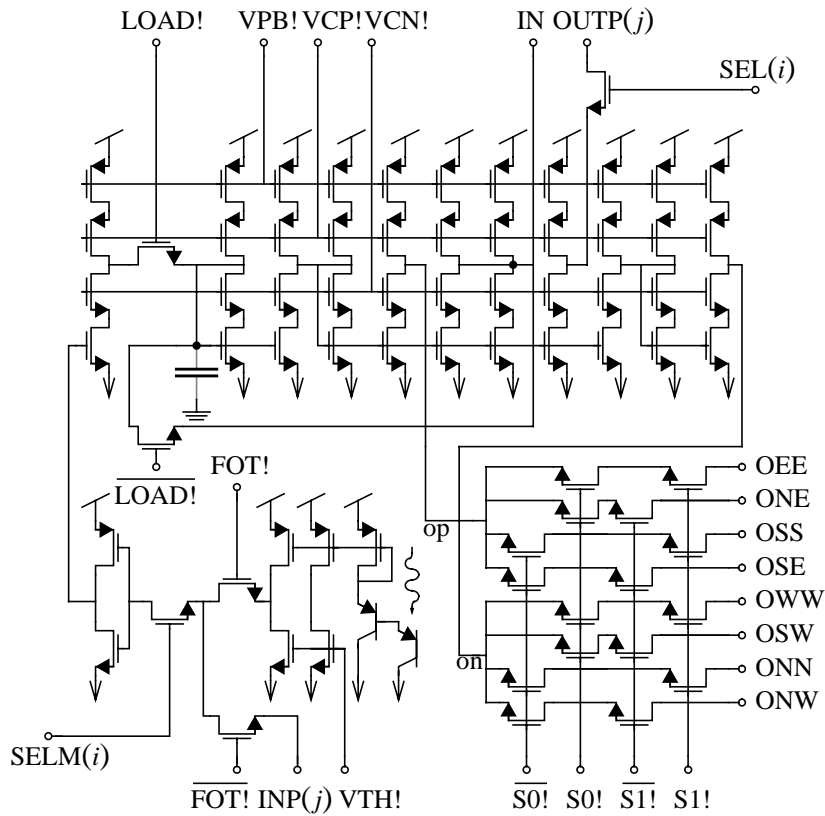


Fig.9: Cell schematic of the prototype (refer to text for dimensions).

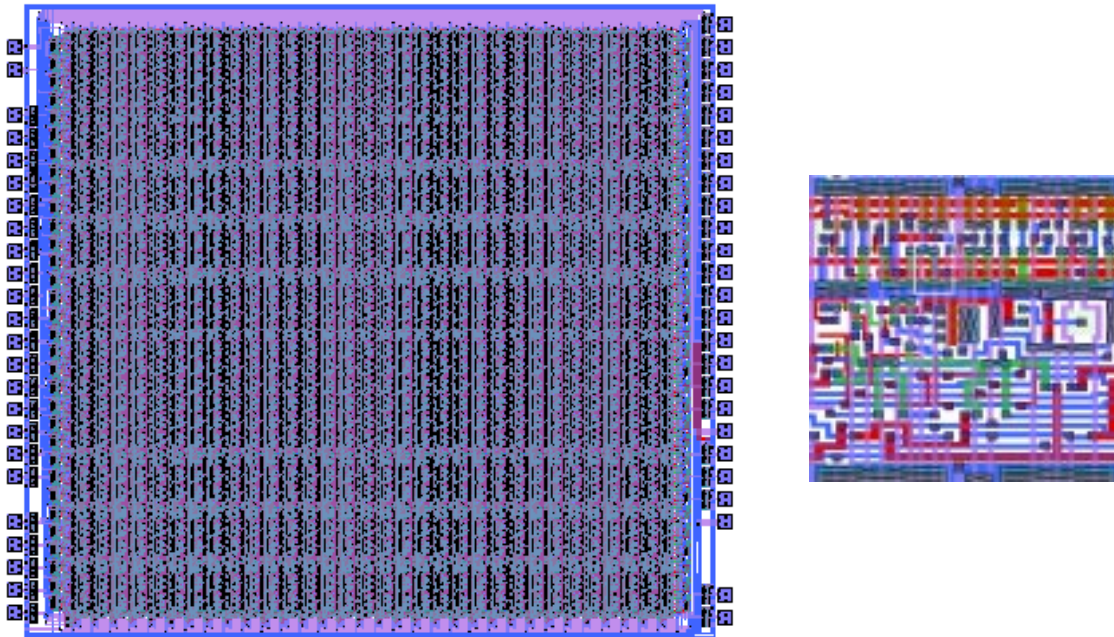


Fig.10: Complete layout of the prototype and expanded cell view.

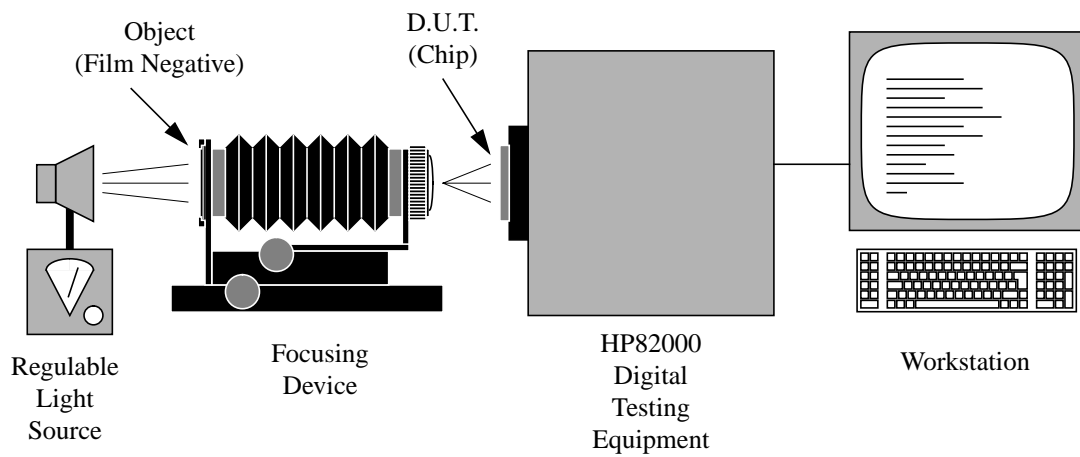


Fig.11: Testing scheme for the optical interface of the prototype.