The EKV/ACM compact models for mismatch modeling down to 90nm and for new emergent non-CMOS nanotechnology FETs

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Outline

- Continuous Weak-to-Strong inversion models for mismatch
- Mismatch characterization chip
- Results for 0.35um CMOS
- Results for 90nm CMOS
- Simulating in Cadence-Spectre
- Modelling Pelgrom’s Distance Term Efficiently
- Extension of continuous CMOS models to new coming nano-FETs
The Mismatch Behavior

- Small random, transistor size dependent component, ‘true’ mismatch component
- Gradient surface, transistor distance dependent component, can be eliminated with layout techniques

\[ \sigma^2 (\Delta P) = f_A(W, L) + f_D(D) \]
Historical Perspective. Mismatch Models in Strong Inversion

\[ \sigma^2(\Delta P) = f(W, L) + S_P^2 D^2 \]

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<th>(\sigma^2(\Delta V_{T0}))</th>
<th>(\sigma^2(\Delta \theta))</th>
<th>(\sigma^2(\Delta \theta_o))</th>
<th>(\sigma^2(\Delta \theta_e))</th>
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\[ \Delta \theta = \Delta \theta_o + \frac{V_D S|_{sat}}{V_{GS} - V_T} \Delta \theta_e \]

\[ \theta_o = \theta + 2 \frac{\mu C_{ox} l d R}{L} \]

\[ \theta_e = \frac{\mu}{L} \left( \frac{1}{2 v_s} - C_{ox} l d R \right) \]
A Continuous Transistor Model from Weak to Strong Inversion. The ACM Model

\[ I_{DS} = I_s (i_f (V_P - V_S) - i_r (V_P - V_D)) \]

\[ V_P - V_{S(D)} = \phi_i \left( \sqrt{1 + i_f(r)} - 2 + \ln(\sqrt{1 + i_f(r)} - 1) \right) \]

\[ V_P = \frac{V_G - V_{TO}}{n} \]

\[ n = 1 + \frac{\gamma}{2\left(\sqrt{V_G - V_{TO}} + 2\phi_F + \gamma \sqrt{2\phi_F + 1/4\gamma} - 1/2\gamma\right)} \]

\[ I_S = I_s' n = \mu n C_{ox} (W/L) \left(\frac{\phi_t}{2}\right) \]

- Continuous for all transistor operation regions
- Based on a reduced set of physically meaningful parameters \{\[ I_s, V_{TO}, \gamma, \phi_F \}\}
- Drain/Source symmetric
Introducing Continuously Second Order Effects

\[ I_{DS} = \frac{I_S(i_f - i_r)(1 + \lambda(V_D - V_S))}{(1 + \theta_o[V_P - V_S]^+)(1 + \theta_e V_{DS_{eff}})} \]

traditionally,
\[ V_{DS_{eff}} = V_{DS} \quad \text{in ohmic region;} \]
\[ V_{DS_{eff}} = V_P - V_S \quad \text{in saturation.} \]

define smoothed rectification \([\ ]^+\)

\[ [x]^+ = \begin{cases} 
0 & \text{if } x < -E \\
\frac{(x + E)^2}{4E} & \text{if } -E < x < E \\
x & \text{if } x > E
\end{cases} \]

redefine
\[ V_{DS_{eff}} = \left| [V_P - V_S]^+ - [V_P - V_D]^+ \right| \]
with \( E = 0.3 V_{DS} \)
A Continuous Mismatch Model Valid from Weak to Strong Inversion

\[ I_{DS} = \frac{I_S(i_f - i_r)(1 + \lambda(V_D - V_S))}{(1 + \theta_o[V_P - V_S]^+)(1 + \theta_e V_{DS_{eff}})} \]

\[ \frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta I_S}{I_S} + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_P} \frac{\partial V_P}{\partial V_{T0}} \Delta V_{T0} + \left( 1 + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \gamma} \frac{\partial \gamma}{\partial n} \right) \Delta n + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta_o} \Delta \theta_o + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \theta_e} \Delta \theta_e \]

\[ \left\{ \frac{\Delta I_S}{I_S}, \Delta V_{T0}, \Delta \gamma, \Delta \theta_o, \Delta \theta_e \right\} \]
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Mismatch Characterization Chip

DECORDER

Bus

DN  DP  S  G

W1/L1

W6/L5

W1/L2

Enable

row select
column select
Measuring Curves: 7 Measured Curves

- \( V_{DS} = 1,65V \)
  **Curve 1:** \( I_{DS}(V_{GS}) \), \( V_{SB} = 0V \), \( V_{GS} \in [0, 3,3] \)
  **Curve 2:** \( I_{DS}(V_{GS}) \), \( V_{SB} = 1V \), \( V_{GS} \in [0, 3,3] \)

- \( V_{DS} = 0,1V \)
  **Curve 3:** \( I_{DS}(V_{GS}) \), \( V_{SB} = 0V \), \( V_{GS} \in [0, 3,3] \)
  **Curve 4:** \( I_{DS}(V_{GS}) \), \( V_{SB} = 1V \), \( V_{GS} \in [0, 3,3] \)

- \( V_{G} = 1,25V_{S} + \alpha \)
  **Curve 5:** \( I_{DS}(V_{S}), \alpha = \alpha_{1}, V_{S} \in [0, 3,3] \)
  **Curve 6:** \( I_{DS}(V_{S}), \alpha = \alpha_{2}, V_{S} \in [0, 3,3] \)
  **Curve 7:** \( I_{DS}(V_{S}), \alpha = \alpha_{3}, V_{S} \in [0, 3,3] \)

where:

\( \alpha_{1}, \alpha_{2} \) and \( \alpha_{3} \) are values of \( V_{G} \) from curve 1 so that we are in weak, moderate and strong inversion respectively.
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Computing Statistics

\[ \sigma(\Delta I_S / I_S) \]

\[ \sigma(\Delta \gamma) \]

\[ \sigma(\Delta V_{T0}) \]

\[ \sigma(\Delta \theta_e) \]

\[ \sigma(\Delta \theta_o) \]
Computing Statistics

\[
\sigma(\Delta I_S/I_S) \quad 1/(\sqrt{W/L})
\]

\[
\sigma(\Delta \gamma) \quad 1/(\sqrt{W/L})
\]

\[
\sigma(\Delta V_{T0}) \quad 1/(\sqrt{W/L})
\]

\[
\sigma(\Delta \theta_e) \quad 1/(\sqrt{W/L})
\]

\[
\sigma(\Delta \theta_o) \quad 1/(\sqrt{W/L})
\]
Predicting $\sigma(\Delta I/I)$ of measured curves and errors $\frac{(\sigma(\Delta I/I))_{\text{meas}} - (\sigma(\Delta I/I))_{\text{pred}}}{(\sigma(\Delta I/I))_{\text{meas}}}$

$$
\sigma^2 \left( \frac{\Delta I_{DS}}{I_{DS}} \right) = \sigma^2 \left( \frac{1}{I_{DS}} \right) ^2 + \left( \frac{1}{I_{DS} \partial V_{TO}} \right) ^2 \sigma^2 + \left( \frac{1}{I_{DS} \partial \gamma} \right) ^2 \sigma^2 + \left( \frac{1}{I_{DS} \partial \theta_o} \right) ^2 \sigma^2 + \left( \frac{1}{I_{DS} \partial \theta_e} \right) ^2 \sigma^2 + \text{correlation}
$$

Curve 1. $V_{DS} = 1.65 V, V_S = 0 V$
Correlations

\[
\Delta \theta_o \quad \Delta \theta_e \quad \Delta \gamma \quad \Delta V_{T0}
\]

\[
\frac{\Delta I_S}{I_S} \quad \Delta V_{T0} \quad \Delta \gamma \quad \Delta \theta_e
\]

\[
\Delta \theta_e \quad \Delta \theta_o \quad \Delta \gamma \quad \Delta V_{T0}
\]

40\,\mu m

20\,\mu m

10\,\mu m

5\,\mu m

2\,\mu m

0,8\,\mu m
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Mismatch Measurements

Nominal Measured Curves

W = 0.12 μm
L = 0.1 μm

W = 12 μm
L = 10 μm

CMOS Transistors
90nm process
25 different sizes
64 devices each size

Measured Curves with Mismatch
Mismatch Measurements

![Graphs showing mismatch measurements for different widths and lengths.](image-url)
Extracted Mismatch Parameters

Standard NMOS transistors 90nm process
Measured vs. Predicted Current Mismatch
Standard NMOS transistors 90nm process

![Graphs showing measured vs. predicted current mismatch for different channel lengths and widths.](image)
Error in Current Mismatch Prediction
Standard NMOS transistors 90nm process

![Graphs showing current mismatch prediction errors for different channel lengths and widths.](image)
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Spectre Mismatch Model Implementation

- Our intention is to create a model of a MOS transistor that fits with the results of the model.
- This model has been implemented in AHDL (Analog Hardware Description Language) and can be used in Simulator Spectre.
- The model implementation is based on a current in parallel with a spectre library transistor that emulates the mismatch behaviour.
Spectre Mismatch Model Implementation

\[ I_{DS} \rightarrow \Delta I_{DS} \]

Random Number Generator \( x_1, x_2 \)

\[ \Delta - parameters \]

\[ \Delta I_{DS} \] Generator \( \Delta I, \Delta \theta \)

\[ \Delta I_{DS} \] Generator \( I_s, \theta \)

ACM Model

Standard deviations and correlations

Large signal parameters

Parameters

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Spectre Mismatch Model Implementation

Parameter box stores the 5 large signal parameters and the standard deviations and correlations of the 5 mismatch parameters.
Spectre Mismatch Model Implementation

\( \Delta \) parameters Generator box obtains the five mismatch parameters using 5 uncorrelated random numbers and data stored on Parameters box.

- Random Number Generator
- \( \Delta \) parameters Generator
- Parameters
- ACM Model
- Large signal parameters
- Standard deviations and correlations

\( I_{DS} \) \( \Delta I_{DS} \)
Spectre Mismatch Model Implementation

\[ I_{DS} \rightarrow \Delta I_{DS} \]

- Random Number Generator
- \( x_1 \) and \( x_5 \)
- \( \Delta - \text{parameters} \)
- \( \Delta I \), \( \Delta \theta \)
- Parameters
- ACM Model
- Large signal parameters
- Standard deviations and correlations

ACM Model box is used to obtain the large signal current using the 5 large signal parameters.
Spectre Mismatch Model Implementation

\[ \Delta I_{DS} \] Generator box obtains the current in parallel using the 5 large signal parameters calculated in the ACM Model box and the 5 mismatch parameters obtained in the \( \Delta \)-parameters Generator box.

Random Number Generator

\( x_1 \) \hspace{1cm} \( x_5 \)

\( \Delta \)-parameters Generator

\( \Delta I_5 \) \hspace{1cm} \( \Delta \theta \)

Parameters

\( I_2 \) \hspace{1cm} \( \theta \)

Large signal parameters

Standard deviations and correlations

ACM Model

\( \Delta I_{DS} \) Generator

\( \Delta I_{DS} \)
Spectre Mismatch Model Implementation

Comparissson between simulated and fitted data for curve 1 and all transistor sizes

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\[ \sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p D^2 \]

- Size dependent term
- Distance independent
- Size independent
- Distance dependent term

(lot of literature) (little literature)
By analyzing the mathematical derivation.

\[ \sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 D^2 \]
Gradient Component

\[ P(x, y) = Ax + By + C \]

random planes from die to die

random numbers
die average
Generate random numbers $A$ and $B$

$$P(x, y) = Ax + By + C$$
Generate random numbers $A$ and $B$

$$P(x, y) = Ax + By + C$$

Gradient-induced mismatch

$$\Delta P_{grad_{ij}} = A(x_i - x_j) + B(y_i - y_j)$$
Generate random numbers $A$ and $B$

$$P(x, y) = Ax + By + C$$

Gradient-induced mismatch

$$\Delta P_{\text{grad}_{ij}} = A(x_i - x_j) + B(y_i - y_j)$$

Statistics over many planes

$$\sigma^2(\Delta P_{\text{grad}_{ij}}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2$$
Generate random numbers $A$ and $B$

\[ P(x, y) = Ax + By + C \]

Gradient-induced mismatch

\[ \Delta P_{\text{grad}_{ij}} = A(x_i - x_j) + B(y_i - y_j) \]

Statistics over many planes

\[ \sigma^2(\Delta P_{\text{grad}_{ij}}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2 \]

no preferred directions: $\sigma(A) = \sigma(B)$

\[ \sigma^2(\Delta P_{\text{grad}_{ij}}) = \sigma^2(A)[(x_i - x_j)^2 + (y_i - y_j)^2] = \sigma^2(A)D_{ij}^2 \]
Generate random numbers $A$ and $B$

$$P(x, y) = Ax + By + C$$

Gradient-induced mismatch

$$\Delta P_{grad\_ij} = A(x_i - x_j) + B(y_i - y_j)$$

Statistics over many planes

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2$$

no preferred directions: $\sigma(A) = \sigma(B)$

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)[(x_i - x_j)^2 + (y_i - y_j)^2] = \sigma^2(A)D_{ij}^2$$

$$\sigma^2(\Delta P_{ij}) = \frac{A_P^2}{WL} + S_P^2D_{ij}^2$$

$$S_P = \sigma(A) = \sigma(B)$$
Mismatch Modelling in a CAD Tool

\[ P_i = P_{mean} + \Delta P_{global} + \Delta P_{\text{rand}_i} + \Delta P_{\text{grad}_i} \]

- **Technology Average**: (common for whole die)
- **Corner**: (common for whole die)
- **Size-dependent mismatch**: (2-10 random numbers per transistor)
- **Gradient-induced mismatch**: (2 random numbers per die) need layout coordinates
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Motivations: Why?

- New nano devices are rapidly appearing offering new functionality and memory capabilities

![NOMFET](image1.png)
![OG-CNFET](image2.png)
![ZnO-MemoryFET](image3.png)

- Parallely, new circuits and architectures should be devised exploiting new capabilities
- Models are needed to simulate architectures and circuits
- Physical modelling is a slow, complex and sophisticated process
- Fitting new devices to a compact CMOS model has the advantage that circuit simulators are available allowing quick design and simulation of new architectures
- Hybrid nano-CMOS architectures can be easily simulated
EKV Compact Model [Enz et al. 1995]

\[
\begin{align*}
I_{DS} & = \frac{I_F - I_R}{1 + \theta(V_P - \min(V_D, V_S))} + I_{off} \\
I_F & = I_{s1f}(V_P, V_S) \\
I_R & = I_{s1r}(V_P, V_D) \\
V_P & = \frac{V_G - V_{TO}}{n} \\
i_f(r) & = \left[ \ln \left( 1 + \exp \left[ \frac{V_P - V_{SD}}{2U_t} \right] \right) \right]^2
\end{align*}
\]
ACM Compact Model [Cunha et al., 1995]

Other compact models could have been used [Iñiguez et al., 1995]
NABAB Nano Devices: OG-CNFET

- OG-CNFET: Optically Gated Carbon Nanotube FET
- P-type Carbon nanotubes single/network coated with photosensitive polymers act as memory devices
- Change in conductance four orders of magnitude upon illumination
- Response to light robust and reversible
NABAB Nano Devices: NOMFET

- NOMFET: Nano Particle Organic Memory FET Transistor
- Three terminal device
- $p^+$ common gate/200nm SiO$_2$/gold source-drain electrodes/inter-electrode gap 0.2-20μm
- Au nanoparticles deposited on the inter-electrode gap before pentacene deposition
- NPs are afterwards immobilized using surface chemistry
- Pentacene (organic p-type semiconductor) deposited on top
NABAB Nano Devices: ZnO NW memory FETs

- ZnO nanowires dispersed on a SiO$_2$-coated Si substrate
- 100nm thick SiO$_2$
- Drain/source metal electrodes grown by photolithography
- Coated with layer of ferroelectric nanoparticles shifts threshold voltage positively or negatively depending on polarization
- Top gate made easy to change the orientation of polarization completely
- Long retention times
- Reversible
Fitting OG-CN Fet to the EKV model. Experimental Results

* Device $L_g=200\text{nm}$, $t_{ox}=2\text{nm}$, single tube:

\[ I_S=0.4\text{nA} \quad n=1.22 \quad V_{TO}=0.7895\text{V} \quad \theta=1.7530\text{V}^{-1} \quad I_{off}=8.7\text{pA} \]

\[ \blacklozenge \text{ Device } L_g=8000\text{nm}, \ t_{ox}=10\text{nm}, \text{ network of nanotubes:} \]

\[ I_S=17.0\text{nA} \quad n=7.78 \quad V_{TO}=0.5396\text{V} \quad \theta=2.2085\text{V}^{-1} \quad I_{off}=6.6\text{pA} \]

\[ \times \text{ Device } L_g=8000\text{nm}, \ t_{ox}=20\text{nm}, \text{ network of nanotubes:} \]

\[ I_S=28.6\text{nA} \quad n=11.82 \quad V_{TO}=1.1904\text{V} \quad \theta=1.6013\text{V}^{-1} \quad I_{off}=2.5\text{pA} \]
Fitting OG-CN Fet to the EKV model. Experimental Results

$V_{ds} = -0.4 \, \text{V}$

![Graph showing experimental results](image-url)
Fitting NOMFET to the EKV model. Experimental Results

Same device

Different programming conditions.

Writing

\[ V_{GS} = -50 \text{V} \text{ for 30 seconds} \]

Erasing

\[ V_{GS} = 50 \text{V} \text{ for 30 seconds} \]

* Device \( W=1000 \mu m, L=1 \mu m, t_{ox}=200 \text{nm} \), initial:

\[ I_S = 58.6 \mu A \quad n = 177 \quad V_{TO} = -44.95 \text{V} \quad \theta = 0 \text{V}^{-1} \quad I_{off} = 1.7 \mu A \]

\( \times \) Device \( W=1000 \mu m, L=1 \mu m, t_{ox}=200 \text{nm} \), after writing:

\[ I_S = 65.4 \mu A \quad n = 199 \quad V_{TO} = -48.74 \text{V} \quad \theta = 0 \text{V}^{-1} \quad I_{off} = 0.6 \mu A \]

\( \diamond \) Device \( W=1000 \mu m, L=1 \mu m, t_{ox}=200 \text{nm} \), after erasing:

\[ I_S = 6.7 \mu A \quad n = 140 \quad V_{TO} = -28.44 \text{V} \quad \theta = 0 \text{V}^{-1} \quad I_{off} = 0.6 \mu A \]
Fitting ZnO Memory FET to the EKV Model. Experimental Results

\[ V_{ds} = 0.1 \text{ V} \]

\begin{align*}
\text{Device bottom gated ZnO nanowire, } L &= 3 \mu m, \ t_{ox} = 100nm, \ V_{GS} \text{ swept } -10V \text{ to } 15V: \\
I_S &= 0.5521nA \quad n = 1.84 \quad V_{TO} = -2.3675V \quad \theta = 0.0006V^{-1} \quad I_{off} = 0.0259pA
\end{align*}

\begin{align*}
\text{Device bottom gated ZnO nanowire, } L &= 3 \mu m, \ t_{ox} = 100nm, \ V_{GS} \text{ swept } 15V \text{ to } -10V: \\
I_S &= 6.7\mu A \quad n = 10.88 \quad V_{TO} = 1.6554V \quad \theta = 0V^{-1} \quad I_{off} = 0.1926pA
\end{align*}
Conclusions

• We have shown how to extend in a compact manner the continuous EKV/ACM model to model mismatch including 2nd order effects relevant for mismatch.

• The model has been tested on 0.35um and 90nm CMOS technologies.

• We have indicated how one can simulate the model in a conventional circuit simulator.

• We have indicated how to include Pelgrom’s Distance Term efficiently in a CAD layout-aware mismatch simulator.

• We have shown the potential of the EKV/ACM continuous model to model some of new nano-FET devices.
References


