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TESIS DOCTORAL

SUBSAMPLING RECEIVERS WITH APPLICATIONS TO SOFTWARE DEFINED RADIO SYSTEMS

José Ramón García Oya

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por

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RESUMEN DE LA TESIS

La presente Tesis Doctoral propone la utilización sistemas basados en submuestreo como una alternativa para la implementación de la etapa de *down-conversion* de los receptores de radio frecuencia empleados para aplicaciones multi-estándar y *Software Defined Radio*. Uno de los objetivos principales será el de optimizar el diseño en cuanto a flexibilidad y simplicidad, las cuales son propiedades inherentes en los sistemas basados en submuestreo. Por tanto, como reducir el número de componentes al mínimo es clave cuando un mismo receptor procesa diferentes estándares de comunicación, se han seleccionado estas arquitecturas basadas en submuestreo, para las que es posible alcanzar un alto grado de reusabilidad de los componentes. De este modo, se reducirá el coste total del receptor de comunicación, así como de los equipos de test y certificación que emplean este tipo de arquitecturas.

Un motivo adicional por el que los sistemas basados en submuestreo han sido seleccionados es el concerniente a la topología del receptor. Como el objetivo del *Software Defined Radio* es implementar todas las funcionalidades del receptor (filtrado, amplificación) en el dominio digital, el convertidor analógico-digital (ADC) deberá estar localizado en la cadena de recepción lo más cerca posible a la antena, siendo el objetivo final el convertir la señal directamente de RF a digital. Sin embargo, con los actuales ADCs no es posible implementar esta idea debido al alto ancho de banda que requieren, sin perder resolución, para cubrir las especificaciones de los estándares de comunicaciones inalámbricas. Por tanto, los sistemas basados en submuestreo se presentan como la opción más adecuada para implementar este tipo de receptores, debido a que pueden muestrear la señal de entrada por debajo de la tasa de Nyquist, si se cumplen ciertas restricciones en cuanto a la elección de la frecuencia de muestreo. De este modo, los requerimientos del ADC serán relajados ya que, usando las arquitecturas propuestas, dicho componente procesará la señal a frecuencias intermedias con más altas prestaciones de resolución.

Una vez se han introducido los conceptos principales del submuestreo, esta tesis doctoral presenta el diseño de una tarjeta de adquisición de datos basada en este tipo de técnicas con la finalidad de ser implementada como receptor de test y certificación multi-estándar de banda ancha. El sistema propuesto proporciona una alta resolución para un elevado ancho de banda, a partir del uso de un *sample & hold* (S&H) de bajo *jitter* y de un ADC que trabaja a frecuencias intermedias. El prototipo es implementado usando dispositivos comerciales en una placa de circuito impreso, cuya caracterización experimental muestra una resolución de

más 8 bits para un ancho de banda analógico de 20 MHz. Concretamente, la resolución medida será mayor de 9 bits hasta una frecuencia de entrada de 2.9 GHz, y mayor de 8 bits para una frecuencia de entrada de hasta 6.5 GHz, lo que resulta suficiente para cubrir los requerimientos de la mayor parte de los actuales estándares de comunicaciones inalámbricas (GPS, GSM, GPRS, UMTS, Bluetooth, Wi-Fi, WiMAX).

Sin embargo, los receptores basados en submuestreo presentan algunos importantes inconvenientes, como son adicionales fuentes de ruido (*jitter* y plegado de ruido térmico) y una dificultad añadida para implementarlo en escenarios multi-banda y no lineales. Acerca del plegado de ruido en la banda de interés, esta tesis propone el uso de una técnica basada en una arquitectura de reloj múltiple, con el objetivo de aumentar la resolución y cubrir un número mayor de estándares para su test y certificación. Empleando una frecuencia de muestreo mayor para el caso del S&H, se conseguirá reducir el efecto del plegado de ruido, aumentando la resolución en 0.5-1 bit respecto al caso de sólo usar una fuente de reloj. Las expresiones teóricas de esta mejora son desarrolladas y presentadas en esta tesis, siendo posteriormente corroboradas de modo experimental.

Por otra parte, la presente tesis también propone novedosas técnicas para la aplicación de los sistemas de submuestreo en entornos multi-banda y no lineales, los cuales presentan desafíos adicionales por el hecho de existir la posibilidad de solapamiento entre la señal de interés y los otros canales de comunicación, así como de solapamiento con sus armónicos. De este modo, se extenderá el uso de los sistemas basados en submuestreo para este tipo de entornos, proponiendo técnicas para la elección de la frecuencia óptima de muestreo que evitan el solapamiento entre señales, a la vez que consiguen incrementar la resolución del receptor. Finalmente, se presentará la optimización en cuanto a características de ruido de un receptor concreto para aplicaciones de banda dual en entornos no lineales. Dicho receptor estará basado en las técnicas de reloj múltiple presentadas anteriormente y en una estructura de multi-filtro localizada entre el S&H y el ADC. El sistema diseñado podrá emplearse para diversas aplicaciones a ambos lados de la cadena de comunicación, tal como son su utilización en receptores de detección de espectro para radio cognitiva, o implementando el bucle de realimentación de un transmisor para la linealización del amplificador.

Por tanto, la presente tesis doctoral cuenta con tres contribuciones diferenciadas. La primera de ellas es la dedicada al diseño de un prototipo de recepción multi-estándar basado en submuestreo para aplicaciones de test y certificación. La segunda aportación es la dedicada a la optimización de las especificaciones de ruido a partir de las técnicas presentadas basadas en reloj múltiple. Por último, la tercera contribución principal es la relacionada con la extensión de este tipo de técnicas a sistemas multi-banda en entornos no lineales. Todas estas contribuciones han sido estudiadas teóricamente y experimentalmente validadas.

ABSTRACT

This thesis work proposes a subsampling based system as a feasible alternative to the RF down-conversion stage in receivers for Software Defined Radio (SDR) and multi-standard applications, leading to extreme flexibility and simplicity proper of the subsampling based systems. Since reducing the number of components to a minimum is key when the same receiver has to process different standards, subsampling architectures have been selected.

In this thesis, a data acquisition module for a wideband multi-standard receiver test system is presented. Based on a subsampling architecture, the proposed system provides high resolution over a large bandwidth using only a low-jitter wideband Sample-and-Hold (S&H) and an intermediate frequency Analog-to-Digital Converter (ADC). The system was implemented with commercial devices on a multilayer printed circuit board and experimental results show more than 8 bits resolution for a 20 MHz signal bandwidth, obtaining an Effective Number Of Bits (ENOB) larger than 9 bits up to 2.9 GHz and 8 bits up to 6.5 GHz, which are enough to cover the test system requirements for most of present wireless communication standards.

However, subsampling receivers have some significant drawbacks, as extra noise sources and an additional difficulty to implement these receivers in nonlinear and multi-band scenarios. About the thermal noise folded into the interest band, this thesis proposes a technique based on multiple clocking in order to increase the total resolution of the receiver, so that most of wireless communication standards can be covered. The theoretical expressions to estimate the expected improvement have been developed in this thesis work, and experimentally corroborated.

Besides these multi-standard applications, this thesis proposes to extend subsampling techniques to multi-band and nonlinear scenarios, which means an additional challenge about avoiding the aliasing between channels and harmonics. This thesis details some innovative techniques to avoid this overlapping effect without reducing the resolution, and presents a design and optimization of concurrent dual-band multi-standard subsampling receiver in nonlinear and interfering environments.

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LIST OF ACRONYMS

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BGA	Ball Grid Array
BoM	Bill of Materials
BP	Band Pass
BPS	Band Pass Sampling
BW	Bandwidth
CMOS	Complementary Metal-Oxide Semiconductor
COTS	Commercial Off The Shelf
CPLD	Complex Programmable Logic Device
CR	Cognitive Radio
DAC	Digital-to-Analog Converter
DDC	Digital Down Converter
DDS	Direct Digital Synthesizer
DPD	Digital Pre-Distorter
DSP	Digital Signal Processing
EMI	Electromagnetic Interference
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array

FR4	Flame Retardant 4
GP	General Purpose
IC	Integrated Circuit
IF	Intermediate Frequency
IMD3	3rd order Intermodulation Distortion
I-Q	In-phase and Quadrature
IRF	Image Rejection Filter
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Pass
LPS	Low Pass Sampling
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MOS	Metal-Oxide Semiconductor
NF	Noise Figure
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PSD	Power Signal Density
RD	Receiver Design
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SFDR	Signal Free Dynamic Range
SMA	Subminiature version A
SMD	Surface Mount Device
SNDR	Signal-to-Noise and Distortion Radio

SNR	Signal-to-Noise Ratio
S&H	Sample & Hold
THD	Total Harmonic Distortion
UWB	Ultra Wideband
VCO	Voltage Control Oscillator
VCXO	Voltage Control Crystal Oscillator
VIA	Vertical Interconnect Access
VLSI	Very-Large Scale Integration
WPAN	Wireless Personal Area Network

CHAPTER 1

INTRODUCTION

CHAPTER CONTENTS

By introducing the context which includes the research presented in this thesis work, this chapter describes the main motivations that have driven to performance the thesis. Additionally the main points of the work methodology are detailed and, finally, a thesis outline is presented to describe the structure of the document.

1.1 Motivation

Nowadays, there are a large number of different communication standards due to the widespread acceptance of wireless technologies. As a consequence, there is a tendency to design extremely flexible transceivers for multiple standards and multiple functions into a wireless device that can be used anywhere [1.1-1.8]. Therefore, it will be necessary to eliminate as many expensive external components as possible to reduce the bill of materials (BoM) and to get a high reusability level.

A similar problem arises in the test industry, where providers of testing and certification services to the wireless communication industry need multi-standard receivers in order to reduce the cost in testing equipment.

Concerning the topology of a multi-standard receiver, the place of the ADC within the front-end chain is crucial, as shifting the analog blocks (filter, mixer and amplifier) to the digital domain increases the flexibility of the receiver. The extreme case is known as the SDR paradigm [1.9,1.10], where the ADC is placed right behind the antenna to directly digitize the RF signal.

The classic SDR transceiver defined by [1.9] is illustrated by Figure 1.1. As it can be observed, this transceiver is only composed by the antenna, the circuitry dedicated to the conversion between the analog and digital domains (the ADC at the receiver and the DAC at the transmitter) and, finally, a completely digital radio.

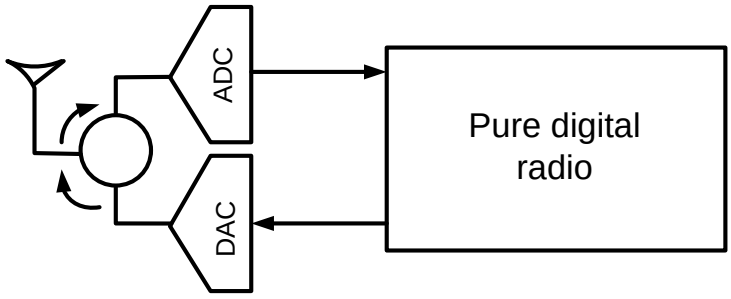

Figure 1.1 Classic SDR architecture

Recent research is focused on Cognitive Radio (CR), whose target is achieving a kind of flexible intelligence to employ in future radios, cell phones and other wireless communication devices [1.11,1.12]. This coming technology should enable any wireless system to locate and link with any locally available unused radio spectrum. This approach should supply the consumer, in presence of limited spectral resources, an increase of the number of provided services from a single handset adapted to a global roaming.

The SDR and CR objectives only can be obtained with a receiver whose front-end accommodates a wide range of frequency bands and channel

bandwidths. The original idea in SDR is to place the ADC right after the antenna, doing all the filtering digitally on-chip and only using a RF passive off-chip filter additionally. However, today it is not possible to design a SDR receiver due to the current ADC dynamic range limitations. Thus, these architectures impose, for the current communication standards, ADC requirements beyond the state of the art.

These performance limitations have been explored in many works [1.1,1.13] and are particularly influential over the final specifications when implementing SDR for ultrawideband (UWB) communication systems [1.14,1.15]. In this case, the extremely high sampling rates that would be required lead to large amounts of sampled data and large digital processing power.

Since high performance ADCs would dissipate more power as well, both causes, the wide dynamic range requirement and high power consumption, make unfeasible to use a Nyquist rate ADC in wideband receivers. Although other receiver architectures have been proposed to overcome this problem, such as direct conversion [1.16], or low Intermediate Frequency (IF) [1.17], incorporating subsampling techniques [1.18,1.19] can alleviate the performance limitation of ADCs. This approach will not only relax the ADC requirement but also eliminate some of analog down-conversion stages.

In subsampling receivers the RF signal is sampled using a frequency lower than the maximum input frequency, but larger than two times the signal bandwidth. One of the low frequency replicas resulting from the sampling process, which contains the baseband signal, is then directly digitized.

The flexibility is the main advantage of the subsampling technique, by using an S&H to produce low frequency replicas of the RF signal, because most of the signal processing is made in the digital domain. In addition, it reduces the number of analog building blocks and relaxes the specifications of the ADC. Otherwise, the drawbacks of subsampling are the demanding specifications required for the S&H (wide input bandwidth and low aperture jitter) and a high noise due to folded thermal noise in the band of interest. Therefore, besides to exploit the advantages of subsampling techniques, an additional motivation of this thesis will be to reduce the effects of these drawbacks. Particulary, this work proposes a multiple clocking technique implementation in order to reduce the folded noise effect.

Finally, the study of subsampling receivers is extended in this thesis to multi-band and nonlinear cases. Due to the emergence of several co-existing wireless technologies, subsampling techniques can be useful to implement a receiver for multi-band applications [1.20]. This multi-band receiver subsampling technique may be used in other applications, such as the feedback loop for linearization of dual-band power amplifiers in RF transmitters [1.21]. In both cases, subsampling receivers will have additional limitations, due to the harmonics (nonlinear case) and the other carrier frequencies (multi-band case) are

subsampled and might be overlapped with the interest signal. Therefore, to find the valid sampling frequencies in these scenarios is a major challenge in order to avoid this overlapping between signals without reducing the total resolution.

1.2 Work methodology

This thesis work is based on the need to design a low-cost multi-standard data acquisition module for testing and certification purposes, in order to achieve the specifications given by the CENIT project named Telmax (PI-0553/2007), developed from the collaboration between the Electronics Engineering Group (GIE, University of Seville) and the company AT4 Wireless. These specifications required a data converter system for SDR and wideband applications (up to 3 GHz of carrier frequency), with a resolution higher than 8 bits integrating in a 20 MHz analog bandwidth.

Once an architecture based on subsampling was proposed due to its typical advantages detailed in the last section, the real capabilities of these techniques were validated by doing a state of the art staudy of the main necessary commercial components (i.e., S&H and ADC), and by an experimental characterization based on commercial of the shelf (COTS). After obtaining the expected results, the system was implemented on a printed circuit board (PCB) designed, manufactured and experimentally validated, successfully achieving the original objectives and publishing the obtained results.

Since these results showed how the most influential effect in the band of interest (up to 3 GHz input frequency) was the thermal noise folded in the signal bandwidth, the next step was to analyze how to reduce this effect in order to cover a higher number of wireless communications standards. The proposed architecture is based on using two different clock sources with the idea of maximizing the sampling frequency at the S&H. The theoretical expressions to reduce the signal-to-noise ratio (SNR) degradation were deduced before experimentally validating them at COTS and PCB levels.

Finally, with the objective to extend the proposed architectures to more real scenarios, where multiple signals are present in nonlinear environments, a new approach was proposed to provide an additional applicability of this thesis work. After studying the different published works about these fields, we contacted with the iRadio Lab group from the Electrical and Computer Engineering Department of the University of Calgary, in order to perform an internship to investigate about these topics within this experienced research group. An optimization of dual band receivers design in nonlinear environments was performed, integrating the previously presented multiple clocking techniques with the algorithm developed to find the optimal valid sampling frequency in order to avoid the aliasing between signals. The proposed solutions based on multi-filter architectures were experimentally validated.

1.3 Thesis outline

After doing a brief introduction in the present Chapter 1, Chapter 2 is dedicated to describe the context and the applicability of this thesis. A first section reviews the main concepts about SDR, detailing its main benefits and inconveniences. This section presents an introduction to cognitive radio as well. A second section is dedicated to review the main receiver architectures, focusing on their main advantages and disadvantages to be implemented as multi-standard receivers. This section concludes in the convenience of using subsampling architectures for multi-standards purposes.

The subsampling concepts are described in Chapter 3, focusing this description on its theory of operation and the main non idealities proper of these architectures, i.e., the jitter noise and the folded thermal noise. This chapter finalizes describing some examples of applications based on subsampling.

A data acquisition board based on subsampling for high performance low-cost multi-standard test equipment is presented in Chapter 4. Previously, a state of the art study and an experimental evaluation at COTS level were performed. With a signal bandwidth of 20 MHz it achieves 8.5 bit resolution for a programmable carrier frequency ranging from 0 up to 3.3 GHz, and more than 8 bit resolution up to 4 GHz.

A final section of Chapter 4 is dedicated to describe the obtained improvement of the noise performance by using multiple clocking techniques. This approach allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to total the folded thermal noise. This section is structured in a first part dedicated to the theoretical study and a second part dedicated to the experimental validation of these techniques. Considering a signal bandwidth of 20 MHz, the improved data acquisition system achieves an ENOB of more than 9 bits for a programmable carrier frequency up to 2.9 GHz and 8 bits up to 6.5 GHz, presenting an improvement in the resolution of 0.5-1 bit.

Chapter 5 presents the additional challenges of implementing subsampling techniques for multi-band and nonlinear applications. A particular case for dual band signals in a nonlinear environment is studied, integrating both effects and describing different architectures in order to optimize the total resolution.

Finally, Chapter 6 details the main conclusions and possible future directions of this thesis work, prior to presenting additional useful information in two different appendices. Appendix A is dedicated to describing the receivers based on interleaved ADCs as an alternative for several applications, whereas Appendix B describes the entire PCB process design used in the thesis.

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CHAPTER 2

OVERVIEW OF SOFTWARE DEFINED RADIO AND MULTI-STANDARD RECEIVER ARCHITECTURES

CHAPTER CONTENTS

This chapter is dedicated to describing the context and the applicability of this thesis. A first section reviews the main concepts about SDR, describing its evolution and detailing its benefits and the current problems that avoid getting this paradigm. This section presents an introduction to cognitive radio as well. A second section reviews the main receiver architectures, focusing on their main advantages and disadvantages when implemented as multi-standard receivers. This section concludes with the convenience of using subsampling architectures. The chapter finalizes describing several published multi-standard receiver architectures.

2.1 Software defined radio systems

2.1.1 Software defined radio idea and evolution

A SDR radio is a communication system that performs most of its signal processing tasks in a programmable digital signal processing (DSP), being fully adaptable by real time downloadable software, and enabling the adjustment of various communications scenarios automatically, adapting to different regional interfaces as well [2.1]. In other words, SDR means a radio where functionality and signal processing are defined in software, and it supports multi-band multi-user radio communication.

These systems will have a key role in future radio configurations because the emergence of new wireless technologies, and the necessity of integration of a larger number of communication standards in multi-standard and multiband radios in order to implement a *universal handset* that provides worldwide access.

Some benefits at top level are, for subscribers, an easier international roaming, improved and more flexible services, and increased personalization. For mobile network operators, some top-level benefits are the potential to rapidly develop and introduce new, personalize, and customized services [2.2].

A SDR system uses a single hardware front end but can be reprogrammed by software its frequency of operation, occupied bandwidth, and adherence to several wireless standards by calling various software algorithms, allowing inexpensive, efficient interoperability, and increasing flexibility via increased programmability. At the same time, SDR architectures simplify hardware component tradeoffs and provide new ways of managing the complexity of the emerging standards.

The SDR software reprograms the DSP segment in order to reconfigure the system and, thus, implement multiple radios. This segment performs the signal processing and conditions the signal to be modulated and demodulated, being the processing engine a combination of general purpose (GP) microprocessors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs) and specialized co-processors [2.3]. The DSP system is coupled to the air interface and antenna by analog-to-digital and digital-to-analog converters, as shown in Figure 1.1.

Note that, although the SDR paradigm allows a single terminal to adapt to multiple radio interface standards by software converting directly to digital domain after the antenna, an evolution process is still active, which has been described and predicted. This evolution is illustrated in the receiver of Figure 2.1 and is referred to the part of the radio architecture that is covered by the software

processing tools [2.2]. Therefore, new data conversion techniques are currently researched in order to get this paradigm in the future.

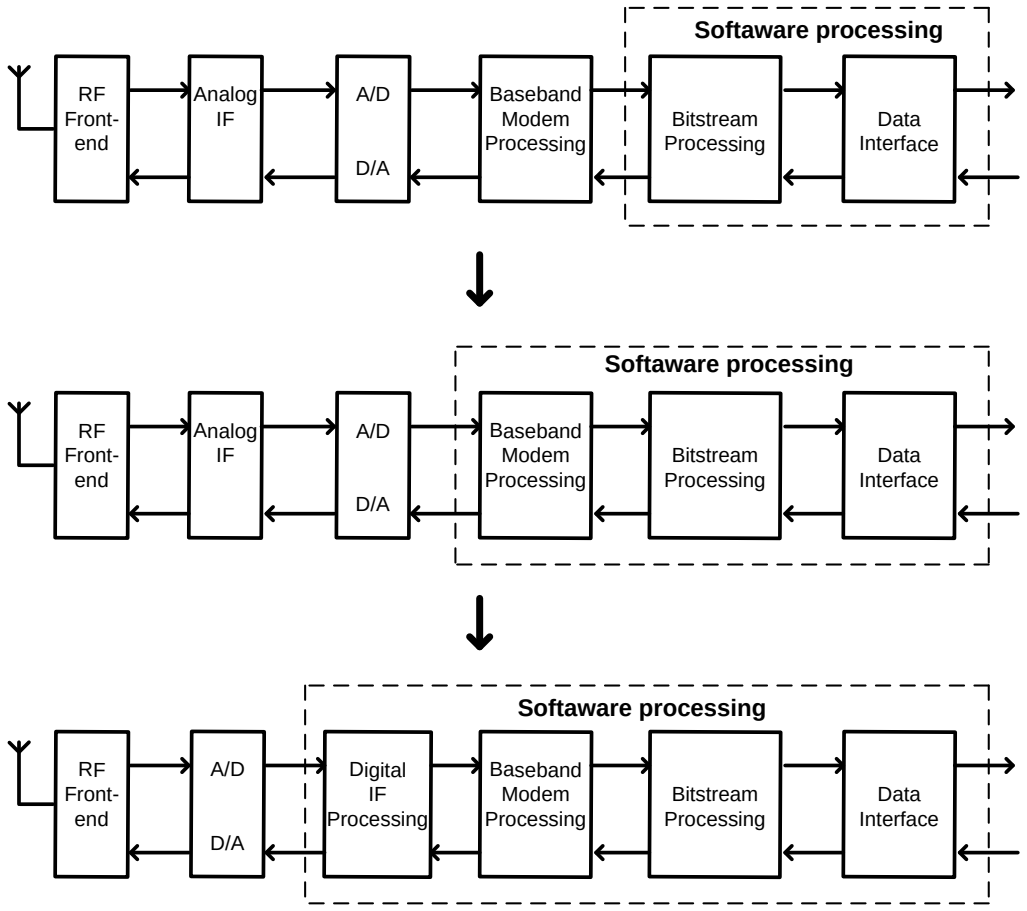

Figure 2.1 SDR Evolution

On the other hand, there are different download mechanisms [2.1]: static, pseudo-static and dynamic software download. Static download is the situation where SDR can support a variety of standards and is programmed in a static manner to address one of these possibilities. This means a first step about reconfigurability capabilities. Pseudo-static download refers to using the air interface to download and pre-configure a terminal to accommodate a defined set of applications, and protocols. This option increases the flexibility of the radio over the static option and, moreover, this upgrade can appear transparent to the user. Finally, the dynamic option offers a higher flexibility, due to allowing the reconfiguration during, for instance, a call, providing a concrete configuration on demand.

2.1.2 Software defined radio architecture

In this section a general scheme of a SDR transceiver will be described, presenting the main functionalities implemented in both sides, i.e., transmitter and receiver. Since this work is orientated to the receiver implementation, in following

sections the most convenient architectures for this part of the system will be described more concretely.

A block diagram of the signal processing functionalities in a SDR transceiver is illustrated in Figure 2.2. This diagram ranks of tasks known as *Primary Signal Processing Tasks* [2.3], which includes frequency translation, filtering and data conversion. Two more signal processing groups are classified for a SDR system, one dedicated to synchronization and another one dedicated to improve the response to the dirty RF [2.4] (*Secondary and Tertiary Signal Processing Tasks*, respectively). Both of them are described briefly in the end of this section.

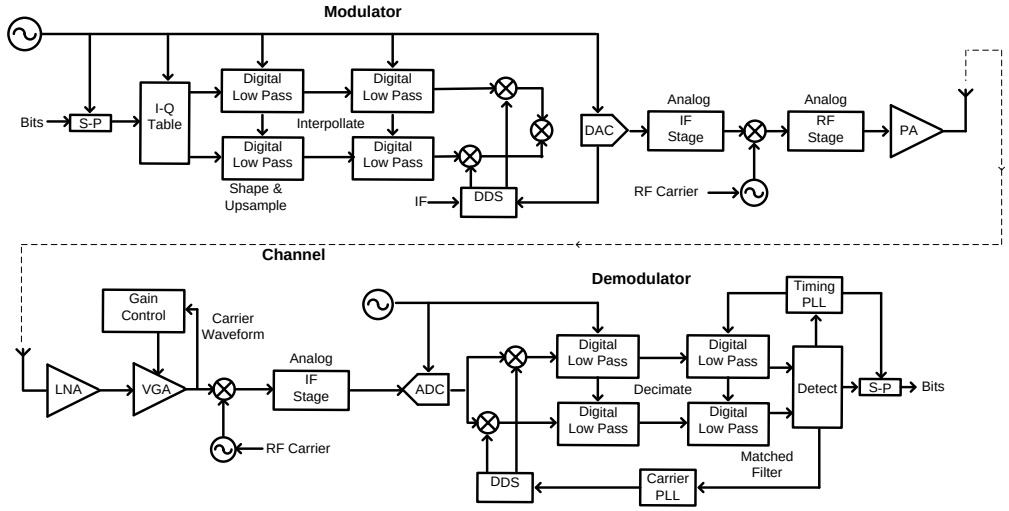

Figure 2.2 Block diagram of *Primary Signal Processing Tasks* in a typical transmitter and receiver

Centering the description in the receiver side (Figure 2.2), the received signal will be amplified and translated to suitable intermediate frequencies (IF) prior to being converted to digital domain. However, this architecture is only a first approximation because the SDR paradigm leads to implement this down-conversion digitally, i.e., placing the ADC just after the antenna. The converted signal is sampled by the demodulator, which down-converts the IF-centered signal with a digital down-converter (DDC). The current baseband-centered signal has a sample rate above the required to satisfy the Nyquist criteria so it will be reduced by the decimating filter. Therefore, these two processes mirror and cancel the up-conversion and the interpolation[1], respectively, implemented in the transmitter side. Finally, the reduced sample-rate signal is used as input of the detector and is processed to maximize its output SNR.

[1] Usually this output sample rate is fixed at some sufficiently high value that can be used for a large IF range.

Although it is possible to observe from Figure 2.2 that the transmitter and the receiver side are almost complementary, the receiver also performs a number of tasks not present in the transmitter, such as to estimate unknown parameters of the received signal as amplitude, frequency offset, or timing offset. To implement these functionalities some elements as a channel equalizer, a digital automatic gain control (AGC), a DC canceller, and a SNR estimator are necessary in the receiver part, although they are omitted from the block diagram by simplicity.

On the other hand, some of the *Secondary Signal Processing Tasks* in the receiver are the modulation carrier alignment, symbol clock alignment, and scaling the received signal with its SNR. In fact, when the alignment process is performed properly, the receiver is able to collect all the energy in the receive signal, estimating the transmitted waveform's amplitude with maximum SNR. Consequently, SDR radios work over a large range of stressed signal levels.

Finally, the *Tertiary Signal Processing Tasks* help to minimize the problems caused by the tolerance, and gain and phase imbalances from the analog world. Also, other non idealities contribute to the signal degradation. These effects include the non linearity in the power amplifier, ADC and mixers, DC offsets and coupled spectral lines, oscillator phase noise, sampling aperture jitter and clock jitter. Therefore, the receiver includes some compensating processing DSP blocks to reduce the effects from the analog components. These blocks are DC cancel, Phase and Gain Balance, and Channel Equalization.

2.1.3 Benefits and inconveniences of the software defined radio

An SDR has advantages in cost and performance. Since almost all the functionalities are performed in the digital domain, these designs are less expensive to manufacture, due to the Moore's Law, and offers a better general performance as well as reduced sensitivity to age, temperature and environmental influences. Analog components such as resistors or capacitors are manufactured with specific tolerances. Also circuits designed from analog components suffer from mismatch and imbalance effects, which limit the performance of the system.

Moreover, note that, although an SDR design uses digital techniques, differs from a DSP radio (also called *software-controlled digital radios* [2.1]) in that its radio parameters are not fixed, i.e., they are reconfigurable. The main advantage of this reconfigurability is that an SDR system supports communications between a wide range of communication systems. This programmability includes programmable RF bands, channel access modes, and channel modulation. Moreover, as new waveforms, features and standards are developed and incorporated, the SDR can be reprogrammed, through software upgrades, to increase its capabilities and be a new radio. These benefits will reduce the costs delaying the obsolescence of the communication systems. Therefore, in applications where access to multiple bands with multiple radio

access modes is a necessity, the SDR can reduce hardware size, complexity and power through fewer radio units.

However, SDR is still a radio and, therefore, the rules to design a good radio must be applied as well. As this design requires a larger bandwidth and dynamic range, the DSP section will need reduced levels of dirty RF [2.4] in the analog air interface. The phase noise, the jitter, the level of the third order intercept will have to improve because DSP by itself cannot repair all these sources of signal degradation introduced by the analog components.

Another RF problem in SDR is the necessity to avoid the introduction of processor clock harmonics into the analog RF and IF circuits. Also, when a multiple transmitter is implemented electromagnetic interference (EMI) problems will occur. Nevertheless, some of these inconveniences are present in multiple hardware radios as well.

Moreover, it is difficult to engineer wideband, low loss antennas, and RF and data converters, so new techniques to implement the transceivers must be developed in order to cover most wireless communication standards placing the data converters (ADCs and DACs) as close to the antenna as possible. The present work will be focused in these objectives, about the optimal conversion techniques in the receiver side.

An additional problem of an SDR system is that, due to its flexibility, it can be used to perform functions that are prohibited by legal restrictions, like to transmit in unlicensed frequency bands. This problem must be addressed as well.

Finally, another known drawback is the difficulty to place the ADC right after the antenna, due to the current ADC specifications. This problem will be address throughout this thesis work.

2.1.4 Introduction to cognitive radio

At this point it is necessary to introduce the cognitive radio idea. Due to another functionality of the SDR is its capability to adapt itself the transmission scenario in order to minimize the interference with other signals in the air interface, the system will require the ability to scan the spectrum from low to high frequency using software. With this objective in mind, the idea of CR [2.5] is to build on an SDR, where the radio adapts itself to the environment by optimizing the carrier frequency, modulation, and choice the radio standard to minimize interference and maintain communication in a given scenario. One of the most promising objectives of CR is to increase the spectrum occupancy, the radio utilizing spectrum that is not used by other radio at this moment. Another main objective will be to be able to implement a highly reliable communication whenever and wherever needed. The three fundamental cognitive tasks can be found described in [2.6]:

- Radio-scene analysis
- Channel-state estimation and predictive modeling
- Transmit-power control and dynamic spectrum management

In summary, this SDR radio does not just transmit and receive. In the transmitter case, it characterizes the available transmission channels, probes the propagation paths, build an appropriate modulation and transmit in the right direction, selecting the appropriate power level. In the receiver case, it characterizes the energy distribution in the identified channel and in adjacent channels, estimates other parameters as channel interference levels and subscriber locations, recognizes the mode of the incoming transmission, adaptively nulls interferers, estimates the properties of the desired-signal multipath, combines desired-signal multipath, decodes the channel modulation, and then corrects residual errors decoding the signal with lowest possible bit error rate (BER) [2.1].

2.2 Receiver architectures

2.2.1 Superheterodyne receiver

In the super-heterodyne receiver (Figure 2.3) the signal received at the antenna is translated to the baseband using two down-conversion mixers, previously to be converted to digital domain. Due to the first mixing process from RF to IF, it is mandatory to use an image-reject filter (IRF) in front of the mixer. The channel selection is performed in the IF stage, baseband stage and in the digital domain [2.7]. After the first down-conversion the desired channel is translated into IF, the channel selection being mainly performed by an IF band pass filter. This filter is usually an external surface acoustic wave (SAW) filter. After the second down-conversion, the desired channel is translated to a lower frequency. Then a band pass (BP) filter is employed before ADC to avoid aliasing and to select the channel. A digital filter is often used to eliminate the out-of-channel quantization noise, contributing to the channel selection as well.

There are two main options to implement the superheterodyne receiver [2.8]. Figure 2.3 illustrates the first option, which is a two stages down-conversion receiver where the signal is translated to a low frequency band.

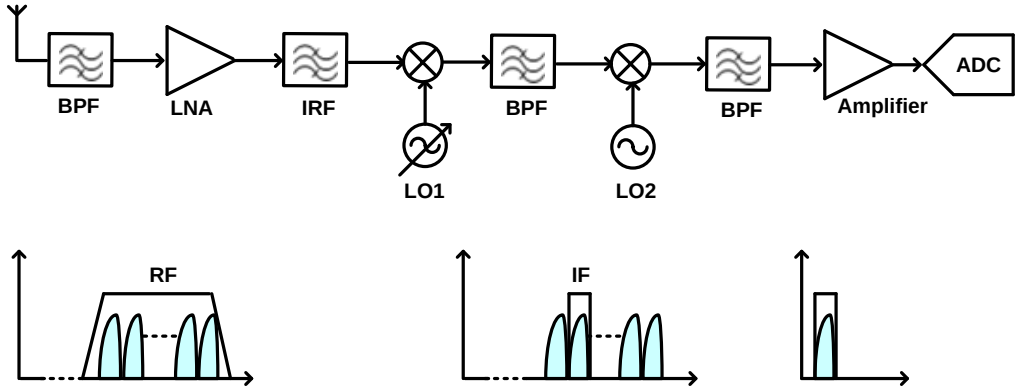

Figure 2.3 Conceptual diagram of the two-stages down-conversion superheterodyne receiver

However, if the second IF of a two stage down-conversion receiver is equal to zero (Figure 2.4), the second down-conversion separates the signal to in-phase quadrature (I-Q) components and the corresponding demodulation and detection are performed at baseband. This second down-conversion is implemented by quadrature mixers, which have a 90º phase shift between the two Local Oscillators (LO). Thus, any offset between the nominal phase and amplitude mismatches between I-Q components will increase the BER. However, since conversion from a real to a complex signal is done at one fixed frequency, only an I-Q, amplitude balanced LO is required.

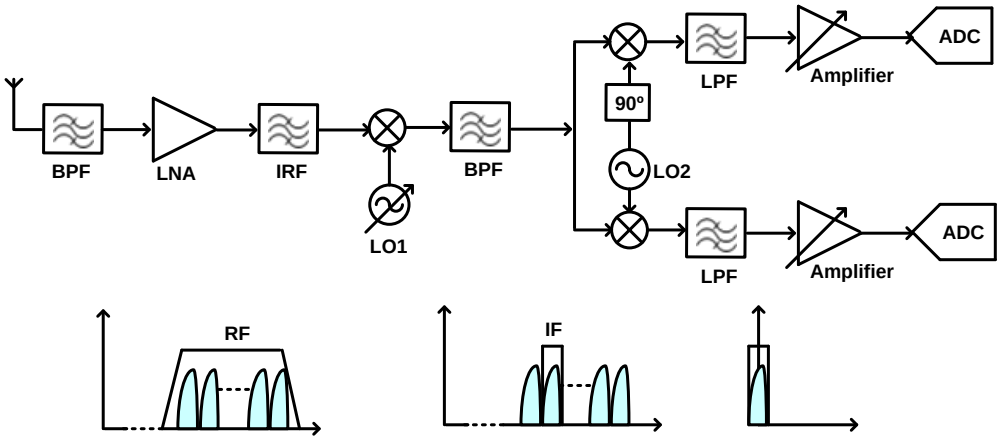

Figure 2.4 Conceptual diagram of the two-stages down-conversion superheterodyne receiver with the second IF equal to DC

A third option to implement a superheterodyne receiver is illustrated in Figure 2.5 [2.9], where the first down-conversion is implemented in RF hardware and the second one in the DSP. Further intermediate conversions can be realized in the DSP via decimation processes. Although the I-Q is implemented in digital domain, the ADC will process IF frequency, increasing its requirements.

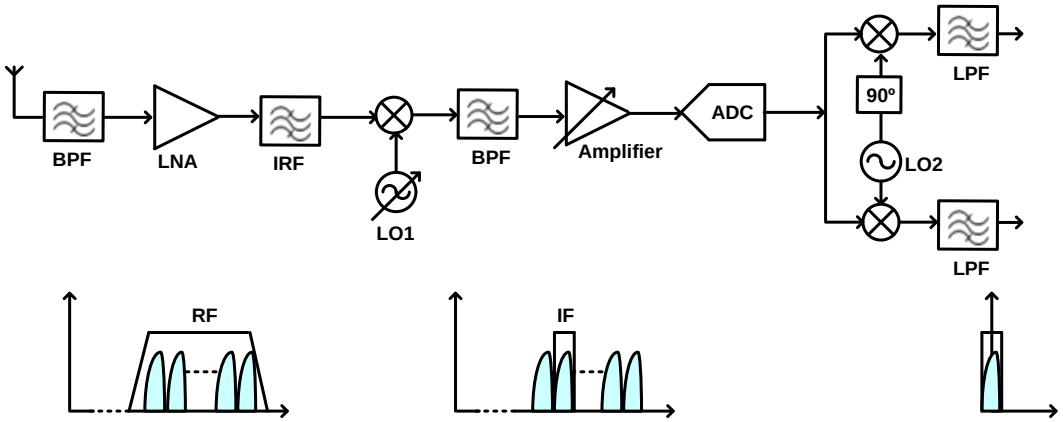

Figure 2.5 Conceptual diagram of the two-stages down-conversion superheterodyne receiver with the second IF translated to DC digitally

In other hand, the selected IF will influence over features as sensitivity (image rejection) and selectivity (channel selection). When IF is high the channel selection filter will require a high Q-factor and, however, the image band is located far away from the interest signal such it is possible to eliminate this image easily by an IRF. On the contrary, if IF is low the channel selection is easier but the image rejection is harder to implement. Thus, several stages of down-conversion help to implement the superheterodyne architecture with enhanced selectivity and sensitivity, selecting a first IF high enough to eliminate the image and a lower second IF to be able to efficiently select the channel.

About the image rejection, other architectures have been proposed in the literature to eliminate the need the IRF. An example is the image reject architecture proposed by Hartley (Figure 2.6 [2.10]), based on mixing the RF signal with the quadrature phases of a LO, and shifting one of these outputs 90º before adding them together. It can be shown that the image will have opposite polarity at the summation, and the signal has the same polarity. Therefore, image will be canceled after summation. The main drawback of this architecture is its sensitivity to the gain and phase imbalance between two branches. Also, the loss and the noise introduced by the phase shift block and the nonlinearities in the adder will degrade the overall performance.

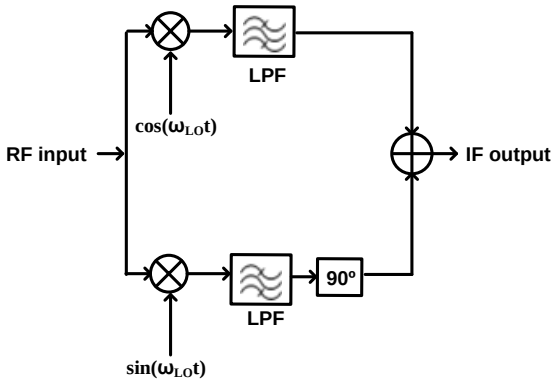

Figure 2.6 Hartley's receiver architecture

Another image reject architecture was proposed by Weaver (Figure 2.7 [2.11]), where the 90º phase shifter block is replaced by a second quadrature mixing stage. The mismatches between both paths and nonlinearities of the components are the main problem again. Although the noise introduced by the phase shifter block is eliminated, a second image effect can be introduced if the second down-conversion mixer translates the IF signal to a nonzero center frequency.

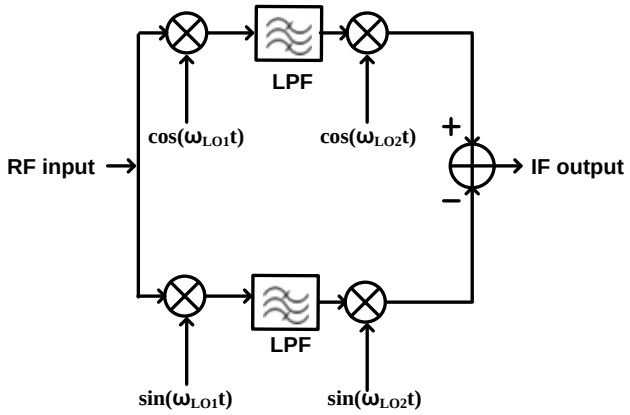

Figure 2.7 Weaver's receiver architecture

Besides the channel selection filtering and the image rejection filtering, there is a third filtering group in the superhetorodyne receiver. This filtering group is necessary at the first stages chain, and employed to reject the out-of-band signals produced by the nonlinearities in the low noise amplifier (LNA) and that can interfere with the in-band signals.

Unfortunately, superheterodyne receivers have additional problems in respect to being applied in SDR applications. The complexity of this architecture is high, requiring several local oscillator signals. Generally, different fabrication technologies are used, making full on-chip integration more difficult, due to the necessary high Q-factors of the discrete components, as the specialized IF filters required by this structure. These difficulties increase the cost, area and power

consumption. In addition, coming off onto a chip at 50 ohms impedance, required by most specialized filters, could cause problems with IC design, where impedance levels usually are of the order of hundreds of Ohms.

Also, these receivers are usually designed to a specific channel, i.e., for a particular wireless standard. This fact limits the expansion of the receiving band to be used with signals whose modulation formats and occupied bandwidths are different [2.14]. Therefore, this configuration is not an attractive option for use in SDR receivers do to its complicated expansion for multiband applications.

2.2.2 Zero-IF receiver

The zero-IF receiver (or homodyne receiver) [2.12] is another approach, which is illustrated in Figure 2.8, being a simplified version of the superheterodyne architecture. In this case there is not IF stage between RF and baseband (Figure 2.8), the channel selection being implemented by just a low pass filter before the ADC, which helps to avoid aliasing as well. Part of the channel selection can also be performed in the digital domain. This channel selection stage is the most important for applications that use wideband ADCs to digitize several channels at the same time

The whole received RF signal is selected by a band pass filter and amplified by a LNA, as in the previous architecture. It is then directly down-converted to base band by a mixer and converted to digital domain by an ADC. Previously, the signal is passed by a low pass LP filter, in order to reject the adjacent channels and avoid the aliasing, and amplified by a baseband AGC (Automatic Gain Control), providing the majority of the whole gain, i.e., a higher value than the LNA gain [2.9].

This architecture lets the number of analog components reduces in respect to the superheterodyne structure, decreasing the complexity, offering significant power save and evolving towards a fully integrated single chip. Since the LO frequency is equal to the carrier frequency, the desired signal and the image are the same, and the IRF is not necessary. Therefore, this scheme allows increasing the integration level, being suitable for use in multiband applications.

However, if there is not a proper isolation, the output of the LO may leak to the input signal port of the mixer (or the LNA). This leaked signal will be mixed with the LO output and produce a DC component at the output of the mixer, falling in the desired signal band. This effect is called self-mixing. Moreover, LO leakage to the antenna may result in a time-varying DC offset due to self-mixing [2.8]. This LO leaked will be reflected back into the receiver from the antenna. The reflected signal will vary with the physical environment where the antenna is placed.

These effects (DC component and DC offset) will corrupt the interested signal at baseband, which also will be affected by the flicker (1/f) and the second order distortion product mixed down. An additional problem of this architecture is about the mismatches in gain and phase between the I-Q outputs, because both signals must be balanced over a wide frequency. Finally, since most of the signal gain is implemented at one frequency band it is possible to create an instability effect [2.9].

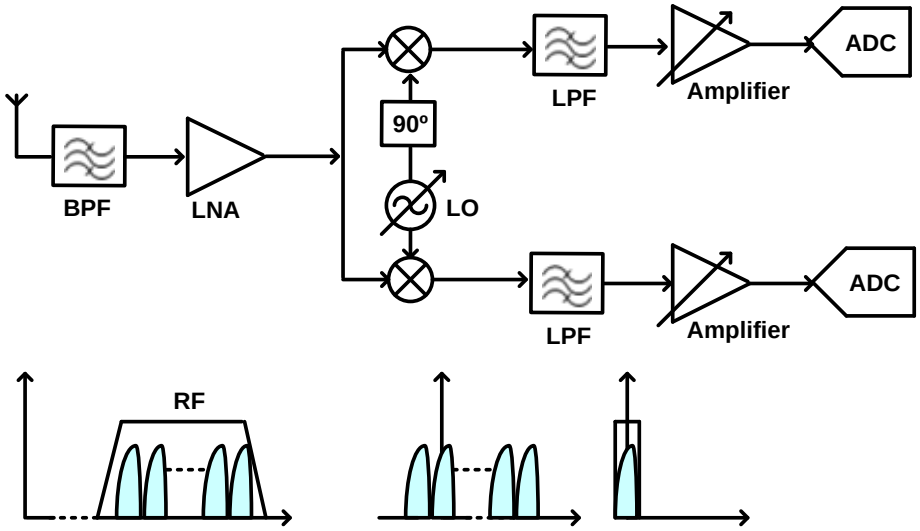

Figure 2.8 Conceptual diagram of the zero IF receiver architecture

2.2.3 IF receivers

To provide full integration and to overcome the problems associated with the traditional heterodyne and homodyne architectures, IF receivers have been designed. The received RF is down-converted to IF by a LO [2.13], IF being either one or two times the information bandwidth (low IF-receivers) or arbitrary (wideband-IF receivers), depending on the specifications in terms of sensitivity and selectivity [2.8].

2.2.3.1 Low IF receivers

The low IF receiver presents a scheme similar to zero IF architecture, the RF signal being mixed down to a nonzero low or moderate IF instead of translating directly to base band frequencies (Figure 2.9). In this case, a RF band pass filter is applied to the incoming signal, the low IF signal is directly converted to the digital domain. The next step is the channel selection, which can be performed with a LP or BP filter. Although generally a LP filter is enough if IF is very close to DC, a BP filter can be preferable in order to suppress both the DC offsets and flicker noise, which can be removed without severely deteriorating the signal. Another option is to implement this BP filtering in digital domain. Meanwhile, due to the low Q requirement, a typical IF SAW filter employed in the superheterodyne receiver can be replaced by an integrated CMOS filter.

The next down conversion from low IF to baseband is implemented in the digital domain, avoiding the problems caused by the I-Q mismatches in the analog domain.

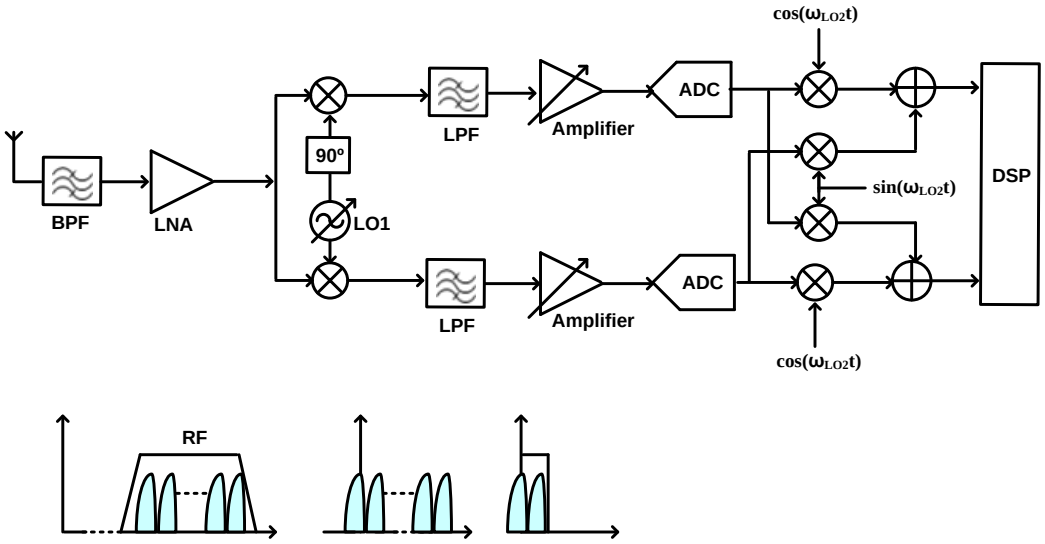

Figure 2.9 Conceptual diagram of the low IF receiver architecture

This structure is also simple and still allows a high level of integration and does not suffer from the zero-IF architecture problems (DC offsets or flicker noise) because the desired signal is not folded to DC. However, in this case, the image frequency disadvantage is reintroduced, due to being difficult to reject it, thus being the major drawback of this architecture. Both image and desired signal will be digitized by the ADC. Thus a digital filtering for channel-selection will be implemented by the DSP as well. An additional problem is about the ADC power consumption, which is increased because now a higher conversion rate is required.

Another option to eliminate the image interferer is to use an IF polyphase after the down-conversion, as shown in Figure 2.10 [2.7]. This makes this architecture very suitable for multi-standard receivers, since this filter can be shared by different standards. Any changes in the RF frequencies can be solved by using corresponding LO frequencies and down-converting the RF signal to the same IF, filtering the corresponding image by the polyphase filter.

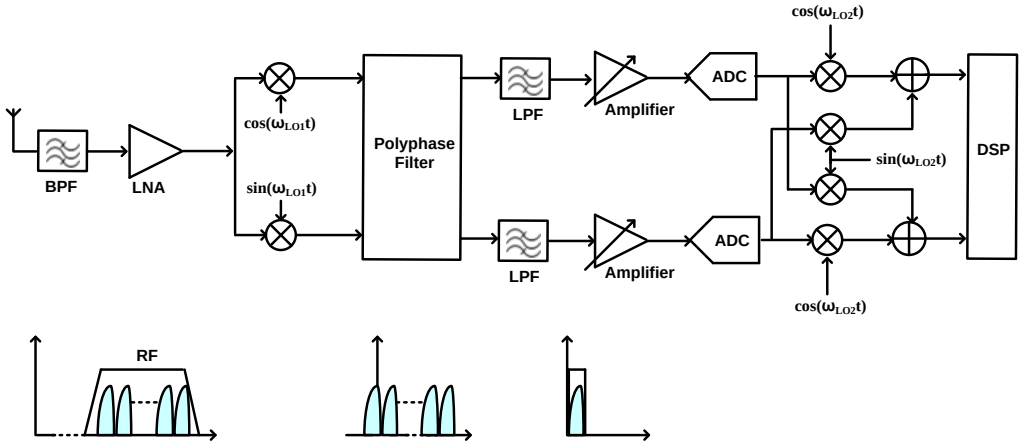

Figure 2.10 Conceptual diagram of the low IF receiver architecture with polyphase filtering

2.2.3.2 Doble low IF receivers

The basic idea of these receivers, whose block diagram is illustrated in Figure 2.11, is to up convert the I-Q channels, generated previously at IF, to a high frequency using a fixed frequency synthesizer [2.15]. The signal then feeds to an IF filter, usually off chip, being its integration level lower than in the low IF case.

The double low IF architecture is more immune to DC problems, like in the low IF case. Also similar to a low IF receiver, the close proximity of the image signal means its suppression is not possible by only the RF filter. Although, these receivers would be limited to standards with moderate adjacent channels or stringent requirements of the IRF, unlike the low IF receiver, the signal is up converted to a high IF, where a very high-Q discrete filter is employed to remove the image. This filter will contribute to the suppression of the image in conjunction with low pass filter at the first IF stage, providing a higher selectivity performance and a compromise between selectivity and integration level.

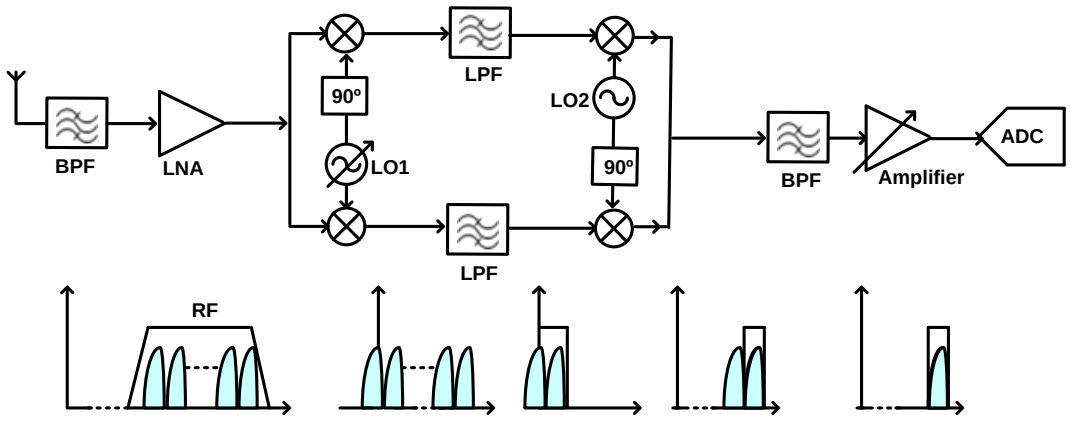

Figure 2.11 Conceptual diagram of the double low IF receiver

2.2.3.3 Wideband IF receivers with double conversion

A receiver which uses a RF channel-select frequency synthesizer and an IF or baseband channel-select filter is a narrowband receiver. An alternative architecture based on IF receiver structures to use for multi-standard applications is the wideband IF receiver (Figure 2.12), where the entire RF band containing the information is translated to IF by multiplying the LO output with a fixed frequency [2.15]. All the channels at IF are then translated to DC using a tunable, channel-select LO and, finally, the selected low pass channel feeds the ADC. Previously a variable gain has been provided. As in the case of zero IF receivers, channel filtering can be performed at baseband, where digital programmable filters can enable more multi-standard receiver features.

This approach is similar to superheterodyne receivers in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne architecture, the first LO frequency translates the whole RF band, maintaining a large bandwidth at IF. Moreover, the wideband IF receiver has an additional advantage about a higher capability to facilitate the synthesizer integration than the rest of receivers described previously. Therefore, the integration of this architecture is also feasible, although the I-Q mismatches problems in the analog domain are reintroduced. Similar to the zero IF receivers, other inconvenience of wideband IF architectures is its susceptibility to flicker noise, DC offset and distortion due to second order intermodulation.

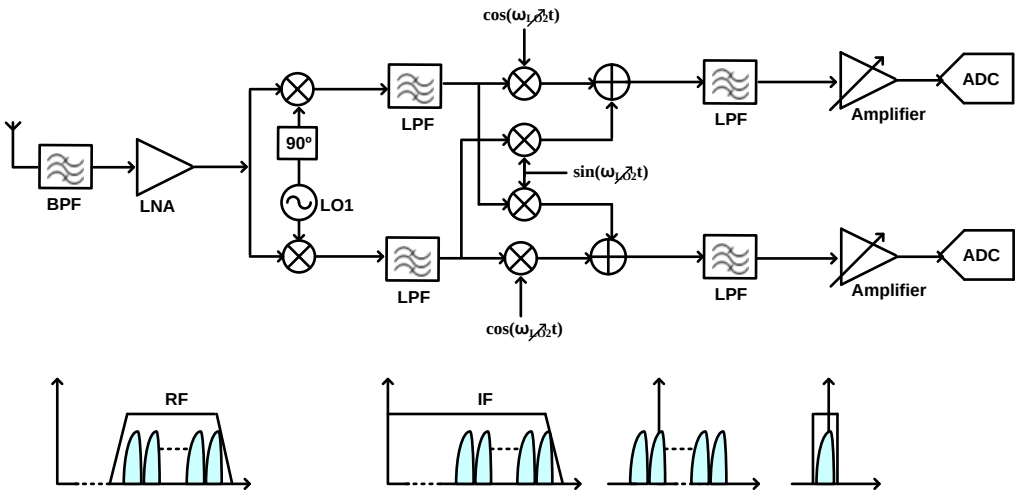

Figure 2.12 Conceptual diagram of the wideband IF receiver architecture with double conversion

2.2.4 Subsampling receiver

A feasible alternative to the previous solutions is the receiver based on subsampling, which is illustrated in Figure 2.13. The received signal is filtered by a RF band pass filter that can be a tunable filter or a bank of filters. The incoming band pass signal is sampled under Nyquist criteria [2.16,2.17], using some

sampling properties and avoiding aliasing, as is described in Chapter 2. This sampled signal is converted to digital using an ADC at intermediate sampling rate. The main advantage of this scheme is its simplicity, the number of components being reduced, and being possible to place the data conversion closer to the antenna. Therefore, lots of functions like filtering, frequency translation and demodulation can be implemented in digital domain, taking advantage of low cost digital VLSI solutions, leading to a high integration and eliminating problems such as DC offset, 1/f noise.

In addition to system cost reduction, pushing these functions in digital domain eliminates the many of the sensitivities of analog solutions, such device matching, environmental sensitivity, and performance variation over time. The flexibility and reconfigurability required by SDR applications is also increased by moving the ADC into IF stage and, moreover, it is possible to use this architecture for wideband and multi-standard applications because of its large analog bandwidth. In this architecture, a single ADC can sample multiple signal channels, which are then separated and demodulated in parallel in digital domain.

However, some critical requirements exist when this structure is employed, as the needed analog input bandwidth of the S&H. Since this bandwidth must include the RF carrier frequency, the bandwidth of the S&H inside the ADC cannot be large enough for the required dynamic range, resolution and sample rate using the current technologies. A common solution is to place a previous external S&H.

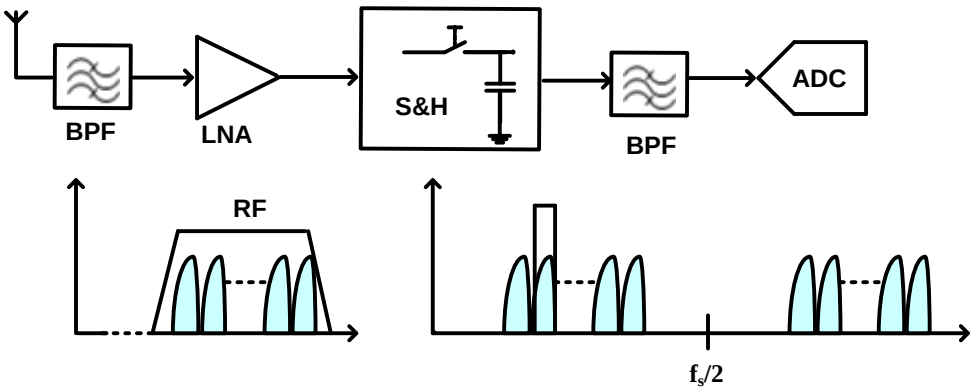

Figure 2.13 Conceptual diagram of the subsampling receiver architecture

An intermediate alternative, about simplicity and S&H requirements, is to do a previous translation to IF, as shown in Figure 2.14. This concept is called IF-sampling [2.18], being this digital-IF architecture a step toward SDR idea where the last down-conversion stage in heterodyne receivers is replaced by an ADC stage.

If the Nyquist theorem is met the sampling function is called Low Pass Sampling (LPS) and the IF signal is directly sampled and converted by the ADC,

avoiding the I-Q mismatches problems. However, since the IF signal have to be large, in order to avoid the filtering rejection problems, the ADC requirements will be very demanding. Therefore, for this architecture, to sample without meeting Nyquist theorem (only with a sampling frequency higher than twice the information banwidth) allows to obtain more relaxed ADC. This sampling function is called Band Pass Sampling (BPS) and it is equivalent to realize a down conversion mixing by spectral folding, as shown in Chapter 2. This scheme will avoid the I-Q mismatches problems as well.

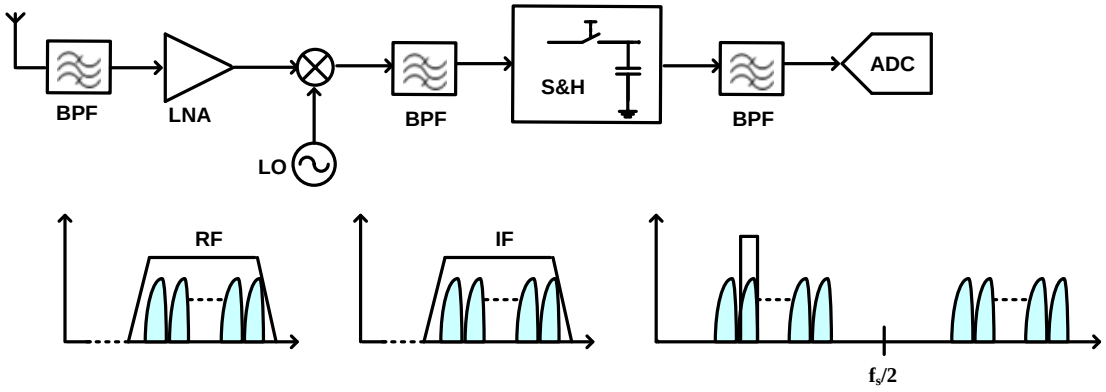

Figure 2.14 Conceptual diagram of the subsampling architecture with an intermediate down-conversion

Finally, subsampling receivers have additional problems as some noise sources, as the jitter and thermal noise folded in the interest band, finally these effects being minimized in this thesis work.

Moreover, RF band pass filtering is required when avoiding overlap between folded signals is necessary. These BP filters, especially on-chip filters, are difficult to implement at high frequencies. Although external filters, such as SAW filters, can be used, they are only available at limited number of frequencies, so it is not a practical solution to design multi-standard receivers.

Alternatively, higher sampling frequency is often used to reduce the required selectivity. However, this solution has some drawbacks as the high technology and high cost required by the ADC, whose resolution and dynamic range will be degraded as compared to lower sample rate ADC alternatives. Also power consumption is increased with sample rate. Therefore, the cost, performance, and power consumption of other devices (such as ADC clock sources, digital circuits after the ADC) also will be impacted by the ADC sample rate. In this thesis some novel techniques, about the sampling frequency plan, are addressed in order to avoid this overlapping between signals, reducing the complexity of the RF filtering. On the other hand, additional adjacent interferers not overlapped with the desired signal can be suppressed by additional channel filtering in digital domain.

2.2.5 Receivers based on interleaving

An alternative scheme to the subsampling techniques, in order to place the analog-to-digital conversion close to the antenna, is a time-interleaved ADC architecture. This scheme is an effective approach for achieving very high sampling rates [2.19,2.20]. A time-interleaved ADC operates *M* parallel ADCs at different sampling times, creating the image of a single ADC operating at a much higher sampling rate. The concept is illustrated in Figure 2.15 [2.20]. Ideally, the *ith* ADC, $i = 0, ..., M - 1$, samples periodically the input signal at time instants t_i, t_{i+M}, t_{i+2M}, with sample rate f_s/M, where $t_m = mT_s$ and $T_s = 1/f_s$ is the sampling period of the time-interleaved ADC. The final output is created by multiplexing all of the individual ADC outputs in the proper order (e.g. ADC_0, ADC_1, …, ADC_{M-1}, ADC_0, ADC_1, etc.).

Thereby, the final effect is as if the input signal were sampled once every Ts seconds, i.e., with sample rate f_s. This approach has been widely adopted in the industry, since the converters can be working at lower speeds without sacrificing the overall system performance.

However, it should be noted that each individual ADC deals with the entire analog input signal, and, therefore, its S&H circuit must be able to preserve the full input signal bandwidth. This is the main inconvenient to use these architectures for multi-standard receivers, besides the mismatch between ADCs, being this thesis focused mainly in subsampling techniques. Nevertheless, an approach to receivers based on interleaving is addressed in Appendix A.

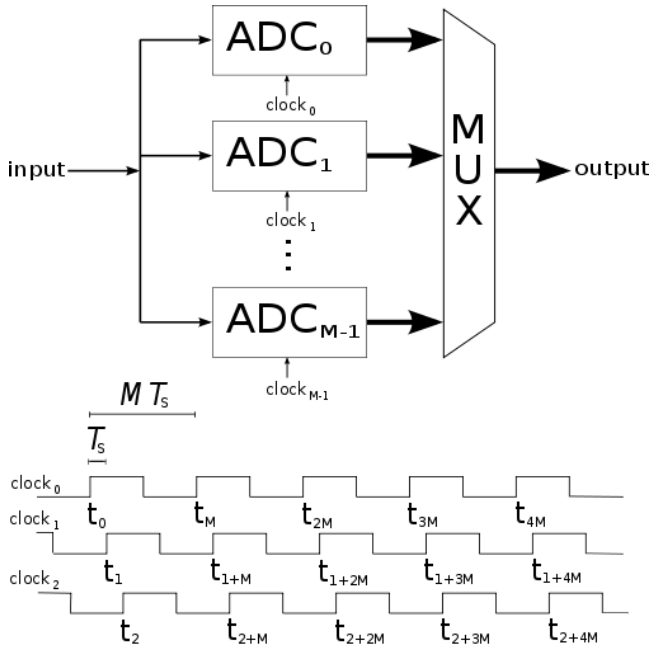

Figure 2.15 Conceptual diagram of the receiver based on interleaving architecture

2.2.6 Multi-standard receivers

Stacking several receivers for different standards into a single receiver, operating in parallel, is not a feasible option to implement a multi-standard receiver because the area and the power consumption would be extremely high. Therefore, a multi-standard receiver should share the available hardware resources as possible and make use of the tunable and programmable devices, increasing the level of integration. From the view of high level integration, the zero IF receiver, low IF receiver, wideband IF receiver and subsampling receiver are most suitable, while the double IF receiver presents a compromise between selectivity and integration level.

From the view of placement of the ADC, both the zero IF receiver and the subsampling receiver are candidates for SDR implementation because the ADC directly has an interface to RF or higher IF signals. However, due to some inconveniences of zero IF receivers, as DC offset or LO leakage, this thesis will be addressed to subsampling receivers.

Regarding the radio section, note that the different standards require different front-end performance. The most straightforward solution would be satisfying the most critical specifications for each one. Some of the more typical standards that need to be covered by multi-standard receivers are illustrated in Figure 2.16.

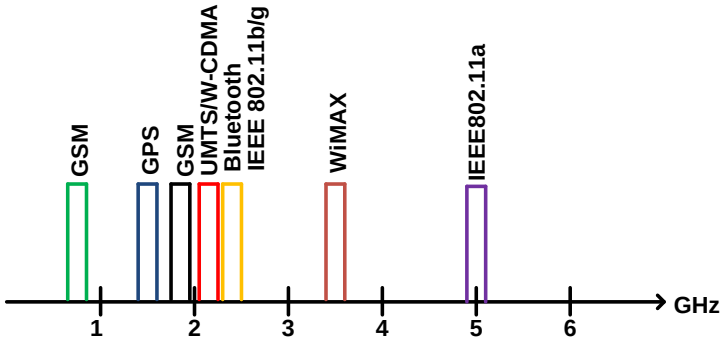

Figure 2.16 Multi-standard frequency spectrum

In this section two examples of conventional multi-standards receivers are described. The multi-standard receiver based on subsampling, designed in this thesis work, is described in the following chapters and compared with other published subsampling receivers for multi-standard applications.

2.2.6.1 Multi-standard zero IF receiver

Figure 2.17 [2.21] illustrates a single-chip multi-mode receiver for four standards (GSM900, DCS1800, PCS1900 and W-CDMA), which was designed in a zero IF scheme. An external digital controller selects the different standards and the hardware is shared as much as possible by different standards. These standards

use two different channel selection filters, and the quadrature LO signals are obtained by using a divide-by-two-circuit for the mixers. Since the LO signal is generated on-chip, the LO leakage on the PCB to the RF input, which is a typical problem for homodyne receivers, is eliminated more efficiently. However, the level integration will be lower in this case.

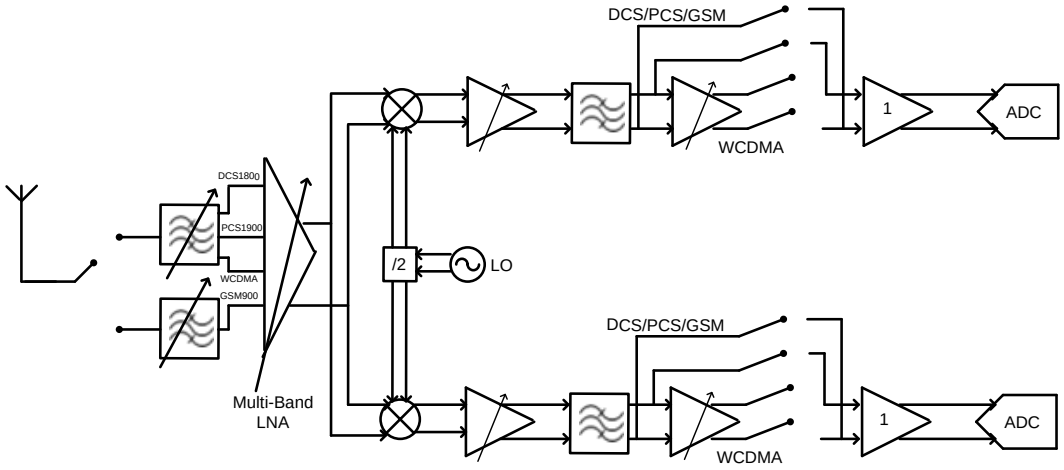

Figure 2.17 Multi-standard receiver architecture by zero IF

2.2.6.2 Multi-standard low IF receiver

Figure 2.18 [2.22] illustrates another fully integrated multi-standard receiver designed in low IF, with several SAW BP filters and a multi-band LNA preceding this architecture. This design supports five wireless communication standards, Bluetooth, GSM (DCS1800 for Europe, or PCS1900 for USA), UMTS, 802.11b/g and 802.11a. It is possible to observe in the diagram block how the Bluetooth channel is active all the time, while the other four standards, which cover five different frequency bands, are activated by an RF switch before feeding the rest of the low IF receiver due to how they do not need to be covered at the same time, i.e., when an application is active, the others can be switched off or in idle mode, in order to save power and reuse hardware resources. Otherwise, Bluetooth needs to operate concurrently to other standards, allowing to have activated the wireless link during a phone call or data communication.

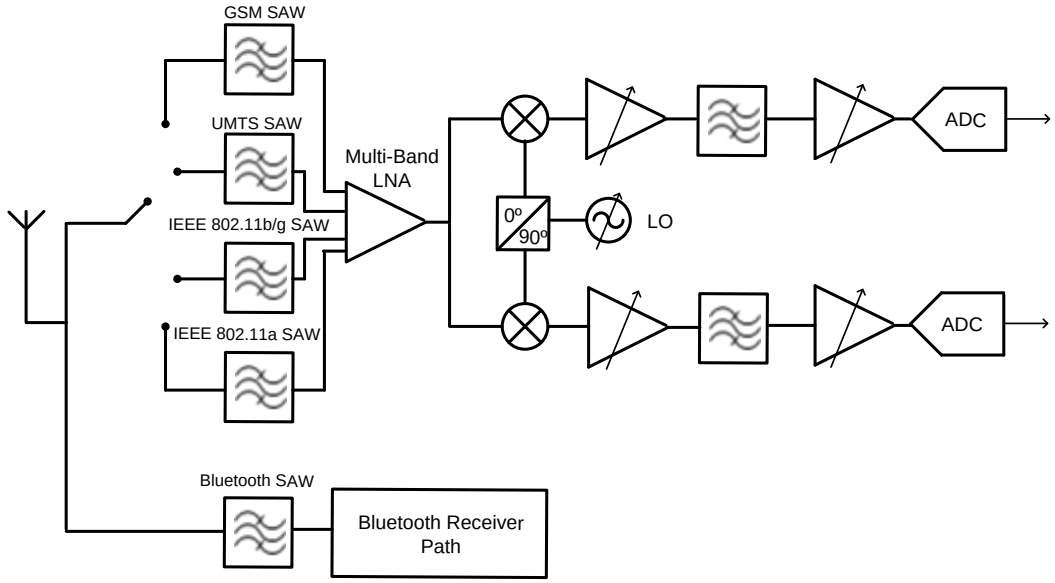

Figure 2.18 Multi-standard receiver architecture by low IF

In this section a comparative of multi-standard receivers about digitalization techniques (i.e., mixing or subsampling based systems) have been introduced. There is a second research field about the band strategy (i.e., wideband or narrow band strategy). While the examples described in this section [2.21,2.22] are narrowband multi-standard receivers because of they employ dedicated channels, other published works [2.23-2.26] can be considered universal receivers, covering a large input frequency range. Although these wideband solutions are more flexible, their main inconvenience is the RF front-end must meet the requirements for each standard and they are not optimum for any standard. These alternative receivers will be studied more precisely when they are compared with the works described in Chapter 3.

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CHAPTER 3

SUBSAMPLING RECEIVERS

CHAPTER CONTENTS

This chapter presents an overview of the subsampling techniques. The two first sections are dedicated to detailing the used signal representation and to

reviewing the sampling theory, respectively. The subsampling concepts are described in a third section, focusing on the theory of operation and the requirements to find the valid sampling ranges in order to avoid aliasing. A fourth section details the typical non idealities proper of these architectures, i.e., the jitter noise and the folded thermal noise. This chapter finalizes describing some published examples of applications based on subsampling.

3.1 Signal representation and definitions

In current wireless communication links (Figure 3.1) [3.1], a complex modulated baseband signal containing the useful information can be expressed as:

$$s(t) = A(t)e^{j\varphi(t)} = I(t) + jQ(t) = A(t)\cos\varphi(t) + jA(t)\sin\varphi(t) \qquad (3.1)$$

This signal is usually up-converted to an RF band pass signal around a carrier frequency f_c to be transmitted through a wireless channel and detected by a receiver and converted back to base band again. The pass band transmitted signal can be written as follows

$$\tilde{s}(t) = \Re[s(t)e^{jw_c t}] = \Re[A(t)e^{j\varphi(t)}e^{jw_c t}] = A(t)\cos(w_c t + \varphi(t)) \qquad (3.2)$$

Where $w_c=2\pi f_c$ and $A(t)$ and $\varphi(t)$ are amplitude and phase of the complex base band signal, and the transmitted signal, $\tilde{s}(t)$, is the real part ($\Re[.]$) of the complex envelope of the RF pass band signal after up-conversion. In practice situations the bandwidth of the base band signal assumed BW hereinafter is much less that the carrier frequency *fc*.

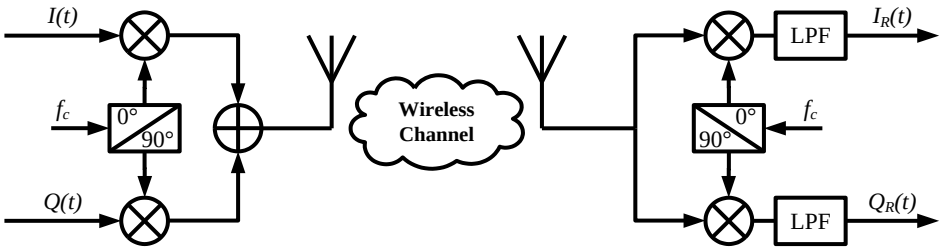

Figure 3.1 A typical wireless link

The radio channel is modeled as a linear time invariant system; however, due to the different multipath waves which have propagation delays which vary over different spatial locations of the receiver, the impulse response of the linear time invariant channel should be a function of the time, *t*, and the position of the receiver, *d*, in such case, the channel can be described by *h(d,t)*.

The pass band signal at the mobile receiver can be expressed as

$$\tilde{s}_R(d,t) = \tilde{s}(t) \otimes h(d,t) \qquad (3.3)$$

In case of stationary receiver the above equation can be reduced to

$$\tilde{s}_R(t) = \tilde{s}(t) \otimes h(t,\tau) = \int_{-\infty}^{t} \tilde{s}(t)h(t-\tau)d\tau \qquad (3.4)$$

The received baseband signal can be obtained following a frequency down conversion and channel equalization of the received pass band signal as follows

$$
\begin{aligned}
&s_R(t) = (\tilde{s}_R(t)e^{-jw_c t}) \otimes h^{-1}(t,\tau) \\
&= \tfrac{1}{2} A_R(t)\cos\varphi_R(t) + \tfrac{1}{2} A_R(t)\cos\varphi_R(t)\cos 2w_c t - \tfrac{1}{2} A_R(t)\sin\varphi_R(t)\sin 2w_c t \\
&+ \tfrac{1}{2} jA_R(t)\sin\varphi_R(t) - \tfrac{1}{2} jA_R(t)\sin\varphi_R(t)\cos 2w_c t - \tfrac{1}{2} jA_R(t)\cos\varphi_R(t)\sin 2w_c t
\end{aligned} \tag{3.5}
$$

and the high frequency components ($2\omega_c t$) are filtered out using low pass filters shown in Figure 3.1. The I/Q component of the received base band signal can be expressed as

$$I_R(t) = A_R(t)\cos\varphi_R(t) \;\; and \;\; Q_R(t) = A_R(t)\sin\varphi_R(t) \tag{3.6}$$

3.2 Sampling theory and reconstruction

At the receiver end of the communication system, the RF signal are decomposed into their respective I and Q baseband components. A continuous time domain signal *x(t)* should be sampled such that the signal can be reconstructed and no information is lost. Using ADCs, the continuous time domain signal is converted to a discrete time domain signal *x[n]* through a uniform sampling process taking at sampling period *Ts*, and their relation is *x[n]=x(nTs)*.

Discrete time sampling affects the resolution of the final time domain signal being processed. Consider a sine wave operating at 200 Hz, and continuous time domain signal representation is shown in Figure 3.2a. Using a sampling frequency of 10 kHz, the sine wave is still visible in Figure 3.2b. However, using a sampling rate of 2 kHz as in Figure 3.2c results in a less accurate representation of the sine wave.

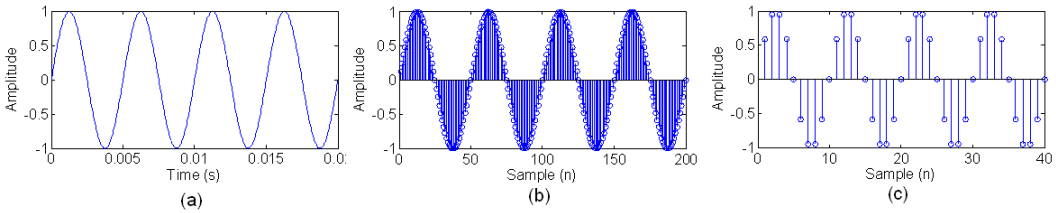

Figure 3.2 Time domain representation of (a) 200 Hz continuous sine wave (b) sampled at 10 kHz and (c) sampled at 2 kHz

However, uniform or periodic sampling presents a frequency domain ambiguity when the original signal frequency has to be obtained. Consider the continuous time-domain sinusoidal signal defined as

$$x(t) = \sin(2\pi f_c t) \tag{3.7}$$

And then

$$x(n) = \sin(2\pi f_c n T_s) \tag{3.8}$$

Equation (3.8) defines the value of the *n*th sample of *x(n)* sequence to be equal to the original sine wave at the time instant nt_s. Since two values of a sinusoidal signal are identical if they are separated by an integer multiple of 2π radians, equation (3.8) can be rewritten as

$$x(n) = \sin(2\pi f_c nT_s) = \sin(2\pi f_c nT_s + 2\pi m) = \sin(2\pi(f_o + \frac{m}{nT_s})nT_s) \qquad (3.9)$$

If m is an integer multiple of *n*, $m=nk$, we can rewrite equation (3.9) as

$$x(n) = \sin(2\pi(f_o + \frac{k}{T_s})nT_s) \qquad (3.10)$$

Being $f_s=1/T_s$, equations (3.8) and (3.10) can be equated as

$$x(n) = \sin(2\pi f_c nT_s) = \sin(2\pi(f_o + kf_s)nT_s) \qquad (3.11)$$

Therefore, f_c and (f_c+kf_s) factors equal, the implication of equation (3.11) being critical because it means that an *x(n)* sequence represents a sine wave of f_c Hz and f_c+kf_s Hz as well. These ambiguities must be taken into account in all practical signal processing algorithms, and they can also be used to our advantage, as described in section 3.3.

On the other hand, the discrete time signal *x[n]* can be viewed as a multiplication of the continuous wave function *x(t)* with a train of impulse functions [3.2]. The sampled version of the signal can be expressed as

$$x_S(t) = x(t)\delta_T(t) = \sum_{n=-\infty}^{\infty} x(nT_S)\delta(t - nT_S) \qquad (3.12)$$

The impulse train can be further expressed as a Fourier series

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_S) \xleftrightarrow{\Im} \omega_S \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \qquad (3.13)$$

where $\omega_s=2\pi/T_s$. Since a multiplication in the time domain results in convolution in the frequency domain, the Fourier transform of the sampled signal, $X_S(\omega)$ in relation to the RF signal's Fourier transform, $X(\omega)$, is

$$X_S(\omega) = \frac{1}{2\pi} X(\omega) * \left[\omega_S \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \right] = \frac{1}{T_S} X(\omega) * \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \qquad (3.14)$$

Using the convolution property of the impulse function, the simplified version of the impulse-modulated signal becomes

$$X_S(\omega) = \frac{1}{T_S} \sum_{k=-\infty}^{\infty} X(\omega - k\omega_S) \qquad (3.15)$$

showing that the spectrum is replicated every ω_s.

Choosing a sampling frequency for a band limited signal[2] affects the reconstruction process. A band limited signal with total bandwidth (*BW*) is denoted in Figure 3.3. Once the continuous signal is represented by a sequence of discrete sample values, its spectrum takes a replicated form, with these replicas separated f_s. In other words, a continuous signal cannot be represented in a digital machine in its current band limited form.

For Figure 3.3a, the sampling frequency $f_s=1/T_s=\omega_s/2\pi$ is much larger than the bandwidth, and perfect reconstruction is possible because the infinite replications are not aliased. Similarly, for the case when $f_s=BW$ as in Figure 3.3b, the spectrums do not overlap, or alias, over each other and the signal can still be decoded properly. However, in Figure 3.3c, f_s is less than *BW*, and aliasing occurs over the signal. This aliasing corrupts the information in the signal and is unrecoverable.

The minimum sampling rate, or the Nyquist sampling rate, should be $f_s >= BW$ in order to correctly decode the signal. In practice, an *anti-aliasing* filter (LP filter) will be necessary before the analog-to-digital conversion in order to eliminate any energy signal located above *BW*/2 or below –*BW*/2 that would be folded over the band of interest.

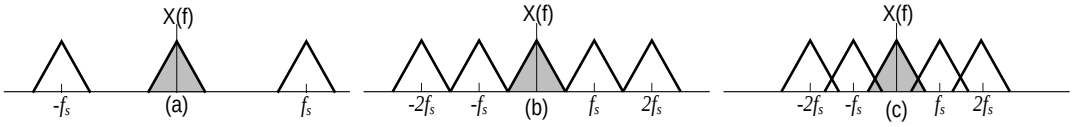

Figure 3.3 Sampling of a signal using (a) $f_s >> BW$ (b) $f_s = BW$ and (c) $f_s < BW$

3.3 Subsampling theory

3.3.1 Concept of subsampling

As mentioned before, moving the ADC closer to the antenna increases the flexibility of the receiver. However, this conversion just after the antenna would prohibitively increase the bandwidth and sampling frequency requirements of the ADC. Nevertheless, the bandwidth of a bandpass signal is usually a fraction of its center frequency, so that it is possible to subsample the signal (i.e., violating the Nyquist condition) avoiding aliasing between replicas.

Subsampling is the process of sampling a signal with a frequency lower than twice the highest signal frequency, and higher than the signal bandwidth *BW*. Using an ideal S&H device with sampling frequency f_s will generate harmonics at

[2] From a practical standpoint, the term *band-limited signal* merely implies that any signal energy outside the range [-*BW*/2,*BW*/2] is below the sensitivity of the system.

f_s, $2f_s$...mf_s, where m is an integer. In the case for Figure 3.4a, a bandpass RF signal is centered at f_c, while the m^{th} closest harmonic generated by the S&H and lower than f_c is k, where $k = floor(f_c/f_s)$. The replicas of the signal that are generated by the S&H exist at $-mf_s + f_c$, while the mirrored versions replicas exist at $(m + 1)f_s - f_c$. Figure 3.4b shows these replicas, and the signal replica within the [0-f_s/2] range (centered at $f_{if}=f_c-kf_s$) can be used to extract the original RF signal.

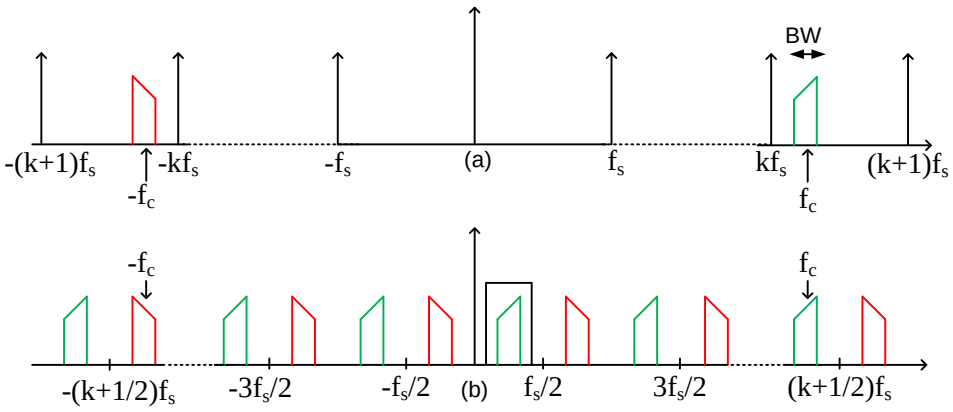

Figure 3.4 Illustration of the concept of subsampling: (a) Frequency domain representation of the RF passband input signal along with the subsampling frequency and S&H harmonics and (b) signal replicas following subsampling process when selecting $f_s=(f_c-f_{if})/k$ and $f_s>BW$

3.3.2 Selecting the sampling frequency

This section provides the method to select the optimal sampling frequency (f_s) for a given signal bandwidth (BW) and carrier frequency (f_c). Usually, the minimal sampling frequency is determined by the Nyquist Theorem: $f_s>2(f_c+BW/2)$. However, for a bandpass signal a sampling frequency lower than the Nyquist frequency can be selected if equation (3.16) still holds [3.3]:

$$2(f_c - BW/2)/(m-1) > f_s > 2(f_c + BW/2)/m \qquad (3.16)$$

where m is the number of replicas of the signal spectrum in the range [0, f_c-$BW/2$], and lies between 1 and $floor((f_c+BW/2)/BW)$. An appropriate value is $f_s=4f_c/m_{odd}$ which produces a replica at $f_s/4$ and sometimes it is called "optimal" sampling frequency. Using an odd integer m_{odd} ensures that the signal is at $f_s/4$, while m_{even} generates the low frequency alias of the signal at $3f_s/4$.

As an example, for a given input signal at 1070 MHz, with a signal bandwidth equal to 20 MHz, Table 3.1 shows its first ten valid ranges and its first ten optimal sampling frequencies.

On the other hand, an example that illustrates the convenience of sampling at $4f_c/m_{odd}$ can be observed in Figure 3.5, which shows the output spectrum when an input signal at 1070 MHz is sampled at f_s of 475.56MHz (Figure 3.5a) and at nearby frequency of 480 MHz (Figure 3.5b). It can be seen how the second order

harmonic at 237.78 MHz is placed further from away the desired signal in the case of Figure 24a compared with Figure 3.5b (at 220 MHz). Therefore, sampling at $4f_c/m_{odd}$ results in a larger subsampling frequency bandwidth and relaxes the filtering requirements after the S&H. As f_s, f_c and f_{if} are all directly related, there are bandwidth and frequency tradeoffs when selecting the subsampling frequency.

Table 3.1 Valid sampling ranges and optimal sampling frequency for an input signal at 1070 MHz and signal bandwidth equal to 20 MHz

Upper Limit (MHz)	Lower limit (MHz)	Optimal frequency (MHz)
2040	1120	1462.7
1020	746.7	856
680	560	611.4
510	448	475.6
408	373.3	389.1
340	320	329.2
291.4	280	285.3
255	248.9	251.8
226.7	224	225.3
212	196.4	203.8

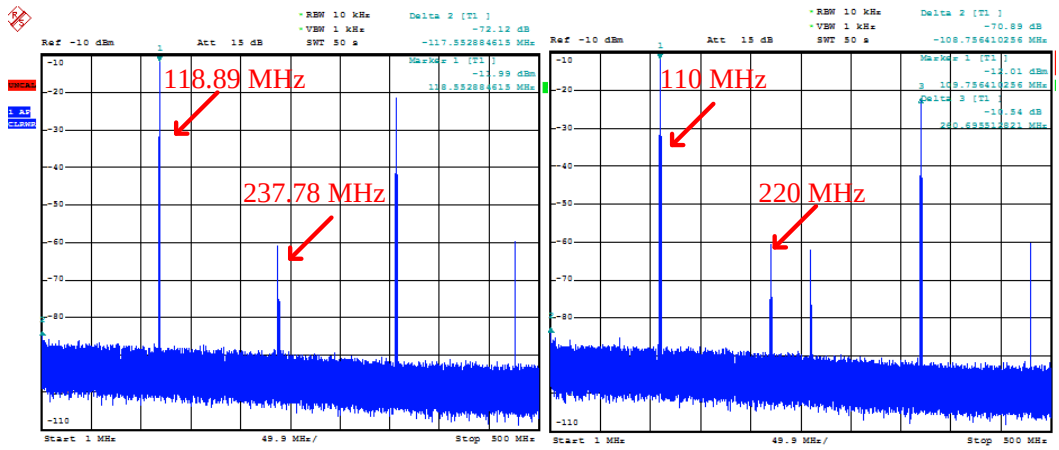

Figure 3.5 Output spectrum of the subsampler when the 1070 MHz RF signal is subsampled at a f_s of (a) 475.56 MHz (m_{odd}=9 and f_{if}=118.89 MHz) and (b) 480 MHz (m_{odd}=9 and f_{if}=110 MHz)

Another option in order to relax the ADC requirements could be to place the replica at a lower frequency. However, in practice, high performance ADCs are *fine-tuned* during design and manufacture to ensure maximum linearity at frequency, their use at lower frequencies not being recommended. Moreover, to sample close to the limits of the valid range could not be prudent because the analog band pass filters have non idealities and sample rates at the clock generator can present instabilities. Therefore, in these cases it would be convenient to consider a band guard be added to the signal bandwidth [3.4].

Finally, there is a case when subsampling is not possible. If a continuous bandpass signal's lowest frequency is less than the bandwidth, we have a not permissible situation. This condition is shown in Figure 3.6 where f_c-BW<BW. There is no way to fold any spectral replicas between this lowest frequency component and DC. In this case, it is only possible to sample the signal meeting Nyquist criteria, i.e., using a sample rate of at least twice the highest frequency component, i.e., $f_s > 2(f_c+BW)$.

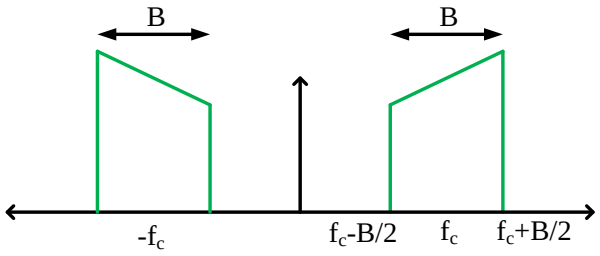

Figure 3.6 Continuous signal spectrum where subsampling is not posible because f_c-BW<BW

3.4 Non idealities in subsampling

A general scheme for a subsampling receiver is shown in Figure 3.7. It deserves to be mentioned that this receiver is very simple, especially if it is compared to the conventional heterodyne architecture. However, as the S&H processes high frequency signals, its requirements are much more restrictive than those expected from the signal bandwidth. The main non-idealities to be considered in the S&H are jitter and folded thermal noise and will be described in the sub-sections.

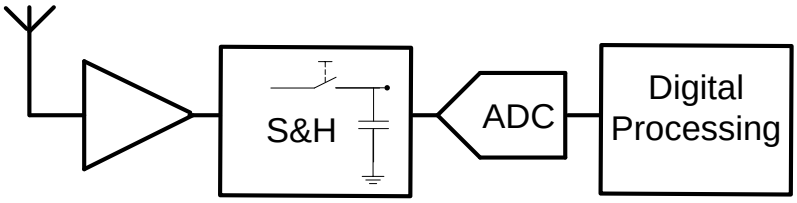

Figure 3.7 Subsampling receiver scheme

3.4.1 Jitter and phase noise

3.4.1.1 Phase noise

Clock jitter is an important limitation in the data acquisition systems at high signals frequencies because leads to sampling time uncertainly. Jitter is the deviation of the reference edges of the clock signal with respect to their ideal position in time. In this chapter we will consider this deviation as a random noise. As shown in Figure 3.8, a random error τ_n from the nominal sampling time instant t_n causes a random error $\varepsilon_\tau(n)$ in the amplitude of the sampled signal [3.5]. This effect can be seen as an addition of noise to the output signal, resulting in a degradation of the output Signal-to-Noise Ratio (SNR).

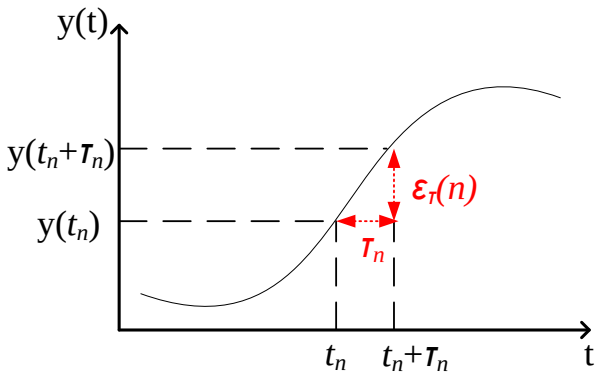

Figure 3.8 Concept of jitter

The amplitude error (v_{error}) is proportional to the derivative of the input signal [3.5,3.6]:

$$v_{error} = \Delta t \frac{dv_{in}}{dt} \tag{3.17}$$

With a jitter value of Δt. For a sine wave of frequency f_{in} and amplitude A_{in}, the maximum error is [3.5,3.6]:

$$v_{error\_\max} = \Delta t A_{in} 2\pi f_{in} \tag{3.18}$$

There are two main sources of jitter noise, the phase noise associated to the clock reference and the aperture jitter of the S&H. The aperture jitter of an S&H implemented with a MOS transistor is signal-dependent, as the transistor threshold voltage depends on the input signal. Concerning the system clock, there are two primary mechanisms that cause jitter: the thermal noise and the coupling noise. The latter can be caused by crosstalk and/or ground loops within, or adjacent to, the area of the circuit. Special care has to be taken designing the power lines in the data acquisition board that will be described in Chapter 3.

In a first order approach, these two sources of jitter noise can be considered as uncorrelated Gaussian stochastic processes, each one with a particular standard deviation. Being Δt_{rms} the standard deviation of jitter (or root mean square), which usually defined as a percentage of the sampling period, the sampling error in equation (3.17) can be re-written as [3.5]:

$$\sigma(v_{error}) = \Delta t_{rms} \sigma(dv_{in}/dt) = \Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}} \tag{3.19}$$

where $\sigma()$ is the standard deviation.

Therefore, the resulting SNR on the sampled signal is then [3.5]:

$$SNR_{jitter} = 20\log\left(\frac{A_{in}/\sqrt{2}}{\Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}}}\right) = -20\log(\Delta t_{rms} 2\pi f_{in}) \tag{3.20}$$

This approximation will be true if $2\pi f_{in}\Delta t_{rms} << 1$, otherwise the general expression for the SNR due to the uncorrelated random jitter noise for a sinusoidal input signal can be expressed as follows [3.7,3.8]:

$$SNR_{jitter} = 20\log\left(\begin{cases} 1/4\pi^2 f_{in}^2 \Delta t_{rms}^2 : 2\pi\ f_{in}\Delta t_{rms} << 1 \\ 1/2(1-e^{-2\pi^2 f_{in}^2 \Delta t_{rms}^2}) : otherwise \end{cases}\right) \tag{3.21}$$

The expression of SNR for $2\pi f_{in}\Delta t_{rms} << 1$ is valid for all jitter distributions while the other SNR expression only applies to a random jitter with Gaussian distribution $N(0, \Delta t_{rms})$ [3.7]. Moreover, small jitter noise can be approximately

regarded as sampled Additive White Gaussian Noise (AWGN) while for large jitter, this assumption is not valid anymore.

Note that the SNR is degraded when the input frequency increases. This SNR will be added to the SNR in the analog-to-digital conversion stage (SNR_{ADC} in equation (3.22) [3.5]), i.e., the degradation caused by thermal noise and quantization noise.

$$SNR_{Total} = -20\log\sqrt{10^{-\frac{SNR_{ADC}}{10}} + 10^{-\frac{SNR_{jitter}}{10}}} \tag{2.22}$$

In the particular case of subsampling, jitter noise is an important limitation due to high input frequencies are processed. Thus, in order to validate this theoretical study, jitter noise is simulated using typical values for receivers subsampling based, i.e., the input frequencies in the GHz range, the sampling frequencies around 500 MHz (which is a typical limit for high resolution commercial ADCs, as is described in Chapter 3), and a 20 MHz signal bandwidth, due to how it is a typical value for many communications standards and is used to characterize experimentally the data acquisition board proposed in Chapter 3.

Therefore, using these values, jitter noise has been simulated (using MATLAB) as a stochastic process with average equal to zero and standard deviation equal to Δt_{rms}. Figure 3.9 [3.9] illustrates the maximum admitted jitter (Axis X) to obtain a concrete SNR (Axis Y) for three different input frequencies (1, 2 and 4 GHz) sampling at the optimum frequency (from equation $f_s=4f_c/m_{odd}$) immediately lower than 500 MHz. In this example, the jitter noise is integrated in a signal bandwidth equal to 20 MHz and it can be observed how the SNR will decrease around 6 dB each time the input frequency is doubled, as can be predicted by equation (3.21).

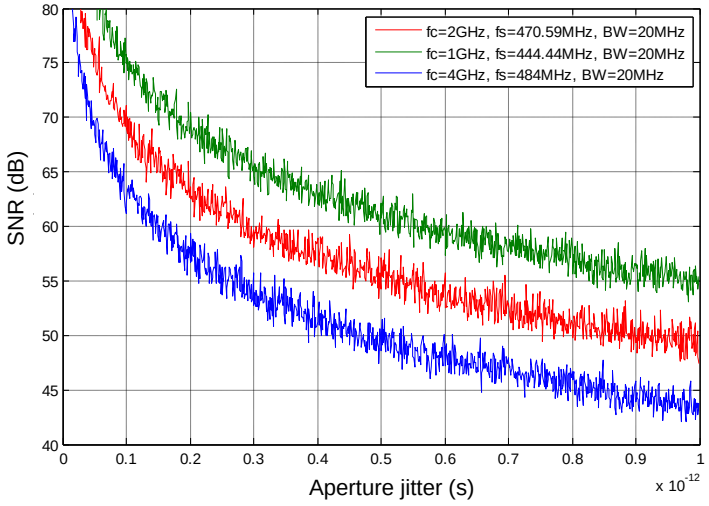

Figure 3.9 SNR requirements as a function of the jitter for different input frequencies

3.4.1.2 Phase noise

This traditional method, based on equation (3.22) to obtain the SNR as a function of clock jitter and signal frequency, has some limitations, as the assumption of a full scale scenario. Although this situation may happen in some applications, most commonly the input signal energy is spread over some bandwidth. In these cases it is more realistic to study the jitter effect from the spectrum domain.

Since the spectrum of jitter is very difficult to measure directly, the most common method to study its effect is by measuring the phase noise, which is the most widely employed parameter to compare between different clock sources and oscillators.

The phase noise is defined as the frequency domain representation of the phase modulation of the clock signal due to the jitter. The clock signal being a sine wave of frequency f_s [3.5]:

$$v_{clock} = A\sin(2\pi f_s(t + \Delta t(t))) = A\sin(2\pi f_s t + \varphi(t)) \qquad (3.23)$$

where $\varphi(t)$is the phase noise in the time domain. Assuming $\varphi(t)$ has small variation around zero, equation (3.23) can be written as [3.5]:

$$v_{clock} \cong A\sin(2\pi f_s t) + A\cos(2\pi f_s t)\varphi(t) \qquad (3.24)$$

The second term of this expression is the additive noise due to the phase modulation. Since the phase noise appears multiplied by a cosine in the above time domain expression, in the frequency domain the spectrum of the phase noise, $\Phi(f)$, is convolved with the noise-free clock and appears as sidebands around its center frequency. This noise is usually represented as $L(f)$ (single-sideband phase

noise power spectrum) and is equal to the noise power spectral density per Hertz at the frequency f_s+f normalized by the clock or oscillator signal power $A^2/2$. It is called single-sideband because only one side of the noise power is taken into account; hence it includes only half the noise energy. Thus [3.5]:

$$L(f) = 10\log\left(\frac{1}{2}\Phi^2(f)\right)$$
$$\Phi(f) = \sqrt{2 \cdot 10^{L(f)/10}} \tag{3.25}$$

L(f) is represented in dBc/Hz. Figure 3.10 [3.1] shows an example of phase noise for a clock frequency equal to 1.9 GHz, which is a typical frequency range for the S&H clock source in the implemented systems, as it will be detailed in the following sections. These experimental measurements show a phase noise of around -95 dBc/Hz, -110 dBc/Hz and -125 dBc/Hz at 100 Hz, 1 KHz and 10 KHz respectively.

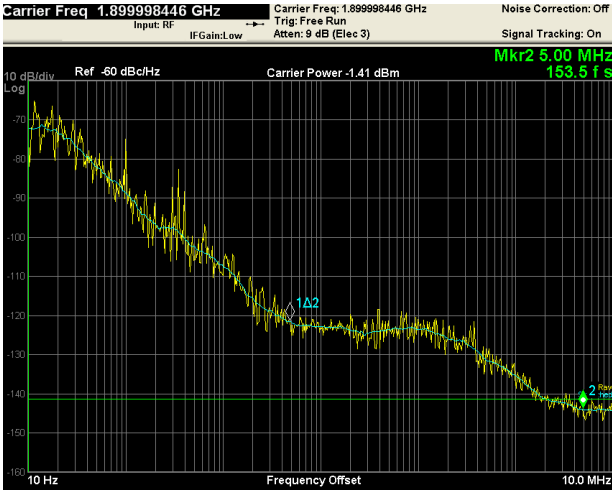

Figure 3.10 Phase noise for a clock frequency equal to 1.9 GHz

From equation (3.23), the relationship between $\varphi(t)$ and jitter is [3.5]:

$$\varphi(kT_s) = 2\pi f_s \Delta t(kT_s) \tag{3.26}$$

That is equivalent to referencing jitter to the clock period. In the frequency domain, where the clock phase noise is most commonly represented, it is then equal to the clock jitter scaled by $2\pi f_s$ [3.5]:

$$\Phi(f) = 2\pi f_s \Delta T(f) \tag{3.27}$$

Therefore, we have the following expression to obtain the total jitter from phase noise [3.5]:

$$\Delta t_{rms} = \frac{1}{2\pi f_s}\sqrt{\int_0^\infty \Phi^2(f)df} = \frac{1}{2\pi f_s}\sqrt{2\int_0^\infty 10^{L(f)/10}df} \tag{3.28}$$

Finally, the SNR degradation can be calculated from the phase noise measurements as well. Assuming a sine wave as input, [3.5,3.10] calculates the expression for the voltage sampling error due to the jitter in the frequency domain:

$$V_{error}(f) = 2\pi f_{in}\frac{A_{in}}{\sqrt{2}}\Delta T(f - f_{in}) \tag{3.29}$$

If we substitute (3.27) in (3.29) the following expression is obtained:

$$V_{error}(f) = \frac{f_{in}}{f_s}\frac{A_{in}}{\sqrt{2}}\Phi(f - f_{in}) \tag{2.30}$$

In order to obtain the in-band noise that will affect the SNR, equation 30 over the system pass band (f_{min}, f_{max}), employing (3.25), results[3]:

$$SNR_{jitter} = 10\log\left(\frac{A_{in}^2/2}{\int_{f_{min}}^{f_{max}} V_{error}^2(f)df}\right) = -20\log\left(\frac{f_{in}}{f_s}\sqrt{\int_{f_{min}}^{f_{max}} 10^{L(f-f_{in})/10}df}\right) \tag{3.31}$$

On the other hand, when an oscillator is used as clock generator it is necessary take account that its phase noise is composed of two main regions as illustrated in Figure 3.11 [3.5,3.11,3.12]. The larger region is due to the thermal noise whose effect is similar to a frequency modulation, generating sidebands that fall inversely proportional with frequency offset, in a slope of -20 dBc/dec. At low frequency offsets, there is a region with a slope of -30 dB/dec due to up-conversion of 1/f noise. The corner frequency between two regions, f_x, is dependent on the oscillator implementation. Finally, the flat curve is usually called "white" phase noise [3.11] and the dashed curve illustrates the combination of the described curves.

[3] Notice that there is no factor 2 because the integration is over only one sideband.

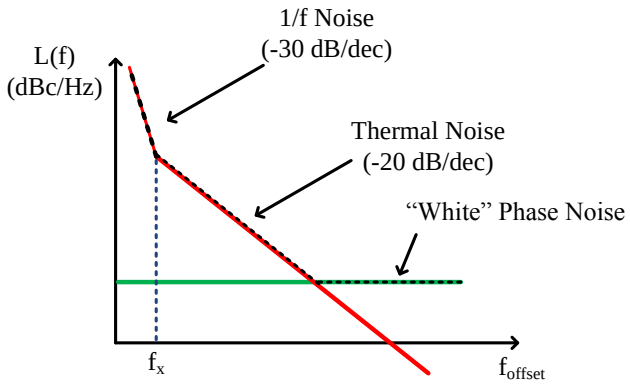

Figure 3.11 Phase noise of an oscillator

However, in systems designs requiring low jitter for different sampling clocks, as described in this thesis, the costs of several low phase noise dedicated crystal oscillators are usually prohibitive. An alternative solution is to employ a phase-locked loop (PLL) in conjunction with a voltage-controlled oscillator (VCO) to "clean up" a noisy system as shown in Figure 3.12. Instead the VCO, other alternative is to use a voltage-controlled crystal oscillator (VCXO), which typically gives a lower phase noise. The PLL will tend to reduce the "close in" phase noise using a narrow band loop filter, and the "white" phase noise by following the PLL output with an appropriate bandpass filter.

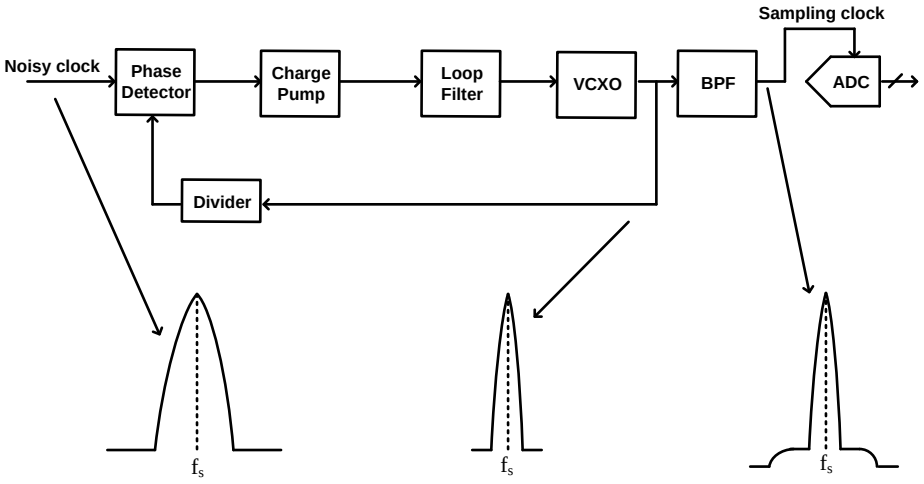

Figure 3.12 Block diagram of a PLL

The improvement of the phase noise at the output of a PLL is given in equation (3.32) [3.5,3.13], considering a phase noise of the input clock reference equal to $\Phi_{in}(f)$ and a phase noise of the VCO equal to $\Phi_{VCO}(f)$. Although it is possible to observe how the PLL applies a gain over the phase noise of the input clock reference, M, equal to the ratio of output frequency to input frequency, its impact is low due to, typically, the input clock is coming from a crystal oscillator and, consequently, has a very low phase noise. Therefore, the effect of this amplification will impact the output phase noise only at very low offset frequencies.

$$\Phi_{out}(f) = \frac{M}{\sqrt{1+\frac{f}{f_{loop}}}}\Phi_{in}(f) + \sqrt{1+\frac{f}{f_{loop}}}\Phi_{VCO}(f) \qquad (2.32)$$

The VCO's phase noise is often relatively large and most of its energy is at low frequencies, as shown in Figure 3.11. The highpass transfer function of the PLL is therefore very convenient and effectively improves the overall phase noise performance[4].

The resulting phase noise spectrum at the output is illustrated in Figure 3.13 [3.5]. It is possible to observe how the VCO's phase noise will get filtered down by a steep 40 dB/dec slope below the PLL loop bandwidth. The input clock reference is relevant only at very low offset frequencies and the internal component (i.e., phase detector and charge pump) can become the dominant phase contribution below the PLL loop bandwidth. Finally, an oscillator can produce coupled noise from the supplies or the substrate. This noise is typically generated by the activity on chip and can produce spurs on the phase noise spectrum. Also a jittered clock can produce these interferences in the desired signal caused by the adjacent channel [3.14]. Therefore, the power density of these interferences will be larger with a higher jitter clock.

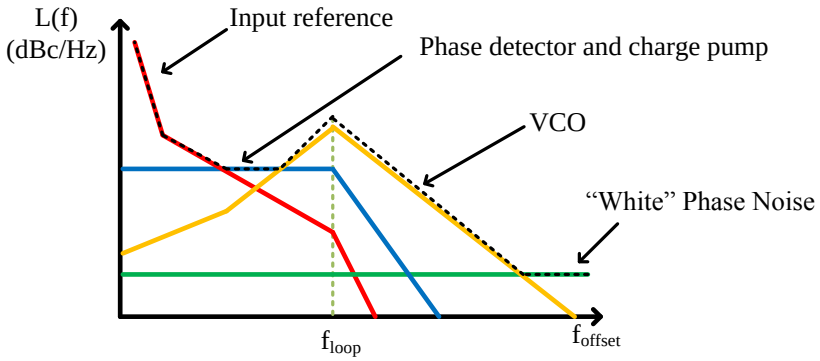

Figure 3.13 Phase noise of a PLL

3.4.2 Foded thermal noise

The other main non ideality of the systems based on subsampling is the folded thermal noise. Being the S&H modeled as shown in Figure 3.14a [3.7], this thermal noise is introduced by the switch and has a power spectral density (PSD) equal to $S_{in}(f)=4kTR_{on}$, where k is the Boltzmann constant, T is the absolute temperature and R_{on} the on-resistance of the switch. This noise is AWGN and will

[4] The PLL internal blocks, specially the phase detector, generate additional noise that is transferred to the output with a lowpass transfer function similar to the input clock reference.

be folded in the band of interest by the subsampling process, as is described in this section (Figure 3.14b [3.15]).

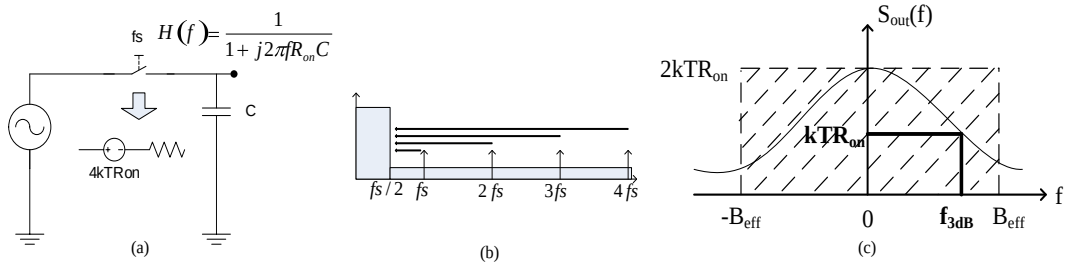

Figure 3.14 (a) Model of the S&H, (b) thermal noise folded in the band of interest and (c) effective noise bandwidth

R_{on} and C model a LP filter (Figure 3.14a) with transfer function $H(f)=1/(1+j2\pi fR_{on}C)$, whose 3-dB cutoff frequency is equal to $f_{3dB}=1/(2\pi R_{on}C)$. Considering the one-side representation of $S_{in}(f)$, the output PSD will be [3.7]:

$$S_{out}(f)=S_{in}(f)\left|H(f)\right|^2=2kTR_{on}\frac{1}{1+4\pi^2 f^2 R_{on}^2 C^2} \tag{3.33}$$

Being the total noise power (by a two-sides representation):

$$P_{out}=\int_{-\infty}^{\infty}S_{out}(f)df=\frac{kT}{C} \tag{3.34}$$

For modeling purposes, the output noise can be considered to be a Gaussian thermal noise filtered by a brick-wall filter of bandwidth equal to B_{eff} (i.e., noise bandwidth, see Figure 3.14c) [3.7]:

$$B_{eff}=\frac{1}{4R_{on}C}=\frac{\pi}{2}f_{3dB} \tag{3.35}$$

Therefore, the power noise can be rewritten as follows [3.7]:

$$P_{out}=\frac{kT}{C}=2kTR_{on}\cdot(2B_{eff}) \tag{3.36}$$

On the other hand, the SNR in $[-B_{eff},B_{eff}]$ is defined as [3.3]:

$$SNR=\frac{P_s}{N_i+(m-1)N_o} \tag{3.37}$$

Where P_s is the signal power spectral density, and N_i and N_o are the in-band and the out-of-band noise spectral power densities, respectively. Then, the degradation of SNR in decibels is:

$$SNR_{\deg} = 10\log\left(1+\frac{(m-1)N_o}{N_i}\right) \tag{3.38}$$

As $2B_{eff}=mf_s$, if m=1 the Nyquist Theorem is met and the SNR is not affected by the folded noise. On the other hand, from equation (3.37), if m>1, and assuming $N_i=N_o=N$:

$$SNR = \frac{P_s}{mN} = \frac{P_s}{N(2B_{eff}/f_s)} \tag{3.39}$$

Therefore, the out-of-band folded noise reduces the SNR by a factor $2B_{eff}/f_s$, the entire wideband noise being folded inside the band of interest. From equation (3.38), we can observe how the noise will be decreased around 3 dB when the sampling frequency is doubled.

It is convenient to select the largest sampling frequency among the set of possible sampling frequencies set by the digital signal processing block specifications. From now on, this one will be termed as the "optimal" sampling frequency (from equation $4f_c/m_{odd}$).

This effect was corroborated experimentally as shown in Figure 3.15 [3.1]. This figure illustrates how the folded noise increases when it is employed a lower optimal sampling frequency for an input signal centered at 1473 MHz.

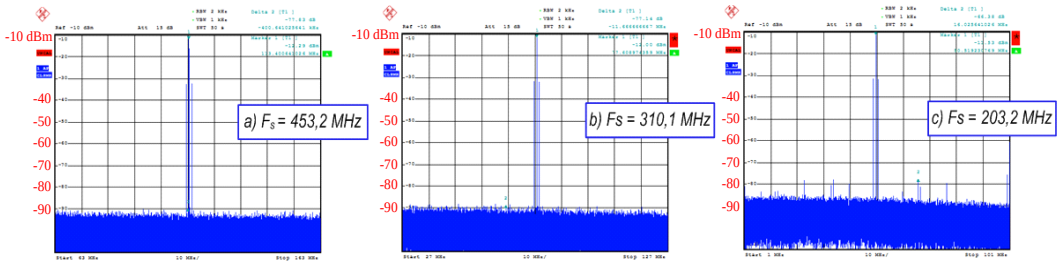

Figure 3.15 Thermal noise effect depending on the sampling frequency

Moreover, an additional advantage of using a higher sampling frequency is that the requirements of the band pass anti-aliasing filter are relaxed. This is illustrated in Figure 3.16 [3.8], where we can observe how the nearest unwanted replica is placed further away from the desired signal when the sampling frequency is increased.

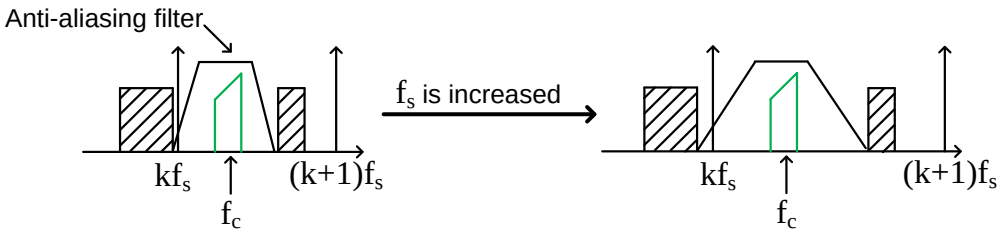

Figure 3.16 Bandpass anti-aliasing filtering requirements in subsampling

3.5 Architectures and applications of subsampling receivers

Firstly, in this section two of the most common architectures based on subsampling are compared in terms on complexity, re-configurability and linearity. Secondly, this section describes some examples of subsampling applications different to multi-standards and SDR receivers.

3.5.1 Subsampling architectures

The most common subsampling architecture is as illustrated in Figure 3.7, i.e., sampling the RF input directly by the S&H in order to obtain the IF replica that will be converted to digital. As described in Chapter 1, an intermediate alternative, between this scheme and the mixer based architecture, is to do a previous translation to IF, as shown in Figure 3.17.

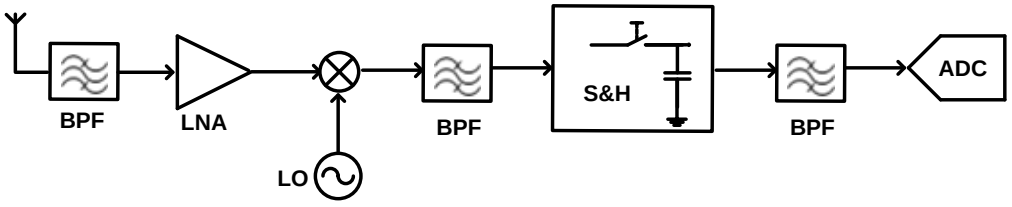

Figure 3.17 IF subsampling receiver

This concept is called IF-subsampling [3.16], or simply IF-sampling. Although this architecture will relax the S&H requirement in comparison with the RF-subsampling scheme (Figure 3.7), the simplicity and re-configurability proper of receivers based on subsampling will decrease. About linearity, RF subsampling receivers may suffer from distortion problems more than IF subsampling receivers because all the gain is realized at RF frequency and high gain with high linearity is more difficult to achieve at high frequencies, due to the increased effect of parasitic and the lower intrinsic gain of transistors at high frequencies. However, IF subsampling receivers may have a higher distortion performance than RF subsampling receivers due to the use of a mixer that may introduce additional distortion products. Including all these factors, IF-subsampling architectures can be considered an intermediate step toward SDR paradigm.

3.5.2 Subsampling applications

One of the most common applications based on subsampling is its utilization in ΣΔ modulators [3.17,3.18]. ΣΔ ADCs have been extensively studied because they are robust against circuit imperfections, have an inherent linearity due to the use of single-bit quantizers and can achieve high resolution with lower power consumption.

A continuous-time bandpass ΣΔ modulator is illustrated in Figure 3.18 [3.18]. The center frequency f_{in} is tuned to $(N\text{-}1/4)f_s$, where f_s is the subsampling rate. Since the subsampling process is inside the loop the folded noise will be reduced by the continuous-time bandpass loop filter.

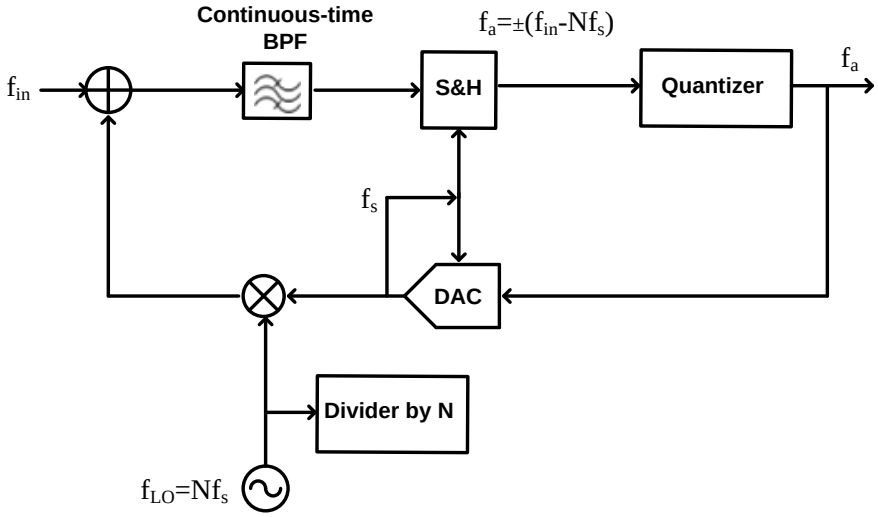

Figure 3.18 Block diagram of a continuous-time bandpass ΣΔ modulator

ΣΔ modulators provide noise shaping on the quantization noise through the feedback loop, SNR performance at the output being increased. Making use of the feedback loop, a ΣΔ modulator provides noise shaping to both the quantization noise and the folded noise due to subsampling.

These modulators can be used for multi-standards applications. [3.17] presents a RF subsampling down-conversion front-end based on continuous time bandpass ΣΔ modulator with sine-shaped feedback DAC, which is used in order to reduce the timing jitter, as described in [3.19]. Figure 3.19 illustrates a block of diagram of the proposed multi-standard receiver based on subsampling ΣΔ modulation. The RF analog block is composed by an antenna, a tunable multiband RF bandpass filter to select the desired wireless communication standard and a LNA.

Using an ADC based on subsampling ΣΔ modulator, the RF bandpass signal is directly sampled and down-converted to IF without using mixers. The

advantage of using a continuous ΣΔ modulator in front end is to reduce the noise of subsampling process without increasing the power consumption of the ADC.

Moreover, using the continuous-time filter of the modulator the requirements of the anti-aliasing filter before the modulator will be less restricted. Otherwise, with the purpose of translating the different RF bands to same IF, this implementation selects a sampling frequency such as the frequency distance between the optimal IF ($f_s/4$) and the IF of each RF band is minimal.

The ΣΔ modulation (whose block diagram is similar as shown in Figure 3.18) is followed by a digital programmable decimation filter in order to remove the unwanted components frequency and reduce the oversampled rate to the Nyquist rate of the channel. This decimation filtering is implemented by using multiple stages, each stage being designed for the desired band of each standard.

Finally, each standard is down-converted to baseband through the I-Q paths and controlled by a numerical oscillator. After a LP filtering stage the baseband signal is digitally processed.

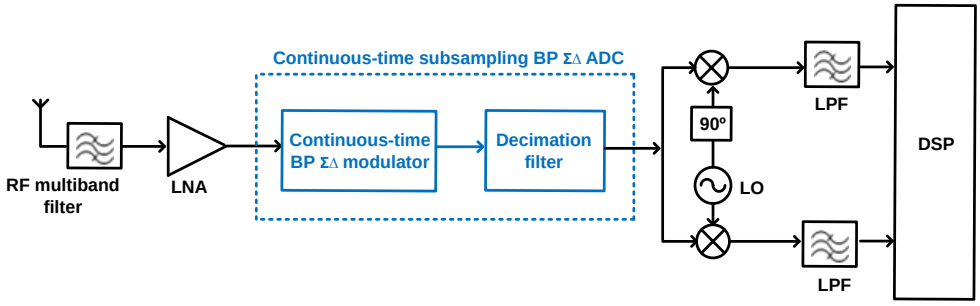

Figure 3.19 RF subsampling multi-standard ΣΔ receiver

Another interesting application based on subsampling is the impulse radio architectures used in ultra wideband (UWB) radio [3.20,3.21]. UWB presents a high variety of applications, including imaging, surveillance, high-speed data communication and high-resolution location [3.22,3.23]. A common application that works in the 3.1-10.6 GHz band (with a minimum bandwidth of 500 MHz) is indoor communication, which has implementations in high speed short distances (less than 10 m) systems for wireless personal area network (WPAN), or in low data rate communications, such as sensor networks. [3.20] proposes to implement a low complexity 3.1-10.6 GHz UWB system which transmits passband pulses using a pulser and an antenna, and down-converts the received signal via subsampling.

A challenge of UWB is to fully exploit the features of the wideband radios for low power and low cost designs in order to increase the efficiency of narrowband systems. Therefore, a feasible alternative to implement these systems will be the subsampling architectures. In this case, the receiver chain will process non sinusoidal carriers, so called impulse radios.

Moreover, UWB has a relatively low received SNR, due to the signal transmission power is limited by regulations, a large in-band noise due to the wideband circuit noise and possible interferences. As a result, a UWB receiver requires only a moderate ADC resolution, i.e., 4-6 bits [3.19]. Thus, the quantization noise is more dominant than the folded thermal noise, being the subsampling receiver a very promising architecture for UWB. For the same reason, the jitter constraint will be much less stringent.

On the other hand, [3.21] presents a flexible subsampling receiver based on line spectrum estimation techniques, which are applied in the frequency domain in order to recover the position and the amplitude of the received pulses [3.24]. These pulses will be distorted by the transceiver antennas and the channel, being this pulse distortion very variable among the multipaths employed in these systems. Therefore, delay lines will be implemented in the analog domain in order to equalize the different paths. On the other hand, digital based receivers provide more flexibility and accuracy, but require ADCs sampling at Nyquist rate which are hardly realizable and highly power consuming. An architecture based on interleaved ADCs could be a feasible option but the area is increased and it requires appropriate techniques to compensate circuit mismatches between the parallel branches. As a result, a subsampling architecture is an alternative to implement this application because it provides the flexibility of a digital design without increasing the power consumption or area.

Moreover, some applications specifically oriented to multiband and non linear systems employ subsampling techniques. This section introduces a couple of examples which work in these scenarios. However, these applications will be studied in more detail in Chapter 4, due to the necessity of additional restrictions in order to avoid the overlapping between signals and harmonics.

Firstly, [3.25] presents a subsampling receiver for cognitive radio applications. The main utility of this multiband system, whose block diagram is illustrated in Figure 3.20, is to scan the wireless spectrum to know what slots in the whole spectrum are underutilized in order to be managed more efficiently and to able to be reused dynamically. This receiver presents the advantages proper of the subsampling based systems, such as, low complexity and flexibility, but there will be an additional challenge in order to avoid the overlapping between different slots when this spectrum is subsampled.

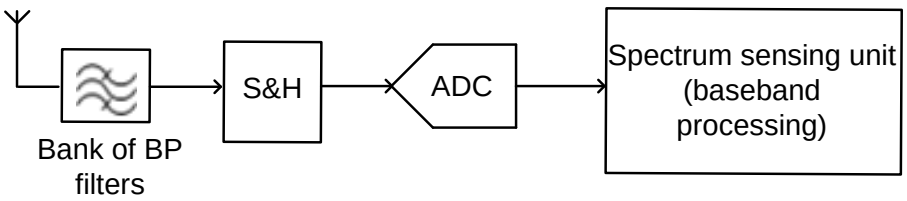

Figure 3.20 Subsampling based receiver for spectrum sensing

Secondly, an example of a subsampling application in a non linear scenario is presented in [3.26]. The proposed system consists of the implementation of a subsampling receiver in the feedback loop of a transmitter. This feedback loop is utilized to accomplish the digital pre-distortion (DPD) linearization process of the power amplifier [3.27,3.28], whose idea is illustrated in Figure 3.21.

This concept is based on extracting the behavioral model of the nonlinear transmitter, estimating its inverse behavior model, in order to pre-distort the digital baseband signal (previously to be transmitted) to compensate the extracted effects in the power amplifier. Therefore, since $g()=f^{-1}()$ in Figure 3.21, it is possible to obtain the input signal as $y=f(g(x))=f(f^{-1}(x))=x$.

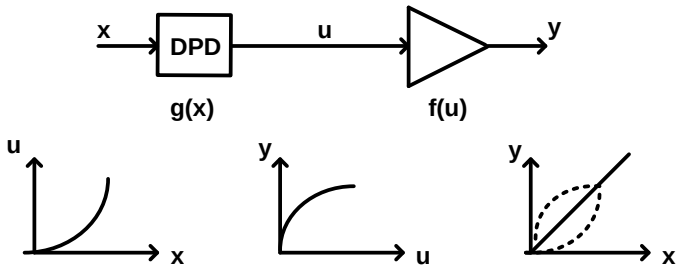

Figure 3.21 Digital pre-distortion idea

The concept behind the DPD technique is based on extracting the behavioral model of the nonlinear transmitter, estimating its inverse behavior model, in order to pre-distort the digital baseband signal (previously to be transmitted) to compensate the extracted effects in the power amplifier.

Since the power amplifier is the main source of nonlinearity, because its highest efficiency state is operating close to the maximum output power, a scheme as showed in Figure 3.22 will be necessary. This architecture implements a transmitter for dual-band applications. It is possible to observe how the baseband signals x_1 and x_2 are pre-distorted to obtain x_{pd1} and x_{pd2} by the digital block that implements the inverse function of the power amplifier. These signals are converted to analog domain and up-converted to RF and combined in order to feed the power amplifier and be transmitted. This RF signal will be coupled to a feedback loop that is composed by a subsampling receiver, i.e., a BP filter, an S&H and an ADC.

The subsampling receiver reduces the power consumption and the complexity in comparison with the typical feedback loops for linearization and it is employed to extract the IF signal which be digitally down-converted in order to obtain the baseband nonlinear signals y_1 and y_2. These baseband signals, besides x_{pd1} and x_{pd2}, will feed the digital analyze block in order to obtain the necessary coefficients that will be employed as inputs by the pre-distorted blocks, besides the input signals x_1 and x_2, in order to adjust the pre-distorters dynamically.

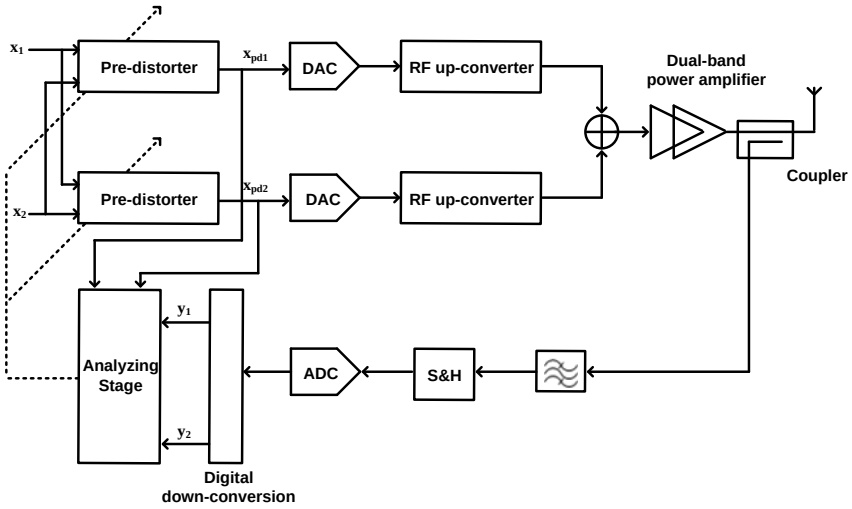

Figure 3.22 Dual-band digital predistortion with subsampled feedback loop

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CHAPTER 4

DATA ACQUISITION SYSTEMS BASED ON SUBSAMPLING FOR TESTING WIDEBAND MULTI-STANDARD RECEIVERS

CHAPTER CONTENTS

As described in Chapter 2, if a multi-standard receiver is implemented by stacking different receivers for different standards into a single receiver, the area and power consumption will be extremely high. Therefore, a properly designed multi-standard receiver must share the hardware resources and use tunable and programmable devices, reducing the area and power consumption, which is a very important approach for battery power devices. Otherwise, for multi-standard applications such as instrumentation or validation, the main constraint is the capability of covering the maximum number of standards as possible.

A data acquisition board based on subsampling for high performance low-cost multi-standard test equipment is presented in this chapter. Due to the necessity of flexible and low cost receivers in the test industry, the selected architecture is based on subsampling techniques. Previously, a state of the art study and an experimental evaluation at COTS level were performed in order to validate the design and determine the real specifications of the data acquisition system. With a signal bandwidth of 20 MHz it achieves 8.5 bit resolution for a programmable carrier frequency ranging from 0 up to 3.3 GHz, and more than 8 bit resolution up to 4 GHz. By a proper selection of the center frequency and signal bandwidth, the proposed board can be used to digitize the signal in most of present wireless standards. This design is intended to be part of a test system; that is, the input signal of the subsampling receiver is assumed to be filtered and free of interferences.

A last section describes the achieved improvement of the noise performance by using two clocking stages architecture. This approach allows the sampling frequency of the first stage to increase, resulting in a lower contribution of the first S&H to the total folded thermal noise. This section is structured in a first part dedicated to the theoretical study, where the expressions of the expected improvement are deduced, and a second part dedicated to the experimental validation of these techniques. Considering a signal bandwidth of 20 MHz, the improved data acquisition system achieves an ENOB of more than 9 bits for a programmable carrier frequency up to 2.9 GHz and 8 bits up to 6.5 GHz, presenting an improvement in the resolution of 0.5-1 bit. The chapter finalizes presenting a comparison with other implemented multi-standard receivers.

4.1 Data acquisition systems based on COTS

4.1.1 Choice of components

Since the data acquisition system is based on commercial devices, they will have to be chosen in order to minimize the effects of the main problems encountered using subsampling, i.e., jitter and folded thermal noise, as detailed in Chapter 2. These non idealities fix the specifications of the main building blocks of the system, i.e., the S&H and the ADC.

After a study on commercial components, we decided to use an external S&H before the ADC since an internal S&H bandwidth is limited to 3 GHz approximately with a resolution around 8 bits. However, when using an external S&H, it is possible to obtain a higher resolution for a wider bandwidth. This is a feasible alternative because the S&H can subsample the RF inputs covering a high analog bandwidth and the obtained IF replica can be converted to digital by a high resolution, intermediate frequency ADC.

After realizing a study of the state of the art, the chosen S&H is the Inphi 1821 TH [4.1], with the following features:

- Wider bandwidth (18 GHz), in order to cover most of wireless communication standards.
- Minimum aperture jitter (50 fs).
- Integrated noise over the first Nyquist band (clocking at 1 GHz) equal to 0.64 mV. This value is very similar to the other studied S&H from Hittite [4.2] or Teledyne [4.3].
- Wider frequency range (0-6 GHz) for 10-bit linearity.
- Although the maximum sampling frequency is equal to 2 GS/s, this S&H has the capability to sample at the interested frequency (around 500 MS/s) for this application.

This requirement (500 MS/s) is given by the maximum sampling frequency for commercial 10-bit A/D converters, since using a maximum sampling frequency is convenient in order to reduce the overlapping noise effects. Concretely, the A/D converter chosen is E2V AT84AS001 [4.4].

The rest of components will be described as they are utilized in the experimental characterization that is detailed in the following section.

4.1.2 Experimental results

4.1.2.1 S&H characterization

Since the most critical part is the S&H, due to its processing of high input frequencies, a characterization of this component was previously accomplished to characterize the whole system. Before that some discrete components such cables, baluns, DC-blocks or bias-tees necessary to measure the S&H features, were characterized in order to estimate parameters as loss insertion or unbalance performance which can affect the S&H characterization.

Figure 4.1 illustrates the S&H evaluation board [4.5] and some of these coaxial components (from the Minicircuits manufacturer [4.6]) employed in these experiments.

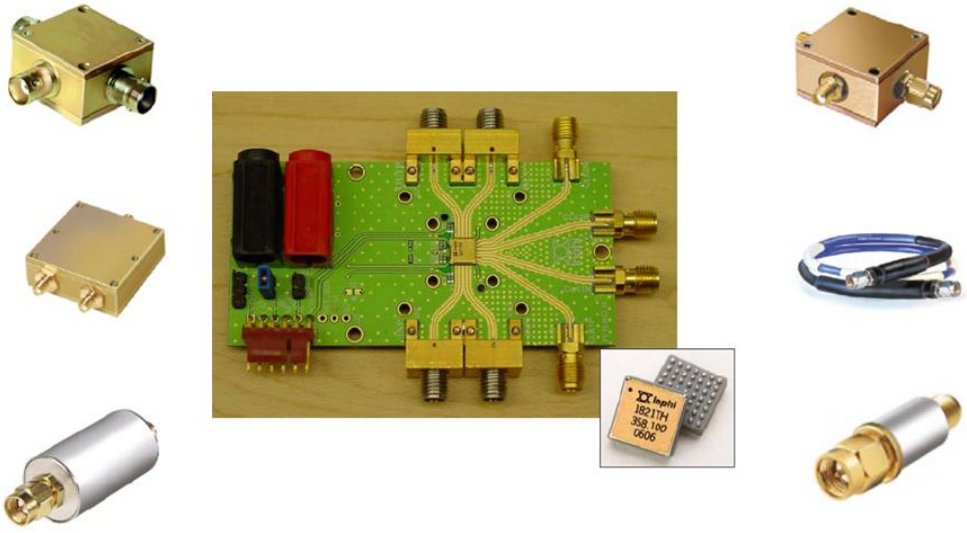


Figure 4.1 Used coaxial components

The S&H characterization has as objectives, firstly, to corroborate the data sheet specifications and, secondly, to prove the benefits of subsampling techniques and corroborate the theoretical study described in Chapter 2.

As an example, Figure 4.2 shows the THD measured at the S&H output for a 1.1-3.2 GHz input range, an input bandwidth of 20 MHz and an input amplitude equal to 0.5 V. In relation with the sampling frequency, two different cases were studied. Firstly, a sampling frequency fixed at 1 GHz was employed in order to be compared with the manufacturer specifications (given at 1 GHz as well). Secondly, the experiments were realized using a sampling frequency very close to the optimal subsampling rate immediately lower than 500 MHz[5] for each

[5] This restriction is given by the maximum sampling rate specification of the E2V AT84AS001.

characterized carrier input. We chose a sampling frequency not exactly equal to the sampling frequency in order to integrate the third order harmonics in the studied bandwidth, i.e., with the objective to avoid the overlapping between the desired signal and the third order harmonics, which happens when the optimal sampling frequency is utilized. Using this *approximated* sampling frequency (about 200-300 KHz from the optimal sampling frequency) we can be sure the third order harmonic will be folded inside the band of interest of 20 MHz.

It is possible to observe how the results on linearity are very similar independently from which sampling frequency clocks the S&H. Nevertheless, the THD obtained when the optimal sampling frequency is employed is slightly higher than clocking at 1 GHz, due to in the first case the harmonics can be maintained more separated from the desired signal, while in the second case the second order harmonics can be folded inside the band of interest.

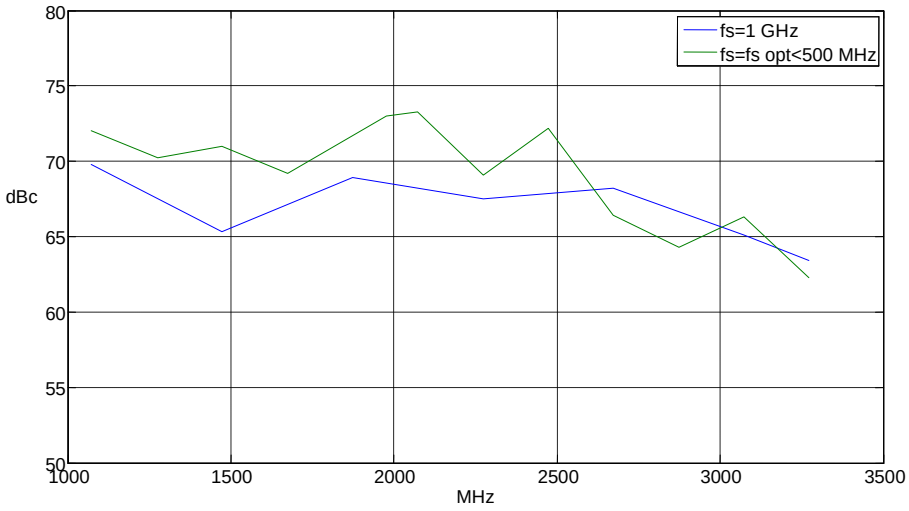


Figure 4.2 S&H THD for the input range 1.1-3.2 GHz

Comparing these results, sampling at 1 GHz, with the specifications given by the manufacturer we can observe very similar results of THD (see Figure 4.3), being around -70 dBc up to 3 GHz input frequency when the amplitude input signal is 0.5 V. However, the THD have been measured for a 20 MHz input bandwidth, but the data sheet does not give this information. Therefore, if the data provided by the manufacturer have been measured in the Nyquist band, our results can be considered worse than given in specifications. In any case, the linearity in our band of interest will be not a limitation to implement the subsampling receiver.

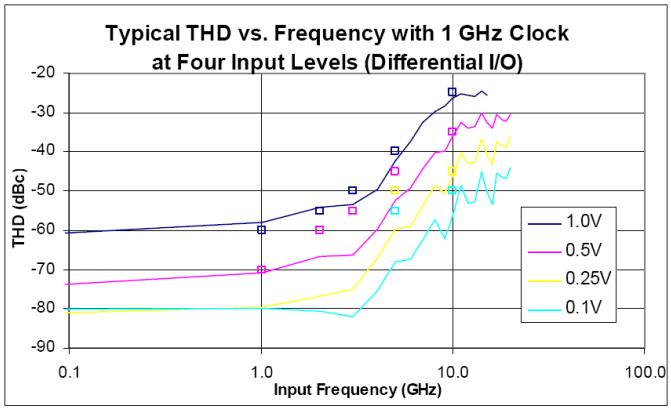


Figure 4.3 THD measured and provided by the manufacturer

About subsampling, some experiments were implemented in order to corroborate the theoretical studies, as the convenience to sample at $4f_c/m_{odd}$ in order to maintain the desired signals and the harmonicas as separated as possible. An example of this convenience was illustrated and described in Figure 3.5 (Section 3.3.2), where showed spectrums were obtained from the characterization of the S&H Inphi 1821TH.

Also, the convenience of sampling at the high optimal sampling frequency as possible, in order to reduce the folded noise in the band of interest, was corroborated experimentally. The obtained spectrums were illustrated in Figure 3.15 (Section 3.4.2) for an input signal centered at 1473 MHz.

4.1.2.2 Subsampling receiver characterization

After the S&H features were experimentally characterized and the theoretical subsampling properties were corroborated, the next step is to implement the proposed subsampling receiver at COTS level.

4.1.2.2.1 Implemented architecture

The block diagram of the proposed scheme is illustrated in Figure 4.4. In this system the GHz input signal is generated and converted to differential to be sampled by the S&H. A unique clock signal is generated in order to be distributed to the S&H and the ADC, being previously converted to differential signal as well. The IF signal at the output S&H is filtered by a LP filter in order to remove the rest of replicas outside Nyquist band.

Most concretely, all the used components are detail in the following list:

- S&H Inphi 1821TH and ADC E2V AT84AS001.
- Low jitter signal generator Agilent E8257D [4.7] to clock the S&H and the ADC.

- Signal generator Rohde & Schwarz SMIQ [4.8] to generate the input signal.

- Logic analyzer Agilent 16760-A [4.9] to process the digital IF output signal. The digital signal acquisition is implemented using the synchronous mode of this equipment (option *full channel 800 MS/s*). Finally, the digital signal processing and SNR measurement are achieved by MatLAB Software, implementing a 65536 points-FFT and using Kaiser window.

- Different power splitters from Minicircuits are used depending on the frequency range. ZAPDJ-2 [4.10] is employed to convert to extract the differential input signal, ZFCSJ-2-4 [4.11] to distribute the clock signal, and ZFSCJ-1-2 [4.12] to extract the differential clock signal.

- DC-blocks BLK-89 [4.13] and bias-tees ZFBT-4R2GW [4.14] from Minicircuits, to eliminate the DC component and coupling the connections between the S&H and the ADC with 50 Ω terminations [4.15], respectively.

- LP filter SLP-250 [4.16] to filter the replicas folded outside the Nyquist band by the subsampling process. Using a maximum sampling frequency of 500 MHz the maximum IF signal will be located at 125 MHz (i.e., $f_s/4$). Therefore, an ideal LP filter would have a cutoff frequency (f_{3dB}) at 135 MHz, i.e., $f_s/4+BW/2$, being BW the signal bandwidth equal to 20 MHz. However, since these filters are not ideal, this system presents a higher SNR when the IF replica is more separated from the cutoff frequency and, therefore, the final choice was the filter SLP-250, with a passband up to 225 MHz.

- Different cables and adapters provided of SMA[6] connections [4.17-4.19].

[6] SubMiniature version A.

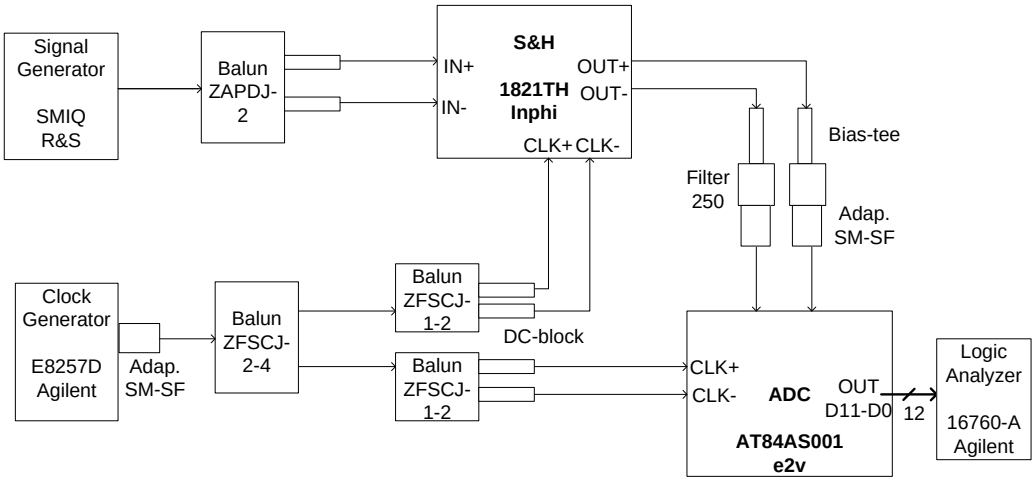


Figure 4.4 Block diagram of the implemented system

Figure 4.5 illustrates the systems at COTS level, where the clock path is not in the picture in order to show more clearly both PCB boards [4.5,4.20] and the signal path.

Figure 4.5 Implemented signal path at COTS level

4.1.2.2.2 Experimental results

4.1.2.2.2.1 Amplitude optimization

Firstly the amplitudes of the input and clock signals were swept in order to find their optimal values to maximize the Signal-to-Noise and Distortion Ratio (SNDR). These experiments were accomplished using different carrier frequencies sampled at a frequency very close[7] to its optimal sampling frequency immediately lower than 500 MHz, in order to include the 3rd order harmonic in the measurements over a signal bandwidth of 20 MHz.

As an example, the results obtained for an input frequency of 1001 MHz subsampled at 445.3 MHz, the optimal sampling frequency being equal to 444.9 MHz, are illustrated in Figure 4.6 where the ENOB is represented in function on the input signal amplitude and parameterized in respect to the clock signal

[7] The offset from the optimal sampling frequency is around 200-500 KHz for all the studied cases.

amplitude. After obtaining similar curves for input frequencies of 2 and 3 GHz the selected amplitudes for the rest of SNDR measurements are 1 dBm and 8 dBm for the input signal and the clock signal respectively.

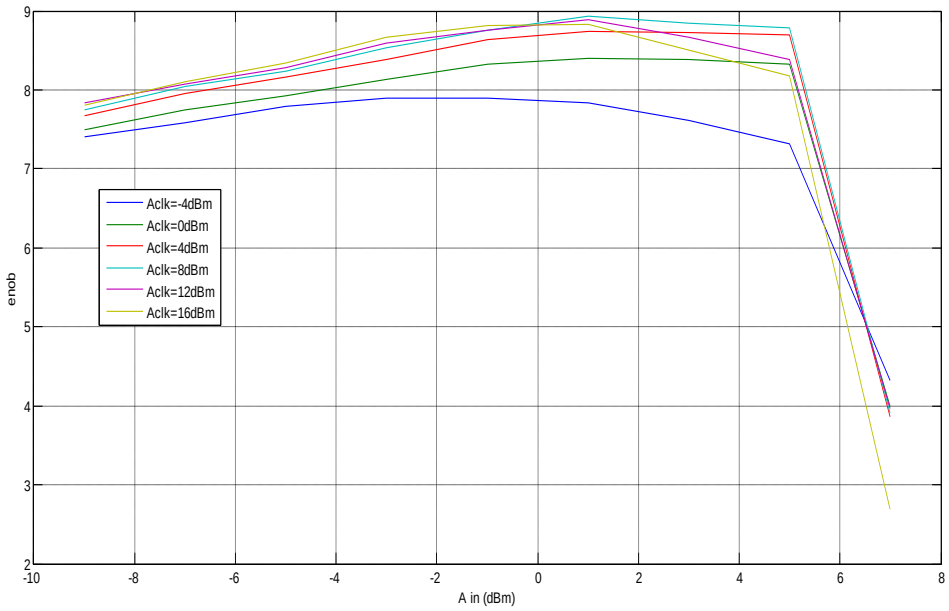


Figure 4.6 ENOB vs. input amplitude for an input signal frequency of 1001 MHz and a sampling frequency of 445.3 MHz

4.1.2.2.2.2 Spurious Free Dynamic Range (SFDR) for a single tone input signal

For these experiments the SFDR in a 20 MHz signal bandwidth was measured for the same input frequencies (1, 2 and 3 GHz) and employing a clock frequency [8] close to the optimal sampling frequency in order to avoid the overlapping between the desired signal and the 3rd harmonic. The SFDR obtained in function with the input frequency is illustrated in Figure 4.7, where it is possible to observe how for the optimal amplitude (1 dBm) the SFDR of the system is around 62-64 dB.

[8] A clock amplitude of 8 dBm is employed for the rest of experiments.

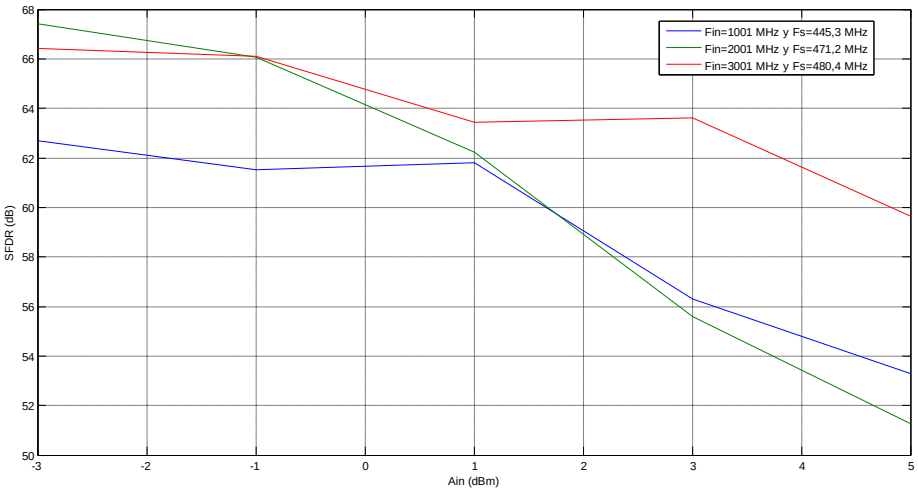


Figure 4.7 Measured SFDR vs. input signal amplitude

4.1.2.2.2.3 3rd order intermodulation distortion (IMD3) measurement

For these experiments a single tone modulated in amplitude (AM modulation) without carrier suppression is employed as input and, therefore, the signal input is composed by three tones equally spaced 1 MHz.

Figure 4.8 illustrates the IM measured for the same input frequencies (1, 2 and 3 GHz) clocking at the optimal sampling frequency. In this case the input amplitude must be reduced in order to optimize the performance, distributing the total energy in the three different tones. Although the characterization of SNDR for the all frequency range has been implemented for a single tone case, as described in the following sections, it is possible to observe how there is an amplitude range (around -3 dBm) where the obtained IMD3 is not a problem and its SNDR have acceptable values, i.e., very close to the optimal performance. Therefore, using several tones as input in this amplitude range would lead to very similar SNDR results as described in the following sections.

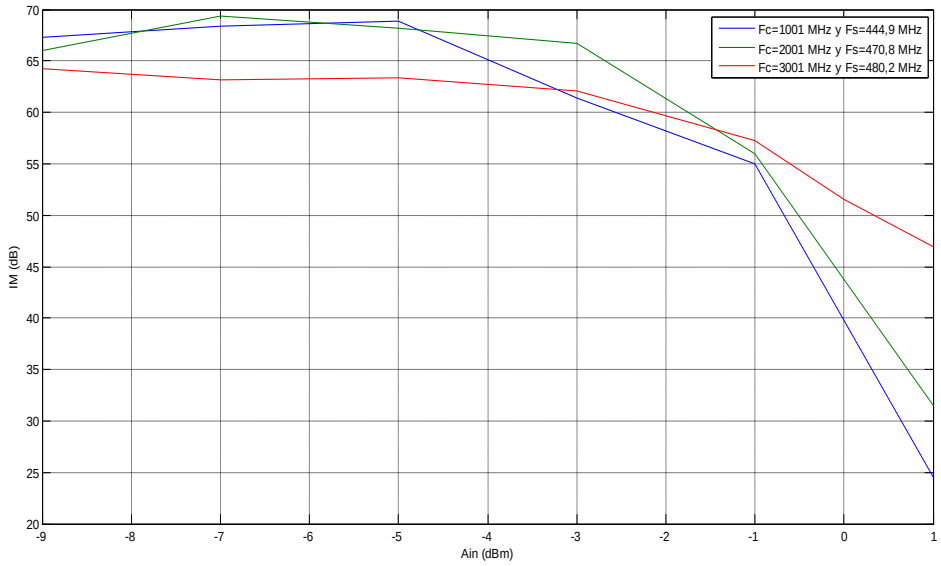


Figure 4.8 Measured IM vs. input amplitude

4.1.2.2.2.4 Subsampling properties in the implemented system

As described about the S&H characterization, this implemented receiver at COTS level can be used to illustrate some subsampling effects studied in the theoretical sections. Firstly, the dependency of the overlapping thermal noise within band signal on the subsampling frequency was experimentally characterized, with its effect illustrated in Figure 4.9 [4.21]. This figure represents ENOB obtained for different optimal subsampling frequencies of an input signal at 2001 MHz with 20 MHz of input bandwidth. As expected the total resolution is decreased when lower sampling frequencies are used.

The same effect can be appreciated from Figure 4.10 and Figure 4.11, where it is possible to observe how the noise floor increases in the case of using the lowest sampling frequency (Figure 4.11).

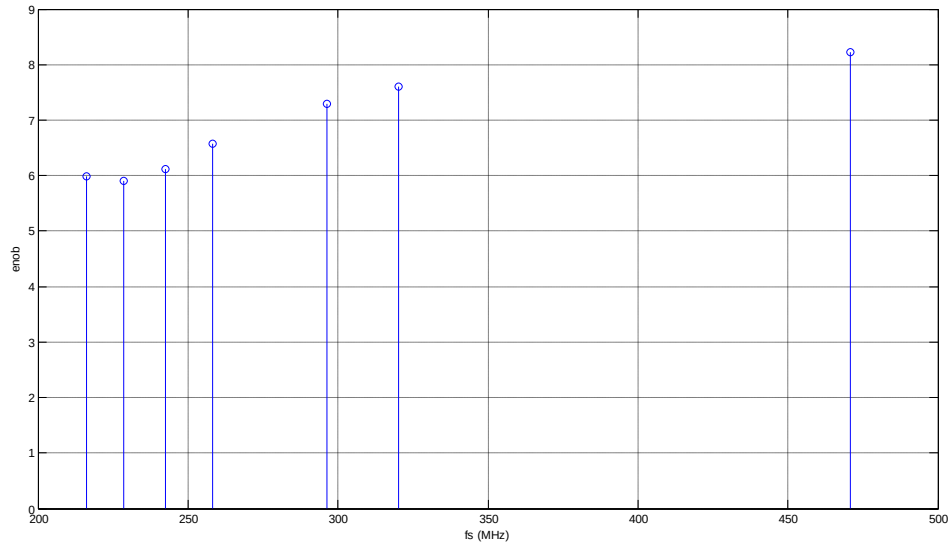


Figure 4.9 Measurement of the overlapping thermal noise: ENOB obtained for different optimal sampling frequencies

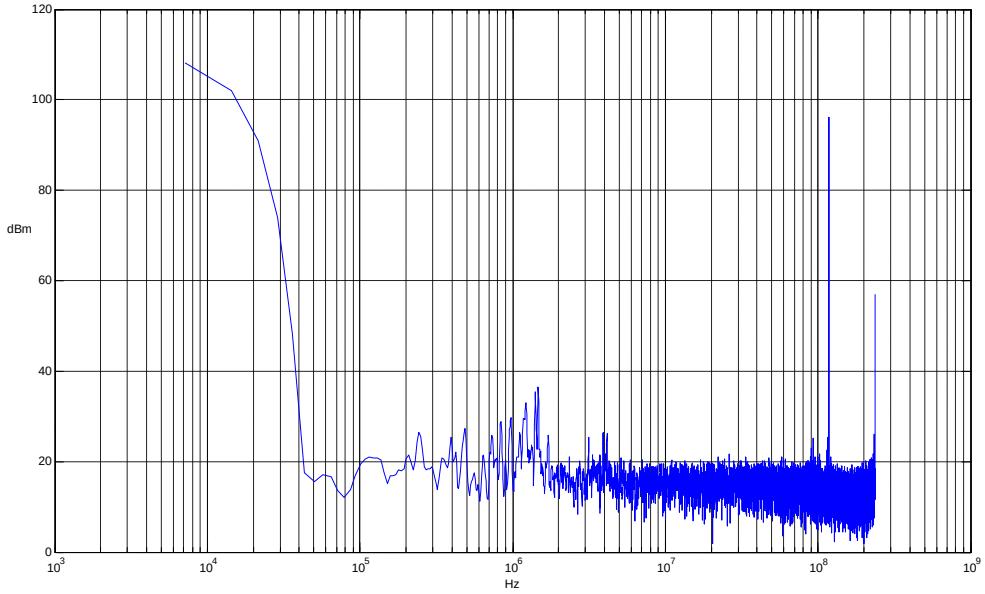


Figure 4.10 Output spectrum of a 2001 MHz input signal subsampled at 470.8 MHz

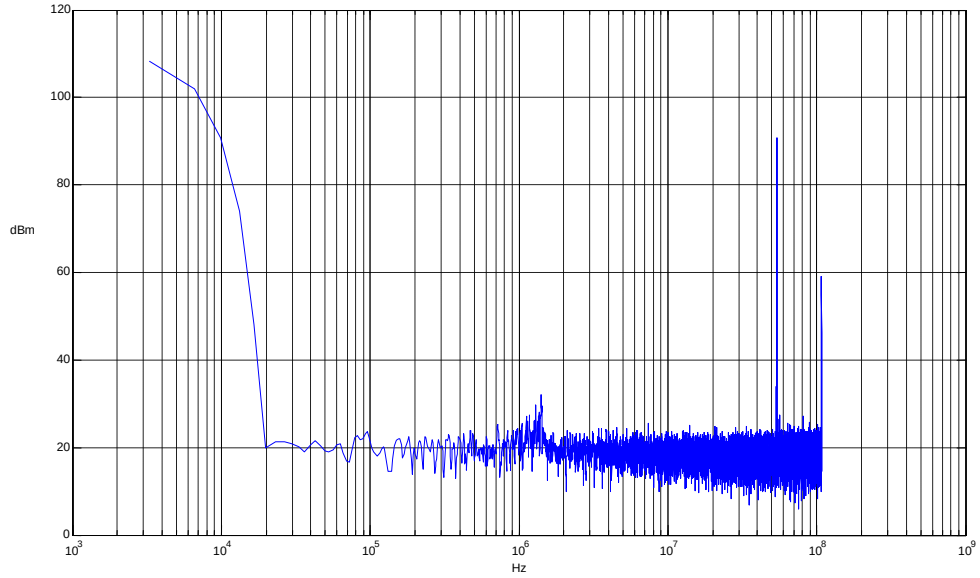


Figure 4.11 Output spectrum of a 2001 MHz input signal subsampled at 216.3 MHz

Another interesting measurement is on the influence of the jitter, which is more critical at higher input frequencies. This effect is illustrated in Figure 4.12 [4.21], showing the ENOB obtained for different input frequencies using the optimal subsampling frequency immediately less than 500 MHz and an input bandwidth of 20 MHz.

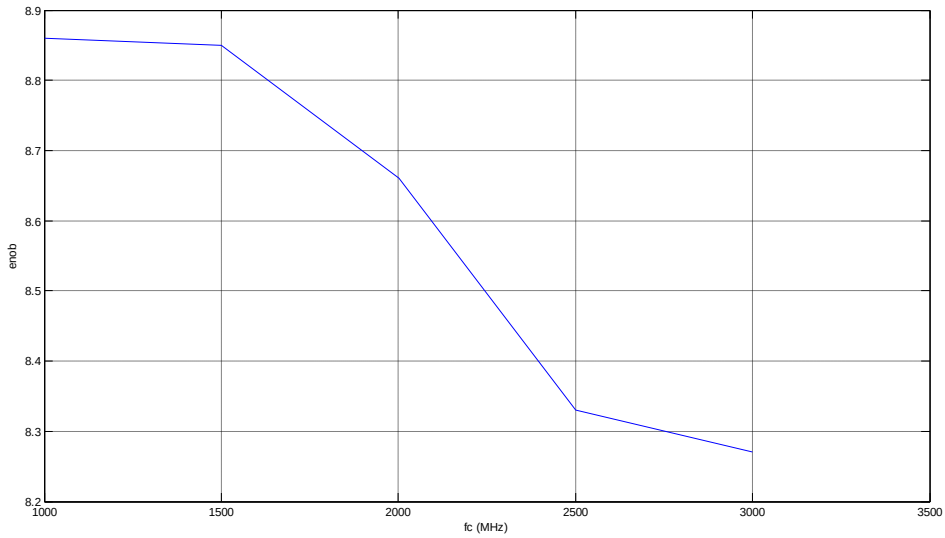


Figure 4.12 Measurement of the jitter noise: ENOB obtained for different input frequencies

4.1.2.2.2.5 Measured resolution for all the input range

Finally, the total resolution of the proposed system is illustrated in Figure 4.13 [4.21]. These results are obtained for an input frequency up to 3.3 GHz integrating in an input bandwidth of 20 MHz and clocking at a frequency close to the optimal sampling frequency immediately lower than 500 MHz. Therefore, these final results show a data acquisition system at COTS level that converts to digital signals with the following resolution:

- Around 9 bits up to 2 GHz input frequency.
- More than 8 bits up to 3.1 GHz input frequency.

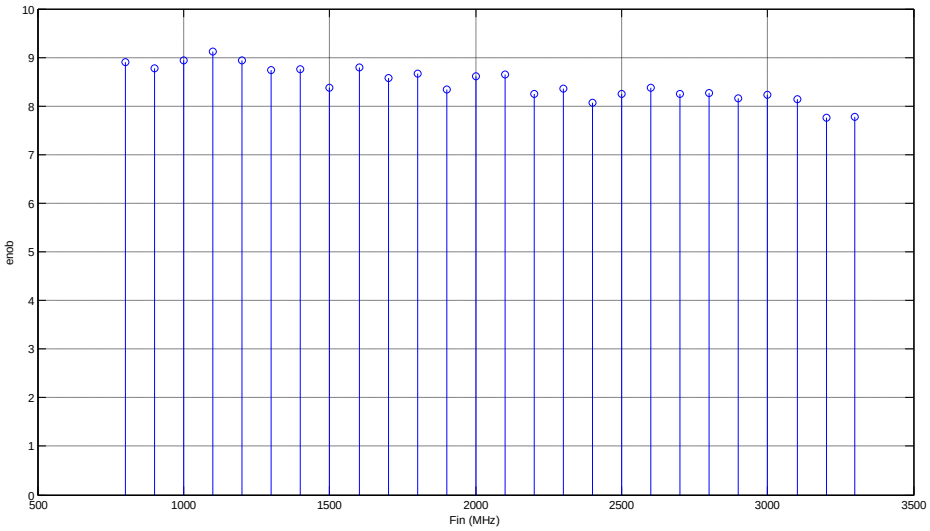


Figure 4.13 ENOB vs. input frequency

The system performance obtained from measurements is summarized in Table 4.1.

As an example, Figure 4.14 [4.21] illustrates the output spectrum for a 3 GHz input frequency and a 480.2 MHz sampling frequency.

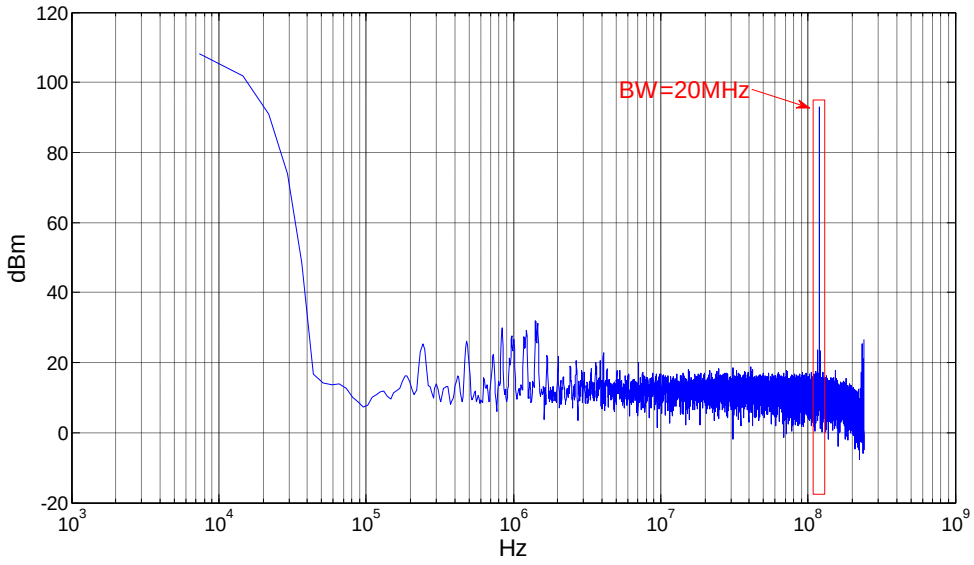


Figure 4.14 Output spectrum for a 3 GHz input frequency

Table 4.1 System performance at COTS level

Maximum Input Frequency	3.1 GHz
Signal Bandwidth	20 MHz
Sampling Frequency	<500 MHz
ENOB (SNDR)	>8.1 bits
SFDR	>61.8 dBc
Voltage Supply S&H	-5,2 V
Voltage Supplies ADC	5 V (Analog), 3.3 V (Digital, Output)
Power Consumption	3.7 W

4.2 Data acquisition systems based on PCB

4.2.1 PCB design

A data acquisition module at PCB level for high performance low-cost multi-standard test equipment was presented in [4.22]. This work provides high resolution over a large bandwidth with only a low-jitter wideband S&H and an intermediate frequency ADC, by means of subsampling. Using commercial devices on a multilayer printed circuit board, experimental results showed more

than 8 bits resolution for a 20 MHz signal bandwidth with up to 3.8 GHz center frequency, enough to cover the requirements of test systems for most of present wireless communication standards. These commercial devices are the same that used at COTS level, i.e., the S&H Inphi 1821TH and the ADC E2V AT84AS001.

These devices are the main components of the proposed data acquisition system for which a multi layer PCB prototype was designed and fabricated (Figure 4.15 [4.22]). Moreover, this prototype includes other components, such as baluns [4.23], bias tees [4.24] and LP passive filters (Minicircuits LFCN-160 [4.25]). Thanks to a higher availability of surface mount devices (SMD), the chosen filters let to implement a better adjustment of the filtering stage because its cutoff frequency is lower and, therefore, the 2nd order harmonics, which are in the 200-250 MHz[9], are more attenuated.

This design uses a Class 7 board with DE104i FR4 dielectric, six metal layers and microstrip lines adapted to 50 Ω. The features of this class and this dielectric are obtained from [4.26] and are detailed in Appendix B. On the other hand, the rules and expressions employed to adapt the components (designing the dimensions of traces and layers) were obtained from [4.27] and also are described in Appendix B.

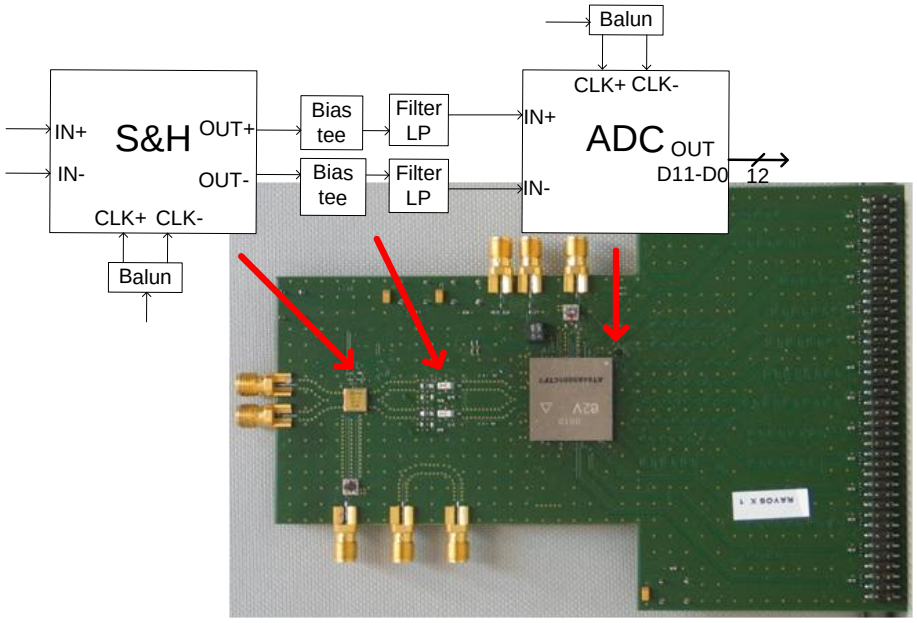


Figure 4.15 Block diagram and designed PCB prototype

Employing the external metal layers (1 and 6) for signals, the adjacent metal layers for ground (2 and 5) and the most internal layers (3 and 4) for power supplies, the resultant stack-up is as showed in Figure 4.16, which follows a

[9] Since the chosen optimal sampling frequency is in the range of 400-500 MHz in order to fold the desired IF replica to $f_s/4$, the 2nd order harmonic will be located in the range of 200-250 MHz.

typical structure proposed by the manufacturer Labcircuits [4.26] and has a thickness equal to 1.22 mm.

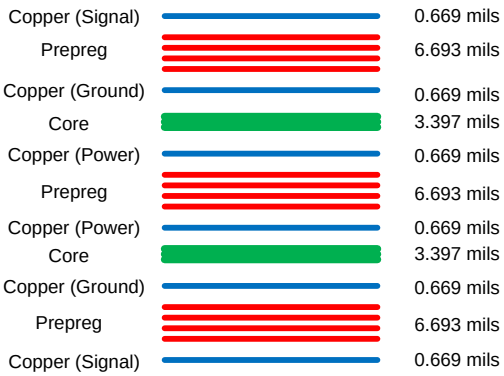


Figure 4.16 Implemented stack-up

The circuit was carefully laid out in order to minimize the jitter effect. The distance between signal tracks, pads and metal layers was carefully chosen in order to reduce crosstalk and inter-symbol interference, which cause jitter. Other rules followed to reduce jitter were a correct decoupling from the power lines and the signal planes employing the technique called *picket fences* [4.28], consisting in placing closely spaced VIAs (vertical interconnect access) between different ground planes. A typical distance between VIAs equal to 1/20 wavelength (λ) was selected. Finally, the dimensions of the designed PCB are 16.05 x 10.64 cm^2.

4.2.2 Experimental results

The data acquisition system was experimentally characterized, with the obtained performance summarized in Table 4.2 [4.22]:

Table 4.2 System performance at PCB level

Signal Bandwidth	20 MHz
Signal Input Frequency	3.3 GHz
Sampling Frequency	<500 MHz
ENOB (SNDR)	>8.2 bits
Linearity (SFDR)	>9.49 bits
IMD3	>60.4 dB
Power Consumption	3.7 W

The measured SFDR and IMD3 were about 60 dB regardless of the input frequency, and thus the ENOB (based on the maximum SNDR) is larger than 8.2 bits for sinusoidal input signals up to 3.3 GHz.

Figure 4.17 [4.22] shows the system resolution as a function of the carrier frequency up to 20 GHz, for a sampling frequency very close to 500 MHz. The results provide a useful characterization of the system response and clearly show the effect of jitter. Up to 3.3 GHz there is no significant influence of jitter, as the ENOB is nearly constant in this range. The resolution falls as the input frequency increases, mostly due to the influence of jitter. The system response provides an ENOB larger than 7 bits up to 6 GHz, 6 bits up to 13 GHz and 5.5 bits at 20 GHz.

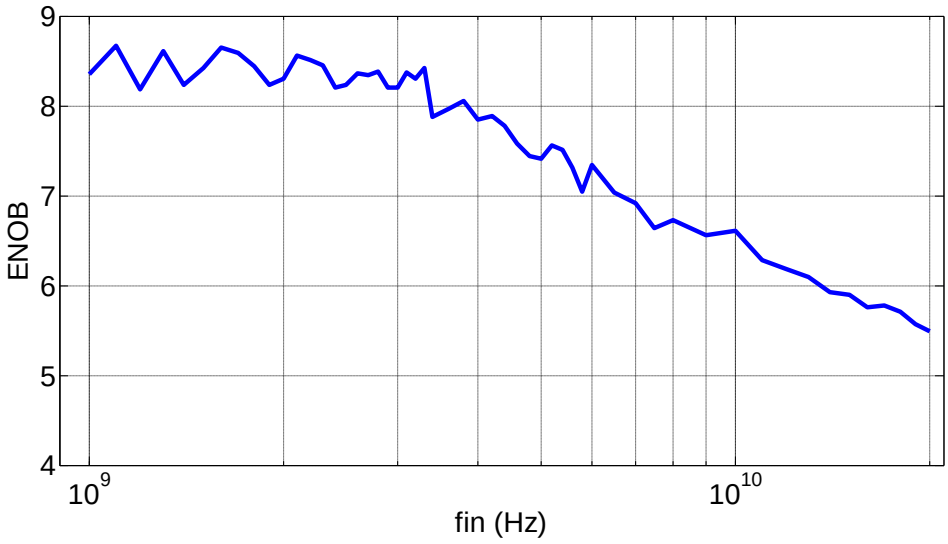


Figure 4.17 ENOB vs. input frequency (20 MHz signal band, up to 20 GHz input carrier frequency)

Therefore, this work presents a data acquisition module for testing wireless receivers based on subsampling, which covers most present wireless communication standards requirements, with an ENOB between higher than 8 bits up to 4 GHz center frequency for a 20 MHz signal bandwidth.

4.3 Noise performance optimization based on multiple clocking techniques

As described in Section 4.2, a limitation of the data acquisition systems based on subsampling is the maximum sampling frequency, which will be given by the ADC specification and is around 400-500 MHz for commercial ADCs with large enough resolution.

In order to reduce the folded noise effect, this section describes a method to improve the resolution, which employs two consecutive subsampling stages

[4.29]. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise, such as described in Section 3.4.1.

4.3.1 Theoretical study

Figure 4.18 shows two different alternatives to implement a subsampling based receiver. Figure 4.18a illustrates the scheme for a unique subsampling process implemented in Section 4.2 while Figure 4.18b illustrates the scheme with two different clocks. The sampling frequency of the first S&H in Figure 4.18b is selected between 1.2 GHz and 2 GHz (given by the maximum sampling frequency clock specifications of the S&H), obtaining a band-limited signal at the output. As the first sampling frequency is very large the folded thermal noise added by this stage is reduced. After filtering, the resulting signal is subsampled again by a second S&H at 400-500 MHz. However, some drawbacks of the proposed system are a higher complexity and power consumption than the one stage subsampling receiver.

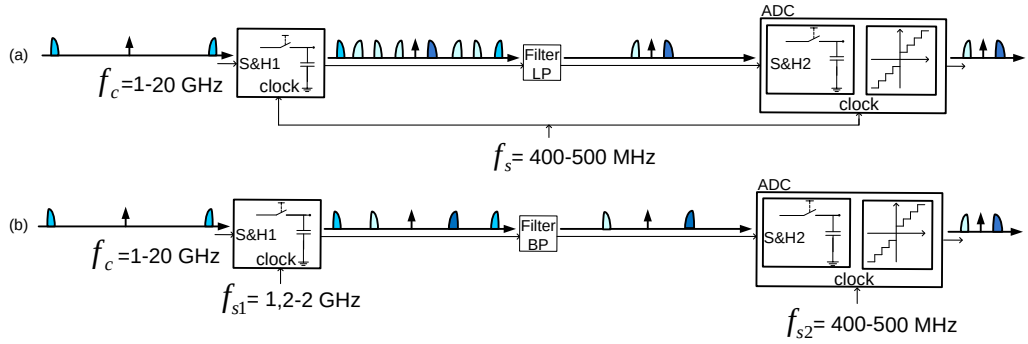


Figure 4.18 Clocking schemes for: (a) a unique clock and (b) two different clocks

The S&H in Figure 4.18 can be modeled as shown in Figure 3.14a, where the switch introduces thermal noise of power spectral density $S_{in}(f)=4kTR_{on}$ that will be filtered by the RC circuit, resulting in an output noise power of $P_{n,out}=kT/C$, as was obtained in Section 3.4.2.

In this section, the output noise was considered to be a Gaussian thermal noise filtered by a brick-wall filter of bandwidth equal to B_{eff} (noise bandwidth), as shown in Figure 3.14c:

$$B_{eff} = \frac{1}{4R_{on}C} = \frac{\pi}{2} f_{3dB} \tag{4.1}$$

Where f_{3dB} is the 3-dB bandwidth of the RC filter.

On the other hand, the SNR in [$-B_{eff}$,B_{eff}] is defined as [19]:

$$SNR = \frac{P_s}{N_i + (m-1)N_o} \tag{4.2}$$

Where P_s is the signal power spectral density, and N_i and N_o are the in-band and the out-of-band noise spectral power densities, respectively. As $2B_{eff}=mf_s$, if m=1 the Nyquist Theorem is met and the SNR is not affected by the folded noise. On the other hand, if m>1, and assuming $N_i = N_o = N$,

$$SNR = \frac{P_s}{mN} = \frac{P_s}{N(2B_{eff} / f_s)} \tag{4.3}$$

Therefore, the out-of-band folded noise reduces the SNR by a factor $2B_{eff}/f_s$.

Assuming the noise of both S&Hs in Figure 4.18 are uncorrelated, the output power spectral density due to the S&Hs white noise in Figure 4.18a and Figure 4.18b, respectively, are [4.29]:

$$\begin{aligned} P_{N(a)} &= \frac{2B_{eff1}}{f_s} N_1 + \frac{2B_{eff2}}{f_s} N_2 \\ P_{N(b)} &= \frac{2B_{eff1}}{f_{s1}} N_1 + \frac{2B_{eff2}}{f_{s2}} N_2 \end{aligned} \tag{4.4}$$

Where N_1 and N_2 are the noise power introduced by $S\&H_1$ and $S\&H_2$, respectively, and B_{eff1} and B_{eff2} their respective noise bandwidths. Note that there will not be folding of N_1 during the second sampling process because the signal is filtered at IF in both cases, using a BP filter in Figure 4.18b Therefore, the SNR improvement obtained with this sampling frequency plan is given by [4.29]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} = \frac{P_s / N_{(b)}}{P_s / N_{(a)}} = \frac{B_{eff1}N_1 + B_{eff2}N_2}{\frac{f_s}{f_{s1}} B_{eff1}N_1 + \frac{f_s}{f_{s2}} B_{eff2}N_2} \tag{4.5}$$

As the first S&H processes high frequency signals, $B_{eff1} >> B_{eff2}$. In addition, the noise power spectral densities of both S&Hs can be assumed to be of the same order of magnitude. Then equation (4.5) can be approximated by [4.29]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} \approx \frac{1}{\frac{f_s}{f_{s1}} + \frac{f_s}{f_{s2}} \frac{B_{eff2}}{B_{eff1}}} \tag{4.6}$$

With f_{s1}/f_s being the most influential term in this improvement, a higher ratio will mean a better SNR improvement.

4.3.2 Experimental results

As theoretically described in the last section, the use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise. In

this section this study will be experimentally corroborated at COTS and PCB levels.

4.3.2.1 COTS level

Firstly, the system was implemented at COTS level, as illustrated in Figure 4.19 [4.31], with many components common with the architecture shown in Figure 4.4. The GHz input signal is generated and converted to differential to be sampled by the S&H. Two different clock signals are generated in this case, one of them up to 500 MHz (ADC) and the other one up to 2 GHz (S&H).

Another difference in respect to Figure 4.4 is the filtering stage. In this case a BP filter is employed in order to keep the desired signals located at $f_s/4$. Since the first sampling frequency is in the range 1.3-2 GHz, a good choice is a BP filter in the range 300-550 MHz. In order to implement this filtering stage, each BP filter was implemented connecting a cascade of a LP filter SLP-550 [4.32] and a HP filter SHP-300 [4.33].

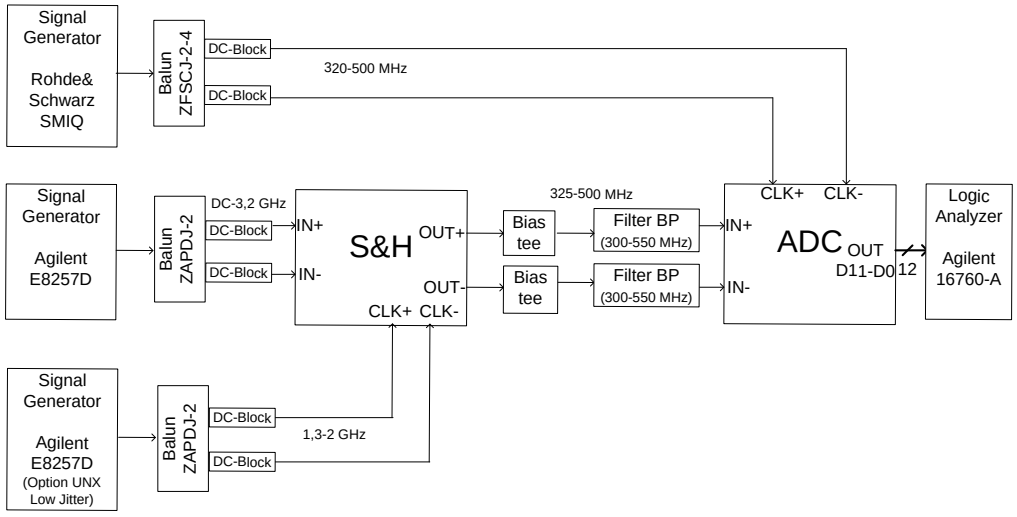


Figure 4.19 Implemented multiple clock system

The system performance obtained from measurements is summarized in Table 4.3 [4.31]. The ENOB (based on the maximum SNDR) is between 8.8 and 9.8 bits for sinusoidal input signals up to 3.2 GHz. The SFDR is about 60 dBc regardless of the input frequency.

Figure 4.20 [59] illustrates the ENOB as a function of the carrier frequency up to 3.2 GHz for a signal bandwidth equal to 20 MHz. The results are compared with the obtained from the unique clock implementation [4.21]. Also this figure shows the expected results according to the increase of the S&H sampling frequency. Figure 4.20 shows how the expected and the measured results are very similar, the resolution improving from 0.5-1 bits. Also this figure shows how the

resolution falls as the input frequency increases, mostly due to the influence of jitter.

Figure 4.21 [4.31] shows the resolution for different ADC clock frequencies, which could be imposed by the digital restrictions given for the maximum sampling rate. Therefore, in the cases where the sampling rate is limited to a maximum by the DSP restrictions, there will be a compromise between the allowed maximum speed and the resolution. Figure 4.21 illustrates how the resolution grows as the sampling frequency increases due to the decreasing of the noise integrated in the 20 MHz signal bandwidth.

Table 4.3 System performance using multiple clocking at COTS level

Maximum Input Frequency	3.2 GHz
Signal Bandwidth	20 MHz
Sampling Frequency S&H	1.3-2 GHz
Sampling Frequency ADC	320.1-480.3 MHz
ENOB (SNDR)	>8.77 bits
SFDR	>61.2 dBc
Voltage Supply S&H	-5,2 V
Voltage Supplies ADC	5 V (Analog), 3.3 V (Digital, Output)
Power Consumption	3.7 W

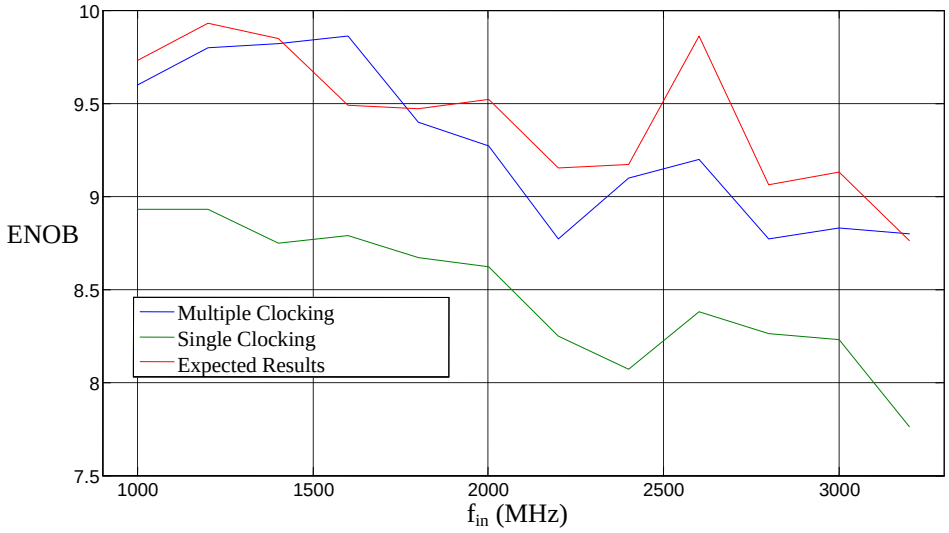


Figure 4.20 ENOB obtained at COTS level for a multiple clocking architecture

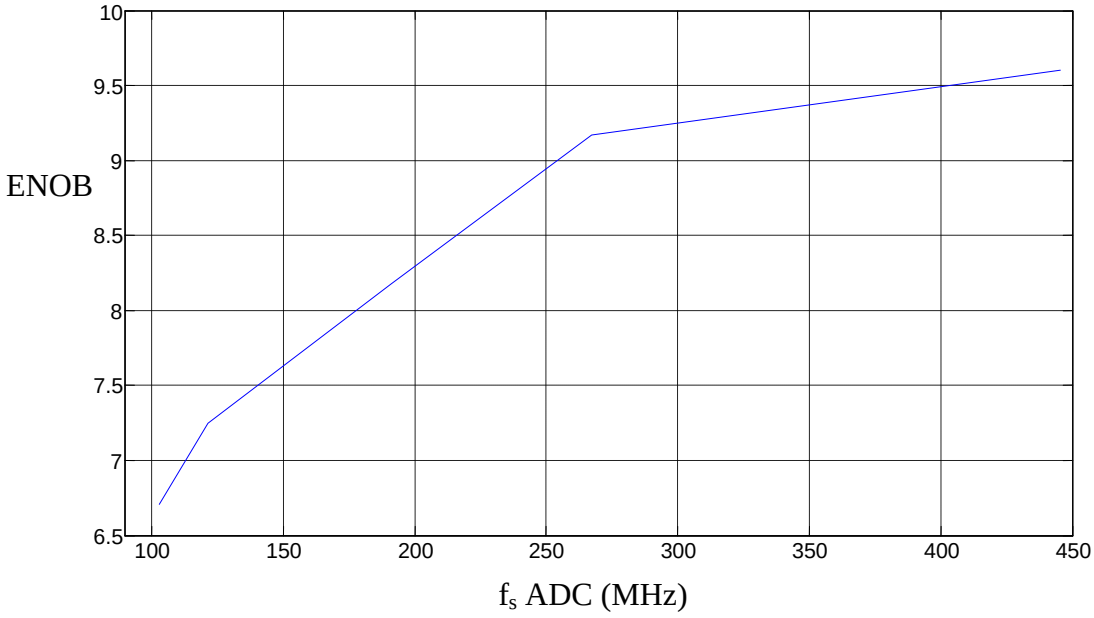


Figure 4.21 Measurement of the folded noise effect (ENOB vs. Optimal sampling frequencies)

Table 4.4 shows the configuration parameters and the specifications required for some of the most common wireless communication standards [4.34]. Also this table shows the experimental results obtained for these standards. Note that the maximum signal bandwidth is 20 MHz. For lower bandwidths, the entire 20 MHz band around the central frequency is converted, and the selected bandwidth is reduced by means of digital signal processing increasing the resolution.

Therefore, we can observe how the implemented data acquisition system can be used in order to evaluate most communication standards in terms of tuning frequency, linearity and noise. Also we can observe how the specifications were not achieved by the system based on a unique clock for some wireless standards [4.21]. For instance, the resolution obtained in [4.21] for Blue-tooth was 10.3 bits while it is 11.26 using the proposed system. Thus, the proposed system based on multiple clocking covers a larger number of wireless communication standards.

Table 4.4 Standards specifications and results at COTS level

	Carrier Frequency (MHz)	Signal BW (MHz)	Resolution Specifications (bits)	SNDR Specifications (dB)	Resolution Results (bits)	SNDR Results (dB)
GSM	1800	0.2	9	55.94	12.72	78.35
UMTS (I)	2110-2170	5	6	37.88	9.8	60.75
Blue-tooth	2400	1	11	67.98	11.26	69.55
IEEE 802.11b (Wi-Fi)	2400	20	8	49.92	9.1	56.54

4.3.2.2 PCB level

The implemented PCB is the illustrated in Figure 4.15, the LP stage filtering being replaced by a BP filtering centered at $fs_1/4$, i.e., around 300-500 MHz approximately. Therefore, the selected filter is the Minicircuits RBP-400 [4.35], with a band pass in the range 292-490 MHz.

System performances, obtained from measurements, are summarized in Table 4.5 [4.29]. Figure 4.22 shows the ENOB as a function of the carrier frequency up to 20 GHz, for a signal bandwidth equal to 20 MHz [4.29]. The solid line shows previous results obtained in [4.22]. The dashed line shows the expected ENOB calculated with equation (4.6), which is met while jitter is not the dominant effect. Finally, the dotted line shows the experimental results obtained from the prototype based on multiple clocking. Note that, although the implemented experimental setup is the same as employed in sections 4.1 and 4.2, an ultra low phase noise option Agilent UNX [4.7] was added to the clock generator in this case. Therefore, there will be a slight improvement over the total SNR where the jitter noise is the dominant effect, i.e., at higher input frequencies for both architectures. Otherwise, when a single clock scheme is employed, the measured SNR is as obtained in [4.22] at lower frequencies.

Table 4.5 System performances using multiple clocking at PCB level

Maximum Input Frequency	20 GHz
Signal Bandwidth	20 MHz
Sampling Frequency S&H	1.3-2 GHz
Sampling Frequency ADC	320.1-480.3 MHz
ENOB (SNDR)	>9 bits up to 2.9 GHz >8 bits up to 6.5 GHz > 6.4 bits up to 20 GHz
SFDR	61.27 (59.57) @ 2 (3) GHz
Noise Figure	2.7 (3.8) dB @ 1 (2) GHz
PSD Noise	-130.6dBm/Hz @ 1 GHz

These experimental results show how the proposed system reduces the effect of the folded noise, increasing the ENOB by 0.5-1 bits in the band of interest. Therefore, it provides an ENOB larger than 9 bits up to 2.9 GHz, 8 bits up to 6.5 GHz, 7 bits up to 12 GHz, and 6.4 bits up to 20 GHz. Concerning linearity and power consumption the results are similar to those obtained in the previous work [4.22].

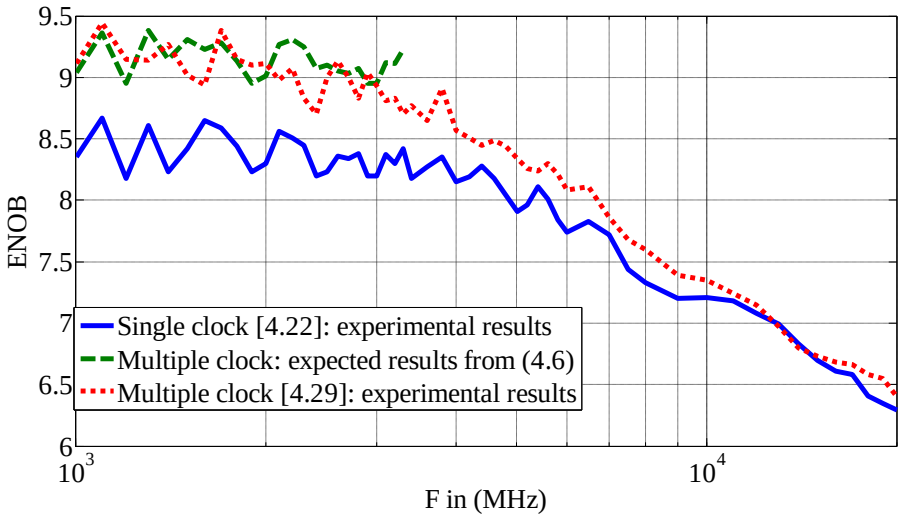


Figure 4.22 Obtained ENOB in function of the input frequency

4.4 Comparison with other implemented multi-standards receivers

There are two main classifications of multi-standards receivers. In section 2.2.6 a comparative of multi-standard receivers about digitalization techniques (i.e., mixing or subsampling based systems) was introduced. Although subsampling techniques have some problems as the folded thermal noise effect or the aliasing in multi-band scenarios (as detailed in Chapter 4), for SDR applications are very convenient in order to place, using a few building blocks, the analog-to-digital conversion stage as close the antenna as possible.

Moreover, multi-standards receivers might be classified about their band strategy, i.e., if they implement a narrow-band strategy or a wide-band strategy. A narrow-band strategy is implemented by the receivers that are designed for some specifics standards, employing dedicated channels, while a wide-band strategy is implemented by the ones that cover a higher number of wireless communication standards. Therefore, narrow-band receivers might provide a finer optimization for specific standards while wide-band receivers might be considered universal receivers and are used for more general applications. Although these wideband solutions are more flexible, their main inconvenience is the RF front-end must meet the requirements for each standard and they are not optimum for any standard.

Since it has been described in this chapter, the works presented in [4.22,4.29] might be an approach to the idea of universal receiver for SDR applications. Other works have been published, which can be considered multi-standard receivers. However, some of these works are based on mixing techniques, losing part of the flexibility and simplicity provided by the subsampling based systems. On the other hand, there are also multi-standard receivers, which although they are based on subsampling, are optimized for a given number of wireless standards, without covering all the applications.

Examples in both directions are present in the literature. [4.36,4.37] are examples of works which employ wideband strategies. [4.37] presents a receiver front-end for multi-standard wireless applications, its analog bandwidth being up to 3.5 GHz. [4.36] presents a wideband-multi-standard system that can be considered as an universal receiver, covering input frequencies between 0.8 and 6 GHz and being based in mixing techniques. Although [4.36] is a more complex solution than [4.29], this work has a large tuning range and other benefits as a high linearity and low power consumption, because of its implementation in IC (Integrated Circuit). As a main inconvenience, since [4.36,4.37,4.22,4.29] are wideband solutions and, therefore, they are not optimum for any standard.

About the narrow-band strategy, [4.34] proposes an alternative multi-standard receiver solution separating into two different RF channels, one for the 2.4 GHz and 5 GHz WLANs and the other for the GSMs. The different channels share a common programmable baseband, this solution being highly efficient, because every path is optimized to a specific standard. On the hand, the main drawback of this work is, besides the limitation of the number of standards, the area consumption, due to the high selectivity is achieved by means of many inductors.

An example of a solution based on narrow-band strategies is showed in Figure 4.23a [4.38]. In this receiver, dedicated Bluetooth and GPS links allow connectivity while making a phone call or/and sending or receiving data through a WLAN. The WLAN path connects to IEEE802.11a/b/g/n routers, while the cellular-dedicated channel can switch from one of the GSM bands to the UMTS/WCDMA. Moreover, the selection is provided by off chip SAW filters, which relax the linearity requirements.

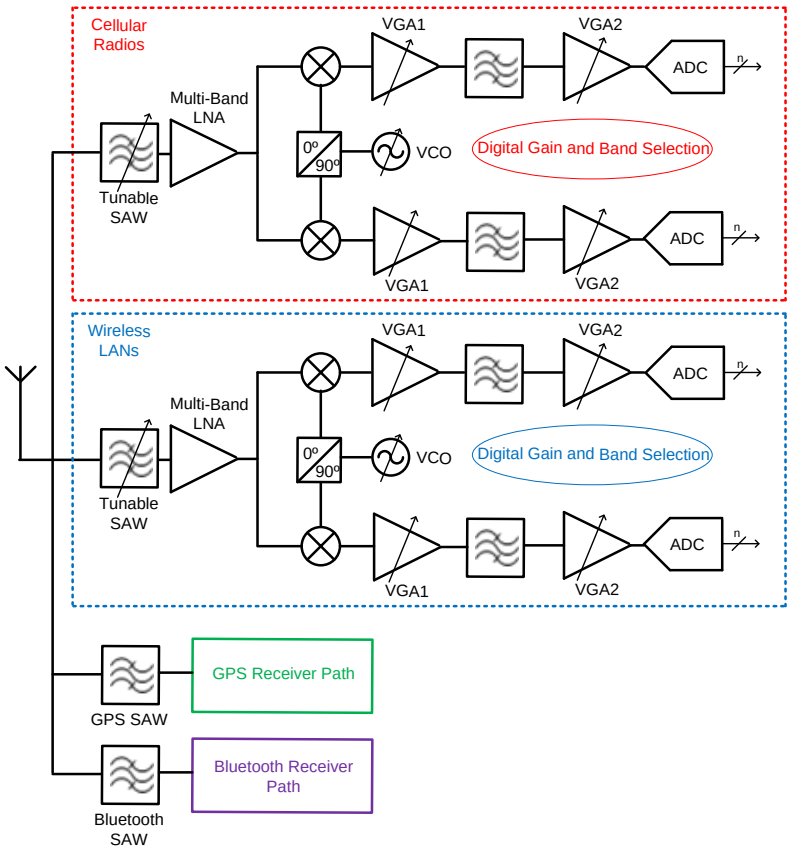
Other works provide a high level of hardware sharing, as [4.39], where the different specific standards employ a common acquisition and digitalization stages. This work proposes a solution for Bluetooth, GSM, UMTS and WLAN, where the last three standards share the same circuitry after the filter bank (Figure 4.23b), allowing reuse some building blocks in the receiver architecture.

This hardware sharing maximization means a minimum area consumption, making it possible thank to all the considered standards, except Bluetooth, do not need to be covered at the same time, i.e., when an application is active, the others can be switched off in order to save power.

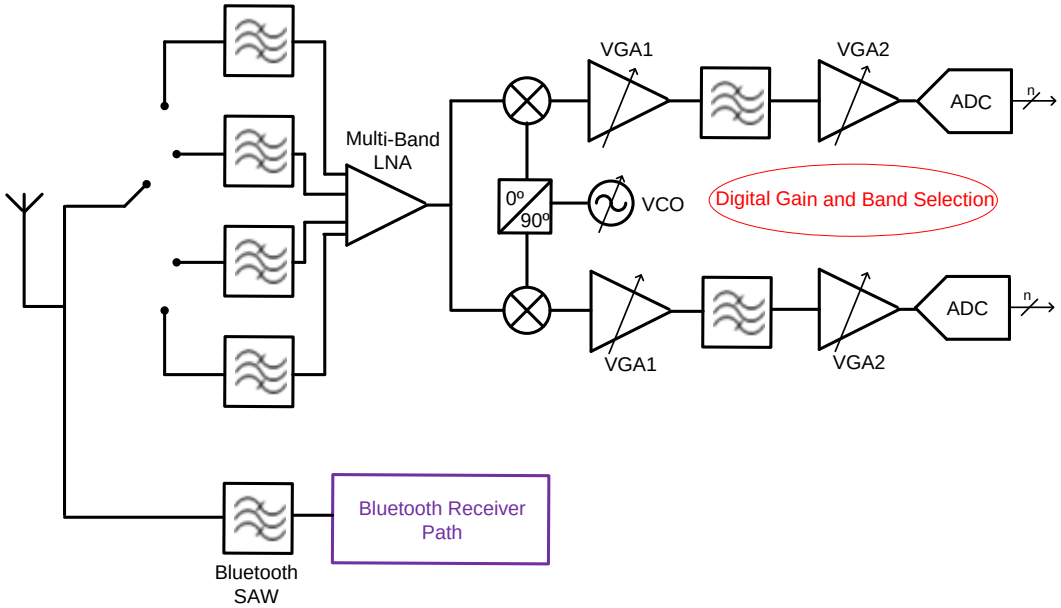
On the other hand, data acquisition systems for different communications standards use subsampling techniques in order to process high frequency signals with only a few components. [4.40] proposes a subsampling receiver for three different standards (GSM, UMTS and IEEE 802.11g), which validates these topologies at a simulation level in order to be applied for multi-standard radio design. An additional goal of this work is the design of the RF and IF filters for the different standards, in order to avoid the aliasing caused by the subsampling process.

In other published works [4.41,4.42], the receivers based on subsampling are implemented experimentally only for fixed bands. [4.41] proposes a low noise subsampling implementation for the 2.1 GHz band, and [4.42] for 2.4 GHz (IEEE 802.11a/g WLAN standards). In [4.41] an IC receiver designed in 0.18 μm CMOS, whose main goal is a tunable LC filter implementation, is proposed. [4.42] shows a 0.18 μm CMOS receiver which represents the most complete subsampling receiver reference, thanks to the optimization performed for parameters as thermal noise level, jitter-induced noise and nonlinearity. Finally, there are also receivers

based on subsampling for UWB applications, like the one in [4.43], which operates in the 3.1-10.6 GHz band with low power consumption.



(a)



(b)

Figure 4.23 Multi-standard receiver architectures proposed in [4.38] (a) and [4.39] (b)

Finally, Table 4.6 [4.29] shows the specifications for most common wireless communication standards [4.34] and the results obtained in some of these previously published works about the noise performance. These results are compared with the obtained in [4.22] in order to observe the benefits of implement a multiple clock technique for multi-standard receivers based on subsampling. It can be seen that, employing the data acquisition system designed in [4.29], only the ENOB specifications for IEEE 802.11a are not achieved, although they are very close. Moreover, note that some specifications, like Noise Figure (NF) for UMTS (I) and 802.11b/g, or resolution for Bluetooth, were not achieved without the improvement proposed in [4.29], i.e., when a unique clock source is used [4.22]. Comparing with the other published work, similar results about NF and Noise PSD can be observed with respect to [4.29], showing a larger influence of the jitter (i.e., reducing the resolution with the input frequency) in the work presented in [4.29].

Table 4.6 Standard specifications and results

	Standard	**GSM 1800**	**UMTS (I)**	**Blue-tooth**	**802.11b/g**	**802.11a**
Standard requirements	**Carrier Freq. (MHz)**	1805.2-1879.8	2110-2170	2400	2400	5000
	Signal Bandwidth (MHz)	0.2	5	1	20	20
	ENOB (bits)	9	6	11	8	9
	NF (dB)	9.3	4.6	10.7	6.5	18.2
Experimental results of previously published acquisition systems	**ENOB [4.22] (bits)**	11.76	9.56	10.36	8.2	7.41
	NF [4.22] (dB)	6.1	6.5	8.3	8.3	13.1
	NF [4.34] (dB)	5.2	5.6		5.8	
	NF [4.37] (dB)	5.8	6	6.5	6.5	
	NF [4.40] (dB)		7.5		7.2	
	Noise PSD [4.42] (dBm/Hz)				-131	
Experimental results of [4.29]	**ENOB (bits)**	12.47	9.97	10.86	8.7	8.34
	NF (dB)	3.6	4.4	6.2	6.2	9.3
	Noise PSD (dBm/Hz)	-129.7	-128.8	-126.9	-126.9	-123.8

4.5 References

[4.1] 1821TH, *18 GHz Bandwidth 2 GS/s THA*, Inphi Corps. Datasheet.

[4.2] HMC660LC4B, *0.02-4.5 GHz Wideband 3 GS/s Track-and-Hold Amplifier*, Hittite Microwave Corporation. Datasheet.

[4.3] RTH010-060 Series, *8-16 GHz Bandwidth 1-4 GS/s Dual Track-and-Hold*, Teledyne Scientific Company. Datasheet.

[4.4] AT84AS001, *12-bit 500 Msps ADC*, E2V Technologies. Datasheet.

[4.5] 1821TH, *18 GHz Track and Hold*, Inphi Corps. Application Note.

[4.6] On line: www.minicircuits.com

[4.7] E8257D PSG, *Microwave Analog Signal Generator*, Agilent Technologies. Datasheet.

[4.8] SMIQ, *Vector Signal Generator*, Rohde & Schwarz. Datasheet.

[4.9] 16720-A, *Measurements Modules for the 16900 Series*, Agilent Technologies. Datasheet.

[4.10] ZAPDJ-2, *Power Splitter/Combiner 2 Way-180º 50Ω*, Minicircuits. Datasheet.

[4.11] ZFSCJ-2-4, *Power Splitter/Combiner 2 Way-180º 50Ω*, Minicircuits. Datasheet.

[4.12] ZFSCJ-1-2, *Power Splitter/Combiner 2 Way-180º 50Ω*, Minicircuits. Datasheet.

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CHAPTER 5

SUBSAMPLING TECHNIQUES FOR NONLINEAR AND MULTI-BAND APPLICATIONS

CHAPTER CONTENTS

Chapter 5 describes the additional challenges of implementing subsampling techniques for multi-band and nonlinear applications. A first section of this chapter is dedicated to introduce the context where these applications are useful, while the next two sections introduce the previously published expressions to implement, separately, subsampling in multi-band and non linear scenarios. A fourth section integrates both effects, detailing the designed algorithm to find the valid sampling frequency ranges and describing an optimization of a particular case for dual band receivers in a nonlinear environment. This optimization is based on the multiple clocking techniques described in Chapter 4 and on a multi-filter structure implementation between the S&H and the ADC. Finally this optimization is experimentally validated.

5.1 Studied scenarios

Due to the emergence of several co-existing wireless technologies in the cellular industry, there is a trend to design multi-standard receivers targeting the optimization of their flexibility, simplicity and power consumption.

The two main drawbacks of the systems based on subsampling are the jitter and the thermal folded noise, which make system implementation even more dificult for multi-band or non-linear applications. There is a challenge when using subsampling concurrently in a multi-signal environment and/or nonlinear conditions, because the replicas of the generated harmonics are folded back in the band of interest and may overlap with the desired signals. This issue was addressed in [5.1] where a universal formula for subsampling in nonlinear system was developed for single band applications. In dual band receiver applications, the main problem of subsampling is the possible overlapping between the replicas of the two desired signals in the IF frequency band. This problem was studied in [5.2] for multiband linear and non interfering environment.

As one example of application, a dual band subsampling receiver has been proposed for use in a feedback loop of a dual band transmitter for linearization purposes [5.3] using digital predistortion. In [5.4] a subsampling receiver for dual band applications was proposed, due its simplicity, to allow the cognitive radio sense different bands and check and see if they are in use. In [5.4], the designed subsampling receiver does not consider any interferers, harmonics or intermodulation effects.

This chapter extends the above study [5.3,5.4] by optimizing the SNR of concurrent dual-band signals at the receiver in a multi-signal or nonlinear environment. The requirement of increasing the analog bandwidth and reducing the effect of the folded noise leads to propose new receiver topologies with the objective of improving these features for a larger number of communication standards. Interferences and spurious signals in the received spectrum can be treated as intermodulation products using the same optimization technique that will be described later, so when these signals are subsampled the resulting aliasing components with these unwanted and spurious signals must not overlap with the desired signal.

As an additional benefit, these extra conditions used in the sampling frequency selection can lead to more relaxed RF filter requirements, due to the known unwanted signals in the spectrum will not affect the desired signal bandwidth at IF and, therefore, they will be filtered more easily after being subsampled.

Figure 5.1 illustrates a basic scheme for a concurrent dual band subsampling based receiver. It consists of low noise amplifier (LNA), S&H, ADC, and band pass filters (located in different parts of the receiver chain to filter out unwanted signals).

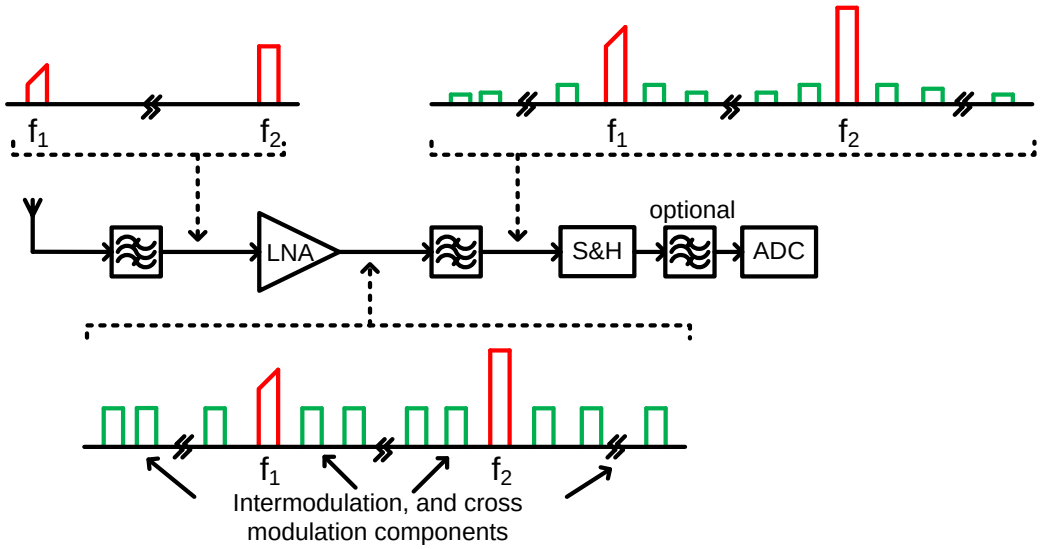

Figure 5.1 Subsampling receiver in multi-band nonlinear environment

In concurrent dual band applications, the LNA [5.5] could introduce intermodulation and cross modulation components at the receiver path right before the S&H block. Proper filtering at the receiver could attenuate the level of unwanted intermodulation components, but not completely remove them all. In subsampling based receivers, these intermodulation and cross modulation leakage signals could be a significant source of noise for the in-band signals. In fact, it depends on the selected subsampling frequency where proper and careful subsampling frequency selection could avoid the overlapping between the desired in-band signals and the unwanted intermodulation and cross modulation signals leakage through the bandpass filter.

Figure 5.1 also illustrates the signal spectra at different points of the receiver. The received signals after the first band pass filtering stage are the desired signals in each band. The purpose of this filter is to remove the signals, which exist in out of the two desired bands. This filter is critical to avoid the possibility of receiving any unwanted signal from the open spectrum at the antenna. Because of the nonlinear nature of concurrent dual-band LNA, intermodulation and cross modulation components are generated in the receiver path. The second bandpass filter attenuates as much of these unwanted

components as possible. The signals at the input of S&H are the two desired signals plus the unwanted components with signal level higher than noise floor.

The signals produced by the LNA nonlinearity can be overlapped when subsampled by the S&H. The architectures proposed in this work in order to avoid this overlapping are based on single and multiple clock techniques; where the objective is to optimize the noise performance and the flexibility of the system for use in multi-standard applications. This architecture was briefly studied at the theoretical level in [5.6]. The work presented in this thesis encompasses an analysis of the multi-signal subsampling receiver from noise and nonlinear distortion perspectives, and proposes optimized architectures to mitigate these aspects to improve the overall performance of the subsampling receiver in multi-signal environment in terms of signal quality and subsampling speed, along with an experimental validation.

5.2 Subsampling in nonlinear environments

When an input signal centered at f_1 (Figure 5.2a) [5.1] drives a nonlinear system, the output signal of this system may produce multiple spectra centered at integer multiples of f_1 (if_1 in Figure 5.2a). Moreover, each spectrum may have different bandwidths. Thus, let two spectra i and j (with bandwidths B_1 and B_2 respectively) be considered, where $j>i$ and $j-1=k$. If f_s is the sampling frequency then there must exist an integer such that [5.1]:

$$if_1 + n_k f_s \le jf_1 < if_1 + (n_k + 1) f_s \tag{5.1}$$

where $n_k = floor((jf_1-if_1)/f_s)$. Therefore, equation (5.1) will be employed in order to find the valid sampling ranges that avoid the overlapping between the multiple spectra and the desired signal.

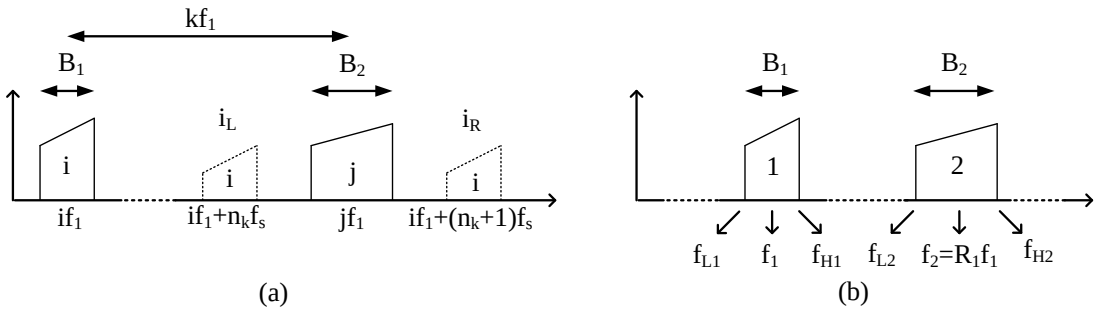

Figure 5.2 (a) Frequency locations in the sampled output spectrum and (b) Spectrum of the dual band RF signal at the input of the S&H with ratio $R_1=f_2/f_1$

5.3 Subsampling for multi-band systems

An algorithm to find the range of valid subsampling frequencies for multiband systems is presented in [5.2]. Considering the particular case of a dual-

band input spectrum as the one shown in Figure 5.2b, the subsampling frequency must be chosen to ensure that the two signals do not overlap in the subsampled domain.

From the general equations obtained in [5.2], and considering a dual band case, the maximum replica order of the lower band (n_1) meets the following equation:

$$n_1 = \left\lfloor \frac{f_{L1}}{f_s} \right\rfloor \leq \left\lfloor \frac{f_{L1}}{2((f_{U1} - f_{L1}) + (f_{U2} - f_{L2}))} \right\rfloor \tag{5.2}$$

where f_{L1} and f_{U1} are the low and the high limits of the lower band and f_{L2} and f_{U2} are the low and the high limits of the upper band. Knowing $f_2=R_1 f_1$, replica orders of the upper band (n_2) meet the following constraint [5.2]:

$$\lfloor R_1 n_1 \_ \leq n_2 \leq \lfloor R_1 n_1 + R_1 \_ \tag{5.3}$$

Therefore, the eight possible ranges for dual band applications are listed in Table 5.1 [5.2]:

Table 5.1 The boundary constraints for the dual band case

Case	Range of valid f_s	Case	Range of valid f_s
1	$\frac{f_{U2}}{n_2+1/2} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2}-f_{U1}}{n_2-n_1}\right)$	**5**	$\max\left(\frac{f_{U1}}{n_1+1}, \frac{f_{U2}}{n_2+1/2}\right) \leq f_s \leq \frac{f_{L1}+f_{L2}}{n_1+n_2+1}$
2	$\frac{f_{U2}}{n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1+1/2}, \frac{f_{L2}-f_{U1}}{n_2-n_1}\right)$	**6**	$\max\left(\frac{f_{U1}}{n_1+1/2}, \frac{f_{U2}}{n_2+1}\right) \leq f_s \leq \frac{f_{L1}+f_{L2}}{n_1+n_2+1}$
3	$\frac{f_{U1}+f_{U2}}{n_1+n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2}}{n_2+1/2}\right)$	**7**	$\max\left(\frac{f_{U1}}{n_1+1}, \frac{f_{U2}-f_{L1}}{n_2-n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2+1/2}$
4	$\frac{f_{U1}+f_{U2}}{n_1+n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1+1/2}, \frac{f_{L2}}{n_2}\right)$	**8**	$\max\left(\frac{f_{U1}}{n_1+1/2}, \frac{f_{U2}-f_{L1}}{n_2-n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2}$

5.4 Subsampling for multi-band systems in non linear environments

This section describes the algorithm employed to integrate both scenarios previously described, i.e., multi-band and non linear systems which utilize subsampling techniques. A couple of applications where this approach is useful are introduced later. Finally, an optimization about noise performance and reconfigurability in the receiver is detailed.

5.4.1 Implemented algorithm

The final sampling ranges will be given by the following expression:

$$F = F_{db} \cap F_{imd} \cap F_{cmd} \cap F_{hmd} \tag{5.4}$$

Where F is the intersection of all the valid ranges calculated from equations (5.1) and (5.2), F_{db}, F_{imd}, F_{cmd} and F_{hmd} are the valid sampling frequency sets for the fundamental signals, intermodulation, cross modulation and harmonic distortion, respectively.

In order to find F an algorithm has been developed and written in MATLAB script. This algorithm calculates these ranges and the location of the replicas where the input parameters are the fundamental frequencies, the number of harmonics (i.e., order of the nonlinearity) and the signal bandwidth. Therefore, knowing the fundamental frequencies and the number of harmonics it is possible to calculate the location of the intermodulation and the cross modulation products.

Note that a distinction between the intermodulation and the cross modulation effects will be applicable when the inputs are multi-carrier signals (or multi-channel), as shown in Figure 5.3 [5.6]. This figure illustrates the effect of a third order nonlinear system over a dual band and two-channel input signal, showing the meaning of in-band intermodulation, cross modulation and out-band intermodulation effects. However, the rest of approaches described in this chapter employ dual-band and single-channel signals as input and, therefore, F_{imd} and F_{cmd} will be treated as a unique group of frequency ranges. Finally, F_{db} will be obtained from the expressions derived from [5.1] and F_{imd}, F_{cmd} and F_{hmd} from the expressions derived from [5.2].

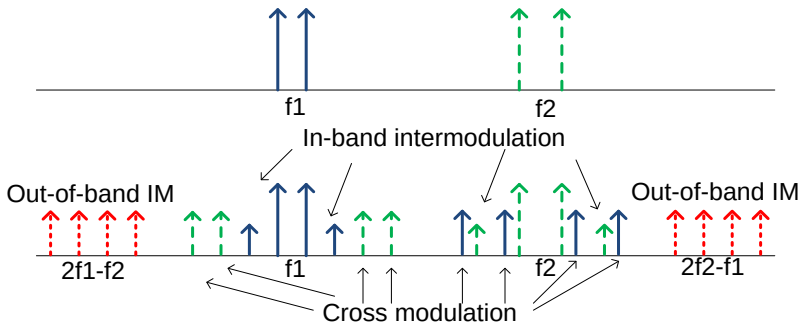

Figure 5.3 Power spectrum at the input (top) and the output (bottom) of a nonlinear system

As an example of the results obtained from this algorithm, Table 5.2 [5.6] shows the three first valid ranges immediately lower than 2 GHz for the fundamentals signals at 1.82 and 2.4 GHz, considering five harmonics and a signal bandwidth equal to 25 MHz. The subsampled spectrum is illustrated in

Figure 5.4 [5.6] for a sampling frequency equal to 2 GHz, showing that there is no overlapping between signals.

Table 5.2 Valid sampling frequencies below 2 GHz

Lower Frequency Bound (MHz)	Upper Frequency Bound (MHz)
1995	2000
1837.5	1978.33
1801.67	1802.5

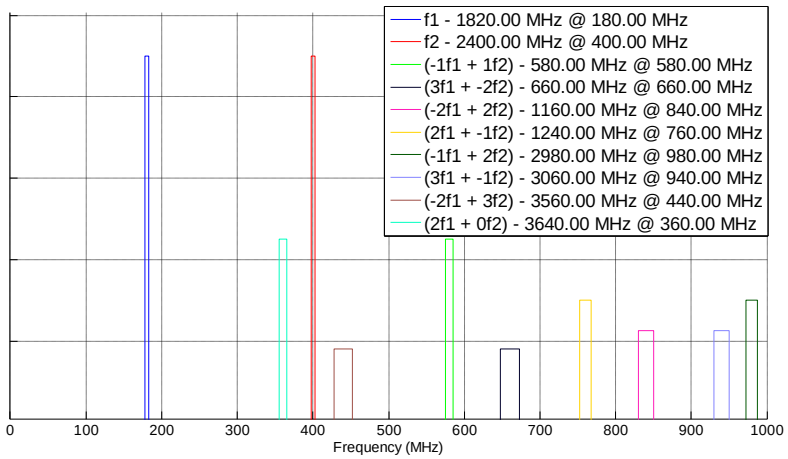

Figure 5.4 Subsampled spectrum for 1.82 and 2.4 GHz input frequency

5.4.2 Subsampling applications for multi-band and nonlinear systems

A subsampling receiver for multi-band applications is more advantageous compared to a wideband receiver because it limits the minimum sampling rate to twice the information bandwidth, instead of the Nyquist frequency [5.7]. Two applications are presented: spectrum sensing for cognitive radio applications, and selective multi-band downconversion for amplifier linearization.

The objective of this description will be to show the applicability of subsampling architectures in both sides of the transceiver, i.e., the transmitter side and the receiver side, as shown in Figure 5.5. In the transmitter side, this figure illustrates a nonlinear effect of the PA over the transmitted signal, which will be received in a feedback loop based on subasmpling in order to implement the DPD process. This scheme was detailed in Figure 3.22. In the receiver side, the received signal suffers from the LNA's nonlinearity effects before being processed by the receiver based on subsampling.

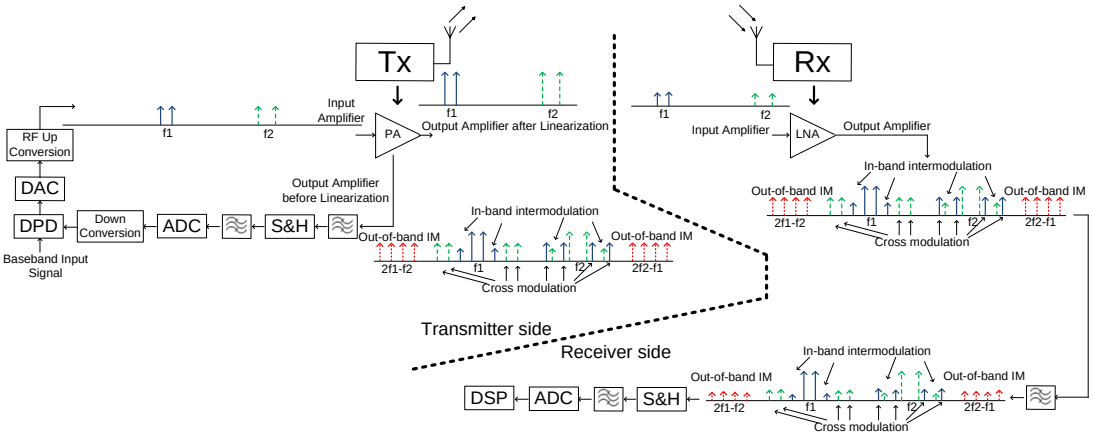

Figure 5.5 Subsampling applications for multi-band and nonlinear systems in the transmitter and receiver sides

5.4.2.1 Spectrum sensing in cognitive radio

Wireless spectrums are regulated by government bodies, and are assigned a fixed frequency slot for transmission. Studies reveal that licensed spectrums are highly underutilized and suggest a more efficient and flexible way for spectrum management [5.8]. Cognitive radio systems aim to reuse these underutilized spectrums through dynamic spectrum allocation, which must integrate a wideband/multiband receiver to scan these spectrums.

A subsampling receiver may allow the cognitive radio to sense different bands to check and see if they are in use. A bank of bandpass filters precedes the input of the receiver to control any interfering signals that may alias over the signal when using subsampling. Figure 5.6a shows a block diagram of the subsampling receiver architecture proposed in [5.4] along with its corresponding validation setup (Figure 5.6b).

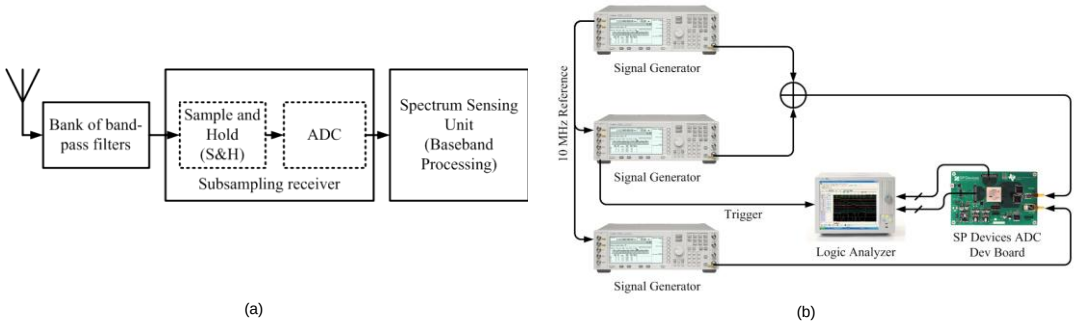

Figure 5.6 (a) Subsampling based receiver for spectrum sensing in cognitive radio systems and (b) measurement setup for validating spectrum sensing concept using subsampling receiver

As an example for spectrum sensing using a subsampling receiver, two RF bands are selected: the official digital video broadcasting band at 698-752 MHz, and an unlicensed band at 902-928 MHz. With these two bands and using the algorithm described in the previous section, a subsampling frequency of 255 MHz is selected.

Figure 5.6b [5.4] shows the measurement setup used for spectrum sensing. Two signal generators are used to obtain the two RF bands, then the bands are combined using a power combiner and passed into the receiver. A SP Devices development board using two TI ADS5474 ADCs [5.9,5.10] operating in a time interleaved manner is used as the subsampling device. A logic analyzer is used to capture the digital data streaming from the ADC board, while another signal generator provides a clock source for the ADC.

A three channel signal is sent in the DVB band, while a 2 channel signal is sent in the unlicensed band. Different power levels are configured for each channel to simulate different received signals. Figure 5.7a shows the spectra of these two bands in the RF domain. Figure 5.7b [5.4] shows the two bands subsampled using a frequency of 255 MHz. Since the ADCs are operating in a time interleaving fashion, the differences between each ADC may cause gain mismatches and timing skew [5.11].

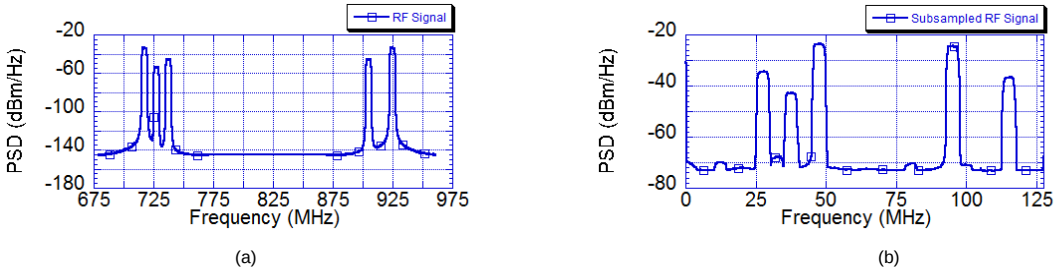

Figure 5.7 Spectra of (a) the input RF signal to the receiver and (b) the subsampled RF signal for bands (698-752 MHz, 902-928 MHz) using a subsampling frequency of 255 MHz

Figure 5.8 [5.4] shows the input signals overlaid with their subsampled output after digital demodulation. With the subsampling receiver, the captured signal has approximately a 50 dB signal to noise floor.

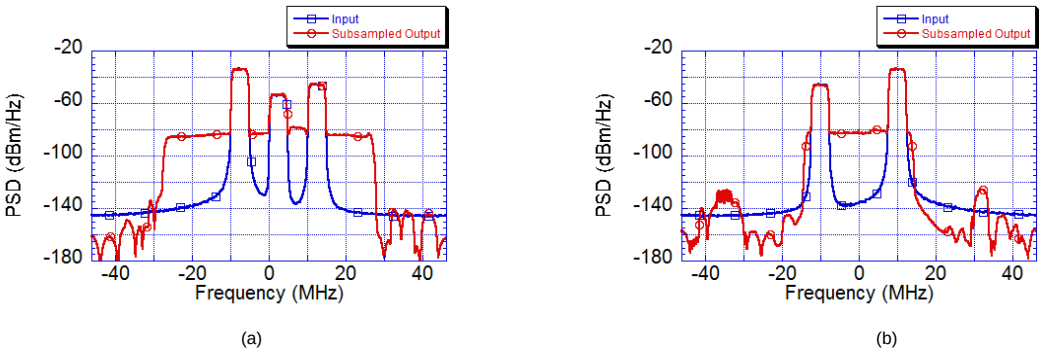

Figure 5.8 Spectra of the input and filtered output baseband signals for the 698-752 MHz band (a) and 902-928 MHz band (b)

The technique may be extended to multiple bands, where changing the subsampling clock may allow different RF bands to be demodulated concurrently. In [5.4], the cognitive radio senses up to 14 bands, sensing two bands at any given time.

5.4.2.2 Subsampling feedback loop for concurrent dual band power amplifier linearization

The power amplification (PA) unit is typically the most inefficient component in wireless transmitters. This is caused by an inverse relationship that exists between efficiency and signal quality based on the signal power being transmitted [5.12]. At low input power, efficiency is low and the amplifier operates in a linear behavior, which results in good signal quality at the amplifier output. However, operating the amplifier at its highest efficiency state close to the maximum output power causes the gain characteristics to become compressed, and the input-output relationship becomes nonlinear. The nonlinear behavior

reduces the in-band signal quality and causes out-of-band spectral regrowth. Nonlinearity is further complicated in a dual band operation, where the device produces many intermodulation and cross modulation signals. This inverse relationship causes difficulties for the wireless operator, and typically a linear operation mode is used such that signal quality is good, and spectral regrowth is minimal and does not cause interference in other channels.

Digital predistortion allows for the operation of signal in the high efficiency region while reducing spectral regrowth and improving signal quality [5.13]. This is performed by analyzing the input and output signals of the power amplifier, and generating an inverse behavioral model (predistorter) of the amplifier. The cascade of both the digital predistorter and the power amplifier results in a linear gain at the output for the full power range. The proposed architecture was illustrated in Figure 3.22 (section 3.5.2).

A dual band PA operating at 880 MHz and 1978 MHz is used to test the subsampling feedback loop for concurrent dual band linearization [5.3]. Two communication signals with 5 MHz bandwidths are sent at the center of these bands. The PA is predicted to have a 5^{th} order nonlinearity, and all the harmonics, intermodulation, and cross-modulation products up to 4 GHz are accounted. In addition, a 25 MHz guard band is placed around each band frequency to account for the spectral regrowth that will happen during the initial analysis stage.

The harmonics, cross-modulation, and intermodulation signals may be ignored; their only restriction is to not lie inside the guard band of the signals, in order to compute the regrowth effect at the DPD block when the signal is downconverted. The subsampling algorithm outlined in section 5.4.1 calculates the minimal subsampling frequency of between 619.7 MHz and 620.1 MHz. Figure 5.9a shows a simulation of the RF spectra of all the components from DC to 4 GHz, while Figure 5.9b shows the subsampled components using a frequency of 619.8 MHz [5.3].

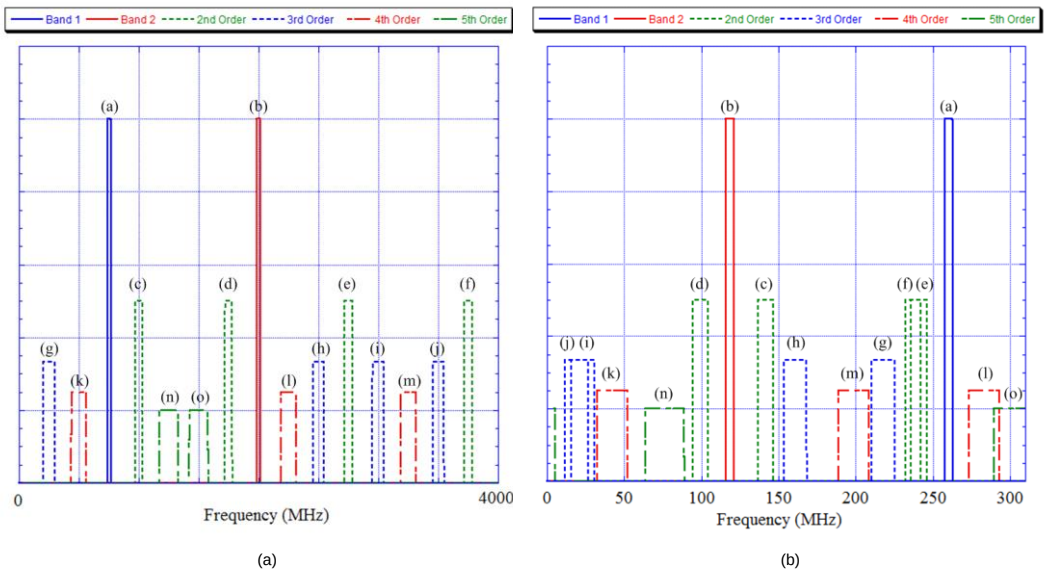

Figure 5.9 The (a) predicted RF fundamental and harmonics up to 4 GHz and (b) subsampled result using a sampling frequency of 619.8 MHz

The same setup described in Figure 5.6b is used to generate the dual band signal, and capture the RF output. Figure 5.10a shows the RF spectra at the output of the PA [5.3]. Compared to Figure 5.9a, there is an extra term *p*, which is a 7th order intermodulation product at 436 MHz. The rejection of the *i* and *j* terms are due to the design of the PA output matching network. Figure 5.10b [5.3] shows the normalized spectra of the subsampled RF PA output. There is attenuation from the upper band signal caused by the limitation of the ADC's bandwidth of 1.4 GHz. The captured time domain signal may be digital filtered and demodulated and to retrieve the amplifier output of the two bands, and further post-processing can determine the digital predistortion model.

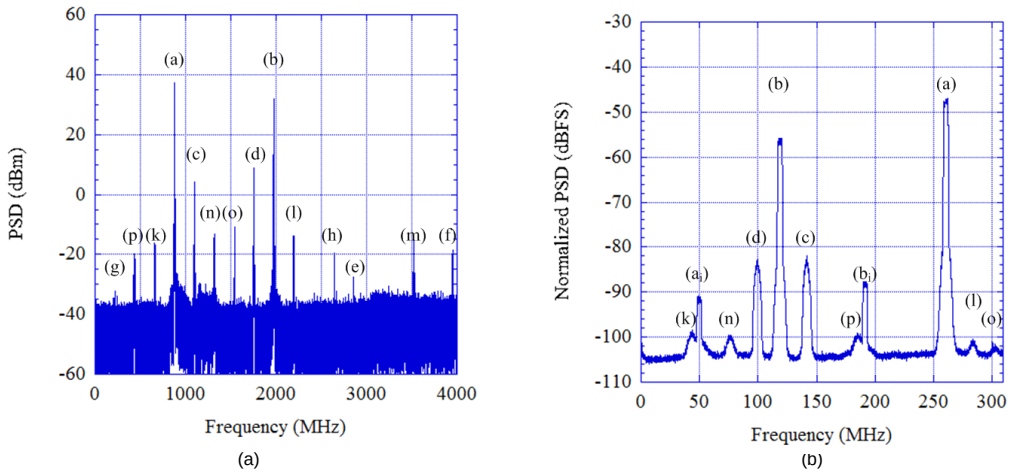

Figure 5.10 (a) RF spectra at the output of the PA and (b) normalized spectra of the captured subsampled signal using an ADC operating at 619.8 MHz

5.4.3 Optimization of dual band receivers in nonlinear environments

An analysis with the objective of noise performance optimization is presented in this section. An independent clock solution for the S&H, and ADC is proposed to limit the noise effects; and a bank of bandpass filters is used to filter out most of the aliased nonlinear and interfering components. Several different subsampling architectures and filter configurations are analysed in theoretical and measurement environments.

5.4.3.1 Subsampling for concurrent dual band and nonlinear systems using multiple clocking techniques

The receiver performance is defined in terms of noise, linearity, sensitivity, dynamic range and bandwidth [5.14]. These parameters define the applicability of a receiver to be employed for a given standard. In the case to implement a multi-standard receiver, it is necessary to maximize the analog input bandwidth and at the same time, the rest of parameters must be optimized in order to cover as many wireless communication standard requirements as possible.

This part of the thesis is focused on an optimized concurrent dual-band subsampling receiver for noise performance and versatility, in order to cover most wireless communication standards. The optimization takes advantage of the flexibility proper of subsampling, it is possible to study different valid alternatives to clock the receiver in order to maximize its noise performance.

In section 3.4 the main sources of noise in a subsampling receiver were described. Jitter noise mainly depends on the input signal frequency (which is a

characteristic of the standard), while increasing the sampling frequency can reduce the folded thermal noise. As described in section 4.3, clocking the S&H and the ADC with the same clock limits the maximum sampling frequency of the system to that of the ADC, which is usually, significantly lower than the maximum sampling frequency of the S&H. Otherwise, employing an additional higher frequency clocking the S&H it is possible to increase the SNR of the receiver. Moreover, for this dual-band application, additional degrees of freedom can be achieved using a multiple clock scheme, in order to cover a higher number of dual-band combinations of wireless communication standards.

Figure 5.11 illustrates the folded noise (green line) for the single clock (Figure 5.11a) and the multiple clock (Figure 5.11b) cases, considering for both cases the same thermal noise level at the input of the S&H (red line) and from the ADC (blue line). Since the effective noise bandwidth of the S&H is typically much larger than that of the ADC, the improvement achieved at the S&H in Figure 5.11b is usually dominant. In Figure 5.11b a BP filter will be necessary in order to decrease the out-of-band noise folded by the second subsampling process, while a LP filter with a cutoff frequency equal to $f_s/2$ is enough in Figure 5.11a. However, this BP filter might reduce the flexibility of the receiver when it is used in multi-band applications and in a nonlinear environment. This work tries to find the optimal filter bandwidth that reduces the folded noise, while avoiding a significant reduction in the number of valid sampling frequencies in order to find a high value within this range.

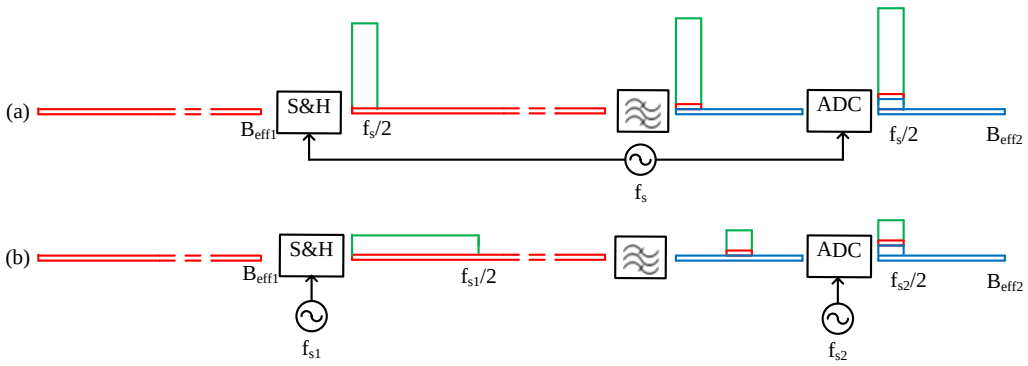

Figure 5.11 Folded noise effects using single clock (a) and multiple clock (b)

Figure 5.12 shows the effects of a third order nonlinearity when a dual band signal passes through a nonlinear subsampling receiver. In the first scenario the S&H and the ADC are clocked at the same rate. In the second scenario the clock rate of S&H and ADC has been chosen differently. Figure 5.12a presents the first scenario where both S&H and ADC are using the same clock rate. The two carrier frequencies at 880 MHz and 1.82 GHz are sampled at 400 MHz, this frequency being calculated by the algorithm described in section 5.4.1. Using this sampling frequency, Figure 5.12a also shows the different Nyquist bands at the S&H input, along which the input signals and their harmonics and

intermodulation products are distributed. The subsampled signals and their harmonics and intermodulation products are all folded to IF. After subsampling, the signal is filtered and converted to digital domain, where the Nyquist Theorem is met. Similarly, Figure 5.12b presents the scenario where the S&H and ADC use different clock rates. In order to reduce the folded noise effect, the S&H sampling frequency is increased to 2 GHz, while the input RF signal at the S&H is the same as in the case of Figure 5.12a. Since there is a second subsampling process, aliasing between the target signals and their harmonics and intermodulation products have to be avoided and, therefore, the second sampling frequency has to be carefully selected using the same method detailed in section 5.4.1. In this particular case, 400 MHz has been chosen to be the second sampling frequency.

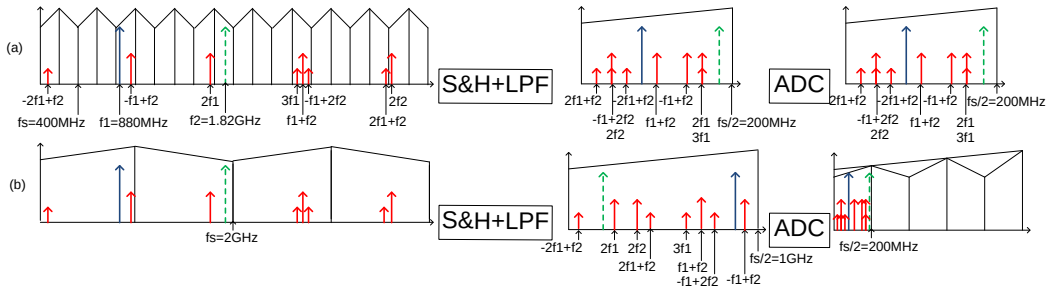

Figure 5.12 Folded effects for harmonics and intermodulation products using a single clock (a) and multiple clock (b) techniques

Besides optimizing the receiver on its noise performance, the architecture based on two independent clock sources is employed to find a valid sampling frequency for most of combinations in case of dual band RF input to a third order nonlinear receiver. From the work presented in [5.6] for some studied combinations it was not possible to find a sampling frequency without avoiding overlapping between the desired signals and their harmonics. With the objective to cover all the studied cases, a bank of filters between the S&H and the ADC was proposed to remove some harmonics in order to have more valid frequency ranges for the second sampling process. Only one filter in the bank of bandpass filters may be active at any given time. The general idea of this receiver is illustrated in Figure 5.13.

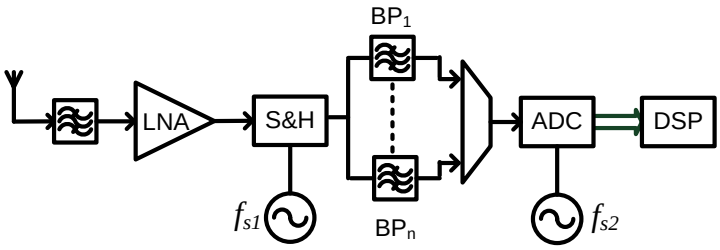

Figure 5.13 Optimized architecture based on multiple clocking and BP filters

These filters will remove some harmonics and intermodulation products relaxing the requirements to find a valid second sampling frequency. The drawback of this architecture is a more restrictive specification about where the desired signal must be folded by the S&H without being filtered. Therefore, in some cases, this restriction can lead to a low valid first sampling frequency (at the S&H), which leads to more folded noise than when an architecture without using a bank of filters is employed.

Figure 5.14 demonstrates the subsampling frequency plan selection used for the optimized architecture. First, the dual band signal's center frequencies at (f_1, f_2), bandwidths (BW_1, BW_2), and an estimate of the nonlinearity order of the system are used to predict the number of intermodulation, harmonics, and cross modulation products. Then, the algorithm outlined in section 5.4.1 generates the range of valid subsampling frequencies for the S&H, F_1. A loop is entered to find the maximum subsampling frequency (less than or equal to the S&H maximum frequency operation), where both dual band signal's subsampled IFs fall into one band pass filter in the filter bank, denoted by $BP_{selected}$. A signal's subsampled IF can be determined by the following equation:

$$f_{ifx} = \begin{cases} rem(f_x, f_{s1}) & if\ \ floor\left(\dfrac{f_x}{f_{s1}/2}\right) is\ even \\ f_{s1} - rem(f_x, f_{s1}) & if\ \ floor\left(\dfrac{f_x}{f_{s1}/2}\right) is\ odd \end{cases} \tag{5.5}$$

where f_x is the input frequency before subsampling and x is either 1 or 2, f_{ifx} is the frequency of the signal after subsampling, f_{s1} is the subsampling frequency, and rem(.) is the remainder of the division operation.

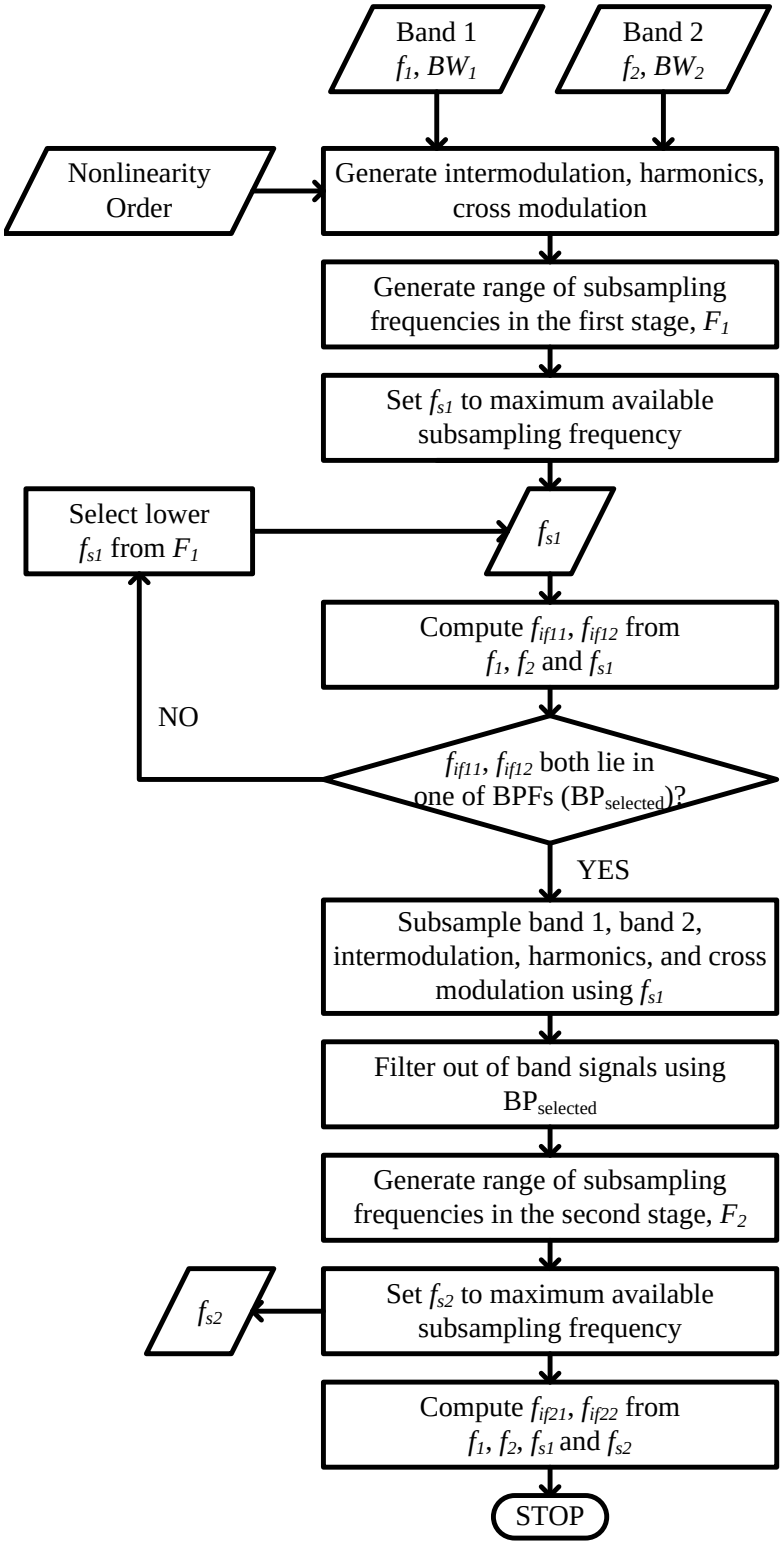

Figure 5.14 Algorithm flow diagram for computing optimal subsampling frequencies in the proposed architecture

After determining the first valid subsampling frequency, f_{s1}, all the signals generated by the nonlinearity are subsampled. The residual signals out of the bandpass filter band are removed from further analysis. The algorithm presented in section 5.4.1 is then re-used to generate another range of valid subsampling

frequencies for the ADC, F_2. The subsampling frequency for the ADC, $f_{s2,}$ will be selected as the closest to the maximum sampling frequency of the ADC within the range F_2.

5.4.3.2 Optimization of the receiver architecture

In order to optimize the noise performance of a dual band receiver in a non linear scenario a particular case has been researched in [5.6], where seven input frequencies have been selected to study the selective combinations for different dual band applications. These chosen standards are WCDMA (V) at 880 MHz, GSM-DCS at 1.82 GHz, WCDMA (I) at 2.12 GHz, Bluetooth at 2.4 GHz, WiMAX at 3.5 and 5.8 GHz, and 802.11a at 5.2 GHz.

Since the main focus is to cover the maximum number of standards, it is mandatory to use an S&H before the ADC in order to have enough analog bandwidth. The S&H features from Inphi with part number 1821TH has been selected as reference for this work, because of its high input analog bandwidth (up to 18 GHz), minimum aperture jitter (50 fs) and a maximum clock frequency equal to 2 GHz.

The first studied scenario is based on high resolution ADC with a high sampling frequency to reduce the folded noise effect. With this focus in mind the selected ADC was a 12-bit ADS5400 from Texas Instruments with maximum clock frequency of 1 GHz [5.15]. Using a sampling frequency of almost 1 GHz, it is possible to cover all the dual band applications, as illustrated in Figure 5.15a (Case 1) [5.6], where the meaning of axis x is detailed in Table 5.3. This table defines each dual-band signal scenario as the combination of two different communication standards. Using as reference the typical resolution given by the datasheets, the theoretical SNR for each dual-band scenario was estimated from equations (3.21) and (4.3), taking in account the jitter and the folded noise effects respectively.

Another option is to use a higher resolution ADC, like the 14-bit ADS5474 from Texas Instruments (Case 2 in Figure 5.15a). This device was selected because its maximum sampling frequency is 400 MHz. However, as shown in Figure 5.15a, this option is less flexible, because it is not possible to find any sampling frequency lower than 400 MHz for the first three scenarios.

In order to improve the SNR without losing flexibility, two steps subsampling approach is proposed, where the sampling frequency of S&H was set at around 2 GHz and the sampling frequency of ADC at around 1 GHz (Case 3 in Figure 5.15a). Therefore, a theoretical 3 dB improvement is achieved from equation (4.6) in respect to Case 1. However, since this first approach is implemented without BP filters, a new folded noise effect will be added from equation (4.3) because a second subsampling process may be necessary. Despite not using BP filters, note that a LP filter with a cutoff frequency equal to $f_{s1}/2$

between the S&H and the ADC is assumed in order to avoid additional folded noise at the ADC stage. Therefore, only the harmonics and intermodulation products located in this part of the spectrum will be used to calculate the valid second sampling frequency f_{s2}.

The last option is to use a multiple clocking architecture employing the ADS5474 (Case 4 in Figure 5.15a) and a first sampling frequency around 2 GHz. Theoretically the SNR is improved around 7 dB from equation (4.6) in respect to Case 2. However, due to the absence of a BP filtering stage, a new folded noise effect at the ADC must be added again.

Table 5.3 Dual band signal construction table

	Dual band signal scenarios											
Standard	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
WCDMA (V) **880 MHz**	x	x	x	x	x	x						
GSM-DCS **1.82 GHz**	x						x	x	x	x	x	
WCDMA (I) **2.12 GHz**		x					x					x
Bluetooth **2.4 GHz**			x					x				x
WiMAX **3.5 GHz**				x					x			
802.11a **5.2 GHz**					x					x		
WiMAX **5.8 GHz**						x					x	

For the rest of combinations of frequencies, the curves present the same tendency, making it possible to cover all the scenarios. However, since cases 2 and 4 present the best results about SNR the next step will be to cover all the dual band applications for these cases. The proposed solution is to use a bank of BP filters between the S&H and the ADC. This solution will be applied to Case 4, because it has more flexible architecture, with a higher number of available valid

ranges. Using this solution, some harmonics will be removed and the flexibility of the receiver will be increased.

A feasible solution proposed in [5.6] is based on two filters, which their band-pass ranges are [0-400] and [400-800] MHz. The maximum sampling frequency was selected in order to have both fundamental replicas in each range. The selected filter corresponds to the higher of these two frequencies (Case 5 in Figure 5.15b [5.6]).

Another solution is to fix a unique BP filter for all the applications (Cases 6 and 7 in Figure 5.15b). In these cases it is possible to cover almost all the standards with only one of these filters, without considerably reducing the resolution. Although, in order to maximize the flexibility and the SNR, the optimal architecture is based on the alternation of several BP filters, for a more concrete application or more relaxed SNR specifications a single BP filter could be used in order to reduce the complexity of the system.

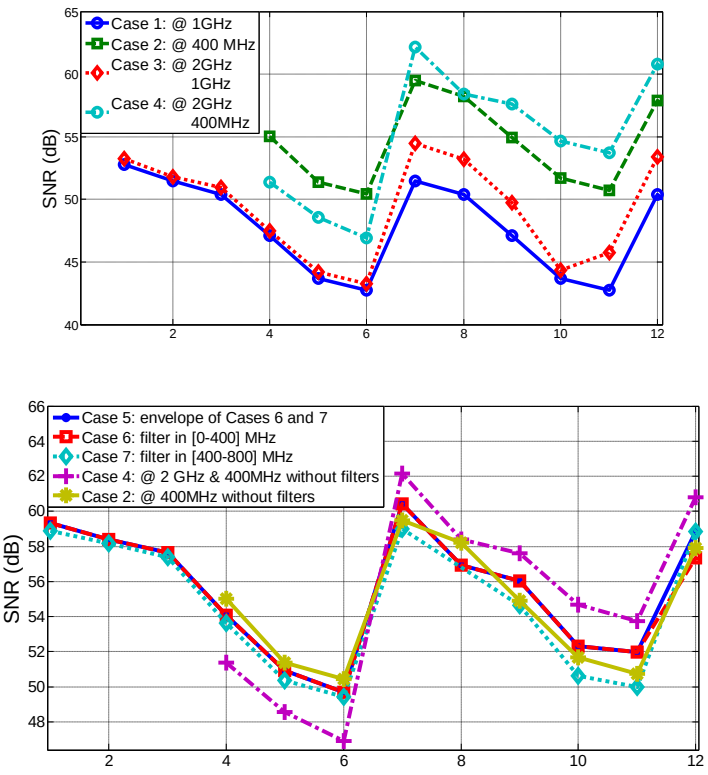

Figure 5.15 Expected SNR (a) for single and multiple clock architectures and (b) for different architectures based on BP filters

5.4.3.3 Experimental validation

An experimental validation using realistic wireless communication scenarios is used below to demonstrate the robustness and appropriateness of proposed technique in multi-standard environment. The seven input frequencies chosen to study the selective combinations for different dual band applications

corresponds to the standards studied in section 5.4.3.2, the grouping for two given bands being showed by Table 5.3.

The experimental setup is illustrated in Figure 5.16. The dual band signals are continuous wave signals to demonstrate the peak SNR that can be achieved, and each signal band is generated by independent Agilent PSG E8257D signal generators [5.16]. A power combiner combines both signal sources into a dual band signal, is amplified using a LNA ZX60-6013 from Minicircuits [5.17], and subsampled by an S&H Inphi 1821TH, and a ADS5474 ADC from Texas Instruments. The signal generator used as clock sources for the S&H and the ADC are the Agilent E8663D [5.18] and the Rohde & Schwarz SMIQ [5.19]. The implemented receiver architecture's design is shown in Table 5.4.

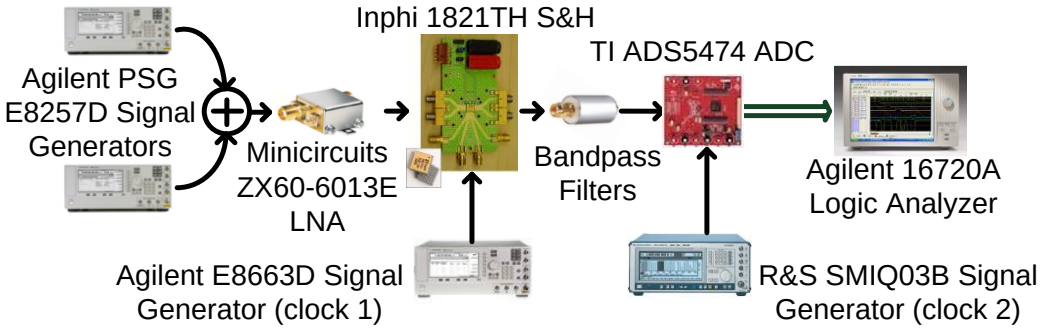

Figure 5.16 Experimental setup for dual band subsampling receiver

Table 5.4 Subsampling receiver's architectures

Receiver Design (RD)	**Receiver's Architecture**
2	Fs1=fs2<400 MHz, without bank of filters
4	Fs1<2 GHz, fs2<400 MHz, without bank of filters
5	Fs1<2 GHz, fs2<400 MHz, with a bank of two filters in [0-400] and [400-800] MHz
6	Fs1<2 GHz, fs2<400 MHz, with a filter fixed in [0-400] MHz
7	Fs1<2 GHz, fs2<400 MHz, with a filter fixed in [0-400] MHz
8	Fs1<2 GHz, fs2<400 MHz, with a filter fixed in [0-200] MHz

The simulated subsampled spectra for RF signals at 2.12 GHz and 2.4 GHz (dual band scenario 12, Receiver Design 4) are shown in Figure 5.17, where the expected bandwidth of each dual band signal is 5 MHz, and a 5th nonlinearity order. The S&H subsampling frequency was set to 1900 MHz, and the ADC subsampling frequency was set to 400 MHz. Figure 5.18 shows the captured output spectrum using the experimental setup. The subsampled signals, their harmonics and intermodulation products are located as predicted by the simulation illustrated in Figure 5.17.

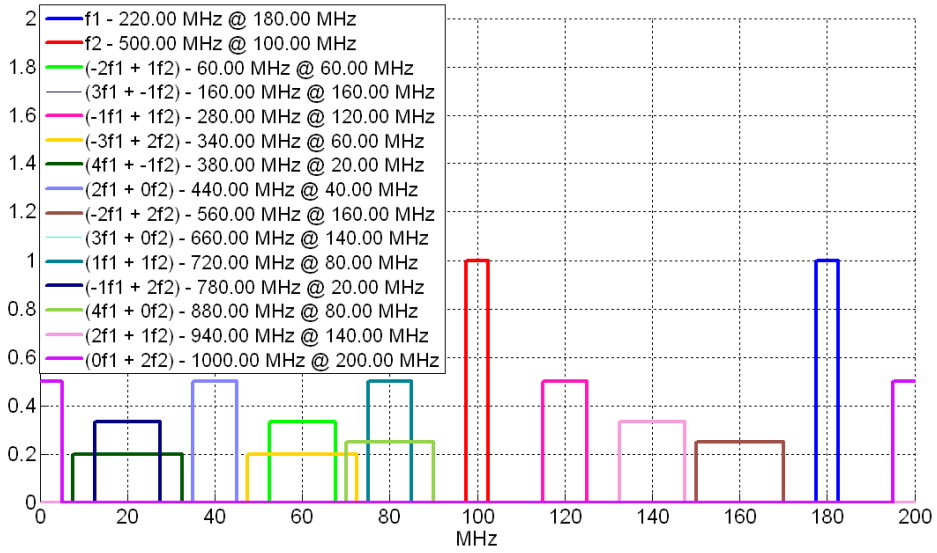

Figure 5.17 Simulated spectra after two-stage subsampling process, using an S&H subsampling frequency of 1900 MHz, ADC subsampling frequency of 400 MHz, and signal bands at 2.12 GHz and 2.4 GHz

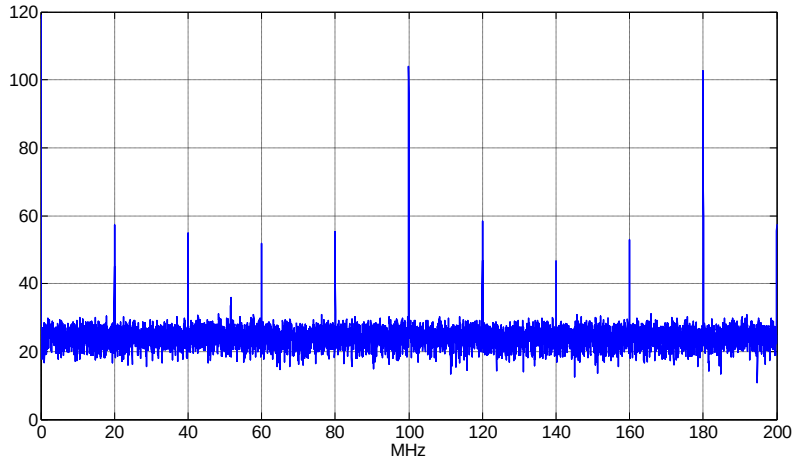

Figure 5.18 Experimental spectra after two-stage subsampling process, using an S&H subsampling frequency of 1900 MHz, ADC subsampling frequency of 400 MHz, and signal bands at 2.12 GHz and 2.4 GHz

These experiments are intended to validate the design optimization approach proposed in this chapter. Figure 5.19 shows the theoretical SNR for the

proposed architectures [5.6]. The SNR values reported are the lower of the two SNR (worst case) in the concurrent dual band application, and each dual band scenario is from Table 5.4. Figure 5.20 shows the measured SNR for 12 different dual band signal scenarios. Both families of curves have the same tendency as shown in Figure 5.19 and Figure 5.20; and the measured values have on average 3 dB reduction in SNR values compared with theoretical ones.

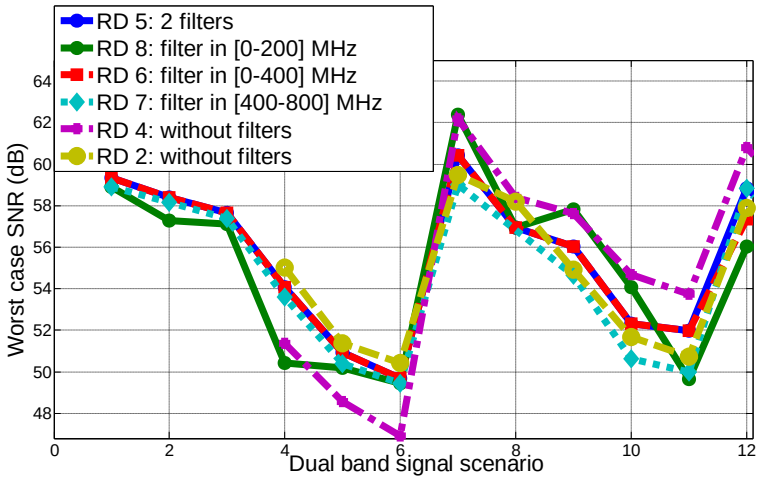

Figure 5.19 Theoretical SNR for the proposed architectures

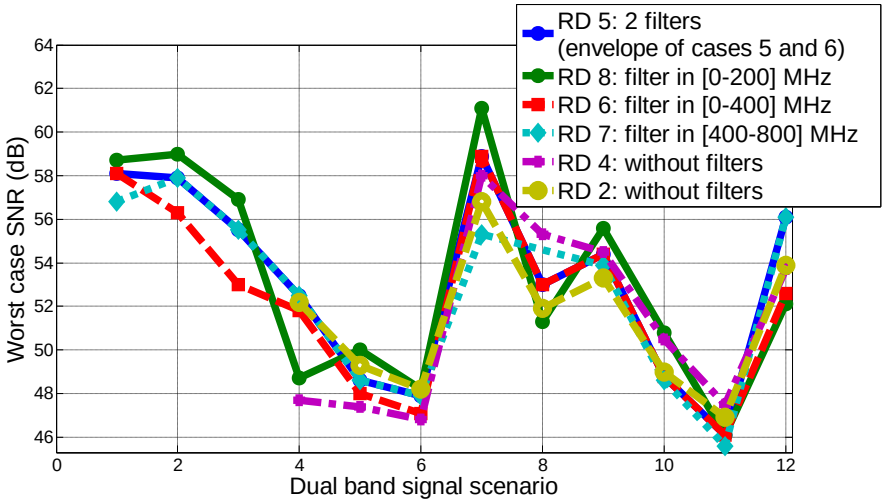

Figure 5.20 Experimental SNR for the proposed architectures (for design 2 and 4, no sub-sampling frequency could be found for scenarios 1, 2 and 3)

In order to observe the difference between the expected and obtained results, Table 5.5 shows the SNR for two concrete dual band applications (dual band scenarios 7 and 11).

Using a multiplexed bank of filters (RD 5) presents more advantages and leads to better signal quality than receiver designs with fixed filters (RD 6/7). The pros for these filter architectures (either fixed or multiplexed) are the elimination of a higher number of harmonics and the reduction of the out-of-band noise in the

input ADC. However, when using any of these filter architectures where the carrier RF separation for the two bands is relatively small, it is more difficult to find a high sampling frequency that folds both bands into one band-pass filter and, therefore, the effect of folded noise increases. It is possible to observe this problem in some dual-band scenarios using RD 8. Taking into account all these considerations, dual filter band-pass architecture seems to be an effective solution that offers reasonable performance without a sharp increase in the complexity (numbers of filters) for well frequency spaced dual-band wireless applications.

Table 5.5 Comparative between expected and experimental SNR

	Receiver Design					
	2	**4**	**5**	**6**	**7**	**8**
Theoretical SNR (dB) for dual band signal scenario 7	59.5	62.2	60.4	60.4	59	62.4
Experimental SNR (dB) for dual band signal scenario 7	56.8	58	58.9	58.9	55.3	61.1
Theoretical SNR (dB) for dual band signal scenario 11	50.7	53.7	51.9	51.9	50	49.7
Experimental SNR (dB) for dual band signal scenario 11	46.9	47.5	46.1	46.1	45.6	46.1

5.5 References

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[5.16] E8257D PSG, *Microwave Analog Signal Generator*, Agilent Technologies. Datasheet.

[5.17] ZX60-6013E, *Connectorized Amplifier 50 Ω*, Minicircuits. Datasheet.

[5.18] E8663D PSG, *RF Analog Signal Generator*, Agilent Technologies. Datasheet.

[5.19] SMIQ, *Vector Signal Generator*, Rohde & Schwarz. Datasheet.

CHAPTER 6

CONCLUSIONS AND POSSIBLE FUTURE DIRECTIONS

CHAPTER CONTENTS

This chapter presents the main conclusions and contributions of this thesis and describes the possible future directions.

6.1 Conclusions

This thesis exploits the benefits of the subsampling based systems to be to the RF down-conversion stage in receivers for Software Defined Radio (SDR). There are three distinguishable contributions in this thesis work that come from the data acquisition design for testing wideband multi-standard purposes, the noise performance optimization from multiple clocking techniques, and extension of subsampling techniques to multi-band and non linear environments. All these contributions have been theoretically studied and experimentally validated.

Since the SDR objectives can only be obtained with a receiver whose front-end accommodates a wide range of frequency bands and channel bandwidths, subsampling architectures are presented as a feasible alternative to the different possible receiver architectures reviewed in Chapter 1. Moreover, a subsampling scheme has been selected because it leads to extremely flexibility and simplicity, the reduction of the number of components to a minimum being a key when the same receiver has to process different standards. In addition, since the digitization stage will be placed just after the antenna by using subsampling techniques, most of the signal processing will be performed in the digital domain, thus avoiding the limitations of the current ADCs. Therefore, the proposed architecture reduces the number of analog of building blocks, and relaxes the specifications of the ADC, which is the current bottleneck towards a fully digital multi-standard software radio.

After describing the subsampling idea in Chapter 2, detailing the main non idealities proper of these techniques (i.e., jitter noise and folded thermal noise), Chapter 3 discusses the usefulness and potential of subsampling technique to design a simple and flexible universal receiver. A data acquisition module for testing wireless receivers based on subsampling has been presented which covers most present wireless communication standards requirements with only one single board. Experimental results of the proposed module show (for a 20 MHz signal bandwidth) an ENOB higher than 8 bits up to 5 GHz center frequency. Another characteristic of the implemented module is its simplicity, with only a few components on a printed-circuit board. These results show that, for testing purposes, the subsampling based receiver is a viable alternative to other typical receiver architectures, with enhanced reconfigurability and programmability.

As a second main contribution, the noise performance of the subsampling based receiver has been optimized by using a novel method based on multiple clocking techniques in order to reduce the folded noise effect. An analytical expression for the improvement factor in the SNR with respect to the single-clock solution has been obtained. Finally, a new version of the data acquisition module for testing of wireless receivers has been presented. For the selected frequency plan, with two successive subsampling processes, the ENOB has been shown to improve in approximately 0.5-1 bit. Experimental results show, for a 20 MHz

signal bandwidth, an ENOB of more than 9 bits up to 2.9 GHz, and more than 8 bits up to 6.5 GHz center frequency. Measurement results show that the design covers the most important wireless standards (i.e., GPS, GSM, GPRS, UMTS, Bluetooth, Wi-Fi, WiMAX) in terms of tuning frequency and noise performance.

As a third main contribution, the subsampling concepts have been extended for multi-band and nonlinear systems, where there is an additional problem about the harmonics and different channel which might be folded in the band of interest. After the challenges and issues on finding the valid subsampling frequencies in multi-band and nonlinear systems have been discussed, an optimized design approach for a concurrent dual band multi-standard subsampling receiver in a nonlinear and / or interfering environment has been presented, proposing a multi-filter architecture along with dual subsampling process. In addition, an efficient algorithm has been developed in order to find the valid sampling frequencies, increasing the flexibility of the receiver and covering the maximum number of dual band applications for different communication standards. As an additional advantage, these conditions used to select the valid sampling frequency can lead to more relaxed RF filter requirements. Experimental results proved the feasibility and the advantages of the proposed architecture, which can be used for different functionalities in a wireless communication transceiver, on both the transmitter and the receiver side.

6.2 Possible future directions

Firstly, future works will be intended to integrate all these contributions in a unique data acquisition board for multi-standard and multi-band testing purposes. Therefore, implementing the designed bank of filters between the S&H and the ADC, it will be possible to extend the functionality of the PCB to multi-band and nonlinear environments.

Another further objective to improve this thesis work will be the implementation of an autonomous prototype. A FPGA will be included in the board to autonomously select the optimal sampling frequency and the optimal filter bandwidth from the developed algorithms, instead of carrying out these tasks by an external computer. Also, this FPGA will perform the required digital signal processing, potentially increasing the usefulness of including this component.

The selected sampling frequency will be used to program a VCO in order to increase the autonomy of the board, avoiding use of an external clock generator. Nevertheless, when the second sampling frequency is not multiple of the first sampling frequency, a second VCO will be necessary, increasing the complexity and the total power consumption. Therefore, other future approach will be to extend the algorithm for dual-band and nonlinear scenario in order to find a new sampling frequency plan based on two multiple frequencies, which reduces the power consumption avoiding a significant noise performance penalty.

Moreover, these researches can be associated to other current projects. Besides increasing the autonomy by using a unique data acquisition board, a second main future challenge is to utilize the optimized dual-band receiver within a current project developed by the *iRadio Labs*, from the University of Calgary. This project includes a subsampling receiver in a feedback loop of a dual-band transmitter for linearization purposes, as described in Chapter 4. Therefore, the focus will be to improve the noise performance in the receiver, avoiding the drawbacks of the previous work (described in section 5.4.2.2), such as the presence of additional spurious due to use an interleaved ADC architecture, or a low analog bandwidth that limits its usefulness for multi-standard applications.

In addition, the final objective of this project consists of a whole transmitter design whose promising validation will be implemented by COTS. Using subsampling, the S&H and the ADC implement the feedback loop for linearization, whereas a DAC is used to set the baseband I-Q signals previously to be modulated. A FPGA is connected to both daughter boards, implementing the digital pre-distortion process and the signal generation from the connection with the ADC and the DAC, respectively. The interface between the FGPA and the daughter boards has already implemented, as well as the communication with an envelope modulator employed to increase the efficiency of the power amplifier.

On the other hand, an alternative to clock the receiver by using VCOs is utilizing a clock generator board based on direct digital synthesizers (DDSs), which is being currently designed within a project developed by the Electronics Engineering Group, from the University of Seville, and the company AT4 Wireless. Clocking the proposed receiver with this generator can be a feasible alternative when a *frequency hopping* implementation is required, in order to receive different input signals by rapidly switching the carrier among many wireless communication standards.

CHAPTER 7

APPENDIX A: DATA ACQUISITION SYSTEMS BASED ON INTERLEAVING TECHNIQUES

CHAPTER CONTENTS

The idea of connecting several ADCs in parallel is to maximize the total data acquisition rate. In this appendix these architectures will be introduced, focusing this description on their advantages and inconveniences, such as the

mismatches errors between the interleaved ADCs, which will need to be compensated. These theoretical concepts will be validated at simulation and experimental levels. Finally, special attention is devoted to the published corrections methods from a bibliographic study detailing the most appropriate calibration techniques in terms of power consumption or digital processing capabilities.

7.1 Theory of operation

7.1.1 Interleaving idea

A time-interleaved ADC operates *M* parallel ADCs at different sampling times, such as illustrated in Figure 2.15 [7.1]. Ideally, the *ith* ADC, $i = 0, ..., M - 1$, samples periodically the input signal at time instants t_i, t_{i+M}, t_{i+2M}, with sample rate f_s/M, where $t_m=mT_s$ and $T_s=1/f_s$ is the sampling period of the time-interleaved ADC. The final output is created by multiplexing all of the individual ADC outputs in the proper order (e.g. ADC_0, ADC_1, ..., ADC_{M-1}, ADC_0, ADC_1, ...). Therefore, the final effect is as if the input signal were sampled once every T_s seconds, i.e., with sample rate f_s.

Although the data acquisition rate is increased without penalty over other ADC features, these systems present several disadvantages. Firstly, it should be noted that each individual ADC deals with the entire analog input signal, and, therefore, its S&H circuit must be able to preserve the full input signal bandwidth. Secondly, different spurs are caused by the mismatches between ADCs, its location in the spectrum being predicted in the next section.

7.1.2 Analysis of time-interleaved ADCs

Let $x(t)$ be an analog signal with Fourier transform $X_a(\omega)$. Consider that the time-interleaved ADC outputs the sequence:

$$x(t_0), x(t_1), x(t_2), ..., x(t_m), ..., x(t_M), x(t_{M+1}), ... \tag{7.1}$$

Define the discrete-time Fourier transform by[10]:

$$X(\omega) = \Sigma x(t_k) \exp(-j\omega t_k) \tag{7.2}$$

Ideally, the samples are spaced T_s seconds apart. Then, it can be shown that:

$$X(\omega) = f_s \Sigma X_a(\omega - k2\pi f_s) \tag{7.3}$$

which is the well-known spectrum representation of a uniformly sampled signal. It results in a periodic spectrum with a period equal to the sampling rate [7.2].

[10] In the literature, it is a common notational practice to replace ωt_k with a single variable $\omega' = \omega t_k$, called *normalized frequency*. Since ω represents ordinary frequency (radians per second), ω' is expressed in units of radians (per sample). Recall also that by sampling the discrete-time Fourier transform, we obtain the discrete Fourier transform (DFT) [7.1].

In practice, however, there are deviations from the ideal behavior that are caused by the mismatches between the individual ADCs. There are three main possible sources of error in time-interleaved ADCs: clock timing errors, gain errors and offset errors [7.3]. A brief review of each of them is included in the next sections.

7.1.2.1 Clock timing errors

Clock timing errors occur when the digitization clocks of the individual ADCs are not appropriately synchronized. As a result, the input signal *x(t)* is sampled in such a way that the sampling time instances are not necessarily uniformly spaced in time. Errors may be systematic (skew) or random (jitter). Taking this factor into account, equation (7.3) becomes [7.2]:

$$X(\omega) = f_s \Sigma H_k(\omega) X_a(\omega - k2\pi f_s / M) \tag{7.4}$$

where:

$$H_k(\omega) = (1/M)\Sigma \exp(-j[\omega - k(2\pi / MT_s)]r_m T_s) \exp(-jkm(2\pi / M)) \tag{7.5}$$

where $r_m=(t_m-mT_s)/T_s$ is a ratio that measures the timing errors (ideally, $t_m=mT_s$).

It can be noticed that, in contrast with the ideal case, the spectrum is repeated in equation (7.4) every integer multiple of the frequency f_s/M (not f_s). In other words, spurious replica spectra (called image spurs) will appear at [7.1]:

$$f_{imagspurs} = \pm f_i + kf_s / M, \quad k = \pm 1, \pm 2, \pm 3, \ldots \tag{7.6}$$

These replicas hamper the interpretation of the spectrum of the input signal, as they may be confounded with true signal's frequency components. In addition, even if the image spurs are eliminated, we find that the spectrum of the signal reconstructed from the given samples is equal to $H_0(\omega)X_a(\omega)$. This is equivalent to passing the original input signal through a filter of transfer function $H_0(\omega)$, which introduces distortion and should be corrected by an equalizer.

Assuming that the input signal is a pure tone of frequency f_i, and that the phase skew error is a normally distributed random variable with zero-mean and variance σ_t^2, the SDNR is approximately found to be [7.4]:

$$SDNR = 20\log(1/\sigma_t 2\pi f_i) - 10\log(1 - 1/M) \tag{7.7}$$

7.1.2.2 Gain errors

The gains of each ADC may be different. As a result, for a dc input (to cite just a simple example) each ADC may produce different output code. The analysis is similar as for timing errors. Gain errors also produce image spurs at:

$$f_{imagspurs} = \pm f_i + kf_s / M, \quad k = \pm 1, \pm 2, \pm 3, \ldots \tag{7.8}$$

where f_i is the input frequency. If the gain error is a normally distributed random variable with mean a and variance σ_a^2, the SDNR can be approximated as [7.4]:

$$SDNR = 20\log(a/\sigma_a) - 10\log(1 - 1/M) \tag{7.9}$$

7.1.2.3 Offset errors

The offsets of each ADC may be also different. As with the gain mismatch case, a dc input may also produce different outputs. Offset errors cause noise peaks (offset spurs) at:

$$f_{offspurs} = kf_s / M, \quad k = 0, 1, 2, 3, \ldots \tag{7.10}$$

Assuming that the offset error is a normally distributed random, with zero-mean and variances σ_o^2, and that the input signal is a sinusoid, the SDNR equals to [7.4]:

$$SDNR = 20\log(1/\sigma_o) \tag{7.11}$$

which is independent of the number of the degree of interleaving M.

7.2 Time-interleaved ADCs validation

7.2.1 Validation at simulation level

At first set of simulations was addressed to corroborate the analytical expressions about the spurs location given in section 7.1.2. By using MATLAB software, systems based on two, three and four individual ADCs in parallel were simulated. Their output spectrums are illustrated in Figure 7.1, Figure 7.2 and Figure 7.3, respectively. It is possible to observe how the spurs location into the Nyquist band is as expected from the theoretical expressions.

These errors have been simulated by using Gaussian random variables[11] with values for which the SNDR obtained from equations (7.7), (7.9) and (7.11) is 50 dB approximately for a dual ADC architecture. The SNR will be slightly lower when a higher number of ADCs is used, due to the *-10log(1-1/M)* factor.

[11] Finally, a jitter effect was introduced at simulation level, in order to simulate a more real system.

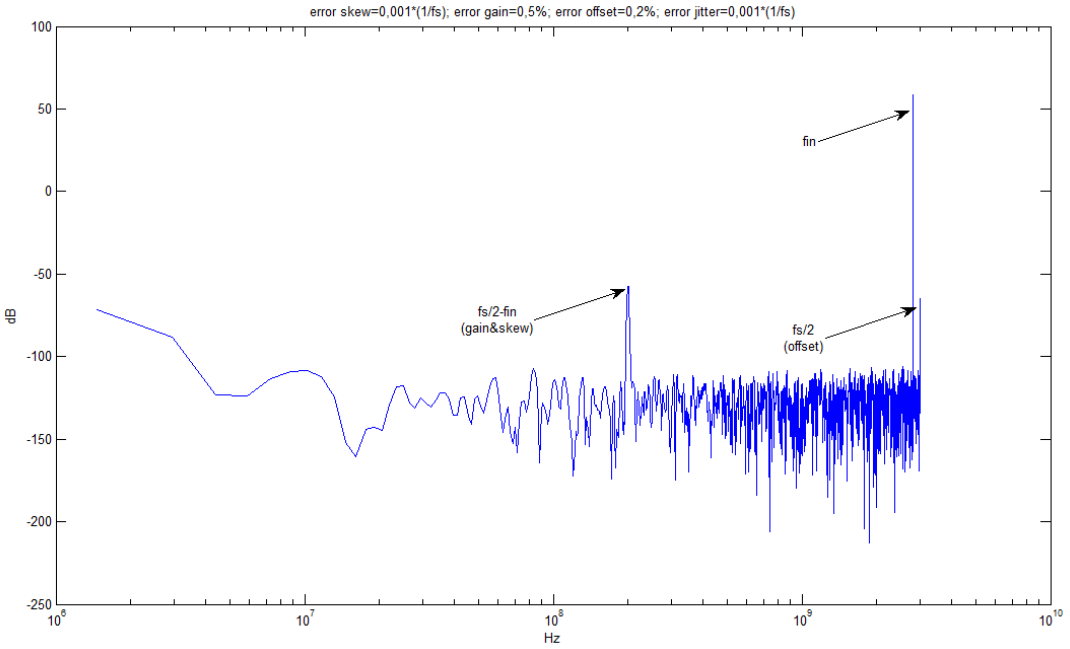

Figure 7.1 Output spectrum of 2-interleaved ADCs (f_c=6 GHz, f_s=2.8 GHz)

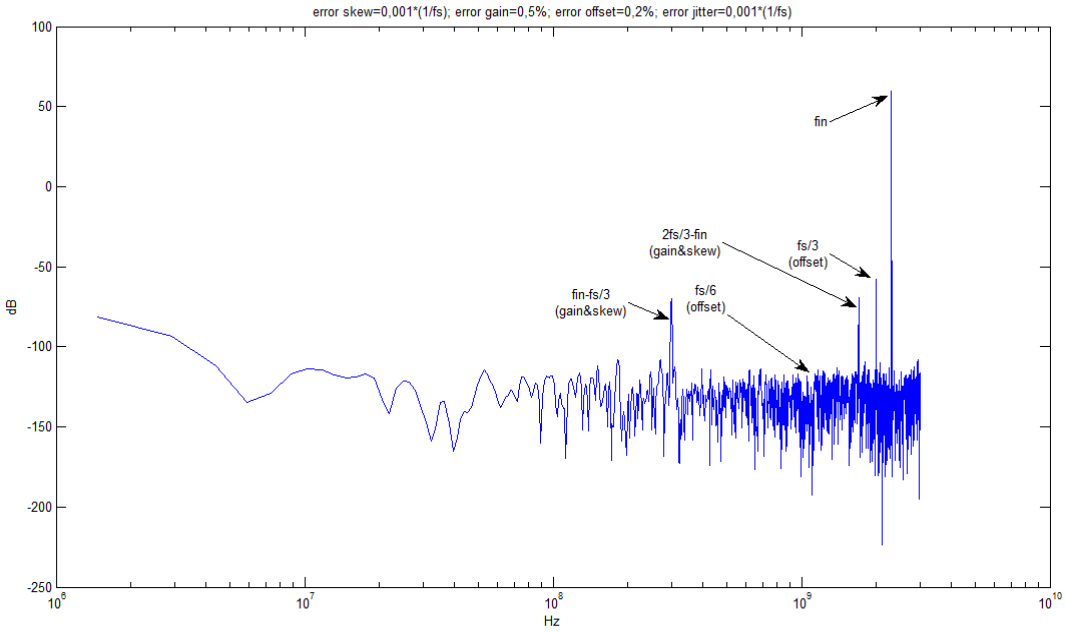

Figure 7.2 Output spectrum of 3-interleaved ADCs (f_c=6 GHz, f_s=2.3 GHz)

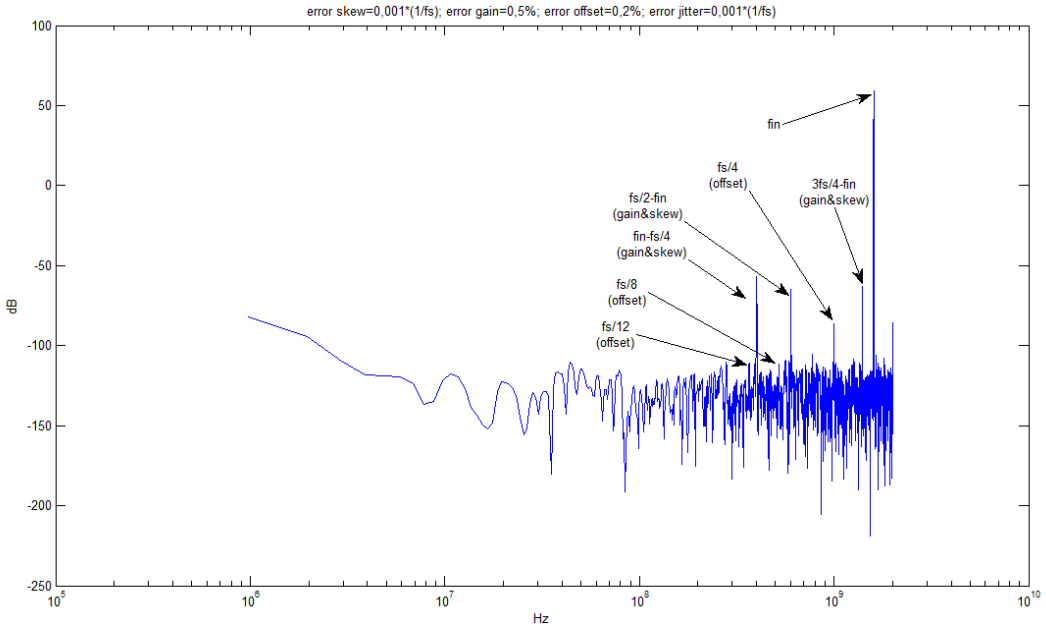

Figure 7.3 Output spectrum of 4-interleaved ADCs (f_c=4 GHz, f_s=1.6 GHz)

Note that all the possible spurs studied in section 7.1.2 are not located into Nyquist band for three and four ADCs cases. For a 3-ADCs implementation some of these spurs will be located into Nyquist band if the conditions listed below are met[12]:

- Spur located at $f_{in}+f_s/3$ if $f_{in}<f_s/6$
- Spur located at $2f_s/3-f_{in}$ if $f_{in}>f_s/6$
- Spur located at $f_s/3-f_{in}$ if $f_s/3<f_{in}<f_s/3$
- Spur located at $f_{in}-f_s/3$ if $f_{in}>f_s/3$

For a 4-ADCs implementation the following spurs can be visualize at Nyquist band:

- Spurs located at $f_{in}+f_s/4$ and $f_s/4-f_{in}$ if $f_{in}<f_s/4$
- Spurs located at $f_{in}-f_s/4$ and $3f_s/4-f_{in}$ if $f_{in}<f_s/4$

7.2.2 Validation at experimental level

The experimental characterization was implemented by using the board EV8AQ160 from E2V [7.5]. This system is based on the connection of four interleaved ADCs in order to obtain a maximum sampling rate of 5 GHz, with a theoretical resolution higher than 7 bits. At this frequency, each individual ADC is

[12] The remaining possible spurs will be located into Nyquist band for any case.

clocked at 1.25 GHz, being the unique external clock frequency equal to 2.5 GHz, which is divided by 2 on board, distributed and phased 90º to the different ADCs.

The calibration of the gain, offset and clock skew parameters will be implemented via serial peripheral interface (SPI). In addition this port is controls other parameters, such as the operation mode (1, 2 or 4 channels) or the analog bandwidth. By using a de-multiplexer, the maximum output digital rate is equal to 625 MHz, being possible to read the digital data by the logic analyzer.

As an example, Figure 7.4 shows the output spectrum without implementing calibration using an input frequency equal to 510 MHz and sampling at 5 GHz. The generated spurs due to the gain and skew mismatches are three: at 1760 MHz (k=1 in equation (7.6) being M=4), 1990 MHz (k=2) and 740 MHz (k=3), whereas the main spur generated by the offset error is located at 1250 MHz.

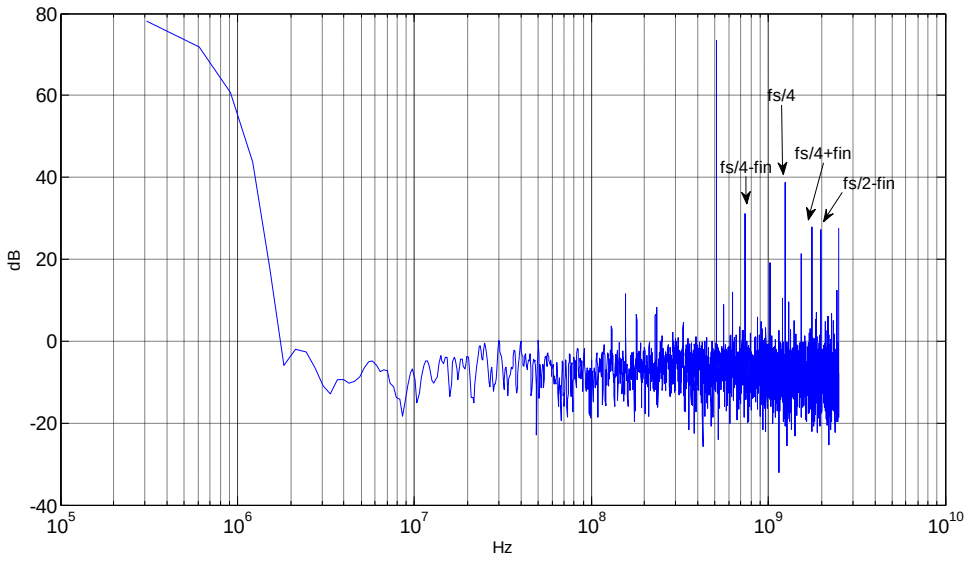

Figure 7.4 Output spectrum without implementing calibration

If these ADCs are calibrated in pairs (ADCs *A*-*B* and ADCs *C*-*D*), it is possible to identify the expected spurs for a dual ADC system (k=1, M=2) at the output spectrum, as shown in Figure 7.5.

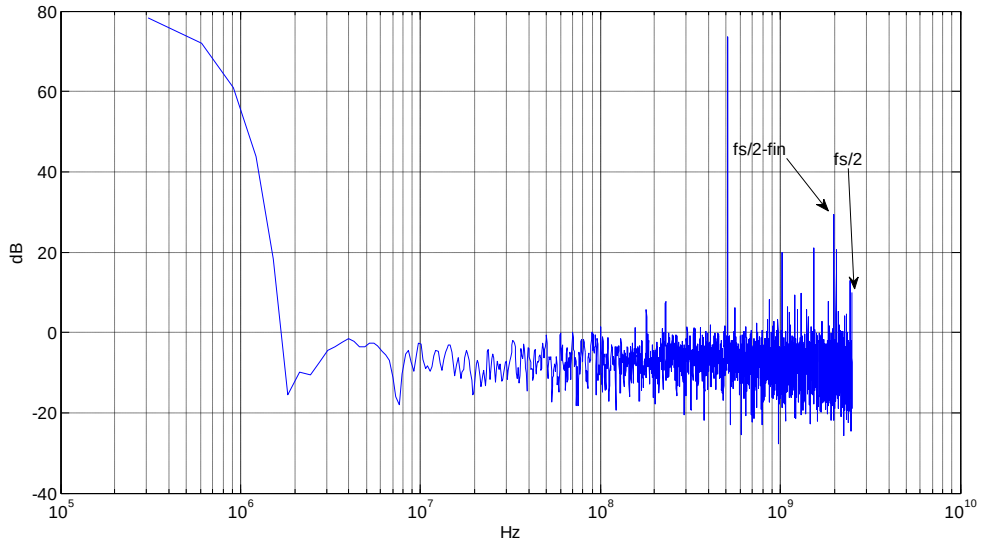

Figure 7.5 Output spectrum after calibrating two couples of ADCs

Finally, the total resolution integrating in the whole Nyquist band (2.5 GHz) is illustrated in Figure 7.6 in function of the input frequency. Sampling at 5 GHz, the implemented data acquisition system achieves a resolution of 6-7 bits up to 1.6 GHz and 5.4-6 bits up to 2.5 GHz input frequency.

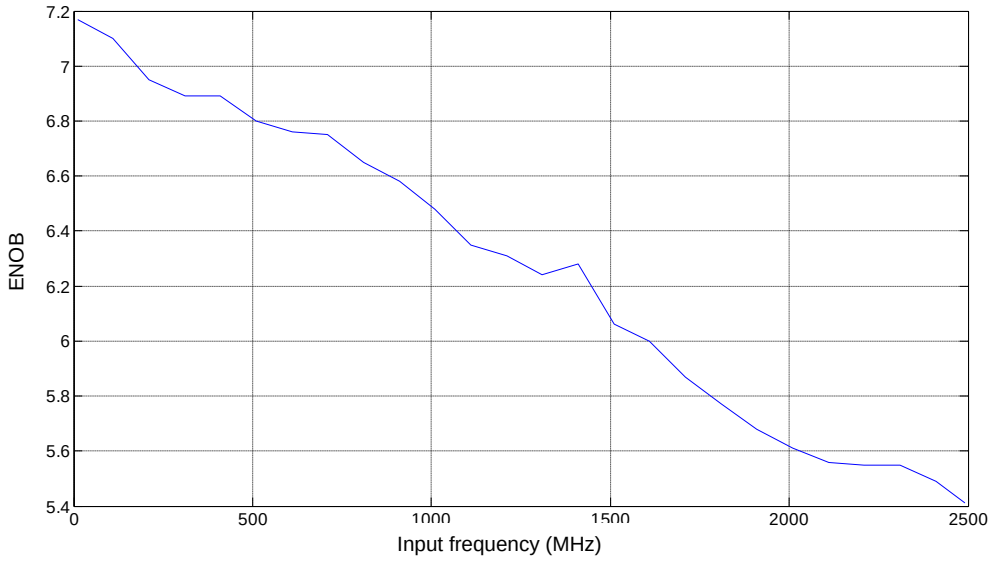

Figure 7.6 Measured resolution for four interleaved ADCs

7.3 Calibration techniques

To implement interleaving systems several approaches, which differ in the calibration method and in the intended application, are possible. This section presents a brief summary that describes the most prevalent calibration methods, discussing their advantages and disadvantages.

In [7.6], where an ADC system for UWB is proposed, two basic (non-exclusive) options to calibrate the system are presented: 1) controlling the ADC mismatches in the integrated circuit fabrication process, and 2) using digital pre-processing or post-processing techniques to mitigate the impact of image and offset spurs.

The first one consists of reducing the electrical and physical differences between the channels. The gain is typically controlled using a common reference voltage and carefully designing the layouts. Phase matching is achieved by ensuring that all the clock paths are as similar in length as possible. Nevertheless, unlike approaches based on digital processing, these techniques are not well-suited for implementations based on COTS, which is very convenient for SDR designs due to its flexibility and ease of programming.

Digital processing techniques have several advantages, including low power consumption and the possibility to be implemented through a cheap CMOS process. Moreover, digital techniques are more efficient for the compensation of timing skews than analog techniques, due to they are more stable with the temperature and the wide bandwidths used in SDR applications. Digital processing techniques are also easier to implement, can be designed with more precision and take advantage of the last advances in high-speed and configurable digital hardware platforms (DSPs, FPGAs, CPLDs, ASICs) [7.7].

In spite of the previously stated digital processing advantages, analog calibration techniques have benefits as well. For example, one advantage of analog offset calibration is that the correction values do not suffer from quantization [7.8]. Thus, the ADC offset can be corrected to less than one LSB without adding the extra bits needed when the offset correction is performed in the digital domain [7.9]. Furthermore, analog gain correction can be implemented by simply adjusting the reference voltage (so that using high-speed multi-bit digital multipliers to scale the ADC outputs becomes unnecessary).

Calibration techniques can be also classified into “background” and “foreground” techniques [7.10-7.12]. Sometimes they are also named as, respectively, “online” and “offline” calibration [7.13]. Offline calibration requires less circuitry, but interrupts the normal operation of the ADC. It is usually applied when the parameters of the circuit do not vary much with environmental parameters (e.g. voltage or temperature) [7.14]. On the other hand, background

techniques enable continuous calibration, with the ADC running in normal operation, and are suitable to be used when disconnecting the ADC is not an option [7.15].

A particularly appealing background approach is the one based on randomization [7.10]. In this approach, the ADC channel is selected randomly for each sampling instant. This can be performed using a digital circuit (thus avoiding the need for new analog circuitry), which constitutes the main benefit of this approach. Considering $M + X$ individual ADCs, we can choose at each time instant among $X + 1$ channels without violating the sampling rate of each individual ADC. This is illustrated in Figure 7.7 [7.16]. In Figure 7.7a, a 3-ADCs system is presented with $M = 3$ and $X = 0$: noting that each ADC samples every 3 T_s seconds, where T_s is the sampling period of the total system, the only possible outputs are *A B C A B C A B C* ... or *A C B A C B A C B* ... For example, considering the first case, after the three channels (*A*, *B*, *C*) have taken a sample we can only choose *A* without violating our sampling constraint. Next, only *B* can be selected and so on. Therefore, to enable the randomization process one or more extra ADCs (i.e., $X > 0$) must be employed [7.16,7.17]. In this way, there always exist at least two available ADCs at each sampling time. This case is illustrated with Figure 7.7b, which considers the case $M = 2$ and $X = 1$: after the first two channels have been selected, for example, *A* and *B*, we can decide between *A* and *C* and so forth.

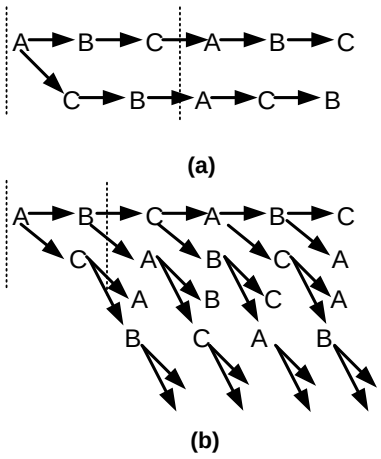

Figure 7.7 (a) Three ADCs (*ABC*) for three times sampling rate, (b) Three ADCs (*ABC*) for a double sampling rate

An example of this architecture is illustrated in Figure 7.8, where ΔM extra ADCs have been added.

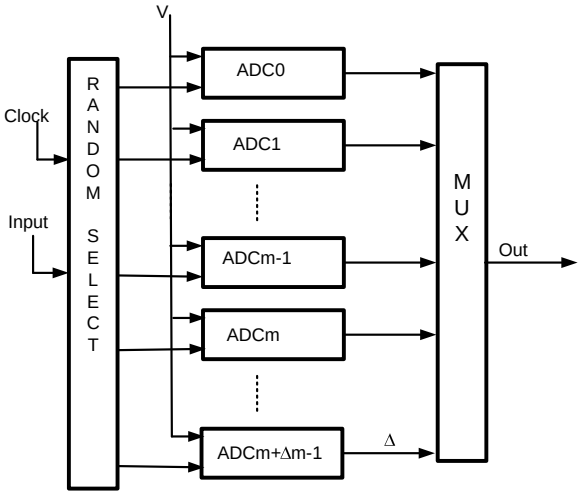

Figure 7.8 Example of a structure with extra ADCs

Although this structure implies an additional hardware cost, [7.16] demonstrates that as *X* tends to zero (in order to reduce the cost), noise becomes non-white (it is not flat). Therefore, it is necessary a trade-off between the value of *X* and the cost of having non-activated ADCs (note that it is not convenient to have largely underutilized ADCs, which occurs when *X* is much larger than *M*). A clock diagram for *M*=4 and *X*=1 is showed in Figure 7.9 [7.16].

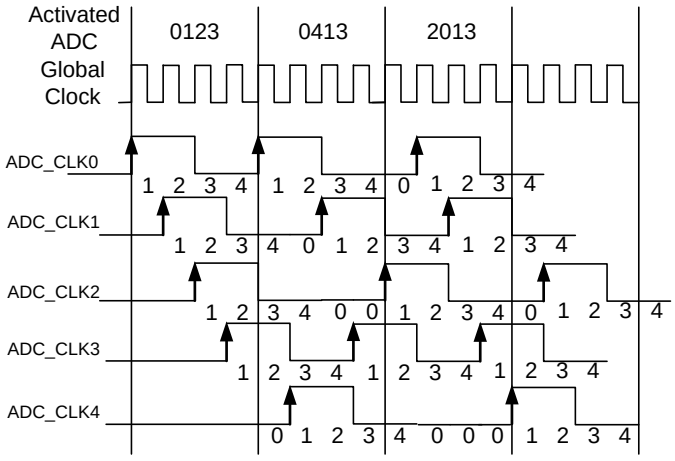

Figure 7.9 Random clock for 5 ADCs

Apart from the use in randomization techniques, an extra ADC might be employed in other background approaches. [7.12] uses an additional ADC to implement an analog background circuit which calibrates the gain and offset mismatch. The basic idea of this technique is to use *M*+1 ADCs so that *M* ADCs are always active while the remaining one is being calibrated. When the calibration cycle is finished, another ADC is selected for calibration, being replaced in the conversion mode by the previously calibrated ADC. The calibration of these ADCs is performed using another ADC as a reference, in order to match gain and offset with it. Therefore, an analog calibration is implemented.

Since this method is based on a background process, it is not necessary to stop the analog-to-digital conversion and, in addition, it will be more efficient as the number of ADCs increases. However, the main drawbacks are the noise introduced by the additional analog circuitry, and the degradation in speed when extra ADCs are used to substitute the ADC under calibration [7.18].

Moreover, there are also calibration techniques specifically devised either for static (i.e., gain and offset) or dynamic errors (i.e., clock skew). For example, an alternative method for calibrating the static mismatches is to employ a DAC with enough resolution to meet the requirements [7.19], using one of these DACs for each ADC in the interleaved structure.

A common alternative to reduce the cost of the extra circuitry due to the added DACs is to implement the gain and offset calibration after a FFT evaluation, via software, achieving the compensation from the study of the output spectrum [7.20]. An additional benefit of this technique is to take the advantage of the repetition and symmetry properties of the FFT [7.21].

On the other hand, clock skew errors are difficult to correct and lead to more stringent limitations on interleaved architectures [7.22], especially for UWB applications, as explained in [7.6], because there are many unknown factors affecting these timing mismatches, such as jitter, paths delay or temperature, that make the estimation of the spurious component level even harder.

Some traditional ideas for correcting the skew errors are to add programmable delay lines or to implement a signal post-processing. Although additional hardware is required, [7.16] propose this method to reduce the spurious level.

Another specific technique for timing errors correction is the one based on polyphase digital filters blocks [7.23,7.24] which can be easily implemented using a FPGA and, therefore, results highly suitable for SDR applications based on COTS. An example of the proposed structure is illustrated in Figure 7.10, where the FPGA includes, as well as the filter implementation, a precision voltage reference, a low jitter clock distribution circuit and a digital sensor to control the effect of temperature on the skew [7.7].

The filter structures used to calibrate these dynamic errors are designed as a function of the number of channels (i.e., number of ADCs). [7.24] gives the ratio (R) between the number of channels (M) and the number of necessary filters (N), this ratio being lower when the number of channels is increased. For instance, in that work N=3 for M=2 (R=0.75), N=5 for M=3 (R=0.556) and N=27 for M=8 (R=0.422). As a consequence, for a high number of ADCs this method is not so efficient. Another inconvenient is that this technique is limited to a single frequency input signal, and the filters coefficients would have to be frequently recalculated, thus increasing the calibration process complexity [7.25].

Lastly, an additional drawback of this method is that conventional filters do not have enough resolution to tune the group delay in the highest frequency systems, where the calibration precisely has to be more accurate [7.26]. Thus, designing these filters is an important challenge in their own.

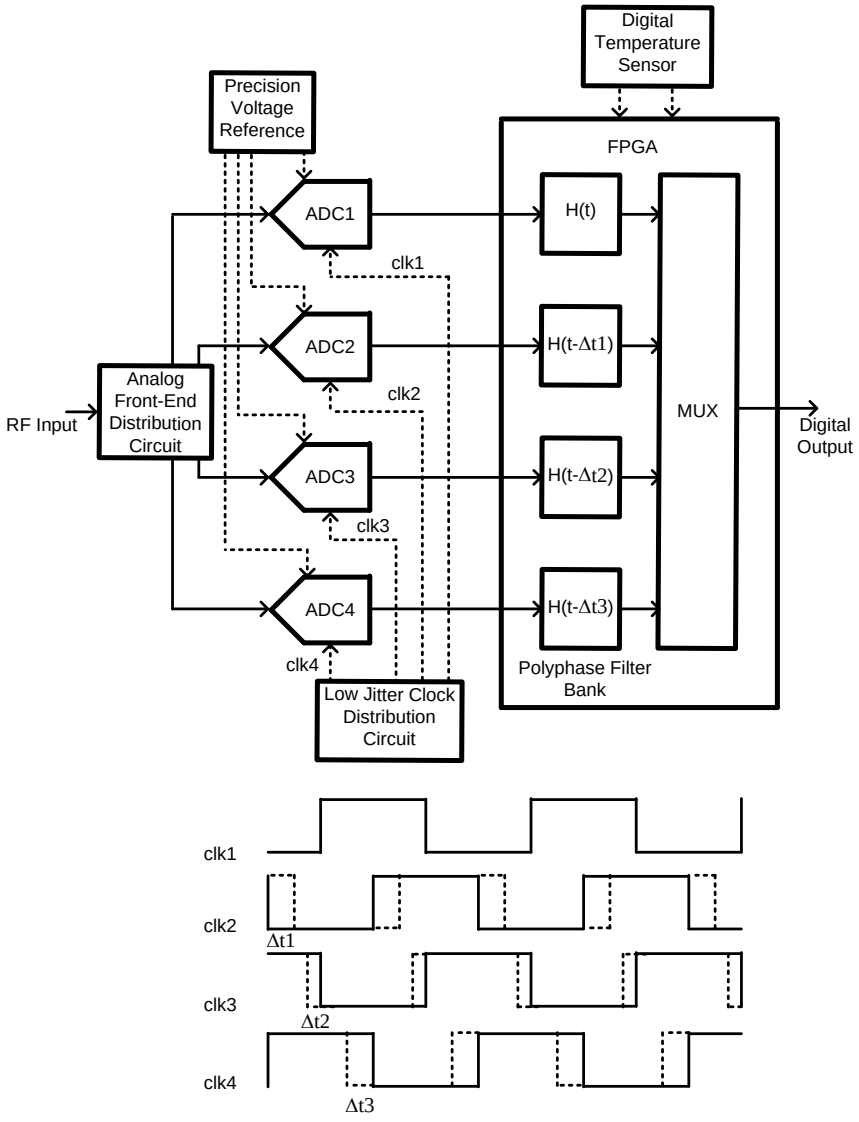

Figure 7.10 Functional diagram using digital filters blocks

7.4 Implemented systems

Many research works have been published in order to implement receivers and analog-to-digital conversion systems based on interleaving techniques. Some of these systems are implemented in IC whereas others are implemented by using COTS, leading to some benefits in SDR applications for testing purposes, like significant time and cost savings comparing with developing an integrated circuit.

An example of a work that implements a time interleaving system based on COTS is [7.6]. In this system eight ADCs [7.27] sampled at 1 GHz are connected to obtain a total sampling frequency equal to 8 GHz. However, since the digital processing is implemented on a FPGA, the final frequency is equal to 6.4 GHz, due to speed restrictions of the device. Although, this is an inconvenience for high-speed circuits, using a FPGA will provide to the system the necessary flexibility for SDR and UWB applications. The proposed system in [7.6] employs a digital calibration scheme based on filters, obtaining a SNR around 30-35 dB (i.e., around 5-6 bits) at the maximum operation frequency.

Other novel systems not implemented by COTS can integrate all the functionalities, including the calibration part (calibration on-chip). This solution it is more convenient for analog or DAC-based calibration, reducing the power consumption. An example is proposed in [7.11]. In this work four ADCs are connected to obtain a SNDR around 48 dB for a total sampling frequency of 2.6 GHz.

There are other interleaving converters which combine analog and digital calibration. For instance, [7.15] uses DACs to correct offset errors in the analog domain and background digital calibration to reduce the clock skew effects. Using both methods this work implements an 8-ADCs array to obtain a resolution of 5 bits at 12 GS/s operation rate. A similar work is described in [7.28], where a resolution of 5.1 bits is obtained with 8 interleaved ADCs operating at 10.3 GS/s. Moreover, there are some interleaved converters that have applied successfully background digital calibration for dynamic and static errors compensation, as [7.29], which obtains 6 bits at 16 GS/s for 8 different channels.

On the other hand, an important issue about the implementation of interleaving converters is the connection between the S&Hs and ADCs. There are two possible structures, which are illustrated in Figure 7.11 [7.22]. One of them uses only one S&H connected to several ADCs (Figure 7.11a). In this case, the main inconvenience is that the number of ADCs connected to the S&H is limited and, therefore, since this number of ADCs is directly proportional to the total sampling rate, the scalability will be limited as well. When each interleaved ADC is preceded by its own S&H (Figure 7.11b) the scalability is theoretically increased because this architecture is not limited by a maximum number of ADCs connected to the S&H. However, the clock skew effect between the different S&Hs will degrade the final SNDR and, therefore, the final number of interleaved ADCs will also be limited in this case, as it is shown in equation (7.7).

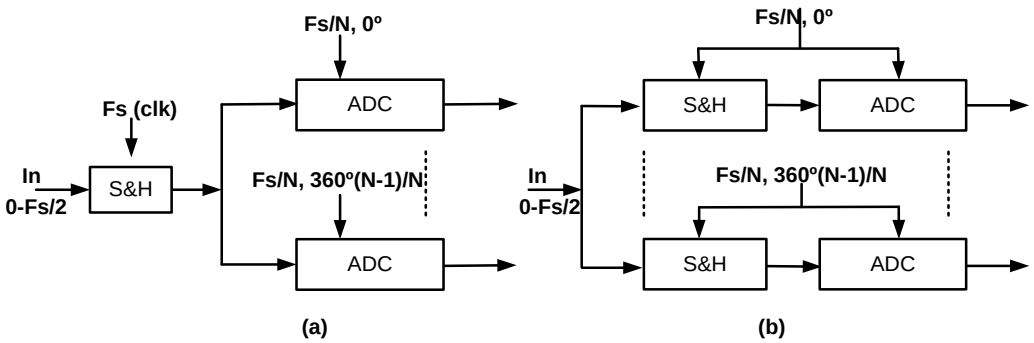

Figure 7.11 Architectures based on: (a) one S&H and (b) several sub-S&H

With the objective of reducing the number of S&Hs, [7.22] proposes a structure based on double sampling (Figure 7.12). Since using this solution the loading of the S&H is not directly depending on the number of interleaved ADCs, the scalability will be increased with respect to the structure shown in Figure 7.11a. Moreover, the mismatch problems and the power consumption will be reduced with respect to the structure shown in Figure 7.11b.

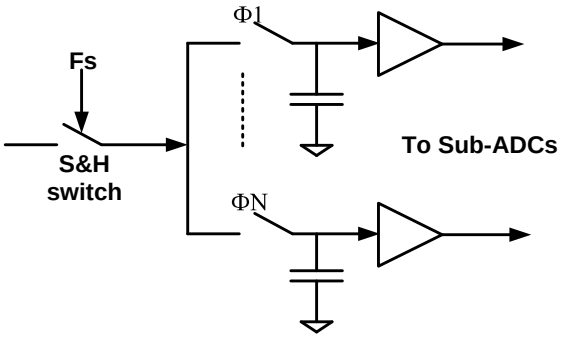

Figure 7.12 Architecture based on double sampling

7.5 References

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CHAPTER 8

APPENDIX B: PRINTED CIRCUIT BOARD DESIGN

CHAPTER CONTENTS

The objective of this appendix is to detail all the followed steps in the data acquisition module design described in Chapter 4, discussing different concepts that must be taken in account when designing a RF printed circuit board. This chapter is distributed in two main sections, one of them dedicated to the design at schematic level and the second dedicated to the design at PCB level.

8.1 Design at component and schematic level

Figure 8.1 illustrates the diagram block of the subsampling based receiver proposed in [8.1], being the S&H Inphi 1821TH and the ADC E2V AT84AS001 the main components on the board.

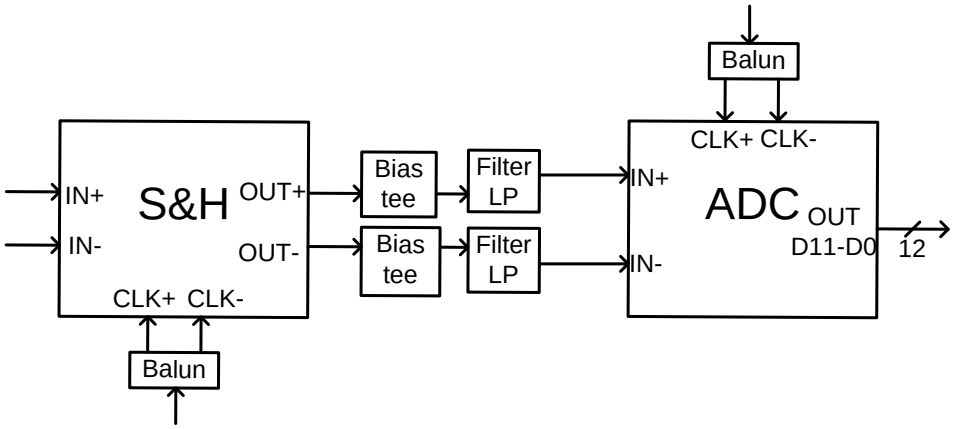


Figure 8.1 Block diagram of the proposed system

This figure shows how the clock signal is converted to differential by using SMD power splitters, while the input signal will be converted externally by a SMA power splitter due to availability reasons. By using a bias-tee in each branch the IF subsampled signal will be adapted at 50 Ω before being filtered. Therefore, just a replica located at $f_s/4$ is at the ADC input.

The 49-pin BGA[13] connection for the S&H is illustrated in Figure 8.2, showing its dimensions and a *pitch* equal to 0.8 mm. The 192-pin BGA connection for the ADC, and its *pinout*, is illustrated in Figure 8.3.

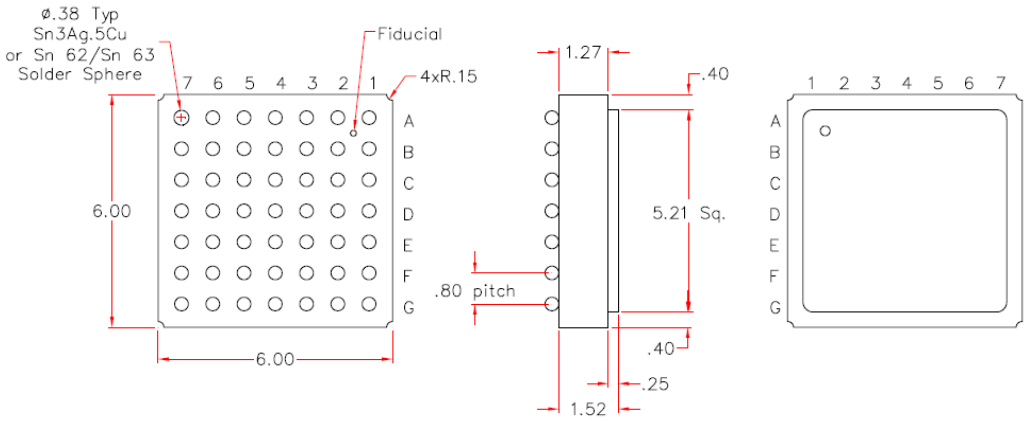


Figure 8.2 BGA dimensions for the Inphi 1821TH

[13] *Ball Grid Array*

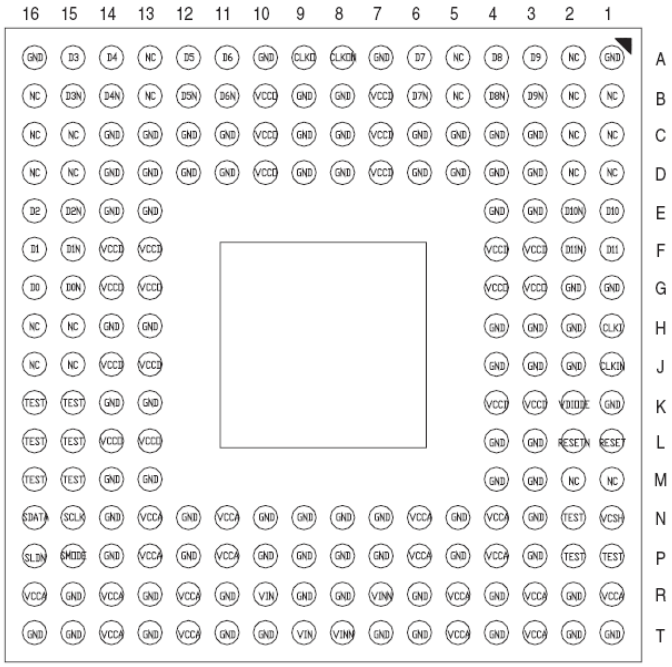


Figure 8.3 *Pinout* of E2V AT84AS001

Others components employed in this design will be overviewed from the schematics developed by using the *Cadence Design Entry CIS Orcad Capture* software.

Page 1 (Figure 8.4), besides decoupling capacities (C62-C68), includes the first part of the signal path, i.e., the S&H (U16), the input SMA connectors (U22, U23), the S&H clock SMA connector (U26), the ADC clock SMA connector (U25) and the SMA connectors employed for a thru-line loss calibration. This structure consists of two SMA connectors and a transmission line (Figure 8.5) whose length is the sum of the lengths of each input and output transmission line. Therefore, the total loss measured on this calibration structure is exactly double the loss of the input SMA connector and line which is exactly the same as the output SMA connector and line.

Other components illustrated in Figure 8.4 are the bias-tee (U39, U40), the LP filters (U41, U42), and the power splitters to clock the S&H (U37) and the ADC (U38). 10 nF capacities (C128, C129) and 49.9 Ω resistors (R33, R35) are employed to adapt the impedance by using the bias-tees. Decoupling capacities (C62-C68) will be placed as close the S&H as possible.

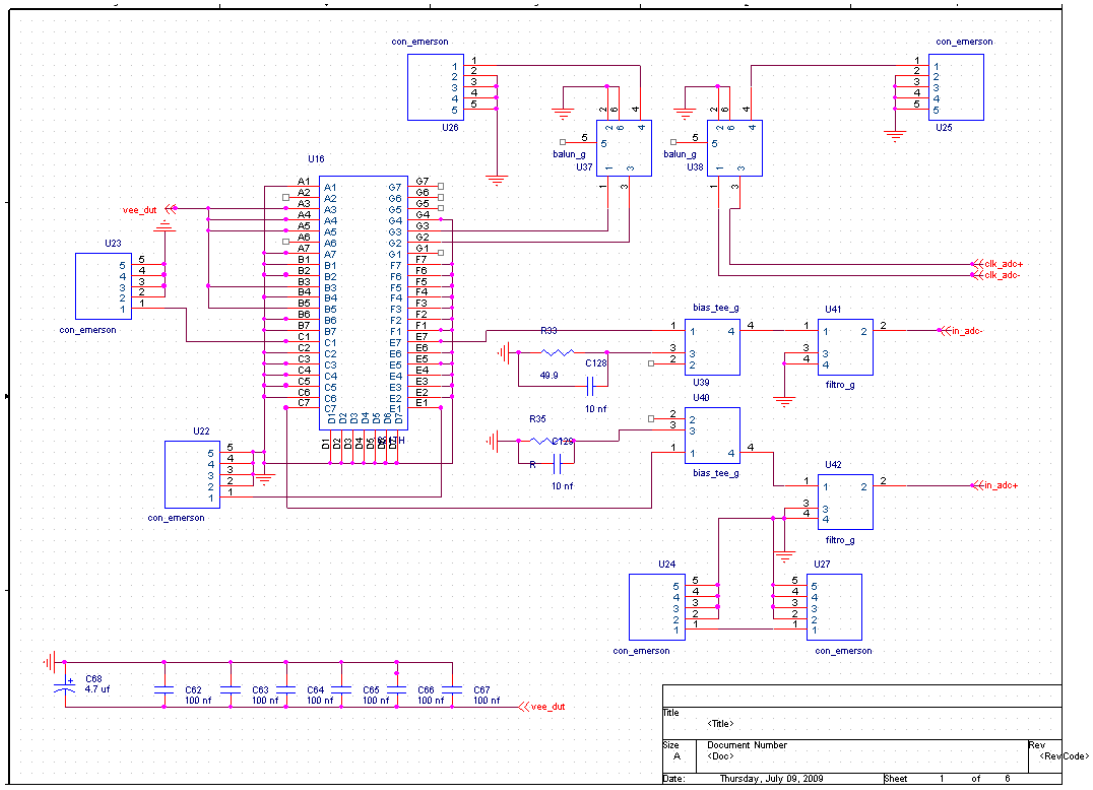


Figure 8.4 Proposed schematic: page 1

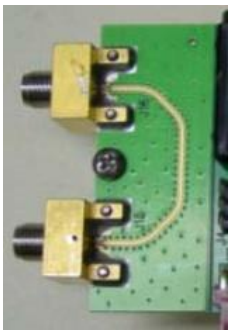


Figure 8.5 Thru-line loss calibration

Figure 8.6 illustrates the part of the schematic that includes the following components:

- ADC (U15)
- Power supplies connectors:
  - 3V3 (U50): 3.3 V supplying a serial bus programming interface.
  - VCCO (U51): 2.5 V supplying the digital outputs.
  - VCCD (U52): 3.3 V supplying the digital part.
  - VCCA (U53): 5 V supplying the analog part.

- Connectors (U33, U34) to apply a reset signal to the ADC, which will be implemented by using a 500 Ω potentiometer (R29). Other components used in this implementation are the 200 Ω resistors and the 10 nF capacities (C46, C47).

- 10 nF capacities (C48-C53) connected to the ADC input for test purposes, but not used in this application.

- 10 nF capacities (C40-C45) used to decoupling the DC components at the signal inputs and the clock inputs.

- C124-C127 are decoupling capacities as well.

- 49.9 Ω resistors (R27, R28) are employed to impedance adaptation.

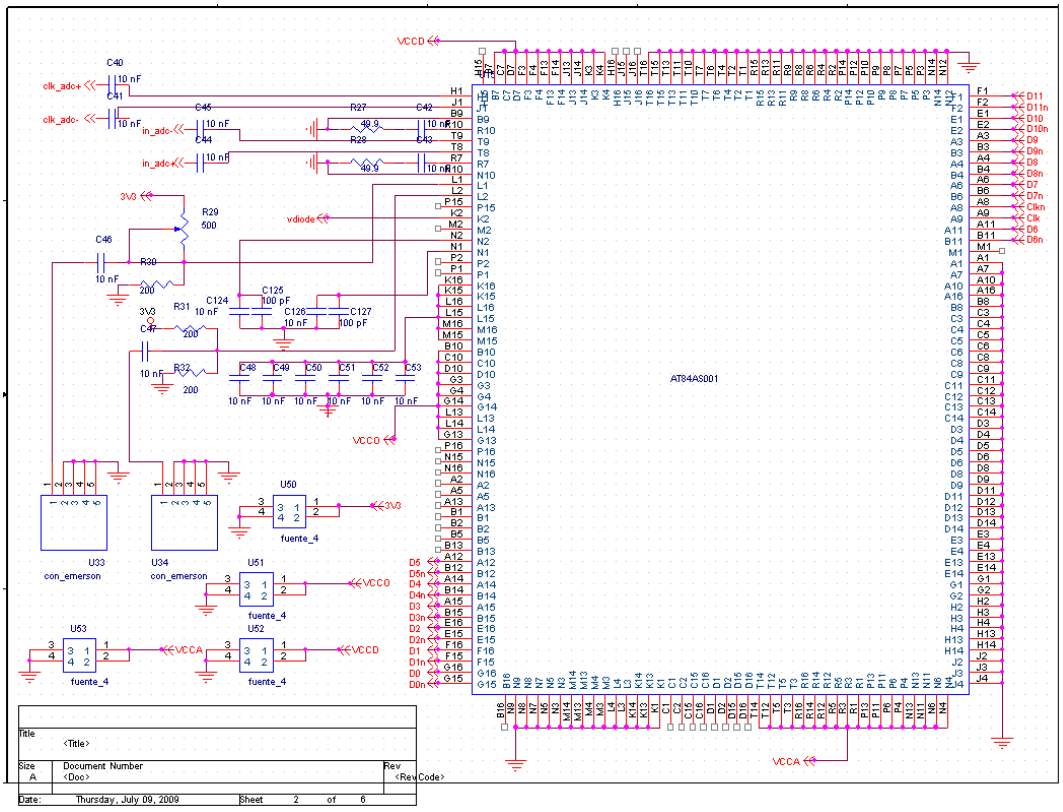


Figure 8.6 Proposed schematic: page 2

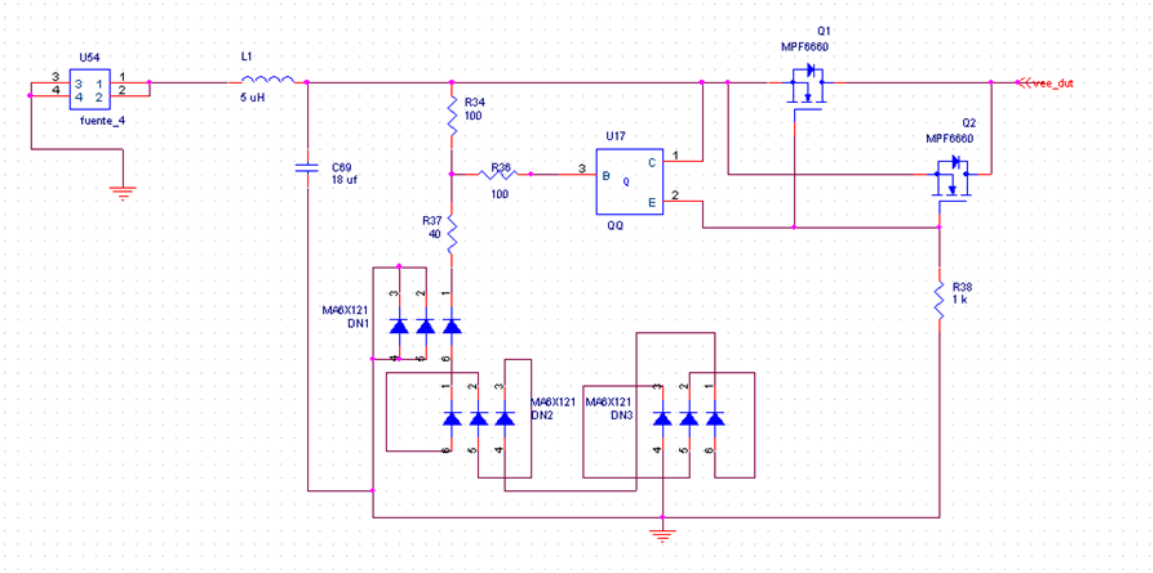


Figure 8.7 Proposed schematic: page 3

Figure 8.7 illustrates the power conditioning circuit of the S&H, whose functionality is described in [8.2]. This circuit is composed of two distinct parts, a RLC LP filter and the diodes and transistors will help to maintain the power voltage within a limited range.

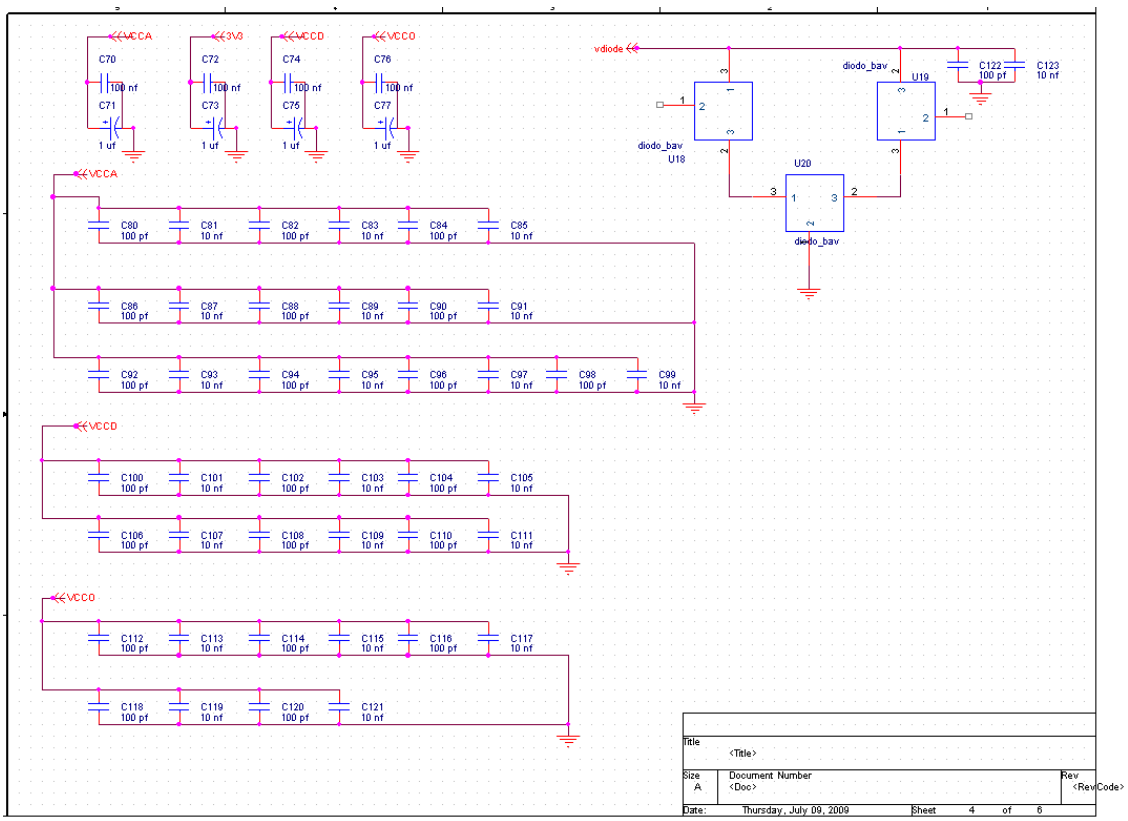


Figure 8.8 Proposed schematic: page 4

Figure 8.8 includes the bypassing capacities (C70-C77) and the decoupling capacities (C80-C121) proposed by the manufacturer. Also a circuit to

temperature monitoring is included in this schematic, being composed by two capacities (C122, C123) and three couples of diodes (U18-U20). Nevertheless, this circuit was not used for this implementation.

Figure 8.9 illustrates the output connector (U57) and its differential *pinout*.

Finally, Figure 8.10 illustrates the 10 pF capacities and the 49.9 Ω resistors employed to adapt the LVDS output and clock signals between the ADC and output connector U57.

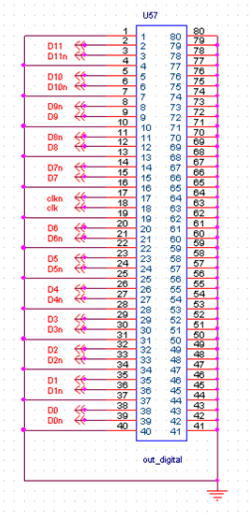


Figure 8.9 Proposed schematic: page 5

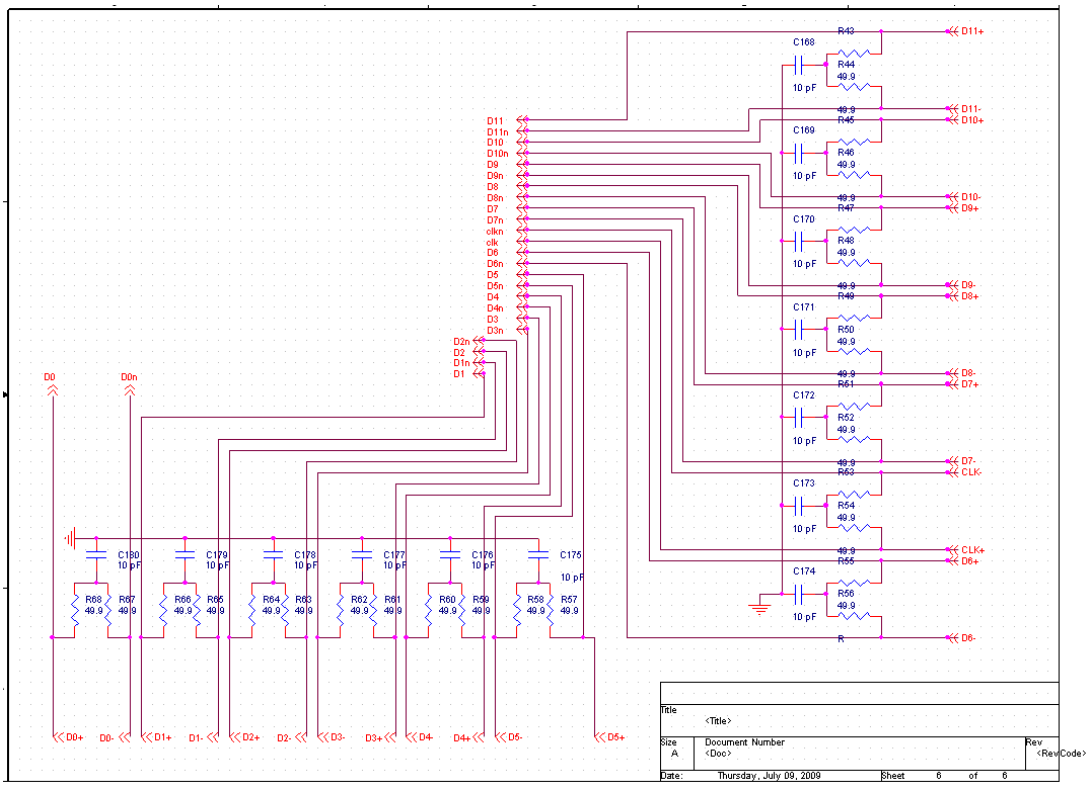


Figure 8.10 Proposed schematic: page 6

8.2 Design at PCB level

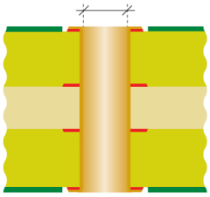
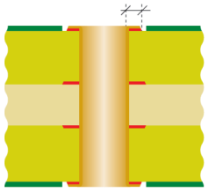
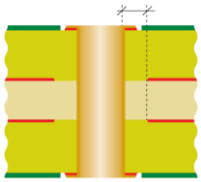
8.2.1 Employed software, design rules and manufacturing features

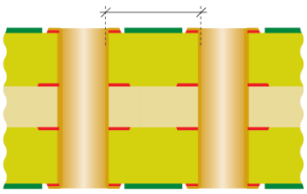
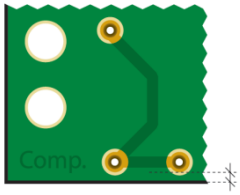
The design was implemented using the software listed below:

- *Cadence PCB Editor Allegro PCB Design GXL*: to design at PCB level.
- *Cadence Pad Designer*: to design the SMD pads and the thru-hole pins employed by using Cadence PCB Editor.
- *ViewMate Gerber Viewer*: to traduce and visualize the gerber files generated by Cadence PCB Editor.

On the other hand, The proposed prototype has been designed according to the design rules imposed by the *Labcircuits* Class 7 [8.3]. The main employed rules are listed in Table 8.1:

Table 8.1 Designs rules

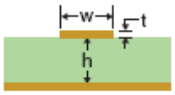
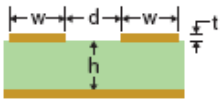
Rule Design	Description	Value
Minimum plated through hole diameter		0.15 mm
Minimum outer layer trace/spacing width		0.1 mm (17 um)
Minimum outer layer annular ring		0.075 mm
Minimum annular spacing in ground plane		0.2 mm

Minimum wall between plated thru-holes		0.4 mm
Minimum distance between trace and contour		0.2 mm

8.2.2 Used dielectric and impedance calculation

The employed dielectric is DE104i (FR4), with a dielectric constant equal to 4.37 ± 0.05 at 1 GHz [8.3]. On the other hand the prototype was manufactured implementing an impedance control process. Previously, the necessary dimensions to obtain a controlled impedance of 50 Ω were obtained from the expressions listed in Table 8.2 [8.4]. These expressions are given for *microstrip* lines in single-ended and differential versions.

Table 8.2 Impedance calculation

	Single-ended	**Differential**
Topology		
Characteristic Impedance	$Z_o = \frac{k}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$ Ω k=87 for 15<w<25 mils k=79 for 5<w<15 mils	$Z_o = \frac{k}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$ Ω k=87 for 15<w<25 mils k=79 for 5<w<15 mils $Z_{Diff} = 2Z_o\left(1 - 0.48e^{\left(-0.96\frac{d}{h}\right)}\right)$ Ω
Restrictions	0.1<w/h<3.0 $1 < \varepsilon_r < 15$	0.1<w/h<3.0 $1 < \varepsilon_r < 15$

Design equations	$w = 7.475he^{\frac{-Z_o\sqrt{\varepsilon_r+1.41}}{k}} - 1.25t$	$w = 7.475he^{\frac{-Z_o\sqrt{\varepsilon_r+1.41}}{k}} - 1.25t$ $d = \ln\left(2.08\frac{-1.04Z_{Diff}}{Z_o}\right)\left(\frac{-h}{0.96}\right)$
Propagation delay	$t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67}$ (ps/in.)	$t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67}$ (ps/in.)

In this design the differential lines considered correspond with the digital outputs. Other differential signals on the board (i.e., input S&H, input ADC and clock signals) are considered as single-ended about the impedance calculation, due to it is not possible to keep the two branches close enough through all the signal path.

Thus, for the single-ended case, the obtained trace width is equal 8.9 mils (0.226 mm), being this value calculated from the following data: Z_o=50 Ω, ε_r=4.37[14], t=47 um[15], and h=0.17 mm[16].

On the other hand, for the differential case, the obtained trace width is equal 6 mils (0.152 mm), being this value calculated from the following data: Z_{diff}=100 Ω, ε_r=4.37, t=47 um, h=0.17 mm, and d=5 mils[17] (0.127 mm).

8.2.3 Stack-up

The proposed stack-up is composed by six metal layers, as shown in Figure 8.11, where the thickness of each layer is given in mils. Although this figure was introduced in Chapter 4, is employed again in this appendix for convenience, in order to describe the chosen structure in more detail. The top and the bottom layers are employed to route the signals, whereas the internal layers 3 and 4 are used to implement the power supplies, being the layers 2 and 5 connected to ground. In order to keep the symmetry with the signal layers we

[14] FR4 DE104i dielectric constant

[15] Imposed by the manufacturer.

[16] Negotiated with the manufacturer. Nevertheless, the real value will be increased in 30 um by the deposition process, being the final thickness equal to 47 um.

[17] This value was calculated to the single ended impedance Z_o is close to 50 Ω as well. This condition is necessary because it is not possible to keep an invariable distance d at some places on the board, like at the ADC outputs or at the output connector, where the traces will be approximated as single-ended transmission lines. In addition, for both single ended and differential cases, it is necessary the parameters w and d are as low as possible in order to easily route the signals from the BGA pinouts.

decided to split all the power supplies in two planes, being isolated from the top and bottom planes by their respective ground planes.

As a summary, the thicknesses for each different layer are listed below:

- 17 um (0.669) for the copper layers, which was proposed by the manufacturer
- 0.17 mm (6.693 mils) for the dielectric (*prepreg*) adjacent the external metal layers, which was negotiated with the manufacturer in order to obtain the desired impedance by using reasonable values of *w*.
- 0.1 mm (3.937 mils) for the *core* dielectric, which was imposed by the manufacturer.
- 0.52 mm (20.472 mils) for the central *prepreg*, which can be modified in order to obtain the desired total thickness. In this case, the total thickness is 1.22 mm (48.11 mils) using this typical *prepreg* thickness proposed by the manufacturer.

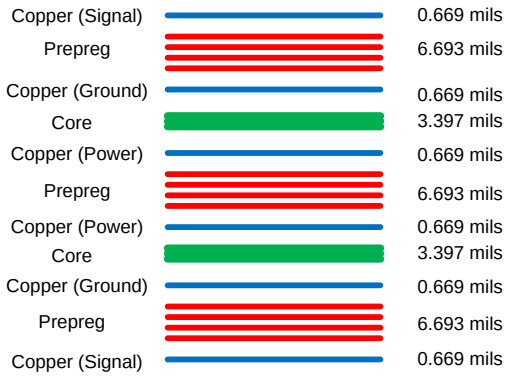


Figure 8.11 Proposed stack-up

8.2.4 Drill and VIAs arrays

Figure 8.12 shows the drill summary provided by the software *Cadence PCB Editor* for the whole prototype.

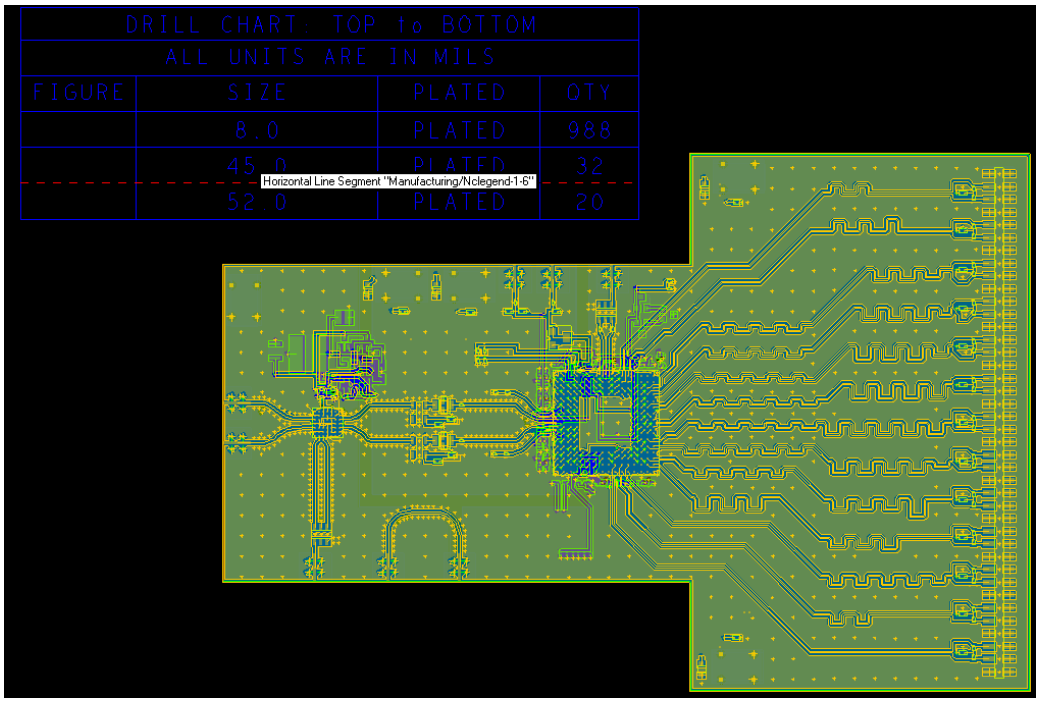


Figure 8.12 Drill chart

The designed VIA that employs the minimum size allowed by the manufacturer is the most used on this board (988 units). The features of this VIA (pad, thermal relief and anti pad sizes [8.5]) are shown in Figure 8.13, provided by the *Pad Designer* software. Using this minimum size will be crucial to route some parts of the board, like the ADC *pinout* shown in Figure 8.14.

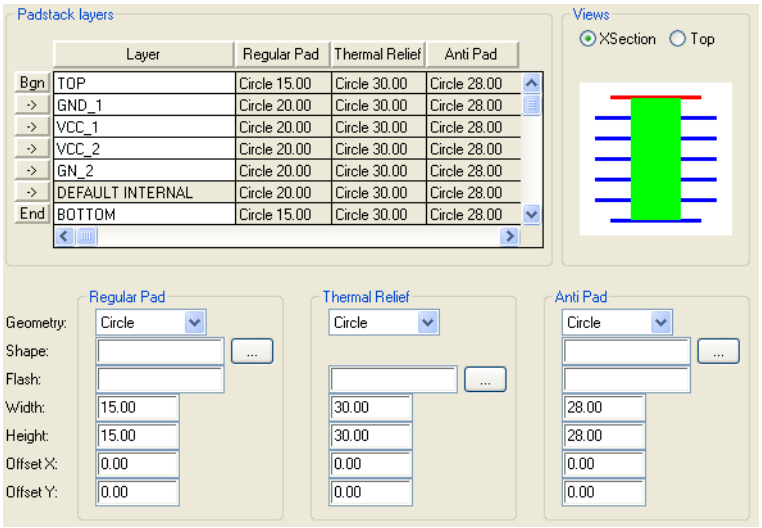


Figure 8.13 VIA with minimum size

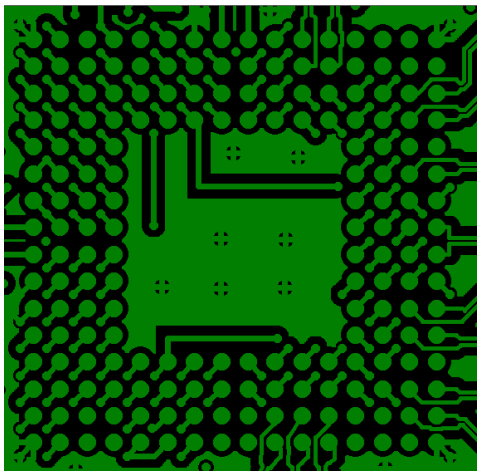


Figure 8.14 ADC fanout

Also this VIA is employed to built VIAs array structures, whose functionality is to connect the Top and Bottom layers to ground as an additional protection way through the whole board. A typical value for the distance between VIAs is 4 mm, as is proposed by the S&H manufacturer [8.2]. Figure 8.15 illustrates a detail of this structure.

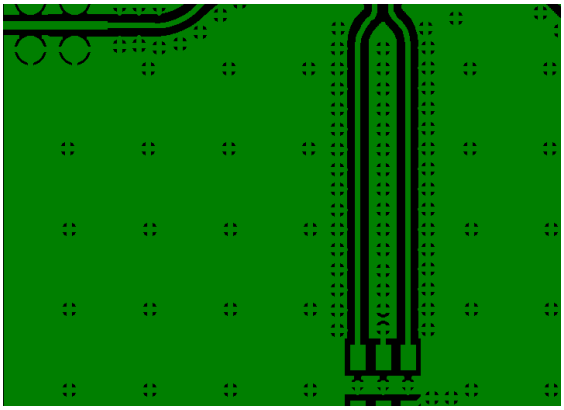


Figure 8.15 VIAs array strcucture

Other VIAs arrays that can be observed in Figure 8.15 are placed at both sides of the transmission lines. These VIAs are connected to the ground planes, being utilized as an additional interference protection for high speed signal paths. These structures are known as *picket fences* and use a distance between them equal to 1 mm approximately in this design, as is recommended by Inphi [8.2]. Knowing that a typical distance is $\lambda/20$ [8.6], being λ the wavelength, this protection will be optimized to 6 GHz signals.

Finally, other sizes of VIAs are employed for the SMA connectors and the power supply connectors, whose dimensions are illustrated in Figure 8.16 and Figure 8.17, respectively.

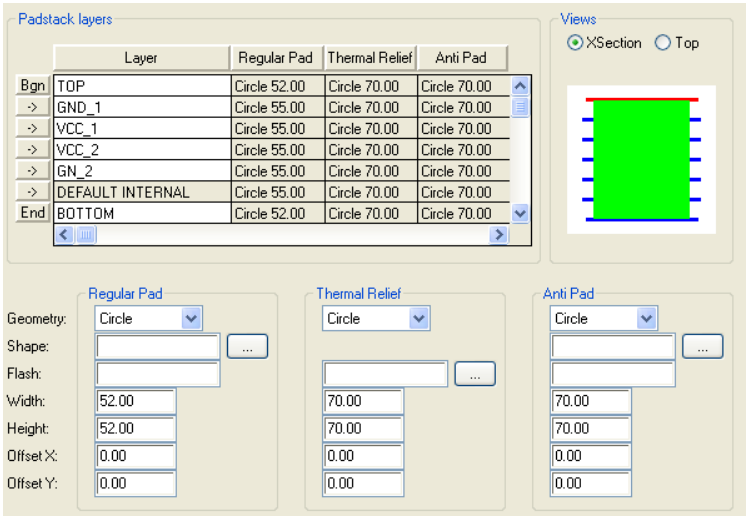


Figure 8.16 VIA employed in SMA connections

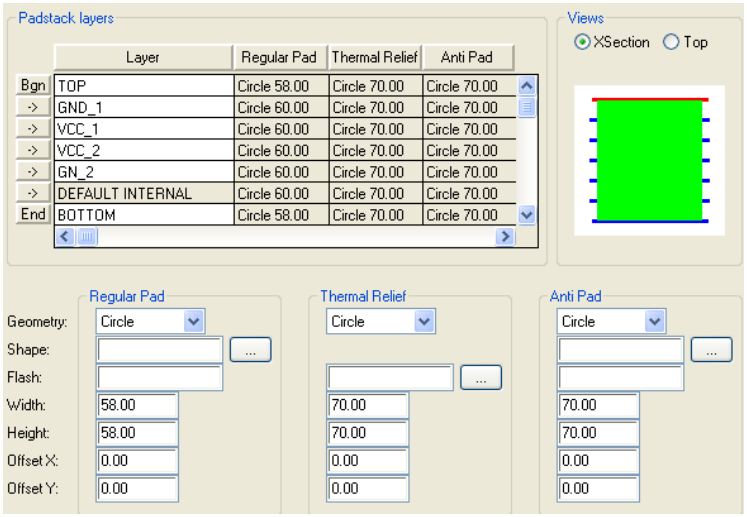


Figure 8.17 VIA employed in power supplies connections

8.2.5 Description by layers

8.2.5.1 Top layer description

The functionality on the top is illustrated in Figure 8.18 and Figure 8.19. These include all the signal path (analog and digital), the clock paths, and the signal processing components, such as S&H, ADC, bias-tee, LP filters, power splitters and output ports.

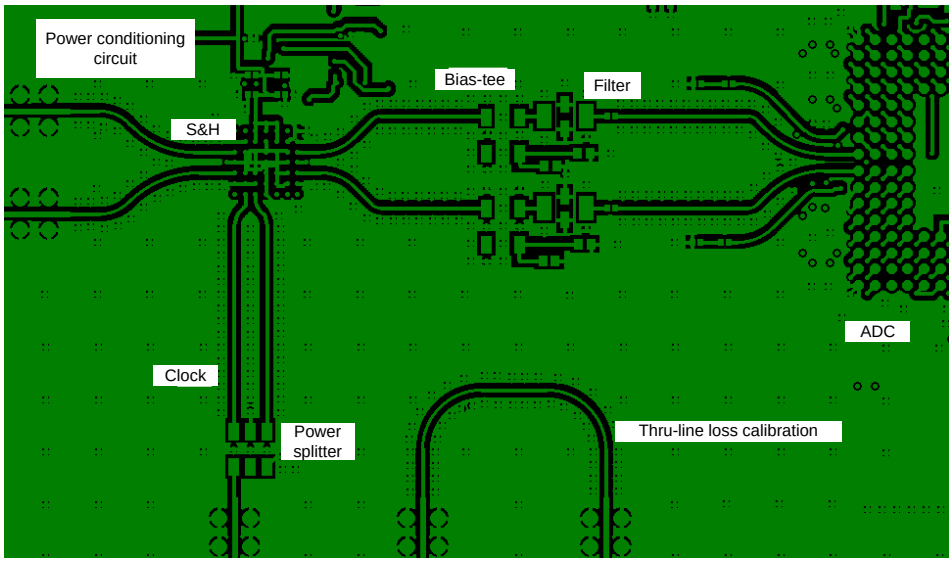


Figure 8.18 Top functionality

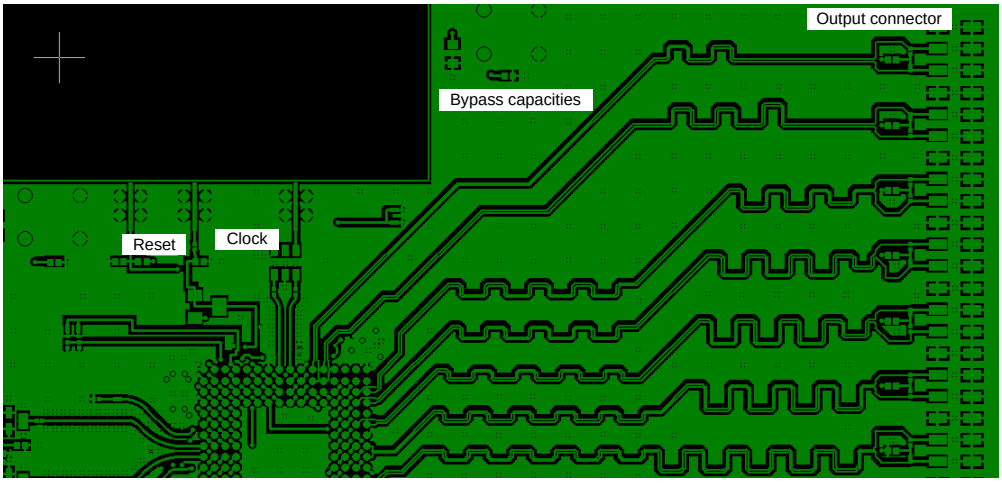


Figure 8.19 Top functionality (II)

8.2.5.2 Bottom layer description

This side of the board includes, as shown in Figure 8.20, most of the components of the S&H power conditioning circuit, the ADC temperature monitoring circuit based on diodes, and the decoupling capacities, which will be placed as close to the S&H and the ADC as possible.

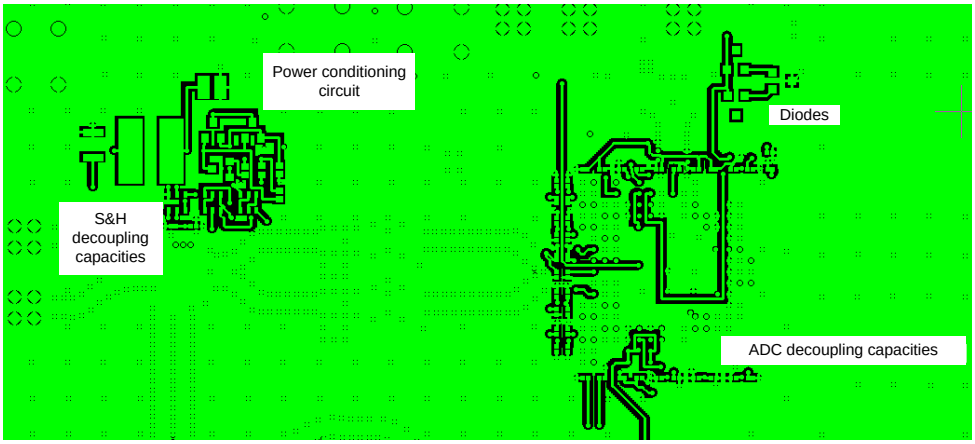


Figure 8.20 Bottom functionality

8.2.5.3 Power supplies layers description

Figure 8.21 and Figure 8.22 illustrate the power supplies layers *VCC1* and *VCC2*, respectively. It is possible to observe how the layers have been symmetrically split for the different power supplies, as well as the S&H power supply is duplicated in order to keep this symmetry. Finally, Figure 8.23 illustrates a capture from the Gerber files, where the final dimensions are indicated.

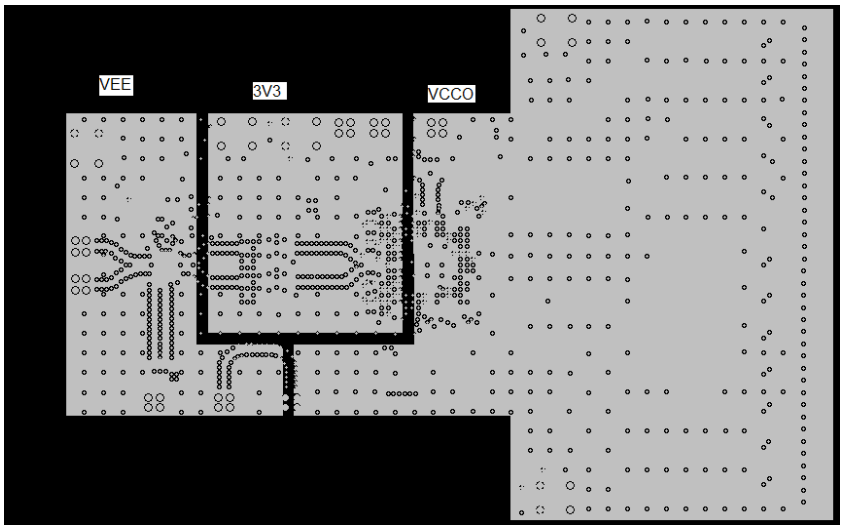


Figure 8.21 Power supplies in layer VCC1

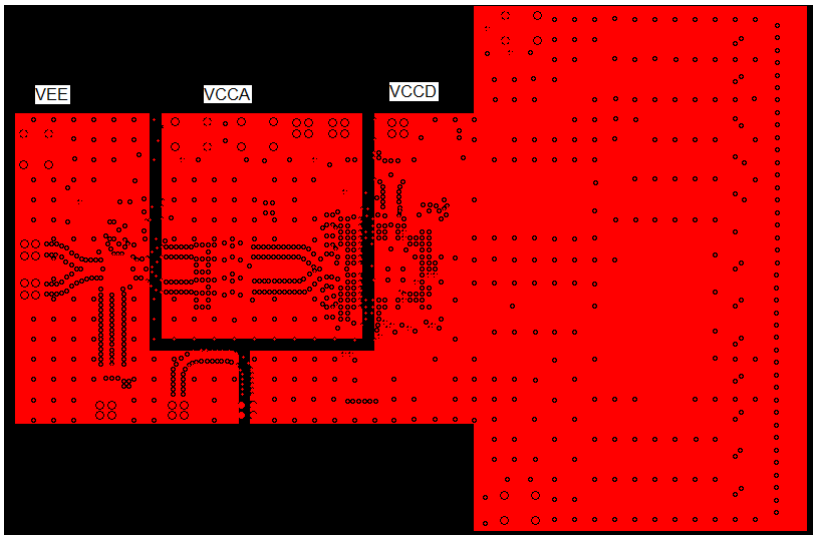


Figure 8.22 Power supplies in layer VCC2

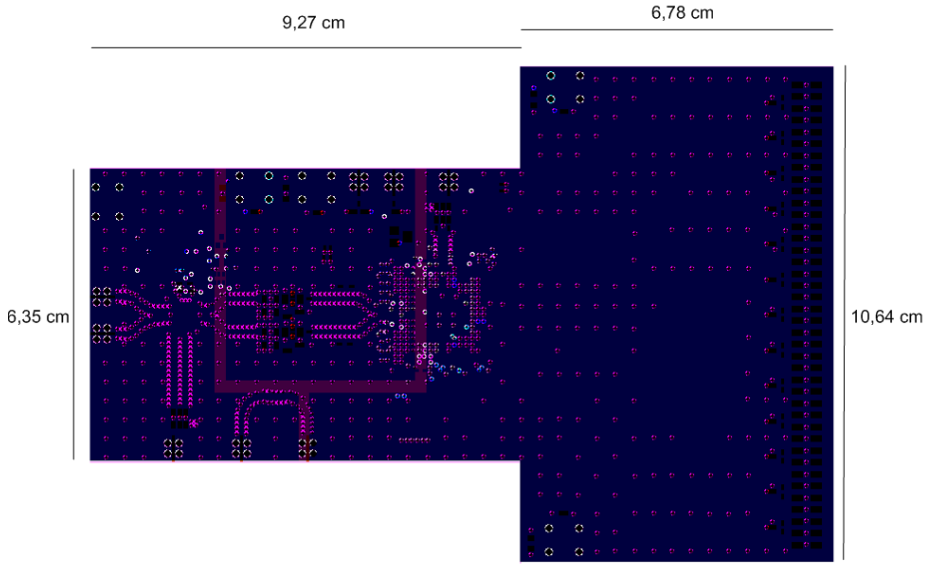


Figure 8.23 Prototype dimensions

8.3 References

[8.1] J. R. G. Oya, F. Muñoz, A. Torralba, A. Jurado, A. J. Garrido, J. Baños, "Data Acquisition System Based on Subsampling for Testing Wideband Multistandard Receivers," *IEEE Transactions on Instrumentation and Measurements*, vol. 60, no. 9, pp. 3234-3237, Sep. 2011.

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CHAPTER 9

APPENDIX C: Publications

CHAPTER CONTENTS

This appendix presents a list of the original publications that represents the main contributions of this thesis work to book chapters, journals and conferences. These journal and conference papers are collected at the end of this appendix. Additionally a list of publications not directly related with the fields exposed in thesis is included in the appendix, the first page of each one of these publications being presented as well.

9.1 Journal papers

[9.1] **J. R. G. Oya**, F. Muñoz, A. Torralba, A. Jurado, A. J. Garrido, J. Baños, "Data Acquisition System Based on Subsampling for Testing Wideband Multistandard Receivers," *IEEE Transactions on Instrumentation and Measurements*, vol. 60, no. 9, pp. 3234-3237, Sep. 2011.

[9.2] **J. R. G. Oya**, F. Muñoz, A. Torralba, A. Jurado, F. Márquez, E. López-Morillo, "Data Acquisition System Based on Subsampling using Multiple Clocking Techniques," *IEEE Instrumentation and Measurements*, vol. 61, no. 8, pp. 2333-2335, Aug. 2012.

9.2 Book chapters

[9.3] **J. R. G. Oya**, A. Kwan, F. Muñoz, F. M. Ghannouchi, M. Healoui, F. Márquez, E. López-Morillo, A. Torralba, "Subsampling Receivers with Applications to Software Defined Radio," *Data Acquisition, InTech*, Chapter 7, pp. 165-194, 2012.

[9.4] **J. R. G. Oya**, F. Muñoz, R. Martín, F. Márquez, E. López-Morillo, A. Torralba, "Analog-to-Digital Conversion Systems for High Data Acquisition Rate," *Data Acquisition, Academy Publish*, accepted to be published, 2012.

9.3 Conference communications

[9.5] **J. R. G. Oya**, A. Jurado, F. Muñoz, A. Torralba, "High Frequency Analog-to-Digital Conversion Based on Subsampling", *XXIV Conference of Design of Circuits and Integrated Systems (DCIS'2009)*, Zaragoza, Spain, Nov. 2009.

[9.6] **J. R. G. Oya**, A. Jurado, F. Muñoz, A. Torralba, F. J. Márquez, E. López-Morillo, "Multiple Clocking High Analog-to-Digital Conversion Based on Subsampling", *XXVI Conference of Design of Circuits and Integrated Systems (DCIS'2011)*, Albufeira, Portugal, Nov. 2011.

[9.7] **J. R. G. Oya**, A. Kwan, S. A. Bassam, F. Muñoz, and F. M. Ghannouchi, "Optimization of Subsampling Dual Band Receivers Design in a Nonlinear Systems," *IEEE MTT-S International Microwave Symposium Digest (IMS'2012)*, pp. 1-3, Montreal, QC, Canada, June 2012.

9.4 Publications partially related with this thesis

9.4.1 Journal papers

[9.8] B. Palomo, F. Muñoz, R. G. Carvajal, **J. R. García**, F. Márquez, "An 8-bit 19 MS/s low-power 0.35 µm CMOS pipelined ADC for DVB-H", *Integration, the VLSI Journal*, vol. 45, no. 2, pp. 222-227, March 2012.

[9.9] E. López-Morillo, F. Muñoz, A. Torralba, F. Márquez-Lasso, I. Rebollo and **J. R. García-Oya**, "Compact low-power implementation for continuous-time ΣΔ modulators", *Integration, the VLSI Journal*, accepted to be published, 2012.

9.4.2 Conference communications

[9.10] T. Sánchez-Rodríguez, F. Muñoz, **J. R. García**, J. M. Rodríguez, M. Jiménez-Fuentes, R. G. Carvajal, "A Novel CMOS Tunable Linear Transconductor Based on Quasi Floating Gate Transistors," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, Grenoble, France, November 2008.

[9.11] B. Palomo, F. Muñoz, R. G. Carvajal, **J. R. García**, H. El-Gimli, A.Torralba, "A Very Low Power 8-Bit 16MSamples/s Pipelined Converter for DVB-H," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, Grenoble, France, November 2008.

[9.12] F. Muñoz, F. Márquez, R. G. Carvajal, **J. R. García**, A. Torralba, "A 185 mW, 6-Bit, 1GS/s, Flash A/D Converter Based on a New Autozering Technique," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, Grenoble, France, November 2008.

[9.13] D. Hely, V.Beroulle, Feng L., **J. R. G. Oya**, "Towards an Unified IP Verification and Robustness Analysis Platform", *IEEE 14th International Symposium on Design and Diagnostics of Electronics Circuits & Systems (DDECS'2011)*, Cottbus, Germany, April 2011.

[9.14] E. López-Morillo, F. Muñoz, A. Torralba, F. Márquez, **J. R. García-Oya**, "A Very Low-Area Amplifier-Less Sigma-Delta Modulator for RFID Applications," *XXVI Conference of Design of Circuits and Integrated Systems (DCIS'2011)*, Albufeira, Portugal, November 2011.

9.5 Published contributions

9.5.1 Journal papers

"Data Acquisition System Based on Subsampling for Testing Wideband Multistandard Receivers," *IEEE Transactions on Instrumentation and Measurements*, 2011.

Data Acquisition System based on Subsampling for Testing Wideband Multi-Standard Receivers

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Abstract— **In this paper a data acquisition module meeting the specifications to become part of a wideband multi-standard receiver test system is presented. With only a low-jitter wideband Sample-and-Hold and an intermediate frequency Analogue-to-Digital Converter, and by using subsampling, the proposed module provides a high resolution over a large bandwidth. Using commercial devices on a multilayer printed circuit board, experimental results show more than 8 bits resolution for a 20 MHz signal bandwidth with up to 4 GHz center frequency, which is sufficient to cover the needs of test systems for most present wireless communication standards.**

Keywords— **Analogue-to-Digital Converter, Software Defined Radio, Jitter Noise, Sample&Hold, Thermal Noise**

I. INTRODUCTION

Due to the widespread acceptance of wireless technologies there is a large number of different communication standards, each one with a specific set of characteristics, such as carrier frequency and bandwidth. As a consequence, there is a trend to design transceivers capable of working with multiple standards in different frequency bands [1]-[2]. A similar problem arises in the test industry, where accurate multi-standard receivers, preferably low cost, are an essential element.

Concerning the topology of a multi-standard receiver, the position of the Analogue-to-Digital Converter (ADC) in the front-end chain is crucial, as shifting the analog blocks (filter, mixer and amplifier) to the digital domain increases the flexibility of the receiver. The extreme case is known as the Software Defined Radio (SDR) paradigm [3], where the ADC is placed right behind the antenna to directly digitize the RF signal. This approach imposes so high requirements on the ADC that it is beyond the state of the art of present technology [4], where the ADC is limited to 7-8 bits for 3 GS/s sampling rate.

Different receiver architectures have been proposed to overcome this problem, such as direct conversion [5], low Intermediate Frequency (IF) [6], and subsampling [7]-[8]. In subsampling receivers the RF signal is sampled using frequencies lower than the maximum input frequency, but larger than two times the signal bandwidth. One of the low frequency replicas of the sampling product, which contains the baseband signal, is then directly digitized.

Subsampling receivers use a Sample&Hold (S&H) to produce low frequency replicas of the RF signal based on pass-band sampling technique [8]. Therefore, the main advantage of the system based on subsampling is its flexibility, because it is possible to process most of the signal digitally [9]. Also, the number of analog building blocks is lower and an ADC with relaxed specifications can be used. The drawbacks of subsampling are the demanding specifications required for the S&H (wide input bandwidth and low aperture jitter) and the resulting high noise figure due to the effect of the folded thermal noise in the band of interest.

As the performances of subsampling receivers are limited by the stringent specifications on the S&H, present implementations of commercial receivers are limited to no more than 7-8 bits, i.e., a Signal-to-Noise Ratio (SNR) between 45-52 dB in the input range 1-2.4 GHz using a 10-bit ADC [10].

In this paper an ADC board based on subsampling meeting the specifications of high performance low-cost multi wireless standards test equipment is presented. The Analog-to-Digital Conversion System achieves, for a signal bandwidth of 20 MHz, an 8.5 bit resolution with a programmable carrier frequency ranging from 0 up to 3.3 GHz, and more than 8 bit resolution up to 4 GHz [11]. As the number of analogue blocks is minimum, by proper selection of the center frequency and signal bandwith the module suits the needs of the different wireless standards (i.e., GPS, GSM, GPRS, UMTS, Bluetooth, Wi-Fi, WiMAX). This design is intended to be part of a conformance test system for multiple wireless standards and thus the signals arriving at the subsampling receiver are assumed to be filtered and interference free. Thus the first analogue stage is not part of the design and the input signal is treated as a bandpass signal with a maximum of 20 MHz bandwidth. For lower bandwidths, the system resolution will be larger than the experimental results shown in section IV.

This paper is organized as follows: section II discusses subsampling and reviews theoretical concepts. Section III presents the components selection and the Printed Circuit Board (PCB) prototype design. In section IV some experimental results are presented. Finally, some conclusions are drawn in section V.

II. A REVIEW OF SUBSAMPLING

A. *Concept of subsampling*

Subsampling is the process of sampling a signal with a frequency lower than twice the signal highest frequency.

Subsampling a bandpass RF signal will fold the signal spectrum to lower frequencies, where these replicas of the RF signal at baseband or IF can be used to extract the original baseband signal (see Fig. 1). In this Section the subsampling process is reviewed.

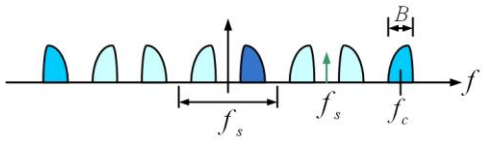


Fig. 1 Subsampling concept (m=3)

B. Selecting the sampling frequency

For a given signal bandwidth (BW) and carrier frequency (f_c) it is convenient to select an appropriate sampling frequency [12].

Usually, the minimal sampling frequency is determined by the Nyquist Theorem: $f_s > 2\ (f_c+BW/2)$. However, for a bandpass signal a sampling frequency lower than the Nyquist frequency can be selected if expression (1) still holds:

$$(2f_c - BW)/m > f_s > (2f_c + BW)/(m+1) \quad (1)$$

where m is the number of replicas of the signal spectrum in the range [0, f_c-BW/2] limited to a maximum of $(fc\text{-}BW/2)/BW$.

An appropriate value is $f_s=4f_c/m_{odd}$ which produces a replica at $f_s/4$. The number of replicas is selected to the odd number m_{odd}.

C. Non-idealities due to the sampling process

A general scheme for a subsampling receiver is shown in Figure 2a. It deserves to be mentioned that this receiver is very simple, especially if it is compared to the conventional heterodyne architecture. However, as the Sample&Hold (S&H) processes high frequency signals, its requirements are much more restrictive than those expected from the signal bandwidth. The main non-idealities to be considered in the S&H are the following:

1) *Jitter Noise*: There are two main sources of jitter noise, (a) the phase noise associated to the clock reference and (b) the aperture jitter of the S&H. In a first order approach, they can be considered to be non-correlated Gaussian stochastic processes.

The aperture jitter of a Sample&Hold implemented with a MOS transistor is signal-dependent, because the transistor threshold voltage depends on the input signal value. For a sinusoidal input signal the Signal-to-Noise and Distortion Ratio (SNDR) at the S&H output is approximately given by expression (2) [13]:

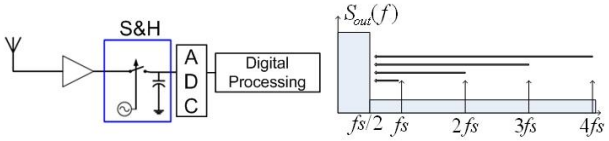
$$SNDR = \frac{A^2/2}{\overline{N_\tau}} = \begin{cases} 1/4\pi^2 f_{in}^2 \sigma_\tau^2 : 2\pi\ f_{in}\sigma_\tau << 1 \\ 1/2\,(1 - e^{-2\pi^2 f_{in}^2 \sigma_\tau^2}) : otherwise \end{cases} \quad (2)$$

Where A is the signal amplitude, $\overline{N_\tau}$ is the average noise power, f_{in} is the input frequency, and σ_τ is the jitter standard deviation.

Concerning the system clock, there are two primary mechanisms that cause jitter: the thermal noise and the coupling noise. The latter can be caused by crosstalk and/or ground loops within, or adjacent to, the area of the circuit. Special care has to be taken with the power lines.

2) *Folded Thermal Noise:* The S&H suffers from *kT/C* noise, as the entire wideband noise folds inside the band of interest (Fig. 2b).

Therefore, although the total noise power is not dependent on the sampling frequency, the noise floor reduces if the frequency increases [13]. In particular, the noise floor is reduced by 3 dB when the sampling frequency is doubled. Therefore, it is convenient to select then largest sampling frequency among the set of possible sampling frequencies. This one will be named as the "optimal" sampling frequency.



(a) Subsampling Receiver (b) Folded Thermal Noise

Fig. 2. a) A subsampling receiver. b) Folded thermal noise due to the sampling process

III. BOARD DESIGN

From the analysis described in Section II and the simulations performed, the specifications of the main building blocks of the module, i.e., the Sample&Hold and the ADC, can be derived. In order to obtain a total resolution larger than 8 bits for a maximum input frequency of 4 GHz and a signal bandwidth of 20 MHz, the main specification of the Sample&Hold is an aperture jitter lower than 100 fs. For the ADC, its main specification is a sampling frequency larger than 400 MS/s in order to reduce the effect of the folded thermal noise.

After a study of the available commercial ADCs, it was decided to use an external S&H since the bandwidth of presently available internal S&Hs is limited to approximately 3 GHz for an Equivalent Number Of Bits (ENOB) of less than 8 bits.

The Inphi 1821 TH [14] was chosen as S&H, because of its low aperture jitter (50 fs). For the target application, other relevant features of this S&H are its large bandwidth (18 GHz), and its large frequency range (0-6 GHz) for 10-bit linearity. In addition it has the capability of sampling at an intermediate frequency of 500 MS/s, which is the maximum sampling frequency for the selected ADC that guarantees a Spurious-Free Dynamic Range (SFDR) larger than 60 dB. The selected ADC is the E2V AT84AS001 [15].

These devices are the main components of the proposed data acquisition system for which a multi layer PCB prototype has been designed and fabricated (Figure 3). Other components, such as bias tees and LP filters, are included between the S&H and the ADC.

This design uses a Class 7 board with DE104i FR4 dielectric, six metal layers and microstrip lines adapted to 50 Ω. The circuit was carefully laid out in order to minimize the jitter effect. The distance between signal tracks, pads and metal layers was carefully chosen in order to reduce crosstalk and inter-symbol interference, which cause jitter. Other rules followed to reduce jitter were a correct decoupling from the

power lines and the so called *picket fences* technique, consisting in placing closely spaced vias between different ground planes. A distance between vias equal to 1/20 wavelength was selected.

IV. Experimental Results

The system performance obtained from measurements is summarized in Table I:

TABLE I
SYSTEM PERFORMANCES

Maximum Input Frequency	**3,3 GHz**
Signal Bandwidth	**20 MHz**
Sampling Frequency	**<500 MHz**
ENOB (SNDR)	**>8.2 bits**
Linearity (SFDR)	**>9.49 bits**
IMD3	**>60.4 dB**
Power Consumption	**3.7 W**

The measured SFDR and IMD3 were about 60 dB regardless of the input frequency, and thus the ENOB (based on the maximum SNDR) is larger than 8.2 bits for sinusoidal input signals up to 3.3 GHz.

Figure 4 shows the system resolution as a function of the carrier frequency up to 20 GHz, for a sampling frequency very close to 500 MHz. The results provide a useful characterization of the system response and clearly show the effect of jitter. From DC to 3.3 GHz there is no significant influence of jitter, as the ENOB is nearly constant in this range. The resolution falls as the input frequency increases, mostly due to the influence of jitter. The system response provides an ENOB larger than 7 bits up to 6 GHz, 6 bits up to 13 GHz and 5.5 bits at 20 GHz.

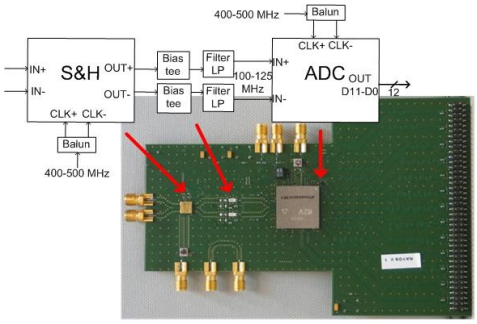


Fig. 3 Block diagram and designed PCB prototype

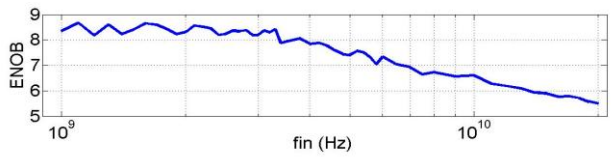


Fig. 4 ENOB vs. Carrier Frequency (20 MHz signal band, up to 20 GHz input carrier frequency)

V. Conclusions

This paper has presented the design of a data acquisition module for testing wireless receivers based on subsampling, which covers most present wireless communication standards requirements, with only one single board configurable by software. Experimental results of the proposed module show (for a 20 MHz signal bandwidth) an ENOB between 8.2 and 8.7 bits up to 3.3 GHz center frequency, and more than 8 bits up to 4 GHz center frequency. Another characteristic of the implemented module is its simplicity, with only a few components on a printed-circuit board. These results show that, for testing purposes, the subsampling based receiver is a viable alternative to other typical receiver architectures, with enhanced reconfigurability and programmability. In future work, an FPGA will be included in the board to autonomously select the optimal sampling frequency and to perform the required digital signal processing (in the present implementation these tasks are carried out by an external computer running LabView).

Acknowledgments

This work has been developed within the scope of the TelMAX Project (www.proyectotelmax.com) and it is partially funded by CDTI–Centro para el Desarrollo Tecnológico e Industrial–, of the Spanish Ministry of Science and Innovation, under the INGENIO 2010 Program/CENIT call.

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"Data Acquisition System Based on Subsampling using Multiple Clocking Techniques," *IEEE Instrumentation and Measurements*, 2012.

Data Acquisition System based on Subsampling using Multiple Clocking Techniques

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Abstract— **This paper presents the implementation of a Data Acquisition System where the folded thermal noise is reduced by using two consecutive subsampling processes. The presented implementation is used to test wideband multi-standard receivers covering most of present communication standards. The proposed system converts a 20 MHz signal modulated with a programmable carrier frequency up to 6.5 GHz, so that it could be used as a universal receiver for Software Defined Radio applications. Experimental results show an ENOB (Effective Number Of Bits) larger than 9 bits up to 2.9 GHz, 8 bits up to 6.5 GHz, and 6.4 bits up to 20 GHz, of input carrier frequency.**

Keywords— **Analog-to-Digital Converter, Multi-standard Receiver, Software Defined Radio, Subsampling, Thermal Noise**

I. Introduction

Providers of testing and certification services to the wireless communication industry need multi-standard receivers in order to cope with present multi-standard transceivers and to reduce the cost in testing equipment. The Software Defined Radio paradigm [1]-[2] is an attractive option where most of signal processing is made in the digital domain and the receiver is configured by software.

Subsampling techniques [3]-[5] can be used to implement the Software Defined Radio paradigm. The subsampling receiver, exploited in a previous work [5], showed to be an advantageous alternative to other conventional receiver architectures based on direct conversion [6] and low Intermediate Frequency (IF) [7]. In [5], a data acquisition system based on subsampling was presented, providing an ENOB of 8 bits for a 20 MHz signal bandwidth with up to 4 GHz center frequency.

This work aims at improving the resolution of the data acquisition system in [5] by using two consecutive subsampling stages. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise. Considering a signal bandwidth of 20 MHz, the improved data acquisition system achieves an ENOB of more than 9 bits for a programmable carrier frequency up to 2.9 GHz, 8 bits up to 6.5 GHz, and 6.4 bits up to 20 GHz.

This paper is organized as follows: section II reviews the subsampling technique. Section III describes the components selected for the printed-circuit board that implements the subsampling process with multiple clocks. In section IV, experimental results are presented. Finally, some conclusions are drawn in section V.

II. Multiple Clock Subsampling

Subsampling techniques can be used to digitize a band limited signal [4] if:

$$2(f_c - BW/2)/(m-1) > f_s > 2(f_c + BW/2)/m \quad (1)$$

Where BW is the signal bandwidth, f_c the carrier frequency, f_s the sampling frequency, and m the number of replicas of the signal spectrum in the range [0, f_c-BW/2], which is a value between 1 and $floor((f_c+BW/2)/BW)$. An appropriate value for the sampling frequency is $f_s=4f_c/m_{odd}$, which produces a replica at $f_s/4$. The number of replicas is selected by the odd number m_{odd}. Since the thermal noise in the band of interest decreases when the number of replicas decreases (Fig. 1a), the largest sampling frequency that meets equation (1) must be selected.

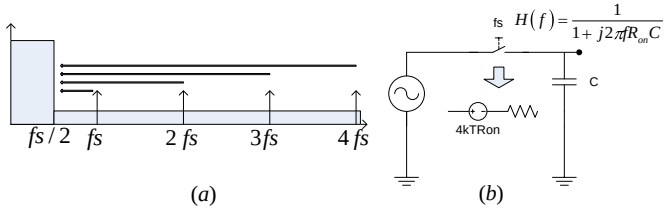

Fig. 1a) Folded Thermal Noise due to the sampling process. b) A switched-capacitor sampling device.

In [5] a unique sampling frequency of 400-500 MHz was selected, as this is the maximum sampling frequency for commercial ADCs with large enough resolution. In this paper, two successive subsampling processes are implemented at different sampling frequencies. The sampling frequency of the first S&H is selected between 1.2 GHz and 2 GHz, obtaining a band-limited signal at the output. As the first sampling frequency is very large the folded thermal noise added by this stage is reduced. After filtering, the resulting signal is subsampled again by a second S&H at 400-500 MHz (Fig.2). However, some drawbacks of the proposed system are a higher complexity and a higher power consumption than the one stage subsampling receiver.

III. Implementation Issues

The S&H in Fig. 2 can be modeled as shown in Fig. 1b, where the switch introduces thermal noise of power spectral density $S_{in}(f)=4kTR_{on}$ that will be filtered by the RC circuit, resulting in an output noise power *of* $P_{n,out}=kT/C$ [8].

For modeling purposes, the output noise can be considered to be a Gaussian thermal noise filtered by a brick-wall filter of bandwidth equal to B_{eff} (noise bandwidth):

$$B_{eff} = \frac{1}{4R_{on}C} = \frac{\pi}{2} f_{3dB} \quad (2)$$

Where f_{3dB} is the 3-dB bandwidth of the RC filter.

On the other hand, the SNR in [$-B_{eff}$,B_{eff}] is defined as [4]:

$$SNR = \frac{P_s}{N_i + (m-1)N_o} \quad (3)$$

Where P_s is the signal power spectral density, and N_i and $N_o$are the in-band and the out-of-band noise spectral power densities, respectively. As $2B_{eff} = mf_s$, if m=1 the Nyquist Theorem is met and the SNR is not affected by the folded noise. On the other hand, if m>1, and assuming $N_i = N_o = N$,

$$SNR = \frac{P_s}{mN} = \frac{P_s}{N(2B_{eff} / f_s)} \quad (4)$$

Therefore, the out-of-band folded noise reduces the SNR by a factor $2B_{eff}/f_s$.

Supposing the noise of both S&Hs in Fig. 2 to be uncorrelated, the output power spectral density due to the S&Hs white noise in Fig. 2a and 2b, respectively, are:

$$P_{N(a)} = \frac{2B_{eff1}}{f_s} N_1 + \frac{2B_{eff2}}{f_s} N_2 ; P_{N(b)} = \frac{2B_{eff1}}{f_{s1}} N_1 + \frac{2B_{eff2}}{f_{s2}} N_2 \quad (5)$$

Where N_1 and N_2 are the noise power introduced by S&H$_1$ and S&H$_2$, respectively, and B_{eff1} and B_{eff2} their respective noise bandwidths. We can observe how the second term only depends on N_2 because of the signal is filtered at IF in both cases, using a BP filter in 2b. Thus, there will not be aliasing of N_1 during the second sampling process. Therefore, the SNR improvement obtained with this frequency plan is given by:

$$\frac{SNR_{(b)}}{SNR_{(a)}} = \frac{P_s / N_{(b)}}{P_s / N_{(a)}} = \frac{B_{eff1}N_1 + B_{eff2}N_2}{\frac{f_s}{f_{s1}} B_{eff1}N_1 + \frac{f_s}{f_{s2}} B_{eff2}N_2} \quad (6)$$

As the first S&H processes high frequency signals, $B_{eff1} >> B_{eff2}$. In addition, the noise power spectral densities of both S&Hs can be assumed to be of the same order of magnitude. Then (6) can be approximated by:

$$\frac{SNR_{(b)}}{SNR_{(a)}} \approx \frac{1}{\frac{f_s}{f_{s1}} + \frac{f_s}{f_{s2}} \frac{B_{eff2}}{B_{eff1}}} \quad (7)$$

Being f_{s1}/f_s the most influential term in this improvement.

IV. Selected Components

The main components chosen in the previous work of [5] were the S&H Inphi 1821 TH and the ADC E2V AT84AS001. In order to implement the new frequency plan of Fig 2b, the maximum sampling frequency for the first S&H is 2 GHz, which is permitted by the S&H Inphi 1821 TH.

As the analog bandwidth of the internal S&H of the E2V AT84AS001is larger than the maximum frequency at the output of the Band-Pass filter Minicircuits RBP-400 (BP in Fig 2b), the second subsampling process can be performed by the internal S&H of the ADC. This analog bandwidth (f_{3dB}) is equal to 1 GHz for the ADC and 18 GHz for the first S&H.

V. Experimental Results

System performances, obtained from measurements, are summarized in Table I. Figure 3 shows the ENOB as a function of the carrier frequency up to 20 GHz, for a signal bandwidth equal to 20 MHz. The solid line shows previous results obtained in [5]. The dashed line shows the expected ENOB calculated with (7), which is met while jitter is not the dominant effect. Finally, the dotted line shows the experimental results obtained with the current work.

TABLE I. System Performances

Maximum Input Frequency	**20 GHz**
Signal Bandwidth	**20 MHz**
Sampling Frequency	**400-500 MHz**
ENOB (SNDR)	**>9 bits up to 2.9 GHz** **>8 bits up to 6.5 GHz** **> 6.4 bits up to 20 GHz**
SFDR	**61.27 (59.57) @ 2 (3) GHz**
Noise Figure	**2.7 (3.8) dB @ 1 (2) GHz**
PSD Noise	**-130.6dBm/Hz @ 1 GHz**
Power Consumption	**3.7 W**

These experimental results show how the proposed system reduces the effect of the folded noise, increasing the ENOB by 0.5-1 bits in the band of interest. Therefore, it provides an ENOB larger than 9 bits up to 2.9 GHz, 8 bits up to 6.5 GHz, 7 bits up to 12 GHz, and 6.4 bits up to 20 GHz. Concerning linearity and power consumption the results are similar to those obtained in the previous work [5].

Table II shows the specifications for most of common wireless communication standards [9] and the results obtained in previously published works and the proposed circuit. It can be seen that only the ENOB specifications for IEEE 802.11a are not achieved, although they are very close. Note that some specifications, like Noise Figure (NF) for UMTS (I) and 802.11b/g, or resolution for Bluetooth, were not achieved without the proposed improvement in this work.

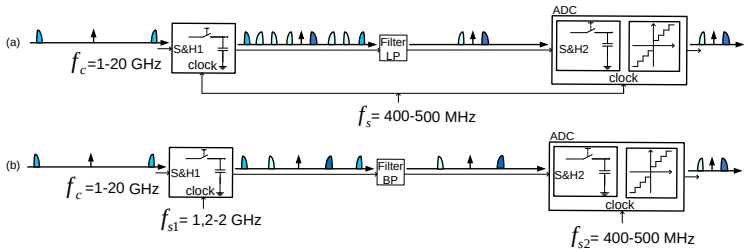

Fig. 2 Clocking schemes of: a) the previous work in [5], and b) the current work.

TABLE II. STANDARDS SPECIFICATIONS AND RESULTS

	Standard	GSM 1800	UMTS (I)	Blue-tooth	802.11b/g	802.11a
Standard requirements	**Carrier Freq. (MHz)**	1805.2-1879.8	2110-2170	2400	2400	5000
	Signal Bandwidth (MHz)	0.2	5	1	20	20
	ENOB (bits)	9	6	11	8	9
	NF (dB)	9.3	4.6	10.7	6.5	18.2
Experimental results of previously published acquisition systems	**ENOB [5] (bits)**	11.76	9.56	10.36	8.2	7.41
	NF [5] (dB)	6.1	6.5	8.3	8.3	13.1
	NF [9] (dB)	5.2	5.6		5.8	
	NF [10] (dB)	5.8	6	6.5	6.5	
	NF [11] (dB)		7.5		7.2	
	Noise PSD [12] (dBm/Hz)				-131	
Experimental results of the presented work	**ENOB (bits)**	12.47	9.97	10.86	8.7	8.34
	NF (dB)	3.6	4.4	6.2	6.2	9.3
	Noise PSD (dBm/Hz)	-129.7	-128.8	-126.9	-126.9	-123.8

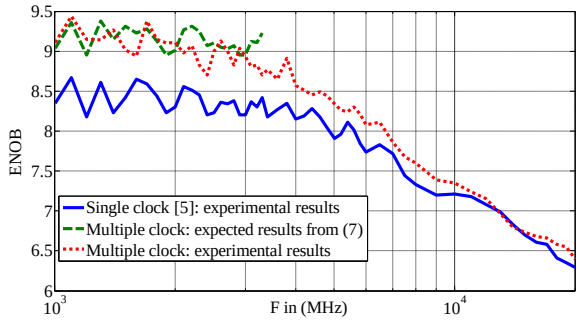

Fig. 3 ENOB vs. Carrier Frequency (20 MHz signal band)

Some of the most significant works related to multi-standard receivers can be found in references [9-12]. Most multi-standard receivers are based on mixing [9]-[10], while the proposed receiver is based on subsampling. This leads to a simpler and more flexible architecture. As additional advantage, the proposed system has a larger tuning range.

There are also published receivers [11]-[12] based on subsampling techniques. For example, [11] is a multi-standard receiver with similar results to the proposed system, but obtained by simulation. [12] presents a 2.4 GHz subsampling receiver with a lower noise. However, note that the receiver in [12] was designed and optimized for a fixed 2.4 GHz central frequency while our solution provides a close value for the Noise PSD despite it has been designed for a wider range.

VI. CONCLUSIONS

In this paper a new versionof a data acquisition module for testing of wireless receivers, based on subsampling, has been presented. The objective is to build a simple and flexible universal receiver on a single printed-circuit board, as part of a portable testing equipment covering the maximum number of wireless communication standards with a high resolution.

The proposed solution implements multiple clocking techniques in order to reduce the folded thermal noise. An analytical expression for the improvement factor in the SNR with respect to the single-clock solution has been obtained. For the selected frequency plan, with two successive subsampling processes, the ENOB has been shown to improve in approximately 1 bit. Experimental results show, for a 20 MHz signal bandwidth, an ENOB of more than 9 bits up to 2.9 GHz, and more than 8 bits up to 6.5 GHz center frequency.

ACKNOWLEDGMENTS

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9.5.2 Chapter books

"Subsampling Receivers with Applications to Software Defined Radio," *Data Acquisition, InTech*, 2012.

Subsampling Receivers with Applications to Software Defined Radio Systems

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Abstract

In this chapter, a complete study about data acquisition systems based on subsampling is presented. The subsampling technique is proposed as a feasible alternative to the RF downconversion stage in receivers for Software Defined Radio (SDR) applications, leading to extremely flexible and simple systems.

In this chapter the subsampling idea is reviewed, with a focus on its main non idealities, i.e., jitter noise and folded thermal noise. According with this study, this chapter proposes a technique based on multiple clocking in order to increase the total resolution of the data acquisition system, so that most of wireless communication standards can be covered.

Besides these multi-standard applications, this chapter proposes to use subsampling techniques in multi-band and nonlinear scenarios, which means an additional problem about the aliasing between channels and harmonics. Thus, this chapter details some innovative techniques to avoid this overlapping effect without reducing the resolution and proposes two subsampling based applications in these environments, such as spectrum sensing in cognitive radios and a subsampling feedback loop for concurrent dual-band power amplifier linearization.

Finally, a data acquisition module for a wideband multi-standard receiver test system is presented. Based on a subsampling architecture, the proposed system provides high resolution over a large bandwidth using only a low-jitter wideband Sample-and-Hold (S&H) and an intermediate frequency Analog-to-Digital Converter (ADC). The system have been implemented with commercial devices on a multilayer printed circuit board and experimental results show more than 8 bits resolution for a 20 MHz signal bandwidth up to 4 GHz center frequency. As the resolution was limited by the folded thermal noise, these features can be improved by using two consecutive subsampling processes, obtaining an Effective Number Of Bits (ENOB) larger than 9 bits up to 2.9 GHz and 8 bits up to 6.5 GHz, which are enough to cover the requirements of test systems for most of present wireless communication standards.

Keywords

Analog-to-Digital Converter, Cognitive Radio, Dual-Band Transmitter, Folded Thermal Noise, Jitter Noise, Linearization Technique, Multi-Standard Receiver, Nonlinear Systems, Sample&Hold, Software Defined Radio, Spectrum Sensing, Subsampling Technique

1. Introduction

Nowadays, there are a large number of different communication standards due to the widespread acceptance of wireless technologies. As a consequence, there is a tendency to design transceivers for multiple standards [1]. A similar problem arises in the test industry, where providers of testing and certification services to the wireless communication industry need multi-standard receivers in order to reduce the cost in testing equipment.

Concerning the topology of a multi-standard receiver, the place of the ADC within the front-end chain is crucial, as shifting the analog blocks (filter, mixer and amplifier) to the digital domain increases the flexibility of the receiver. The extreme case is known as the SDR paradigm [9], where the ADC is placed right behind the antenna to directly digitize the RF signal. For the current communication standards, this approach imposes requirements on the ADC beyond the state of the art, where the ADC is limited to 7-8 bits for 3 GS/s sampling rate.

Different receiver architectures have been proposed to overcome this problem, such as direct conversion [11], low Intermediate Frequency (IF) [12], and subsampling [13]. In subsampling receivers the RF signal is sampled using a frequency lower than the maximum input frequency, but larger than two times the signal bandwidth. One of the low frequency replicas resulting from the sampling process, which contains the baseband signal, is then directly digitized.

The flexibility is the main advantage of the subsampling technique, by using a Sample&Hold (S&H) to produce low frequency replicas of the RF signal, because most of the signal processing is made in the digital domain. In addition, it reduces the number of analog building blocks and relaxes the specifications of the ADC. Otherwise, the drawbacks of subsampling are the demanding specifications required for the S&H (wide input bandwidth and low aperture jitter) and a high noise due to folded thermal noise in the band of interest. In order to reduce the folded noise effect a technique based on multiple clocking will be proposed.

Hence, due to the emergence of several co-existing wireless technologies, subsampling techniques can be useful to implement a receiver for multi-band applications [15]. This multi-band receiver subsampling technique may be used in other applications, such as the feedback loop for linearization of dual-band power amplifiers in RF transmitters [16]. In both cases, the data acquisition involved with the subsampling receiver will have additional limitations, due to the harmonics (nonlinear case) and the other carrier frequencies (multi-band case) are subsampled and might be overlapped with the interest signal. Therefore, to find the valid sampling frequencies in these scenarios is a major challenge. In this chapter, a particular case for dual band applications in a non linear environment will be studied, integrating both effects and describing possible architectures in order to optimize the data acquisition resolution.

To end this chapter, a data acquisition board based on subsampling for high performance low-cost multi-standard test equipment is presented. With a signal bandwidth of 20 MHz it achieves 8.5 bit resolution for a programmable carrier frequency ranging from 0 up to 3.3 GHz, and more than 8 bit resolution up to 4 GHz. By a proper selection of the center frequency and signal bandwidth, the proposed board can be used to digitalize the signal in most of present wireless standards. This design is intended to be part of a test system; that is, the input signal of the subsampling receiver is assumed to be filtered and free of interferences. Finally, an improvement based on the multiple clocking techniques previously described is employed to improve the resolution of the presented data acquisition system. By using two consecutive subsampling stages, this approach allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the

folded thermal noise. Considering a signal bandwidth of 20 MHz, the improved data acquisition system achieves an ENOB of more than 9 bits for a programmable carrier frequency up to 2.9 GHz and 8 bits up to 6.5 GHz, presenting an improvement in the resolution of 0.5-1 bit.

This chapter is organized as follows: section 2 reviews the signal representation and definitions for wireless communication signals while section 3 reviews the sampling theory. Section 4 describes the theoretical concept of subsampling techniques, detailing their advantages and main drawback, i.e., jitter and folded noise. Concerning the folded noise an approach based on multiple clocking is proposed in order to reduce its effect over the resolution. In this theoretical section the typical problems of subsampling techniques are extended to multi-standard and nonlinear applications, and an optimization for receivers in these scenarios is proposed as well. Finally, section 5 describes the implementation of a data acquisition system and performs a comparison with other published multi-standard receivers, which are classified according by architecture: mixing or subsampling based, and wide-band or narrow-band.

2. Signal Representation and Definitions

In current wireless communication links (Figure 1), a complex modulated baseband signal containing the useful information can be expressed as:

$$s(t) = A(t)e^{j\varphi(t)} = I(t) + jQ(t) = A(t)\cos\varphi(t) + jA(t)\sin\varphi(t) \tag{1}$$

This signal is usually up-converted to an RF band pass signal around a carrier frequency f_c to be transmitted through a wireless channel and detected by a receiver and converted back to base band again. The pass band transmitted signal can be written as follows

$$\tilde{s}(t) = \Re[s(t)e^{jw_c t}] = \Re[A(t)e^{j\varphi(t)}e^{jw_c t}] = A(t)\cos(w_c t + \varphi(t)) \tag{2}$$

Where $w_c = 2\pi f_c$ and $A(t)$ and $\varphi(t)$ are amplitude and phase of the complex base band signal, and the transmitted signal, $\tilde{s}(t)$, is the real part ($\Re[.]$) of the complex envelope of the RF pass band signal after up-conversion. In practice situations the bandwidth of the base band signal assumed BW hereinafter is much less that the carrier frequency f_c.

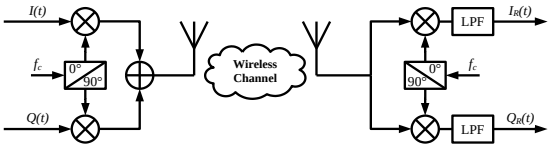


Figure 1. A typical wireless link

The radio channel is modeled as a linear time invariant system; however, due to the different multipath waves which have propagation delays which vary over different spatial locations of the receiver, the impulse response of the linear time invariant channel should be a function of the time, t, and the position of the receiver, d, in such case, the channel can be described by $h(d,t)$.

The pass band signal at the mobile receiver can be expressed as

$$\tilde{s}_R(d,t) = \tilde{s}(t) \otimes h(d,t) \tag{3}$$

In case of stationary receiver the above equation can be reduced to

$$\tilde{s}_R(t) = \tilde{s}(t) \otimes h(t,\tau) = \int_{-\infty}^{t} \tilde{s}(t)h(t-\tau)d\tau \tag{4}$$

The received baseband signal can be obtained following a frequency down conversion and channel equalization of the received pass band signal as follows

$$\begin{aligned} s_R(t) &= (\tilde{s}_R(t)e^{-jw_c t}) \otimes h^{-1}(t,\tau) \\ &= \tfrac{1}{2}A_R(t)\cos\varphi_R(t) + \tfrac{1}{2}A_R(t)\cos\varphi_R(t)\cos 2w_c t - \tfrac{1}{2}A_R(t)\sin\varphi_R(t)\sin 2w_c t \\ &+ \tfrac{1}{2}jA_R(t)\sin\varphi_R(t) - \tfrac{1}{2}jA_R(t)\sin\varphi_R(t)\cos 2w_c t - \tfrac{1}{2}jA_R(t)\cos\varphi_R(t)\sin 2w_c t \end{aligned} \tag{5}$$

and the high frequency components ($2\omega_c t$) are filtered out using low pass filters shown in Figure 1. The I/Q component of the received base band signal can be expressed as

$$I_R(t) = A_R(t)\cos\varphi_R(t) \;\; and \;\; Q_R(t) = A_R(t)\sin\varphi_R(t) \tag{6}$$

3. Review of sampling theory

At the receiver end of the communication system, the RF signal are decomposed into their respective I and Q baseband components. A continuous time domain signal *x(t)* should be sampled such that the signal can be reconstructed and no information is lost. Using ADCs, the continuous time domain signal is converted to a discrete time domain signal *x[n]* through a uniform sampling process taking at sampling period T_s, and their relation is $x[n]=x(nT_s)$.

Discrete time sampling affects the resolution of the final time domain signal being processed. Consider a sine wave operating at 200 Hz, and continuous time domain signal representation is shown in Figure 2a. Using a sampling frequency of 10 kHz, the sine wave is still visible in Figure 2b. However, using a sampling rate of 2 kHz as in Figure 2c results in a less accurate representation of the sine wave.

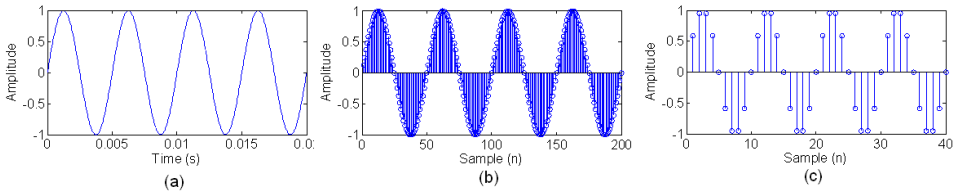


Figure 2: Time domain representation of (a) 200 Hz continuous sine wave (b) sampled at 10 kHz and (c) sampled at 2 kHz

The discrete time signal *x[n]* can be viewed as a multiplication of the continuous wave function *x(t)* with a train of impulse functions [17]. The sampled version of the signal can be expressed as

$$x_S(t) = x(t)\delta_T(t) = \sum_{n=-\infty}^{\infty} x(nT_S)\delta(t-nT_S) \tag{7}$$

The impulse train can be further expressed as a Fourier series

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_S) \xleftrightarrow{\mathfrak{I}} \omega_S \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \tag{8}$$

where $\omega_s=2\pi/T_s$. Since a multiplication in the time domain results in convolution in the frequency domain, the Fourier transform of the sampled signal, $X_S(\omega)$ in relation to the RF signal's Fourier transform, $X(\omega)$, is

$$X_S(\omega) = \frac{1}{2\pi} X(\omega) * \left[\omega_S \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \right] = \frac{1}{T_S} X(\omega) * \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \tag{9}$$

Using the convolution property of the impulse function, the simplified version of the impulse-modulated signal becomes

$$X_S(\omega) = \frac{1}{T_S} \sum_{k=-\infty}^{\infty} X(\omega - k\omega_S) \tag{10}$$

showing that the spectrum is replicated every ω_s.

Choosing a sampling frequency for a band limited signal affects the reconstruction process. A band limited signal with total bandwidth (*BW*) is denoted in Figure 3. For Figure 3a, the sampling frequency $f_s=1/T_s=\omega_s/2\pi$ is much larger than the bandwidth, and perfect reconstruction is possible. Similarly, for the case when $f_s=BW$ as in Figure 3b, the spectrums do not overlap, or alias, over each other and the signal can still be decoded properly. However, in Figure 3c, f_s is less than *BW*, and aliasing occurs over the signal. This aliasing corrupts the information in the signal and is unrecoverable. The minimum sampling rate, or the Nyquist sampling rate, should be $f_s >= BW$ in order to correctly decode the signal.

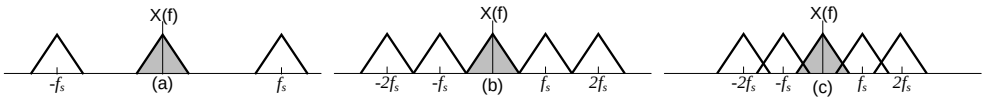


Figure 3: Sampling of a signal using (a) $f_s >> BW$ (b) $f_s = BW$ and (c) $f_s < BW$

4. Theory of operation

This section introduces the subsampling idea, detailing the method to select the optimal sampling frequency. Next, the two main limitations of the subsampling based systems, i.e., jitter a folded thermal noise, are described. Finally, the concept of subsampling is extended to nonlinear systems and multi-band applications, describing a method to optimize the performance in terms of noise.

4.1 Concept of subsampling

As mentioned before, moving the ADC closer to the antenna increases the flexibility of the receiver. However, this conversion just after the antenna would prohibitively increase the bandwidth and sampling frequency requirements of the ADC. Nevertheless, the bandwidth of a bandpass signal is

usually a fraction of its center frequency, so that it is possible to subsample the signal (i.e., violating the Nyquist condition) avoiding aliasing between replicas.

Subsampling is the process of sampling a signal with a frequency lower than twice the highest signal frequency, and higher than the signal bandwidth *BW*. Using an ideal S&H device with sampling frequency f_s will generate harmonics at f_s, $2f_s$...mf_s, where m is an integer. In the case for Figure 4a, a bandpass RF signal is centered at f_c, while the m^{th} closest harmonic generated by the S&H and lower than f_c is k, where k = floor(f_c/f_s). The replicas of the signal that are generated by the S&H exist at $-mf_s + f_c$, while the mirrored versions replicas exist at $(m + 1)f_s - f_c$. Figure 4b shows these replicas, and the signal replica within the [0-$f_s/2$] range (centered at $f_{if}=f_c-kf_s$) can be used to extract the original RF signal.

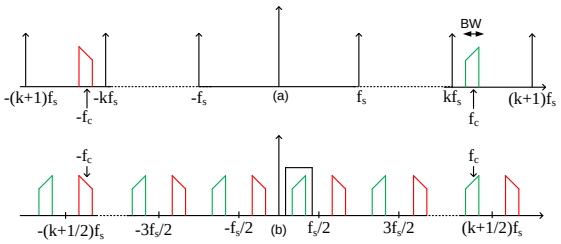


Figure 4. Illustration of the concept of subsampling: (a) Frequency domain representation of the RF passband input signal along with the subsampling frequency and S&H harmonics and (b) signal replicas following subsampling process when selecting $f_s=(f_c-f_{if})/k$ and $f_s>BW$

4.2. Selecting the sampling frequency

This section provides the method to select the optimal sampling frequency (f_s) for a given signal bandwidth (*BW*) and carrier frequency (f_c). Usually, the minimal sampling frequency is determined by the Nyquist Theorem: $f_s>2(f_c+BW/2)$. However, for a bandpass signal a sampling frequency lower than the Nyquist frequency can be selected if expression (11) still holds [14]:

$$2(f_c - BW/2)/(m-1) > f_s > 2(f_c + BW/2)/m \tag{11}$$

where m is the number of replicas of the signal spectrum in the range [0, $f_c-BW/2$], and lies between 1 and $floor((f_c+BW/2)/BW)$. An appropriate value is $f_s=4f_c/m_{odd}$ which produces a replica at $f_s/4$. Using an odd integer m_{odd} ensures that the signal is at $f_s/4$, while m_{even} generates the low frequency alias of the signal at $3f_s/4$.

An example that illustrates the convenience of sampling at $4f_c/m_{odd}$ can be observed in Figure 5, which shows the output spectrum when an input signal at 1070 MHz is sampled at f_s of 475.56MHz (Figure 5a) and at nearby frequency of 480 MHz (Figure 5b). It can be seen how the second order harmonic at 237.78 MHz is placed further from away the desired signal in the case of Figure 5a compared with Figure 5b (at 220 MHz). Therefore, sampling at $4f_c/m_{odd}$ results in a larger subsampling frequency bandwidth and relaxes the filtering requirements after the S&H. As f_s, f_c and f_{if} are all directly related, there are bandwidth and frequency tradeoffs when selecting the subsampling frequency.

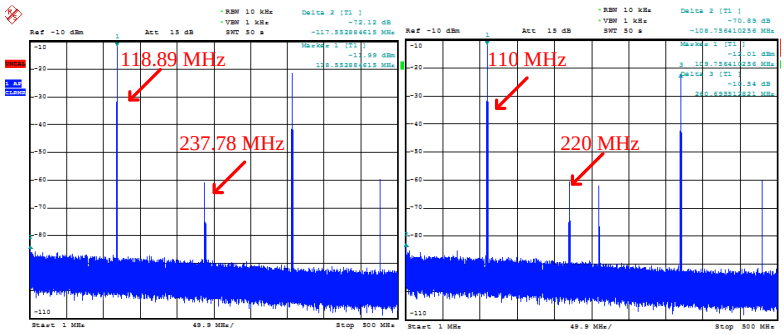


Figure 5. Output spectrum of the subsampler when the 1070 MHz RF signal is subsampled at a f_s of (a) 475.56 MHz (m_{odd}=9 and f_{if}=118.89 MHz) and (b) 480 MHz (m_{odd}=9 and f_{if}=110 MHz)

4.3. Main non idealities of a subsampling system

A general scheme for a subsampling receiver is shown in Figure 6. It deserves to be mentioned that this receiver is very simple, especially if it is compared to the conventional heterodyne architecture. However, as the S&H processes high frequency signals, its requirements are much more restrictive than those expected from the signal bandwidth. The main non-idealities to be considered in the S&H are jitter and folded thermal noise and will be described in the sub-sections.

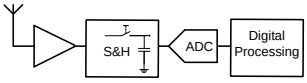


Figure 6. Subsampling receiver scheme

4.3.1. Jitter

Clock jitter is an important limitation in the data acquisition systems at high signals frequencies because leads to sampling time uncertainly. Jitter is the deviation of the reference edges of the clock signal with respect to their ideal position in time. In this chapter we will consider this deviation as a random noise. As shown in Figure 7, a random error τ_n from the nominal sampling time instant t_n causes a random error $\varepsilon_\tau(n)$ in the amplitude of the sampled signal [18]. This effect can be seen as an addition of noise to the output signal, resulting in a degradation of the output Signal-to-Noise Ratio (SNR).

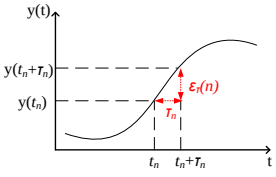


Figure 4. Concept of jitter

The amplitude error (v_{error}) is proportional to the derivative of the input signal [19]:

$$v_{error} = \Delta t \frac{dv_{in}}{dt} \tag{12}$$

With a jitter value of Δt. For a sine wave of frequency f_{in} and amplitude A_{in}, the maximum error is [19]:

$$v_{error\_\max} = \Delta t A_{in} 2\pi f_{in} \tag{13}$$

There are two main sources of jitter noise, the phase noise associated to the clock reference and the aperture jitter of the S&H. The aperture jitter of an S&H implemented with a MOS transistor is signal-dependent, as the transistor threshold voltage depends on the input signal. Concerning the system clock, there are two primary mechanisms that cause jitter: the thermal noise and the coupling noise. The latter can be caused by crosstalk and/or ground loops within, or adjacent to, the area of the circuit. Special care has to be taken designing the power lines in the data acquisition board that will be described in the next sections.

In a first order approach, these two sources of jitter noise can be considered as uncorrelated Gaussian stochastic processes, each one with a particular standard deviation. Being Δt_{rms} the standard deviation of jitter (or root mean square), which usually defined as a percentage of the sampling period, the sampling error in (12) can be re-written as [19]:

$$\sigma(v_{error}) = \Delta t_{rms} \sigma(dv_{in}/dt) = \Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}} \tag{14}$$

where $\sigma()$ is the standard deviation.

Therefore, the resulting SNR on the sampled signal is then [19]:

$$SNR_{jitter} = 20\log\left(\frac{A_{in}/\sqrt{2}}{\Delta t_{rms} 2\pi f_{in} \frac{A_{in}}{\sqrt{2}}}\right) = -20\log(\Delta t_{rms} 2\pi f_{in}) \tag{15}$$

Note that the SNR is degraded when the input frequency increases.

This approximation will be true if $2\pi f_{in}\Delta t_{rms} << 1$, otherwise the general expression for the SNR due to the uncorrelated random jitter noise for a sinusoidal input signal can be expressed as follows [18]:

$$SNR = 20\log\left(\begin{cases} 1/4\pi^2 f_{in}^2 \Delta t_{rms}^2 : 2\pi f_{in}\Delta t_{rms} << 1 \\ 1/2(1 - e^{-2\pi^2 f_{in}^2 \Delta t_{rms}^2}) : otherwise \end{cases}\right) \tag{16}$$

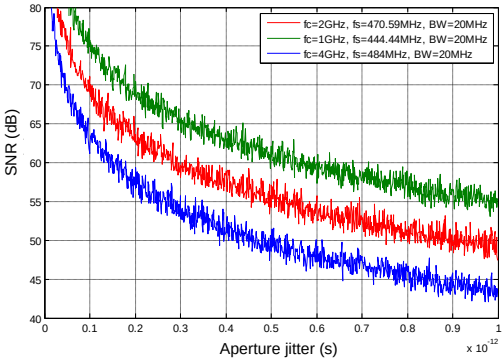
The expression of SNR for $2\pi f_{in}\Delta t_{rms} << 1$ is valid for all jitter distributions while the other SNR expression only applies to a random jitter with Gaussian distribution $N(0, \Delta t_{rms})$ [18]. Moreover, small jitter noise can be approximately regarded as sampled Additive White Gaussian Noise (AWGN) while for large jitter, this assumption is not valid anymore.

In the particular case of subsampling, jitter noise is an important limitation due to high input frequencies are processed. Thus, in order to validate this theoretical study, jitter noise is simulated using typical values for receivers subsampling based, i.e., the input frequencies in the GHz range, the sampling frequencies around 500 MHz (which is a typical limit for high resolution commercial ADCs, as is described in section 5.1), and a 20 MHz signal bandwidth, due to it is a typical value for many communications standards and is used to characterize experimentally the data acquisition board proposed in section 5.1.

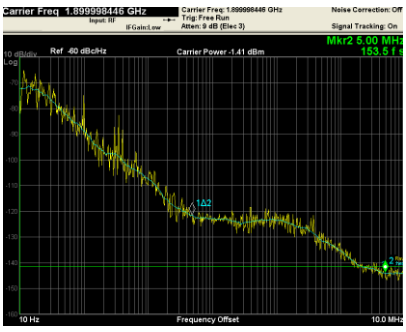
Therefore, using these values, jitter noise has been simulated (using MATLAB) as a stochastic process with average equal to zero and standard deviation equal to Δt_{rms}. Figure 8a illustrates the maximum admited jitter (Axis X) to obtain a concrete SNR (Axis Y) for three different input frequencies (1, 2 and 4 GHz) sampling at the optimum frequency (from equation $f_s=4f_c/m_{odd}$) immediately lower than 500 MHz. In this example, the jitter noise is integrated in a signal bandwidth equal to 20 MHz and it can be observed how the SNR will be decreased around 6 dB each time the input frequency is doubled, as can be predicted by (16).

This traditional method, based on equation (16) to obtain the SNR as a function of clock jitter and signal frequency, has some limitations, as the assumption of a full scale scenario. Although this situation may happen in some applications, most commonly the input signal energy is spread over some bandwidth. In these cases it is more realistic to study the jitter effect from the spectrum domain.

Since the spectrum of jitter is very difficult to measure directly [19], the most common method to study its effect is measuring the phase noise, which is the most widely employed parameter to compare between different clock sources and oscillators.



(a)



(b)

Figure 8. (a) SNR requirements as a function of the jitter for different input frequencies and phase noise for a clock frequency equal to 1.9 GHz

The phase noise is defined as the frequency domain representation of the phase modulation of the clock signal due to the jitter. Being the clock signal a sine wave of frequency f_s [19]:

$$v_{clock} = A\sin(2\pi f_s(t + \Delta t(t))) = A\sin(2\pi f_s t + \varphi(t)) \tag{17}$$

where $\varphi(t)$is the phase noise in the time domain. Assuming $\varphi(t)$ has small variation around zero, equation (17) can be written as [19]:

$$v_{clock} \cong A\sin(2\pi f_s t) + A\cos(2\pi f_s t)\varphi(t) \tag{18}$$

The second term of this expression is the additive noise due to the phase modulation. Since the phase noise appears multiplied by a cosine in the above time domain expression, in the frequency domain the spectrum of the phase noise, $\Phi(f)$, is convolved with the noise-free clock and appears as sidebands around its center frequency. This noise is usually represented as $L(f)$ (single-sideband phase noise power spectrum) and is equal to the noise power spectral density per Hertz at the frequency f_s+f normalized by the clock or oscillator signal power $A^2/2$. It is called single-sideband because only one side of the noise power is taken into account; hence it includes only half the noise energy. Thus [19]:

$$\begin{aligned} L(f) &= 10\log\left(\frac{1}{2}\Phi^2(f)\right) \\ \varphi(f) &= \sqrt{2\cdot 10^{L(f)/10}} \end{aligned} \tag{19}$$

$L(f)$ is represented in dBc/Hz. Figure 8b shows an example of phase noise for a clock frequency equal to 1.9 GHz, which is a typical frequency range for the S&H clock source in the implemented systems, as it will be detailed in the following sections. These experimental measurements show a phase noise of around -95 dBc/Hz, -110 dBc/Hz and -125 dBc/Hz at 100 Hz, 1 KHz and 10 KHz respectively. From (17), the relationship between $\varphi(t)$ and jitter is [19]:

$$\varphi(kT_s) = 2\pi f_s \Delta t(kT_s) \tag{20}$$

That is equivalent to referencing jitter to the clock period. In the frequency domain, where the clock phase noise is most commonly represented, it is then equal to the clock jitter scaled by $2\pi f_s$ [19]:

$$\Phi(f) = 2\pi f_s \Delta T(f) \tag{21}$$

Therefore, we have the following expression to obtain the total jitter from phase noise [19]:

$$\Delta t_{rms} = \frac{1}{2\pi f_s}\sqrt{\int_0^\infty \Phi^2(f)df} = \frac{1}{2\pi f_s}\sqrt{2\int_0^\infty 10^{L(f)/10}df} \tag{22}$$

4.3.2. Folded Thermal Noise

The other main non ideality of the systems based on subsampling is the folded thermal noise. Being the S&H modeled as shown in Figure 9a [18], this thermal noise is introduced by the switch and has a power spectral density (PSD) equal to $S_{in}(f)=4kTR_{on}$, where k is the Boltzmann constant, T is the absolute temperature and R_{on} the on-resistance of the switch. This noise is AWGN and will be folded in the band of interest by the subsampling process, as is described in this section (Figure 9b [7]).

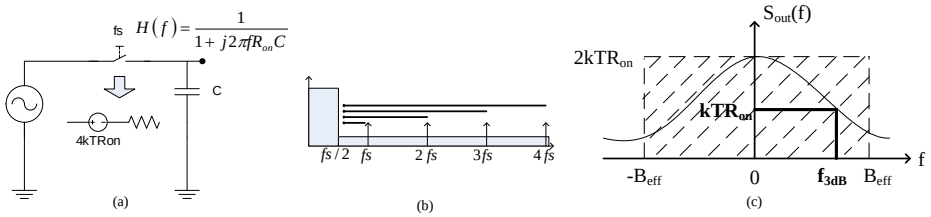


Figure 9. (a) Model of the S&H, (b) thermal noise folded in the band of interest and (c) effective noise bandwidth

R_{on} and C model a LP filter (Figure 9a) with transfer function $H(f)=1/(1+j2\pi fR_{on}C)$, whose 3-dB cutoff frequency is equal to $f_{3dB}=1/(2\ \pi R_{on}C)$. Considering the one-side representation of $S_{in}(f)$, the output PSD will be [18]:

$$S_{out}(f)=S_{in}(f)\left|H(f)\right|^2=2kTR_{on}\frac{1}{1+4\pi^2 f^2 R_{on}^2C^2} \tag{23}$$

Being the total noise power (by a two-sides representation):

$$P_{out}=\int_{-\infty}^{\infty}S_{out}(f)df=\frac{kT}{C} \tag{24}$$

For modeling purposes, the output noise can be considered to be a Gaussian thermal noise filtered by a brick-wall filter of bandwidth equal to B_{eff} (i.e., noise bandwidth, see Figure 9c) [18]:

$$B_{eff}=\frac{1}{4R_{on}C}=\frac{\pi}{2}f_{3dB} \tag{25}$$

Therefore, the power noise can be rewritten as follows [18]:

$$P_{out}=\frac{kT}{C}=2kTR_{on}\cdot(2B_{eff}) \tag{26}$$

On the other hand, the SNR in $[-B_{eff},B_{eff}]$ is defined as [14]:

$$SNR=\frac{P_s}{N_i+(m-1)N_o} \tag{27}$$

Where P_s is the signal power spectral density, and N_i and N_o are the in-band and the out-of-band noise spectral power densities, respectively. As $2B_{eff}=mf_s$, if m=1 the Nyquist Theorem is met and the SNR is not affected by the folded noise. On the other hand, if m>1, and assuming $N_i=N_o=N$:

$$SNR=\frac{P_s}{mN}=\frac{P_s}{N(2B_{eff}/f_s)} \tag{28}$$

Therefore, the out-of-band folded noise reduces the SNR by a factor $2B_{eff}/f_s$, the entire wideband noise being folded inside the band of interest. From (28), we can observe how the noise will be decreased around 3 dB when the sampling frequency is doubled.

It is convenient to select the largest sampling frequency among the set of possible sampling frequencies set by the digital signal processing block specifications. From now on, this one will be termed as the "optimal" sampling frequency (from equation $4f_c/m_{odd}$).

This effect was corroborated experimentally as shown in Figure 10. This figure illustrates how the folded noise is increased when it is employed a lower optimal sampling frequency for an input signal centered at 1473 MHz.

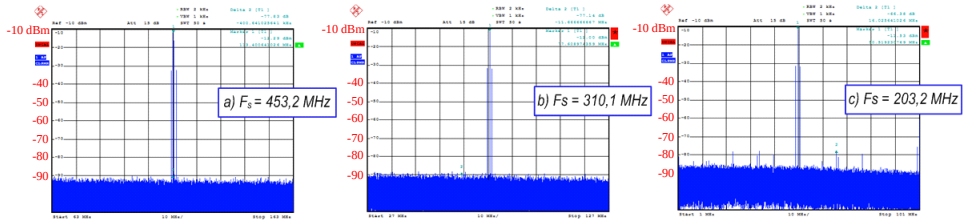


Figure 10. Thermal noise effect depending on the sampling frequency

A limitation of the data acquisition systems based on subsampling will be the maximum sampling frequency, which will be given by the ADC specification and is around 400-500 MHz for commercial ADCs with large enough resolution.

In order to reduce the folded noise effect, this section describes a method to improve the resolution, proposed by [8], which employs two consecutive subsampling stages. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise [8].

Figure 11 shows two different alternatives to implement a subsampling based receiver. Figure 11a illustrates the scheme for a unique subsampling process implemented in [7] while Figure 11b illustrates the scheme with two different clocks proposed by [8].

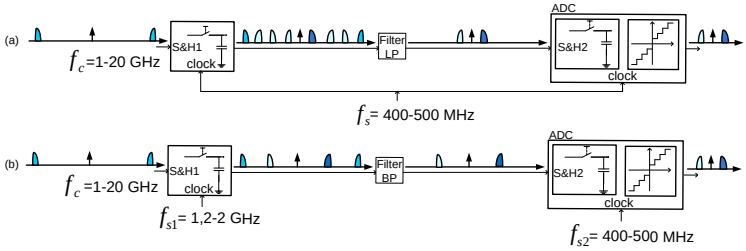


Figure 11. Clocking schemes for: (a) a unique clock source and (b) two clock sources

Assuming the noise of both S&Hs in Figure 11 are uncorrelated, the output power spectral density due to the S&Hs white noise in Figure 11a and 11b, respectively, are [8]:

$$P_{N(a)} = \frac{2B_{eff1}}{f_s} N_1 + \frac{2B_{eff2}}{f_s} N_2; P_{N(b)} = \frac{2B_{eff1}}{f_{s1}} N_1 + \frac{2B_{eff2}}{f_{s2}} N_2 \quad (29)$$

Where N_1 and N_2 are the noise power introduced by *S&H*$_1$ and *S&H*$_2$, respectively, and B_{eff1} and B_{eff2} their respective noise bandwidths. We can observe how the second term only depends on N_2 because of the signal is filtered at IF in both cases, using a BP filter in Figure 11b. In fact, an additional advantage of using a higher sampling frequency is that the requirements of the band pass anti-aliasing filter are relaxed. This is illustrated in Figure 12 [20], where we can observe how the nearest unwanted replica is placed further away from the desired signal when the sampling frequency is increased.

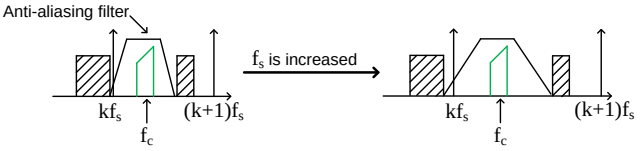


Figure 12. Bandpass anti-aliasing filtering requirements in subsampling

Thus, there will not be folding of N_1 during the second sampling process. Therefore, the SNR improvement obtained with this sampling frequency plan is given by [8]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} = \frac{P_s / N_{(b)}}{P_s / N_{(a)}} = \frac{B_{eff1} N_1 + B_{eff2} N_2}{\frac{f_s}{f_{s1}} B_{eff1} N_1 + \frac{f_s}{f_{s2}} B_{eff2} N_2} \quad (30)$$

As the first S&H processes high frequency signals, $B_{eff1} >> B_{eff2}$. In addition, the noise power spectral densities of both S&Hs can be assumed to be of the same order of magnitude. Then (30) can be approximated by [8]:

$$\frac{SNR_{(b)}}{SNR_{(a)}} \approx \frac{1}{\frac{f_s}{f_{s1}} + \frac{f_s}{f_{s2}} \frac{B_{eff2}}{B_{eff1}}} \quad (31)$$

Being f_{s1}/f_s the most influential term in this improvement. The higher the ratio, the better the SNR improvement.

However, some drawbacks of the proposed system are a higher complexity and higher power consumption than the one stage subsampling receiver.

4.4. Subsampling in multi-band and non linear system

The two main drawbacks of the systems based on subsampling are the jitter and the thermal folded noise, and these make system implementation even harder for multi-band or non-linear applications.

There is a challenge in utilizing the subsampling techniques in nonlinear systems, because the replicas of the generated harmonics are folded in the interest band and may overlap with the desired signals. This issue had been addressed and studied in [21] where a universal formula for bandpass sampling in

nonlinear systems was developed. The extension of this approach for dual band nonlinear systems had been employed in [22].

For dual band applications the main problem of using subsampling is the possible overlapping between the two desired signals in IF frequency band. Although this drawback has been studied in [23], [22] extends this approach in designing the subsampling based receiver and optimizes the system in respect to the typical non idealities of subsampling receivers, i.e., jitter and folded noise.

4.4.1. Subsampling for dual band and non linear systems

The effect of subsampling a dual band signal in a third order nonlinear system is illustrated in Fig. 13 [22], showing the spectrum due to in-band intermodulation and cross modulation.

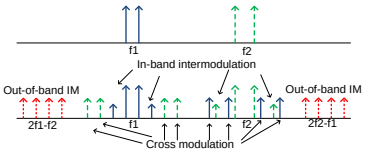


Fig. 13. Power spectrum at the input (top) and the output (bottom) of a nonlinear system

On the other hand, when an input signal centered at f_1 (Figure 14a) [21] drives a nonlinear system, the output signal of this system may produce multiple spectra centered at integer multiples of f_1 (if_1 in Figure 14a). Moreover, each spectrum may have different bandwidths. Thus, let two spectra i and j (with bandwidths B_1 and B_2 respectively) be considered, where $j>i$ and $j-1=k$. If f_s is the sampling frequency then there must exist an integer such that [21]:

$$if_1 + n_k f_s \le jf_1 < if_1 + (n_k + 1) f_s \tag{32}$$

where $n_k = floor((jf_1 - if_1)/f_s)$.

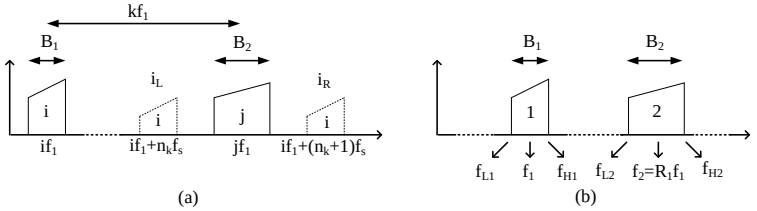


Figure 14. (a) Frequency locations in the sampled output spectrum and (b) Spectrum of the dual band RF signal at the input of the S&H with ratio R1=f2/f1

An algorithm to find the range of valid subsampling frequencies for multiband systems is presented in [23]. Considering the particular case of a dual-band input spectrum as the one shown in Figure 14b, the subsampling frequency must be chosen to ensure that the two signals do not overlap in the subsampled domain.

From the general equations obtained in [23], and considering a dual band case, the maximum replica order of the lower band (n_1) meets the following equation:

$$n_1 = \left\lfloor \frac{f_{L1}}{f_s} \right\rfloor \leq \left\lfloor \frac{f_{L1}}{2((f_{U1} - f_{L1}) + (f_{U2} - f_{L2}))} \right\rfloor \tag{33}$$

Where f_{L1} and f_{U1} are the low and the high limits of the lower band and f_{L2} and f_{U2} are the low and the high limits of the upper band. Knowing $f_2=R_1 f_1$, replica orders of the upper band (n_2) meet the following constraint:

$$\lfloor R_1 n_1 \rfloor \leq n_2 \leq \lfloor R_1 n_1 + R_1 \rfloor \tag{34}$$

Therefore, the eight possible ranges for dual band applications are listed in the following Table 1[23]:

Case	**Range of valid f_s**	**Case**	**Range of valid f_s**
1	$\frac{f_{U2}}{n_2+1/2} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2}-f_{U1}}{n_2-n_1}\right)$	5	$\max\left(\frac{f_{U1}}{n_1+1}, \frac{f_{U2}}{n_2+1/2}\right) \leq f_s \leq \frac{f_{L1}+f_{L2}}{n_1+n_2+1}$
2	$\frac{f_{U2}}{n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1+1/2}, \frac{f_{L2}-f_{U1}}{n_2-n_1}\right)$	6	$\max\left(\frac{f_{U1}}{n_1+1/2}, \frac{f_{U2}}{n_2+1}\right) \leq f_s \leq \frac{f_{L1}+f_{L2}}{n_1+n_2+1}$
3	$\frac{f_{U1}+f_{U2}}{n_1+n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1}, \frac{f_{L2}}{n_2+1/2}\right)$	7	$\max\left(\frac{f_{U1}}{n_1+1}, \frac{f_{U2}-f_{L1}}{n_2-n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2+1/2}$
4	$\frac{f_{U1}+f_{U2}}{n_1+n_2+1} \leq f_s \leq \min\left(\frac{f_{L1}}{n_1+1/2}, \frac{f_{L2}}{n_2}\right)$	8	$\max\left(\frac{f_{U1}}{n_1+1/2}, \frac{f_{U2}-f_{L1}}{n_2-n_1}\right) \leq f_s \leq \frac{f_{L2}}{n_2}$

Table 1. The boundary constraints for the dual band case

Thus, the final sampling ranges will be given by the following expression:

$$F = F_{db} \cap F_{imd} \cap F_{cmd} \cap F_{hmd} \tag{35}$$

Where F is the intersection of all the valid ranges calculated from (32) and (23), F_{db}, F_{imd}, F_{cmd} and F_{hmd} are the valid sampling frequency sets for the fundamental signals, intermodulation, cross modulation and harmonic distortion, respectively.

4.4.2. Optimization of a multi-standard receiver architecture

In order to optimize the noise performance of a dual band receiver in a non linear scenario a particular case has been researched in [22], where seven input frequencies have been selected to study the selective combinations for different dual band applications. These chosen standards are WCDMA (V) at 880 MHz, GSM-DCS at 1.82 GHz, WCDMA (I) at 2.12 GHz, Bluetooth at 2.4 GHz, WiMAX at 3.5 and 5.8 GHz, and 802.11a at 5.2 GHz.

Since the main focus is to cover the maximum number of standards, it is mandatory to use a S&H before the ADC in order to have enough analog bandwidth. The S&H features from Inphi with part number 1821TH has been selected as reference for this work, because of its high input analog bandwidth (up to 18 GHz), minimum aperture jitter (50 fs) and a maximum clock frequency equal to 2 GHz.

The first studies scenario is based on high resolution ADC with a high sampling frequency to reduce the folded noise effect. With this focus in mind the selected ADC was a 12-bit ADS5400 from Texas Instruments with maximum clock frequency of 1 GHz. Using a sampling frequency of almost 1 GHz, it is possible to cover all the dual band applications, as illustrated in Figure 15a (Case 1) [22], where the meaning of axis x is illustrated in Table 2 [22]. Using as reference a typical SNR of the ADC equal to 58 dB, the theoretical SNR for each dual band application was calculated from (15) and (28).

Another option is to use a higher resolution ADC, like the 14-bit ADS5474 from Texas Instruments (Case 2 in Fig. 15a). This device was selected because its maximum sampling frequency is 400 MHz and, therefore, the folded noise would only be around 4 dB higher than Case 1.

X axis	1	2	3	4	5	6
Input Freq (GHz)	0.88-1.82	0.88-2.12	0.88-2.4	0.88-3.5	0.88-5.2	0.88-5.8
X axis	7	8	9	10	11	12
Input Freq (GHz)	1.82 -2.12	1.82-2.4	0.88-3.5	1.82-5.2	1.82-5.8	2.12-2.4

Table 2. Correspondence between dual band applications and axis X

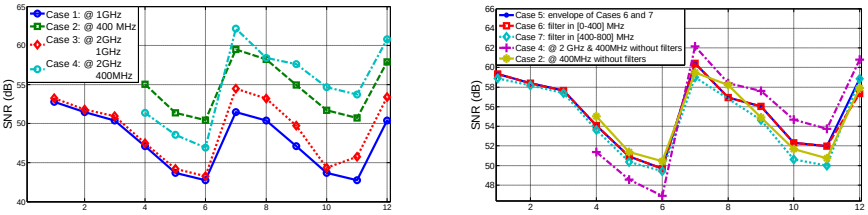


Figure 15. Expected SNR (a) for single and multiple clock architectures and (b) for different architectures based on BP filters

However, as shown in Figure 15a, this option is less flexible, because it is not possible to find any sampling frequency lower than 400 MHz for the first three scenarios. In order to improve the SNR without losing flexibility, two steps subsampling approach is proposed, where the sampling frequency of S&H was set at around 2 GHz and the sampling frequency of ADC at around 1 GHz (Case 3 in Figure 15a). Although this architecture improves the SNR by approximately 3 dB from (28) in respect to Case 1, it could be necessary to implement a second subsampling process and, therefore, a new folded noise effect will be added.

The last option is to use a multiple ADC architecture employing the ADS5474 (Case 4 in Figure 15a) and a first sampling frequency around 2 GHz. Theoretically the SNR is improved around 4 dB in respect to Case 3. In this case, due to the second subsampling process, folded noise effects must be added as well.

For the rest of combinations of frequencies the curves present the same tendency, being possible to cover all the scenarios. However, since cases 2 and 4 present the best results about SNR the next step will be to cover all the dual band applications for these cases. The proposed solution is to use a bank of band-pass filters between the S&H and the ADC. This solution will be applied to Case 4, because it has more flexible architecture, with a higher number of available valid ranges. Using this solution, some harmonics will be removed and the flexibility of the receiver will be increased.

The solution is based on two filters, which their band-pass ranges are [0-400] and [400-800] MHz. The maximum sampling frequency was selected in order to have both fundamental replicas in each range. The selected filter corresponds to the higher of these two frequencies (Case 5 in Figure 15b [22]).

Another solution is to fix a unique BP filter for all the applications (Case 6 and 7 in Figure 14b). In these cases it is possible to cover almost all the standards with only one of these filters, without considerably reducing the resolution. Although in order to maximize the flexibility and the SNR, the optimal architecture is like the one illustrated in Figure 16 [22], for a more concrete application or more relaxed SNR specifications a single BP filter could be used in order to reduce the complexity of the system.

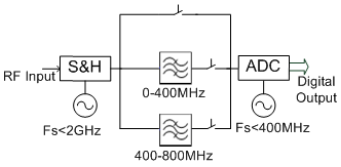


Figure 16. Optimized architecture based on multiple clock and BP filters

4.4.3. Subsampling applications for multi-band and non linear systems

A subsampling receiver for multi-band applications is more advantageous compared to a wideband receiver because it limits the minimum sampling rate to twice the information bandwidth, instead of twice the Nyquist frequency [24]. The reduced sampling frequency allows lower speed commercial ADCs to be used. Two applications are presented: spectrum sensing for cognitive radio applications, and selective multi-band downconversion for amplifier linearization.

4.4.3.1. Spectrum sensing in Cognitive Radios

Wireless spectrums are regulated by government bodies, and are assigned a fixed frequency slot for transmission. Studies reveal that licensed spectrums are highly underutilized and suggest a more efficient and flexible way for spectrum management [25]. Cognitive radio systems aim to reuse these underutilized spectrums through dynamic spectrum allocation, which must integrate a wideband/multiband receiver to scan these spectrums.

A subsampling receiver may allow the cognitive radio to sense different bands to check and see if they are in use. A bank of bandpass filters precedes the input of the receiver to control any interfering

signals that may alias over the signal when using subsampling. Figure 17a shows a block diagram of the subsampling receiver architecture proposed in [15] along with its corresponding validation setup (Figure 17b).

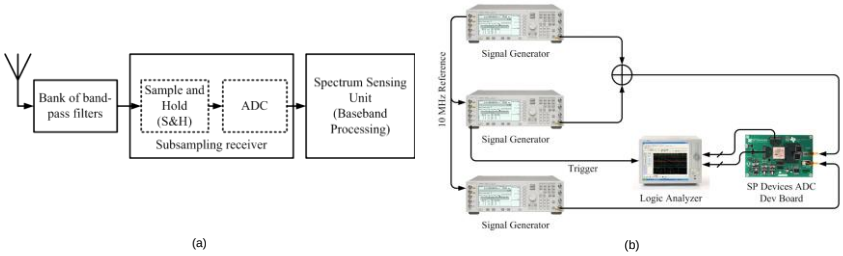


Figure 17. (a) Subsampling based receiver for spectrum sensing in cognitive radio systems and (b) measurement setup for validating spectrum sensing concept using subsampling receiver

As an example for spectrum sensing using a subsampling receiver, two RF bands are selected: the official digital video broadcasting band at 698 – 752 MHz, and an unlicensed band at 902 – 928 MHz. With these two bands and using the formula described in the previous section, a subsampling frequency of 255 MHz is selected.

Figure 17b [15] shows the measurement setup used for spectrum sensing. Two signal generators are used to simulate the two RF bands, then the bands are combined using a power combiner and passed into the receiver. A SP Devices development board using two TI ADS5474 ADCs operating in a time interleaved manner is used as the subsampling device. A logic analyzer is used to capture the digital data streaming from the ADC board, while another signal generator provides a clock source for the ADC.

A three channel signal is sent in the DVB band, while a 2 channel signal is sent in the unlicensed band. Different power levels are configured for each channel to simulate different received signals. Figure 4a shows the spectra of these two bands in the RF domain. Figure 18b [15] shows the two bands subsampled using a frequency of 255 MHz. Since the ADCs are operating in a time interleaving fashion, the differences between each ADC may cause gain mismatches and timing skew [26]. These errors results in attenuated replicas of signals that are being subsampled, specifically at $f_s/2 - f_{in}$, where f_{in} is the subsampled signal frequency.

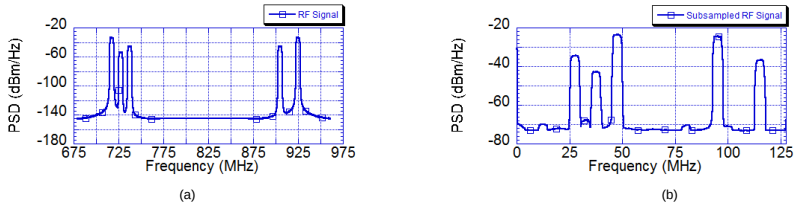


Figure 18. Spectra of (a) the input RF signal to the receiver and (b) the subsampled RF signal for bands (698 – 752 MHz, 902 – 928 MHz) using a subsampling frequency of 255 MHz.

Figure 19a and 19b [15] show the input signals overlaid with their subsampled output after digital demodulation. With the subsampling receiver, the captured signal has approximately a 50 dB signal to noise floor.

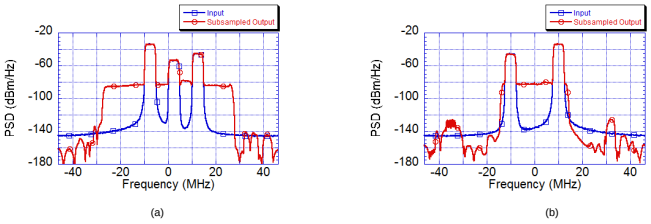


Figure 19. Spectra of the input and filtered output baseband signals for the 698 – 752 MHz band (a) and 902 – 928 MHz band (b)

The technique may be extended to multiple bands, where changing the subsampling clock may allow different RF bands to be demodulated concurrently. In [15], the cognitive radio senses up to 14 bands, sensing two bands at any given time.

4.4.3.2. Subsampling Feedback Loop for Concurrent Dual Band Power Amplifier Linearization

The power amplification (PA) unit is typically the most inefficient component in wireless transmitters. This is caused by an inverse relationship that exists between efficiency and signal quality based on the signal power being transmitted [27]. At low input power, efficiency is low and the amplifier operates in a linear behavior which results in good signal quality at the amplifier output. However, operating the amplifier at its highest efficiency state close to the maximum output power causes the gain characteristics to become compressed, and the input-output relationship becomes nonlinear. The nonlinear behavior reduces the in-band signal quality and causes out-of-band spectral regrowth. Nonlinearity is further complicated in a dual band operation, where the device produces many intermodulation and cross modulation signals. This inverse relationship causes difficulties for the wireless operator, and typically a linear operation mode is used such that signal quality is good, and spectral regrowth is minimal and does not cause interference in other channels.

Digital predistortion allows for the operation of signal in the high efficiency region while reducing spectral regrowth and improving signal quality [28]. This is performed by analyzing the input and output signals of the power amplifier, and generating an inverse behavioral model (predistorter) of the amplifier. The cascade of both the digital predistorter and the power amplifier results in a linear gain at the output for the full power range.

A dual band PA operating at 880 MHz and 1978 MHz is used to test the subsampling feedback loop for concurrent dual band linearization [16]. Two communication signals with 5 MHz bandwidths are sent at the center of these bands. The PA is predicted to have a 5th order nonlinearity, and all the harmonics, intermodulation, and cross-modulation products up to 4 GHz are accounted. In addition, a 25 MHz guard band is placed around each band frequency to account for the spectral regrowth that will happen during the initial analysis stage.

Since the baseband communication signals are known, only the output signals at each band are needed. The harmonics, cross-modulation, and intermodulation signals may be ignored; their only restriction is to not lie inside the guard band of the signals. The subsampling algorithm outlined in the

previous section calculated the minimal subsampling frequency of between 619.7 MHz and 620.1 MHz. Figure 20a shows a simulation of the RF spectra of all the components from DC to 4 GHz, while 20b shows the subsampled components using a frequency of 619.8 MHz [16].

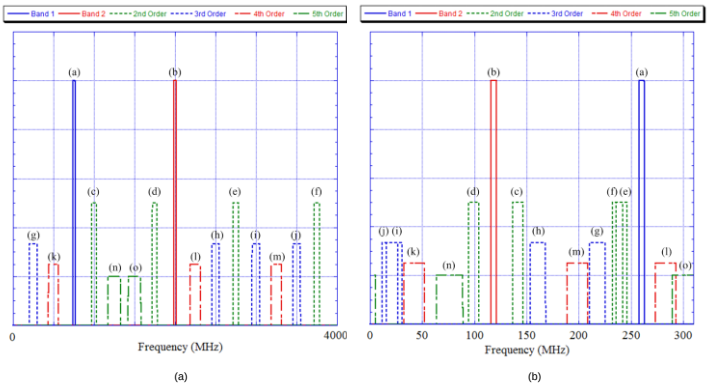


Figure 20. The (a) predicted RF fundamental and harmonics up to 4 GHz and (b) subsampled result using a sampling frequency of 619.8 MHz

The same setup described in Figure 17b is used to generate the dual band signal, and capture the RF output. Figure 21a shows the RF spectra at the output of the PA [16]. Compared to Figure 20a, there is an extra term *p*, which is a 7th order intermodulation product at 436 MHz. The rejection of the *i* and *j* terms are due to the design of the PA output matching network. As explained previously, the time interleaved ADC architecture causes the attenuated signal replicas a_i and b_i. Figure 21b [16] shows the normalized spectra of the subsampled RF PA output. There is attenuation from the upper band signal caused by the limitation of the ADC's bandwidth of 1.4 GHz. The captured time domain signal may be digital demodulated, filtered, and resampled to retrieve the amplifier output of the two bands, and further post-processing can determine the digital predistortion model.

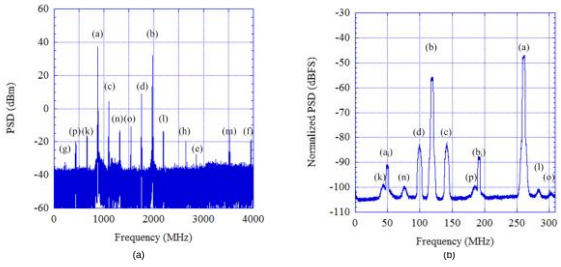


Figure 21. (a) RF spectra at the output of the PA and (b) normalized spectra of the captured subsampled signal using an ADC operating at 619.8 MHz

5. Implemented systems for multi-standard applications

If a multi-standard receiver is implemented by stacking different receivers for different standards into a single receiver, the area and power consumption will be extremely high. Therefore, a properly

designed multistandard receiver must share the hardware resources and use tunable and programmable devices, reducing the area and power consumption, which is a very important approach for battery power devices. Otherwise, for multi-standard applications such as instrumentation or validation, the main constraint is the capability of covering the maximum number of standards as possible.

Moreover, multi-standards receivers might implement a narrow-band strategy or a wide-band strategy. A narrow-band strategy is implemented by the receivers that are designed for some specifics standards, while a wide-band strategy is implemented by the ones that cover a higher number of wireless standards. Therefore, narrow-band receivers might provide a finer optimization for specific standards while wide-band receivers might be considered universal receivers and are used for more general applications.

Finally, multi-standard receivers can be classified by their architectures, i.e., systems based on mixing or subsampling techniques. Although subsampling techniques have some problems as the folded thermal noise effect or the aliasing in multi-band scenarios, for SDR applications are very convenient in order to place, using a few building blocks, the analog-to-digital conversion stage as close the antenna as possible.

5.1. Multi-standard receiver based on subsampling

A data acquisition module for a high performance low-cost multi-standard test equipment is presented in [7]. This work provides high resolution over a large bandwidth with only a low-jitter wideband S&H and an intermediate frequency ADC, by means of subsampling. Using commercial devices on a multilayer printed circuit board, experimental results showed more than 8 bits resolution for a 20 MHz signal bandwidth with up to 4 GHz center frequency, enough to cover the requirements of test systems for most of present wireless communication standards.

From the theoretical analysis and a set of simulations performed, the specifications of the main building blocks of the module, i.e., the S&H and the ADC, can be derived. In order to obtain a total resolution larger than 8 bits for a maximum input frequency of 4 GHz and a signal bandwidth of 20 MHz, the main specification for the S&H is an aperture jitter lower than 100 fs. For the ADC, a sampling frequency larger than 400 MHz is selected in order to reduce the folded noise effect.

After a study of the available commercial ADCs, an external S&H was selected since the bandwidth of presently available internal S&Hs is limited to approximately 3 GHz for an Equivalent Number Of Bits (ENOB) of less than 8 bits. The selected ADC was the E2V AT84AS001.

The Inphi 1821 TH was chosen as S&H, because of its low aperture jitter (50 fs). For the target application, other relevant features of this S&H are its large bandwidth (18 GHz), and its large frequency range (0-6 GHz) for 10-bit linearity. In addition it is able to sample at an intermediate frequency of 500 MS/s, which is the maximum sampling frequency for the selected ADC that guarantees a Spurious-Free Dynamic Range (SFDR) larger than 60 dBc.

These devices are the main components of the proposed data acquisition system for which a multi layer PCB prototype was designed and fabricated (Figure 22a [7]). Other components, such as bias tees and LP passive filters (Minicircuits LFCN-160), have been included between the S&H and the ADC. This design uses a Class 7 board with DE104i FR4 dielectric, six metal layers and microstrip lines adapted to 50 Ω. The rules and expressions employed to adapt the components (designing the dimensions of traces and layers) were obtained from [29].

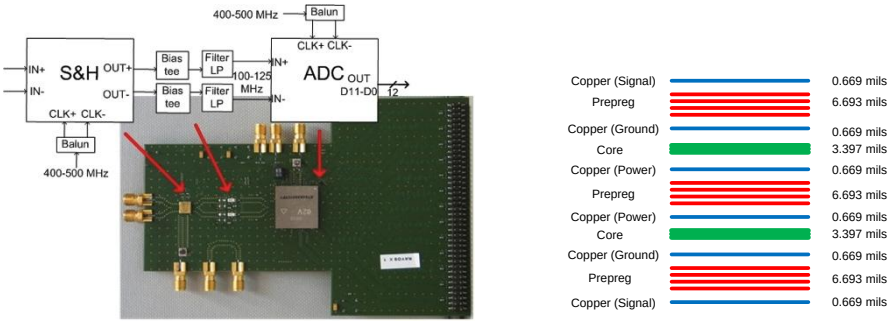


Figure 21. (a) Block diagram and designed PCB prototype and (b) *stack-up* implemented in [6]

Employing the external metal layers (1 and 6) for signals, the adjacent metal layers for ground (2 and 5) and the most internal layers (3 and 4) for power supplies, the resultant *stack-up* is as showed in Figure 22b.

The circuit was carefully laid out in order to minimize the jitter effect. The distance between signal tracks, pads and metal layers was carefully chosen in order to reduce crosstalk and inter-symbol interference, which cause jitter. Other rules followed to reduce jitter were a correct decoupling from the power lines and the so called picket fences technique, consisting in placing closely spaced vias between different ground planes. A distance between vias equal to 1/20 wavelength was selected.

Finally, this board achieves (for a 20 MHz signal bandwidth) an experimental ENOB of 8.5 bits for a programmable carrier frequency ranging from 0 up to 3.3 GHz. An example of the output spectrum is illustrated in Figure 23a:

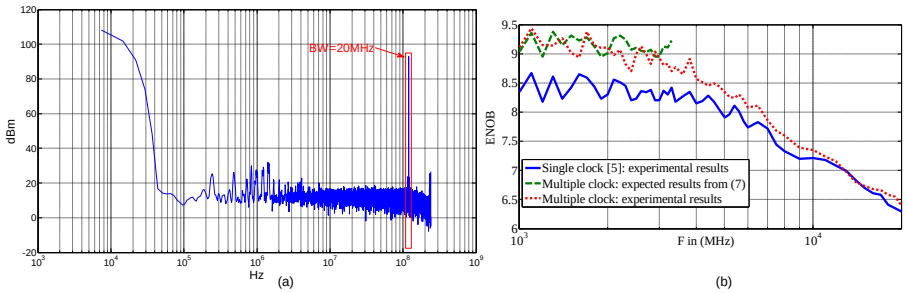


Figure 23. (a) Output spectrum for an input signal at 3 GHz sampled at 480.2 MHz and (b) ENOB vs. Carrier Frequency (20 MHz signal band)

In order to reduce the folded thermal noise effect, a new approach using two consecutives subsampling stages was implemented in [8]. The use of two subsampling processes allows the sampling frequency of the first stage to be increased, resulting in a lower contribution of the first S&H to the folded thermal noise.

In this work, the sampling frequency of the first S&H is selected between 1.2 GHz and 2 GHz, obtaining a band-limited signal at the output. After filtering, the resulting signal is subsampled again

by a second S&H at 400-500 MHz (Figure 11b). However, some drawbacks of the proposed system are a higher complexity and higher power consumption than the one stage subsampling data acquisition system.

Figure 23b [8] shows the ENOB as a function of the carrier frequency up to 20 GHz, for a signal bandwidth equal to 20 MHz. The solid line shows previous results obtained in [7]. The dashed line shows the expected ENOB calculated with (31), which is met while jitter is not the dominant effect. Finally, the dotted line shows the experimental results obtained with in [8].

These experimental results show how the proposed system reduces the effect of the folded noise, increasing the ENOB by 0.5-1 bits in the band of interest. Therefore, it provides an ENOB larger than 9 bits up to 2.9 GHz, 8 bits up to 6.5 GHz, 7 bits up to 12 GHz, and 6.4 bits up to 20 GHz. Concerning linearity and power consumption the results are similar to those obtained in the previous work [7].

5.2. Comparison with other implemented multi-standards receivers

Since it has been described in the last section, [7] might be an approach to the idea of universal receiver for SDR applications. Other works have been published, which can be considered multi-standard receivers. However, some of these works are based on mixing techniques, losing part of the flexibility and simplicity provided by the subsampling based systems. On the other hand, also there are multi-standard receivers which, although they are based on subsampling, are optimized for a given number of wireless standards, without covering all the applications.

Therefore, there are two main research fields about multi-standard receivers, one of them about the digitalization technique (i.e., mixing or subsampling based systems), and the other one about the band strategy (i.e., wideband or narrow band strategy).

Examples in both directions are present in the literature. [1] are examples of works which employ wideband strategies. Reference [5] presents a receiver front-end for multi-standard wireless applications which is composed by a wideband amplifier, source followers, passive mixers and transimpedance amplifiers, its analog bandwidth being up to 3.5 GHz. Reference [1] presented a wideband-multistandard, composed of a wideband LNA, a highly linear downconverter and a programmable digital baseband that performs decimation and filtering. This work can be considered as an universal receiver, covering input frequencies between 0.8 and 6 GHz and being based in mixing techniques. Although, [1] is a more complex solution than [8], this work has a larger tuning range and other benefits as a high linearity and low power consumption, because of its implementation in IC (Integrated Circuit). As a main inconvenience, since [1] are wideband solutions, the RF front-end must meet the requirements for each standard and they are not optimum for any standard.

About the narrow-band strategy, [2] proposes an alternative multi-standard receiver solution separating into two different RF channels, one for the 2.4GHz and 5GHz WLANs and the other for the GSMs. The different channels share a common programmable baseband, this solution being highly efficient, because every path is optimized to a specific standard. On the hand, the main drawback of this work is, besides the limitation of the number of standards, the area consumption, due to the high selectivity is achieved by means of many inductors

An example of a solution based on narrow-band strategies is showed in Figure 24a [3]. In this receiver, dedicated Bluetooth and GPS links allow connectivity while making a phone call or/and

sending or receiving data through a WLAN. The WLAN path connects to IEEE802.11a/b/g/n routers, while the cellular-dedicated channel can switch from one of the GSM bands to the UMTS/WCDMA. Moreover, the selection is provided by off chip SAW filters, which relax the linearity requirements.

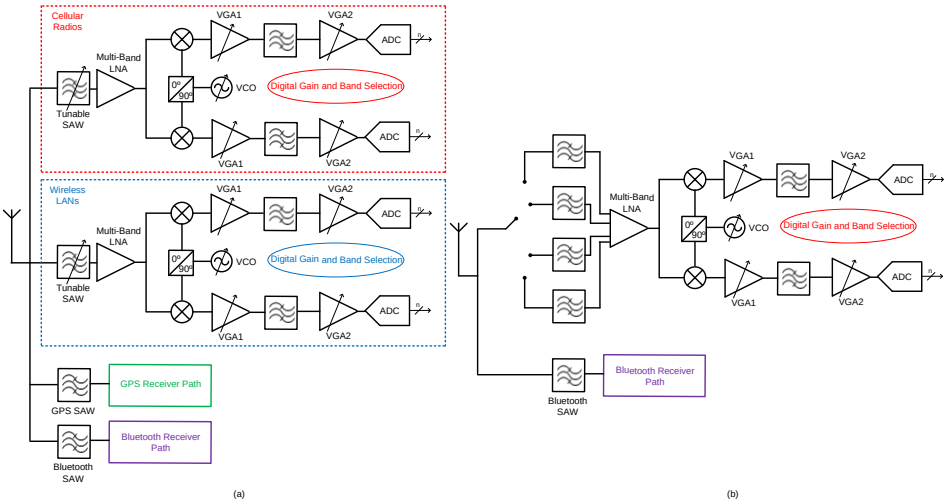


Figure 24. Multi-standard receiver architecture proposed in [3] (a) and [4] (b)

Other works provide a high level of hardware sharing, as [4], where the different specific standards employ a common acquisition and digitalization stages. This work proposes a solution for Bluetooth, GSM, UMTS and WLAN, where the last three standards share the same circuitry after the filter bank (Figure 24b), allowing reuse some building blocks in the receiver architecture.

This hardware sharing maximization means a minimum area consumption, being possible thank to all the considered standards, except Bluetooth, do not need to be covered at the same time, i.e., when an application is active, the others can be switched off in order to save power.

Data acquisition systems for different communications standards use subsampling techniques in order to process high frequency signals with only a few components. Reference [6] proposed a subsampling receiver for three different standards (GSM, UMTS and IEEE 802.11g), which validates these topologies at a simulation level in order to be applied for multi-standard radio design. An additional goal of this work is the design of the RF and IF filters for the different standards, in order to avoid the aliasing caused by the subsampling process. Moreover, the constraints for the IF filter, whose band is fixed, will be relaxed thanks to a subsampling process in the first stage.

In other published works, the receivers based on subsampling are implemented experimentally only for fixed bands. Thus, [30] proposes a low noise subsampling implementation for the 2.1 GHz band, and [31] for 2.4 GHz (IEEE 802.11a/g WLAN standards). In [30] an IC receiver designed in 0.18 µm CMOS, whose main goal is a tunable LC filter implementation, is proposed. [31] shows a 0.18 µm CMOS receiver which represents the most complete subsampling receiver reference, thank to the optimization performed for parameters as thermal noise level, jitter-induced noise and nonlinearity. Finally, there are also receivers based on subsampling for UWB applications, like the one in [32], which operates in the 3.1-10.6 GHz band with low power consumption.

Finally, Table 3 [8] shows the specifications for most of common wireless communication standards [2] and the results obtained in some of these previously published works about the noise performance. These results compared with the obtained in [8] in order to observe the benefits of implement a multiple clock technique for multi-standard receivers based on subsampling. It can be seen that, employing the data acquisition system designed in [8], only the ENOB specifications for IEEE 802.11a are not achieved, although they are very close. Moreover, note that some specifications, like Noise Figure (NF) for UMTS (I) and 802.11b/g, or resolution for Bluetooth, were not achieved without the improvement proposed in [8], i.e., when a unique clock source is used [7]. Comparing with the other published work, similar results about NF and Noise PSD can be observed with respect to [8], showing a larger influence of the jitter (i.e., reducing the resolution with the input frequency) in the work presented in [8].

	Standard	GSM 1800	UMTS (I)	Blue-tooth	802.11b/g	802.11a
Standard requirements	Carrier Freq. (MHz)	1805.2-1879.8	2110-2170	2400	2400	5000
	Signal Bandwidth (MHz)	0.2	5	1	20	20
	ENOB (bits)	9	6	11	8	9
	NF (dB)	9.3	4.6	10.7	6.5	18.2
Experimental results of previously published acquisition systems	ENOB [7] (bits)	11.76	9.56	10.36	8.2	7.41
	NF [7] (dB)	6.1	6.5	8.3	8.3	13.1
	NF [2] (dB)	5.2	5.6		5.8	
	NF [5] (dB)	5.8	6	6.5	6.5	
	NF [6] (dB)		7.5		7.2	
	Noise PSD [31] (dBm/Hz)				-131	
Experimental results of [8]	ENOB (bits)	12.47	9.97	10.86	8.7	8.34
	NF (dB)	3.6	4.4	6.2	6.2	9.3
	Noise PSD (dBm/Hz)	-129.7	-128.8	-126.9	-126.9	-123.8

Table 3. Standard specifications and results

6. Conclusions

In this chapter, a brief review of sampling theory and the advantages of the subsampling techniques in wireless communication transceivers context have been presented. In particular, the usefulness and potential of subsampling technique to design a simple and flexible universal receiver is discussed. A data acquisition module for testing wireless receivers based on subsampling has been presented which covers most present wireless communication standards requirements with only one single board. The main benefits have been presented and a novel method based on multiple clocking techniques to reduce the folded noise effect has been proposed, obtaining an analytical expression for the improvement factor in the SNR with respect to the single-clock solution. The presented board shows (for a 20 MHz signal bandwidth) an experimental ENOB larger than 8 bits up to 4 GHz, while for the selected frequency plan with two successive subsampling processes shows the ENOB improved by in approximately 1 bit. Measurement results show that the design covers the most important wireless standards (i.e., GPS, GSM, GPRS, UMTS, Bluetooth, Wi-Fi, WiMAX) in terms of tuning frequency, linearity and noise. Another characteristic of the implemented module is its simplicity, with only a few components on a printed-circuit board. These results show that, for testing purposes, the subsampling based receiver is a viable alternative to other typical frequency mixing based receiver architectures, with enhanced reconfigurability and programmability.

Moreover, the subsampling concepts have been extended for multi-band and nonlinear systems, where there is an additional problem about the harmonics and different channel which might be folded in the band of interest. In this chapter the challenges and issues on finding the valid subsampling frequencies in multi-band and nonlinear systems are discussed. For this scenario, the noise performance of a dual-band multi-standard receiver has been optimized proposing different architectures based on multiple clocking techniques. Finally, two different applications (spectrum sensing in cognitive radios and a subsampling feedback loop for concurrent dual-band power amplifier linearization) are proposed and characterized experimentally in order to demonstrate the functionality and capability of subsampling techniques for multi-band and nonlinear environments, reducing the cost and the complexity of the receiver architectures.

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8. Authors’ Information

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This chapter explores two of the most promising methods to implement analog-to-digital systems for high data acquisition rate: subsampling and interleaving techniques. These methods are becoming an efficient alternative to conventional receivers as it will be shown in this chapter. Both methods will be explained theoretically, with particular emphasis on its objectives, advantages and disadvantages. The chapter continues with a comprehensive study of the most important works published in both of these fields. A special attention will be paid to the interleaving technique because it is not limited to band-pass signal. Additionally, it is possible to achieve a higher data acquisition rate employing interleaving techniques. Therefore, a more extended comparison will be developed for this method, dedicating a section to describe the main calibration techniques to reduce the harmonics generated by the mismatch errors between analog-to-digital converters (ADCs), which are the main limitation of these systems.

Analog-to-Digital Conversion Systems for High Data Acquisition Rate

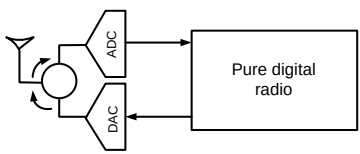
José R. García Oya, Fernando Muñoz Chavero, Rubén Martín Clemente, Fernando Márquez Lasso, Enrique López Morillo, Antonio Torralba Silgado

INTRODUCTION

In general, the analog circuitry determines the sensitivity and selectivity of a data acquisition system. And particularly, the analog-to-digital conversion part is becoming an extremely important block of the receiver architecture, because the location of the ADC into the structure defines which functions are implemented with analog circuitry and what functionality is done by means of digital signal processing. Nowadays there is a trend based on increasing the resolution and speed of the ADC so that it is possible to place it closer to the antenna. Thus the analog front-end is greatly simplified and the flexibility of the receiver is improved, approaching to the Software Defined Radio (SDR) paradigm (Mitola, 1995; Harris and Lowdermilk, 2010; Jondral, 2005), where all the analog functionalities (e.g. mixers, filters, amplifiers, modulators and demodulators) are performed in the digital domain with a higher flexibility and scalability.

The classic SDR transceiver defined by Mitola (1995) is illustrated by Fig.1. As it can be observed, this transceiver is only composed by the antenna, the circuitry dedicated to the conversion between the analog and digital domains (the ADC at the receiver and the DAC at the transmitter) and, finally, a completely digital radio.

Fig.1. Classic SDR architecture.



Recent research is focused on Cognitive Radio (CR), whose target is achieving a kind of flexible intelligence to employ in future radios, cell phones and other wireless communication devices (Jondral, 2005). This coming technology should enable any wireless system to locate and link with any locally available unused radio spectrum. This approach should supply to the consumer, in presence of limited spectral resources, an increase of the number of provided services from a single handset adapted to a global roaming.

However, today it is not possible to design a SDR or CR receiver due to the ADCs limitations. These performance limitations have been explored in many works (Bagheri et al., 2006; El-Sankary and Sawan, 2004; Vun and Premkumar, 2005; Dawoud and Phakathi, 2004) and are particularly influential over the final specifications when implementing SDRs for ultrawideband (UWB) communication systems (Anderson et al., 2009; Romdhane and Loumeau, 2004). In this case, the extremely high sampling rates that are required lead to large amounts of sampled data and large digital processing power.

The analog-to-digital conversion techniques explored in this chapter will be focused in maximizing the data acquisition rates for wireless communications systems. The chapter discusses how the methods based on subsampling and interleaving are feasible solutions for SDR applications in order to meet the stringent requirements about speed and resolution, and provide viable alternatives to the typical receiver architectures based on direct conversion (Abidi, 1995) or low intermediate frequency (IF) (Crols and Steyaert, 1998).

Also, the main benefits and inconveniences of these techniques will be described in the theoretical study section, which is focused on discussing the basic idea and the main non-idealities of subsampling (Grace and Pitt, 1968; Vaughan et al., 1991; Lyons 2001; Sun, 2006; Karvonen 2006) and interleaving techniques (Looney 2003; Jenq 1988; Kurosawa et al., 2001; Petraglia and Miltra, 1991). It will be explored that sampling the input signal below Nyquist rate (subsampling case), a simple scheme with a few components and a wide analog bandwidth can be implemented, whereas by connecting several Analog-to-Digital Converters (ADCs) in parallel (interleaving case) the total data acquisition rate is maximized. Otherwise, the main non-idealities will be the jitter and the folded thermal noise for the subsampling case and the mismatches errors between the different ADCs for the interleaving case.

After this description, the following section details a comparison between the most relevant published works that use subsampling (Oya et al., 2011; Barrak et al., 2009; Pekau and Haslett, 2007; Jakonis et al., 2005; Vanderperren et al., 2006) and interleaving techniques (Anderson et al., 2009; Papari et al., 2011, Doris et al., 2011; El-Chammas and Murmann, 2011; Nazami et al., 2008; Huang et al., 2011). The main benefit of the works based on subsampling will be the high resolution for a wide range of input frequencies, providing a viable choice to implement SDR and multi-standard systems. On the other hand, the main advantage of the published works based on interleaving is the maximization of the data acquisition rate, which is crucial for SDR applications as well,

being the main objective in this chapter. Therefore, and due to the fact that interleaving systems are not limited to band-pass signals, the implemented systems based on these techniques are described in more detail. Thus, this comparison will be introduced by a description of the main calibration techniques, detailing their advantages and inconveniences, in order to compare the published works about their correction methods as well.

THEORETICAL STUDY

As it was introduced before, this chapter explores the possibility of using subsampling and interleaving ADCs to implement SDR receivers. In the next sub-sections the theoretical concepts and the main non-idealities of the techniques based on subsampling and interleaving will be detailed.

Subsampling Techniques

This section begins with the description of the subsampling idea and the optimal sampling frequency selection. A second part will be dedicated to explain the effects of the main non idealities, i.e., jitter and folded thermal noise.

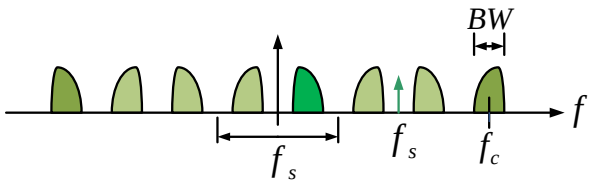
Concept of Subsampling and Optimal Frequency Selection

In this section, a study of how to calculate the optimal subsampling frequency is explored, taking into account the signal bandwidth (*BW*) and the carrier frequency (f_c), in order to avoid aliasing and maintain the spectrum between $-f_s/2$ and $f_s/2$ and the others replicas as far as possible from the desired signal (Grace and Pitt, 1968; Vaughan et al., 1991; Lyons 2001; Sun, 2006; Karvonen 2006).

Hereafter, the following notations will be used (see Fig.2):

- f_s: subsampling frequency
- *BW*: signal bandwidth
- f_c: carrier frequency
- *B*: $f_c + BW/2$

Fig.2. Subsampling concept (m=3).



The minimal sampling frequency is established by the Nyquist Theorem, $f_s>2B$. However, if we are processing band-pass signals, aliasing can be avoided with a lower *fs* when Eq. 1 is satisfied (Vaughan et al., 1991):

$$\frac{2f_c - BW}{m-1} > f_s > \frac{2f_c + BW}{m} \quad (1)$$

where *m* is an integer number representing the number of replicas of the original signal that appears in the range [0, f_c-*BW*/2]. The maximum number of copies needed to avoid aliasing is calculated by the expression Eq. 2 (Vaughan et al., 1991):

$$m_{\max} = floor((f_c + BW/2)/BW) \quad (2)$$

where *floor(x)* is the largest integer not greater than *x*. The optimal value in the range given by Eq. 1 is the one that produces a copy on f_s /4. This frequency is given by Eq. 3 (Vaughan et al., 1991):

$$f_s = \frac{4f_c}{m_{odd}} \quad (3)$$

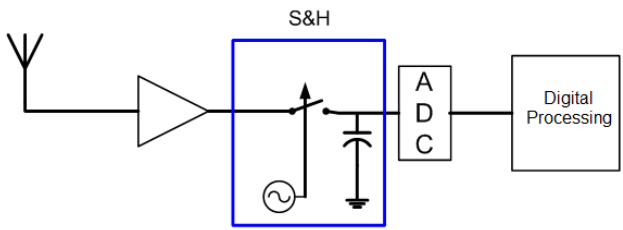
where m_{odd} is an integer odd number greater than 1:

- with m_{odd} = 5,9,13, … there is not spectral inversion
- with m_{odd} = 3,7,11, … there is spectral inversion

Main non idealities

A general scheme of a subsampling based receiver is shown in Fig. 3. Its main advantage is its simplicity, removing a large amount of analog components from the traditional heterodyne structure. However, the specifications of the Sample & Hold (S&H) are much more restrictive than in a traditional receiver. This will be the most critical device in the system, as it processes high frequency signals.

Fig. 3. Receiver scheme based on subsampling.



The main non-idealities produced in S&H are the following:

Jitter:

Ideally, the time interval between samples is a constant value equal to $1/f_s$. Nevertheless, these intervals are different due to jitter. This jitter produces an increment of the output total noise, thus limiting the effective number of bits (ENOB).

Jitter is produced by two different sources: the phase noise associated to the oscillator and the aperture jitter of the S&H. At a first approach we can consider these two sources of jitter as non-correlated Gaussian stochastic processes.

This section shows how jitter affects Signal to Noise Distortion Ratio (SNDR) in the S&H output. The objective is to set the maximum allowed jitter standard deviation depending on the input frequency and the required resolution.

When the input is a sinusoidal signal like $y(t)=A\sin(2\pi f_{in}t)$, SNDR is determined by the Eq. 4 (Sun, 2006):

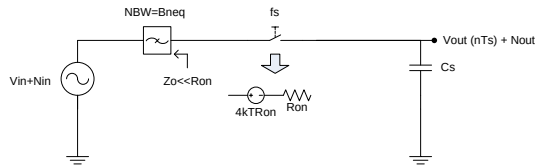
$$SNDR = \frac{\frac{A^2}{2}}{N_\tau} = \begin{cases} \frac{1}{4\pi^2 f_{in}^2 \sigma_\tau^2} : 2\pi f_{in}\sigma_\tau << 1 \\ \frac{1}{2(1-e^{-2\pi^2 f_{in}^2 \sigma_\tau^2})} : other\_case \end{cases} \quad (4)$$

where $\overline{N_\tau}$ is the average power noise and σ_τ is the jitter standard deviation. To deduce the last expression, the spectral density was integrated between 0 and $f_s/2$.

Overlapped Thermal Noise:

A typical S&H produces *kT/C* noise. To simplify the noise analysis we consider a sampling model as the one illustrated in Fig. 4 (Karvonen, 2006). This scheme consists of an input band-pass signal (V_{in}), with an associated noise (N_{in}), which is filtered and later applied to a S&H modeled by a switch and capacitor. Due to the multiple overlapping produced by subsampling, many parts of the signal spectrum will be folded inside of the band of interest.

Fig. 4. Noise analysis scheme.



The switch of the S&H has been modeled with a resistance and a white noise source of power spectral equal to $4kTR_{ON}$. The noise will be filtered by the transfer function (Karvonen, 2006):

$$H(f) = \frac{1}{1 + 2\pi f R_{ON} C_S}$$

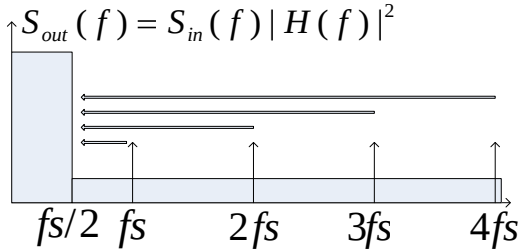
The result is a filtered white noise with a power equal to kT/C_S, whose value is independent of the resistance value and subsampling frequency.

We assume (Karvonen, 2006):

$$f_s << \frac{1}{2\pi R_{ON} C_S}$$

Then, due to the subsampling process, we can approximate that all noise power will be folded between 0 and $f_s/2$, as illustrated in Fig. 5.

Fig. 5. Folded thermal noise effect.



Although the total noise power is not dependent on subsampling frequency, the noise floor is reduced if this sampling frequency grows. In particular, noise floor is reduced 3 dB if subsampling frequency is doubled. Thus, it is convenient to choose the sampling frequency as large as possible to distribute noise floor throughout the entire Nyquist band.

Other considerations regarding the S&H:

- Its bandwidth should be maximized in order to not filter out the GHz signals.
- Although it has a high bandwidth, the S&H should be able to sample frequencies close to MHz, due to these values are the maximum sample frequencies for high-resolution commercial ADCs and low-power Digital Signal Processors.
- Its output ENOB can be limited by linearity, so we should study its THD and SFDR.

Interleaving Techniques

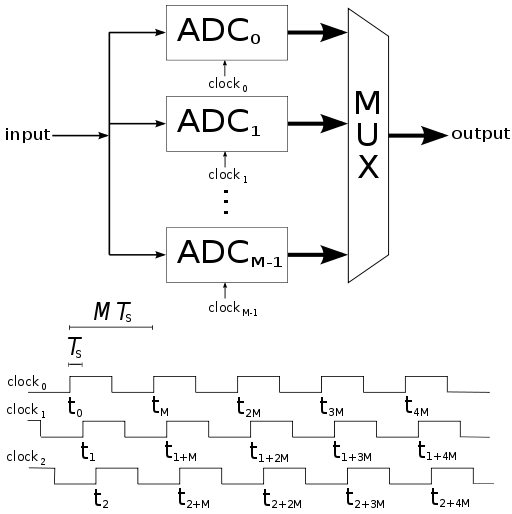
Time-interleaved ADCs are an effective approach for achieving very high sampling rates (Looney, 2003). A time-interleaved ADC operates M parallel ADCs at different sampling times, creating the image of a single ADC operating at a much higher sampling rate. The concept is illustrated in Fig. 6. Ideally, the *ith* ADC, $i = 0, ..., M - 1$, samples periodically the input signal at time instants

$$t_i, t_{i+M}, t_{i+2M}$$

with sample rate f_s/M, where $t_m=mT_s$ and $T_s=1/f_s$ is the sampling period of the time-interleaved ADC. The final output is created by multiplexing all of the individual ADC outputs in the proper order (e.g. ADC_0, ADC_1, …, ADC_{M-1}, ADC_0, ADC_1, etc.).

Thereby, the final effect is as if the input signal were sampled once every T_s seconds, i.e., with sample rate f_s. This approach has been widely adopted in the industry, since the converters can be working at lower speeds without sacrificing the overall system performance. However, it should be noted that each individual ADC deals with the entire analog input signal, and, therefore, its S&H circuit must be able to preserve the full input signal bandwidth.

Fig.6. Architecture of a time-interleaved ADC.



Analysis of time-interleaved ADCs.

Let $x(t)$ be an analog signal with Fourier transform $X_a(\omega)$. Consider that the time-interleaved ADC outputs the sequence:

$$x(t_0), x(t_1), x(t_2), \ldots, x(t_m), \ldots, x(t_M), x(t_{M+1}), \ldots$$

Define the discrete-time Fourier transform by[1]:

$$X(\omega) = \Sigma x(t_k) \exp(-j\omega t_k)$$

Ideally, the samples are spaced T_s seconds apart. Then, it can be shown that:

$$X(\omega) = f_s \Sigma X_a(\omega - k2\pi f_s) \tag{5}$$

which is the well-known spectrum representation of a uniformly sampled signal. It results in a periodic spectrum with a period equal to the sampling rate (Jenq, 1988).

In practice, however, there are deviations from the ideal behavior that are caused by the mismatches between the individual ADCs. There are three main possible sources of error in time-interleaved ADCs: *clock timing errors*, *gain errors* and *offset errors* (Kurosawa et al., 2001). A brief review of each of them is included in the next sections:

Clock Timing errors:

Clock timing errors occur when the digitization clocks of the individual ADCs are not appropriately synchronized. As a result, the input signal *x(t)* is sampled in such a way that the sampling time instances are not necessarily uniformly spaced in time. Errors may be systematic (skew) or random (jitter). Taking this factor into account, Eq. 5 becomes (Jenq, 1988):

$$X(\omega) = f_s \Sigma H_k(\omega) X_a(\omega - k2\pi f_s / M) \tag{6}$$

where:

$$H_k(\omega) = (1/M)\Sigma \exp(-j[\omega - k(2\pi / MT_s)]r_m T_s) \exp(-jkm(2\pi / M))$$

where $r_m=(t_m-mT_s)/T_s$ is a ratio that measures the timing errors (ideally, $t_m=mT_s$).

1 In the literature, it is a common notational practice to replace ωt_k with a single variable $\omega' = \omega t_k$, called *normalized frequency*. Since ω represents ordinary frequency (radians per second), ω' is expressed in units of radians (per sample). Recall also that by sampling the discrete-time Fourier transform, we obtain the discrete Fourier transform (DFT).

It can be noticed that, in contrast with the ideal case, the spectrum is repeated in Eq. 6 every integer multiple of the frequency f_s/M (not f_s). In other words, spurious replica spectra (called *image spurs*) will appear at

$$f_{imagspurs} = \pm f_i + k\frac{f_s}{M}, \quad k = \pm 1, \pm 2, \pm 3, \ldots$$

These replicas hamper the interpretation of the spectrum of the input signal, as they may be confounded with true signal's frequency components. In addition, even if the image spurs are eliminated, we find that the spectrum of the signal reconstructed from the given samples is equal to $H_0(\omega)X_a(\omega)$. This is equivalent to passing the original input signal through a filter of transfer function $H_0(\omega)$, which introduces distortion and should be corrected by an equalizer.

Assuming that the input signal is a pure tone of frequency f_i, and that f_i is a Gaussian variable with zero-mean and variance σ^2 for all m, the signal-to-noise and distortion ratio (SDNR) is approximately found to be (Jenq, 1988):

$$SDNR = 20\log\left(\frac{f_s}{2\pi f_i}\right) - 10\log\left(1 - \frac{1}{M}\right) \tag{7}$$

Gain errors:

The gains of each ADC may be different. As a result, for a dc input (to cite just a simple example) each ADC may produce different output code. The analysis is similar as for timing errors. Gain errors also produce image spurs at:

$$f_{imagspurs} = \pm f_i + k\frac{f_s}{M}, \quad k = \pm 1, \pm 2, \pm 3, \ldots$$

where f_i is the input frequency. A formula for the SDNR, taking into account the contribution of gain and offset errors, will be given a few lines below.

Offset errors:

The offsets of each ADC may be also different. As with the gain mismatch case, a dc input may also produce different outputs. Offset errors cause noise peaks (*offset spurs*) at:

$$f_{off\,spurs} = k\frac{f_s}{M}, \qquad k = 0, 1, 2, 3, \ldots$$

Assuming that the gain and offset errors are Gaussian distributed, with respective variances σ^2_g and f_i, and that the input signal is a sinusoid with amplitude A, the SDNR equals to (Petraglia and Mitra, 1991):

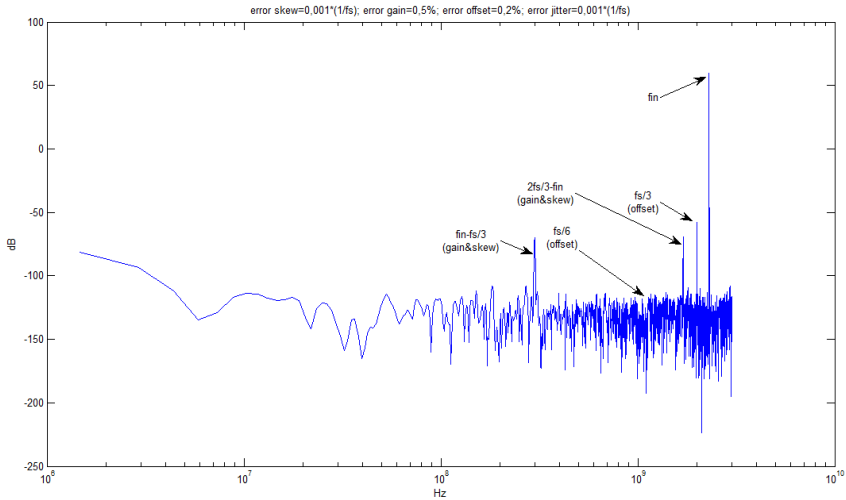
$$SDNR = 10\log\left(\frac{A^2}{A^2\sigma_a^2 + 2\sigma_b^2}\right)$$

which is independent of the number of the degree of interleaving M.

The image and offset spurs are illustrated by the example shown in Fig. 7. The input signal is a sinusoid at frequency 2.3 GHz that is sampled at f_s= 6 GHz and the time-interleaved ADC has three channels (i.e., three individual ADCs in parallel).

In practice, clock timing errors are the most critical (gains and offsets can be calibrated more easily). Several approaches have been proposed to deal with mismatches between individual ADCs. Some of the most relevant will be presented in the next Section.

Fig. 7. Output spectrum of a three channel interleaved ADC.



IMPLEMENTED SYSTEMS

Once the basic concepts and main non-idealities have been studied, the most relevant published works about subsampling and interleaving techniques will be introduced and compared in the next two sub-sections.

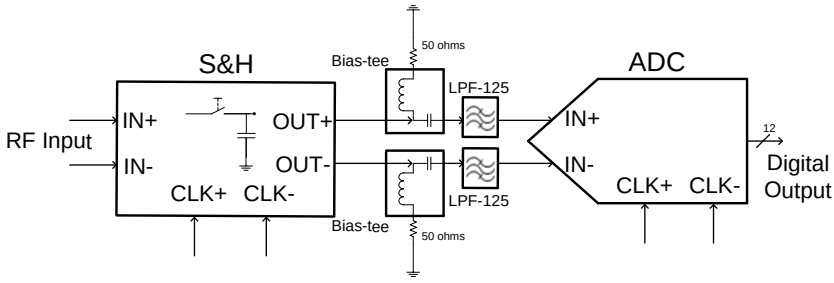
Systems based on subsampling

An important objective of subsampling based systems is its applicability to multi-standard receivers. A relevant data acquisition system based on subsampling for multi-standard applications is presented in (Oya et al., 2011). Using commercial devices on a multilayer printed circuit board (PCB), this work achieves around 8.5 bits up to 3.3 GHz input frequency using a signal bandwidth equal to 20 MHz.

In this work, the main components (i.e., S&H and ADC) were selected in order to minimize the effects of the previously studied non-idealities. The main specification to be met by the S&H is the aperture jitter. In this case, the Inphi 1821 TH (Inphi, 2007) has been chosen due to its minimal aperture jitter (50 fs). Moreover, this device has a large analog bandwidth (18 GHz) and high linearity, which allows the system to fulfill most of existing wireless communication standards. Finally, this S&H is capable to sample at intermediate frequencies (i.e., around 500 MS/s), which are the maximum sampling rates available for 10-bit linearity ADCs. The selected ADC was the E2V AT84AS001 (E2V, 2007), because of its resolution (12 bits) and sampling frequency (500MHz).

Besides to the S&H and the ADC, other discrete components are employed in the designed multi-layer prototype PCB, such as wideband bias tee and LP passive filters in order to remove the harmonics and signal replicas generated by subsampling process. The basic scheme of the circuit presented in (Oya et al., 2011) is shown in Fig. 8, where the simplicity of the subsampling based receiver can be noticed.

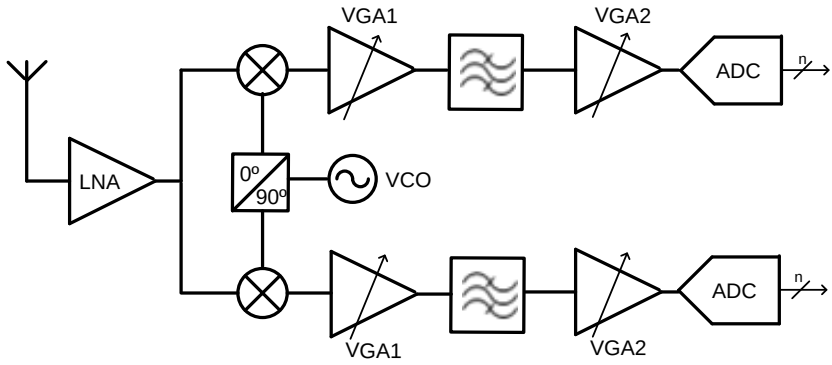
Fig.8. Architecture based on subsampling implemented in (Oya et al., 2011).



Consequently, in (Oya et al., 2011) an approach to the idea of universal receiver for SDR applications is provided, covering the most important wireless standards (i.e., GPS, GSM, GPRS, Bluetooth, Wi-Fi, WiMAX). Another important universal receiver is the work proposed in (Bagheri et al., 2006), which covers input frequencies between 0.8 and 6 GHz. This receiver is based in mixing and, therefore, leads to a more complex architecture than the subsampling based scheme. However, (Bagheri et al., 2006) has a larger tuning range and other benefits as a high linearity and low power consumption, because of its implementation in IC (Integrated Circuit).

In fact, most of multi-standard receivers (Agnelli et al., 2006; Svelto et al., 2008; Brandolini et al., 2005) are based on mixing, being proposed only for specific standards. The receiver in (Agnelli et al., 2006) is used for DCS1800, UMTS and 802.11b-g applications, the one in (Svelto et al., 2008) for different cellular or WLAN standards, and the one in (Brandolini et al., 2005) for GSM, UMTS, Bluetooth and WLAN. Fig. 9 shows a mixing based scheme, where the increase in complexity is illustrated.

Fig.9. Receiver mixing based architecture.



Other analog-to-digital conversion systems for different communications standards use subsampling techniques in order to process high frequency signals with only a few components. For instance, Barrak et al. (2009) propose a subsampling system for three different standards (GSM, UMTS and IEEE 802.11g), which validates, at simulation level, these topologies and design methodologies in order to be applied in the context of multi-standard radio design. An additional goal of this work is the design of the RF and IF filters for the different standards, in order to avoid the aliasing caused by the subsampling process.

In other published works, the subsampling capabilities are validated and implemented experimentally only for fixed bands. For instance, Pekau and Haslett (2007) propose a low noise subsampling implementation for the 2.1 GHz band, and (Jakonis et al., 2005) for 2.4 GHz (IEEE 802.11a/g WLAN standards). In (Pekau and Haslett, 2007) an IC receiver designed in 0.18 µm CMOS, whose main goal is a tunable LC filter implementation, is proposed. Otherwise, Jakonis et al. (2005) show a 0.18 µm CMOS receiver which represents the most complete subsampling receiver reference, thank to the optimization performed for parameters as thermal noise level, jitter-induced noise and nonlinearity. An additional improvement presented by this work is the optimization of the clock path necessary to distribute the Local Oscillator (LO) signal.

Finally, there are also receivers based on subsampling designed for UWB applications, like the one in (Vanderperren et al., 2006), which operates in the 3.1-10.6 GHz band with low power consumption. In this chapter it is showed that interleaving techniques are the most widely accepted option for UWB applications (Anderson et al., 2009; Romdhane

and Loumeau, 2004). However, by means of using subsampling techniques, as in (Vanderperren et al., 2006), it is possible to cover a higher analog bandwidth.

Systems based on interleaving

To implement interleaving systems several approaches, which differ in the calibration method and in the intended application, are possible. Calibration techniques are one of the main trends of the present research, and this section begins with a brief summary of the most prevalent methods, discussing their advantages and disadvantages. Then, a review of several approaches for designing SDR, UWB and Multi-Standard systems will be presented.

Calibration techniques:

The mismatch errors described in the last section need to be corrected in order to maximize the benefits of interleaving systems and increase the ADC resolution, avoiding the degradation of the SFDR and the SNDR of the analog-to-digital system.

In (Anderson et al., 2006), where an ADC system for UWB is described, two basic (non-exclusive) options to calibrate the system are presented: 1) controlling the ADC mismatches in the integrated circuit fabrication process, and 2) using digital pre-processing or post-processing techniques to mitigate the impact of image and offset spurs.

The first one consists of reducing the electrical and physical differences between the channels. The gain is typically controlled using a common reference voltage and carefully designing the layouts. Phase matching is achieved by ensuring that all the clock paths are as similar in length as possible. Nevertheless, unlike approaches based on digital processing, these techniques are not well-suited for implementations based on COTS (Commercial Off The Shelf), which is very convenient for SDR designs due to its flexibility and ease of programming.

Digital processing techniques have several advantages, including a low power consumption and the possibility of being implemented through a cheap CMOS process. Moreover, digital techniques are more efficient for the compensation of timing skews than analog techniques, due to the fact that they are more stable with the temperature and the wide bandwidths used in SDR applications. Digital processing techniques are also easier to implement, can be designed with more precision and take advantage of the last advances in high-speed and configurable digital hardware platforms (DSPs, FPGAs, CPLDs, ASICs) (Looney, 2003).

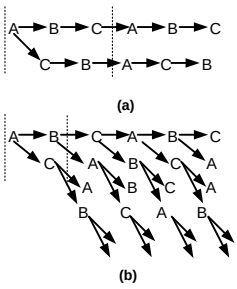
In spite of the previously stated digital processing advantages, analog calibration techniques have benefits as well. For example, one advantage of analog offset calibration is that the correction values do not suffer from quantization (Haykin, 1986). Thus, the ADC offset can be corrected to less than one LSB without adding the extra bits needed

when the offset correction is performed in the digital domain (Fu et al., 1998). Furthermore, analog gain correction can be implemented by simply adjusting the reference voltage (so that using high-speed multi-bit digital multipliers to scale the ADC outputs becomes unnecessary).

Calibration techniques can be also classified into “background” and “foreground” techniques (El-Sankary and Sawan, 2004; Doris et al., 2011; Dyer et al., 1998). Sometimes they are also named as, respectively, “online” and “offline” calibration (Parkey et al., 2011). Offline calibration requires less circuitry, but interrupts the normal operation of the ADC. It is usually applied when the parameters of the circuit do not vary much with environmental parameters (e.g. voltage or temperature) (Poulton et al., 2003). On the other hand, background techniques enable continuous calibration, with the ADC running in normal operation, and are suitable to be used when disconnecting the ADC is not an option (El-Chammas and Murmann, 2011).

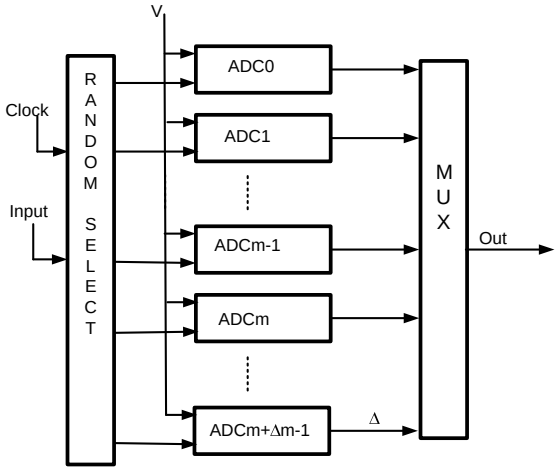
A particularly appealing background approach is the one based on randomization (El-Sankary and Sawan, 2004). In this approach, the ADC channel is selected randomly for each sampling instant. This can be performed using a digital circuit (thus avoiding the need for new analog circuitry), which constitutes the main benefit of this approach. Considering $M + X$ individual ADCs, we can choose at each time instant among $X + 1$ channels without violating the sampling rate of each individual ADC. This is illustrated in Figs. 10a and 10b. In Figure 10a (Tamba et al., 2001), a 3-ADCs system is presented with M = 3 and X = 0: noting that each ADC samples every 3 T_s seconds, where T_s is the sampling period of the total system, the only possible outputs are A B C A B C A B C ... or A C B A C B A C B ... For example, considering the first case, after the three channels (A, B, C) have taken a sample we can only choose A without violating our sampling constraint. Next, only B can be selected and so on. Therefore, to enable the randomization process one or more extra ADCs (i.e., X > 0) must be employed (Tamba et al., 2001; Elbornsson et al., 2003). In this way, there always exist at least two available ADCs at each sampling time. This case is illustrated with Fig. 10b, which considers the case M = 2 and X = 1: after the first two channels have been selected, for example, A and B, we can decide between A and C and so forth.

Fig. 10. (a) Three ADCs (ABC) for three times sampling rate, (b) Three ADCs (ABC) for a double sampling rate



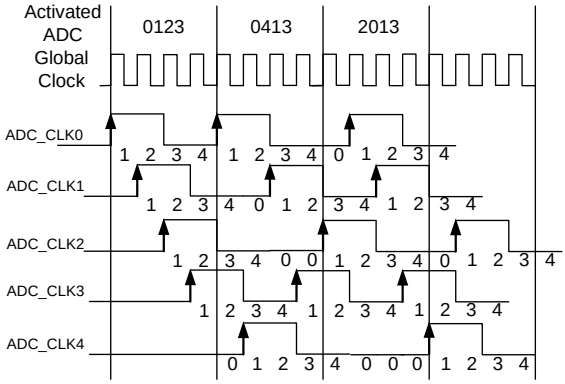
An example of this architecture is illustrated in Fig. 11, where ΔM extra ADCs have been added.

Fig. 11. Example of a structure with extra ADCs.



Although this structure implies an additional hardware cost, Tamba et al. (2001) demonstrate that as X tends to zero (in order to reduce the cost), noise becomes non-white (it is not flat). Therefore, it is necessary a trade-off between the value of X and the cost of having non-activated ADCs (note that it is not convenient to have largely underutilized ADCs, which occurs when X is much larger than M). A clock diagram for M=4 and X=1 is showed in Fig. 12 (Tamba et al., 2001).

Fig. 12. Random clock for 5 ADCs



Apart from the use in randomization techniques, an extra ADC might be employed in other background approaches. Dyer et al. (1998) use an additional ADC to implement an analog background circuit which calibrates the gain and offset mismatch. The basic idea of this technique is to use M+1 ADCs so that M ADCs are always active while the remaining one is being calibrated. When the calibration cycle is finished, another ADC is selected for calibration, being replaced in the conversion mode by the previously calibrated ADC. The calibration of these ADCs is performed using another ADC as a reference, in order to match gain and offset with it. Therefore, an analog calibration is implemented.

Since this method is based on a background process, it is not necessary to stop the analog-to-digital conversion and, in addition, it will be more efficient as the number of ADCs increases. However, the main drawbacks are the noise introduced by the additional analog circuitry, and the degradation in speed when extra ADCs are used to substitute the ADC under calibration (Ingino et al., 1998).

Moreover, there are also calibration techniques specifically devised either for static (i.e., gain and offset) or dynamic errors (i.e., clock skew). For example, an alternative method for calibrating the static mismatches is to employ a DAC (Digital-to-Analog Converter) with enough resolution to meet the requirements (Brown et al., 1996), using one of these DACs for each ADC in the interleaved structure.

A common alternative to reduce the cost of the extra circuitry due to the added DACs is to implement the gain and offset calibration after a FFT (Fast Fourier Transform) evaluation, via software, achieving the compensation from the study of the output spectrum (Pereira et al., 2004). An additional benefit of this technique is to take the advantage of the repetition and symmetry properties of the FFT (Slim and Russer, 2011).

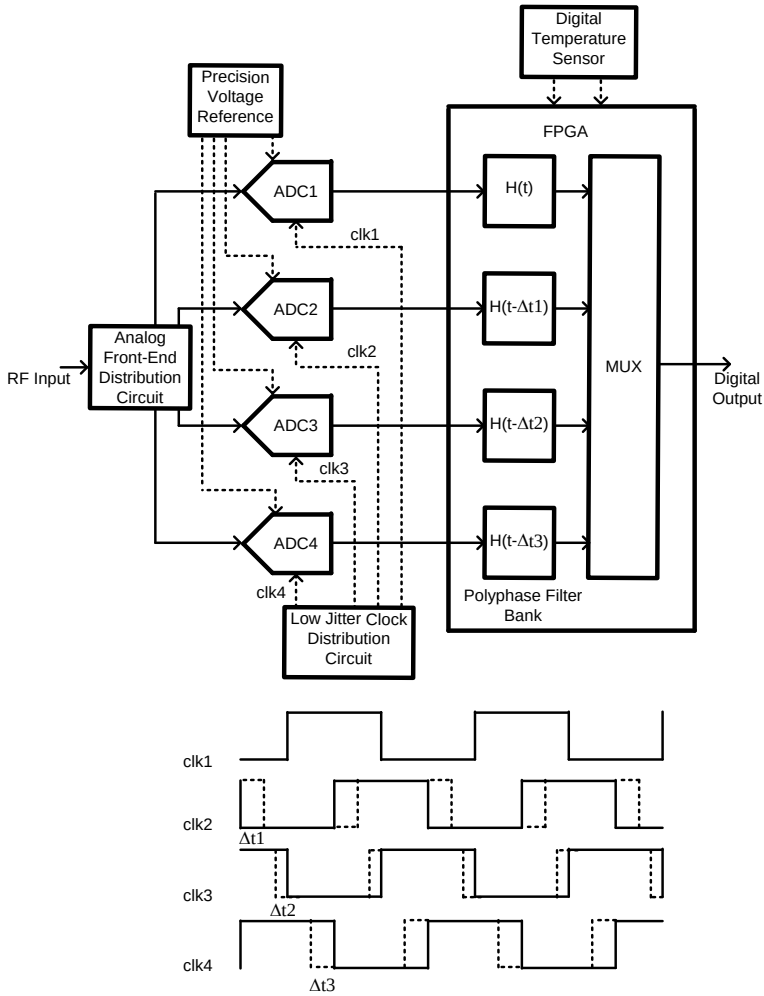
On the other hand, clock skew errors are difficult to correct and lead to more stringent limitations on interleaved architectures (Gupta et al., 2006), especially for UWB applications as explained in (Anderson et al., 2009). Unlike static errors, dynamic errors depend on the input frequency and can be theoretically characterized from the aperture jitter and aperture delay of the internal S&H of each ADC. Although the aperture jitter affects to high frequency systems, its value (less than 1ps) is usually much lower than the delay jitter (a few nanoseconds) and, therefore, it may be ignored in many interleaving based systems. Moreover, the aperture delay strongly depends on the temperature. As a consequence, there are many unknown factors affecting these timing mismatches that make the estimation of the spurious component level even harder.

Some traditional ideas for correcting the skew errors are to add programmable delay lines or to implement a signal post-processing. Tamba et al. (2001) propose this method to reduce the spurious level though additional hardware is required.

Another specific technique for timing errors correction is the one based on polyphase digital filters blocks (Vun and Premkumar, 2005; Lee and An, 2005), which can be easily implemented using a FPGA and, therefore, results highly suitable for SDR applications

based on COTS. An example of the proposed structure is illustrated in Fig. 13, where the FPGA includes, as well as the filter implementation, a precision voltage reference, a low jitter clock distribution circuit and a digital sensor to control the effect of temperature on the skew (Looney, 2003).

Fig. 13. Functional diagram using digital filters blocks.



The filter structures used to calibrate these dynamic errors are designed as a function of the number of channels (i.e., number of ADCs). Lee and An (2005) give the ratio (R) between the number of channels (M) and the number of necessary filters (N), this ratio being lower when the number of channels is increased. For instance, in this work N=3 for

M=2 (R=0.75), N=5 for M=3 (R=0.556) and N=27 for M=8 (R=0.422). As a consequence, for a high number of ADCs this method is not so efficient. Another inconvenient is that this technique is limited to a single frequency input signal, and the filters coefficients would have to be frequently recalculated, thus increasing the calibration process complexity (Abbaszadeh and Dabbagh-Sadeghipour, 2010).

Lastly, an additional drawback of this method is that conventional filters do not have enough resolution to tune the group delay in the highest frequency systems, where the calibration precisely has to be more accurate (Asami et al., 2010). Thus, designing these filters is an important challenge in their own.

Implemented Systems

Many research works have been published in order to implement receivers and analog-to-digital conversion systems based on interleaving techniques, most of them with its application in SDR. Some of these systems are implemented in IC whereas others are implemented with COTS, leading to some benefits in SDR applications like significant time and cost savings comparing with developing an integrated circuit.

The main reference for time interleaved systems design based on COTS is (Anderson et al., 2009). In this system eight ADCs (MAX104, 2002) sampled at 1 GSPS are connected to obtain a total sampling frequency equal to 8 GHz. However, since the digital processing is implemented on a FPGA, the final frequency is equal to 6.4 GHz, due to speed restrictions of the device. Although, this is an inconvenience for high-speed circuits, using a FPGA will provide to the system the necessary flexibility for SDR and UWB applications. Moreover, this solution means a reasonable tradeoff between cost and complexity. The proposed system in (Anderson et al., 2009) employs a digital calibration scheme based on filters, obtaining a SNR around 30-35 dB (i.e., around 5-6 bits) at the maximum operation frequency.

Other novel systems based on interleaving techniques are not implemented by COTS but integrating all the system, including the calibration part (calibration on-chip). This solution it is more convenient for analog or DAC-based calibration, reducing the power consumption. An example is proposed in (Doris et al., 2011). In this work four ADCs are connected to obtain a SNDR around 48 dB for a total sampling frequency of 2.6 GHz.

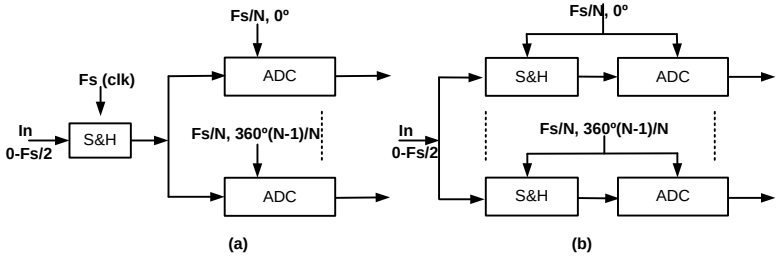
There are other interleaving converters which combine analog and digital calibration. For instance, El-Chammas and Murmann (2011) use DACs to correct offset errors in the analog domain and background digital calibration to reduce the clock skew effects. Using both methods this work implements an 8-ADCs array to obtain a resolution of 5 bits at 12 GS/s operation rate. A similar work is described in (Nazemi et al., 2008), where a resolution of 5.1 bits is obtained with 8 interleaved ADCs operating at 10.3 GS/s.

Finally, there are some interleaved converters that have applied successfully background digital calibration for dynamic and static errors compensation, as (Huang et al., 2011),

which obtains 6 bits at 16 GS/s for 8 different channels and (Papari et al., 2011) that presents an analog-to-digital system for cognitive radio.

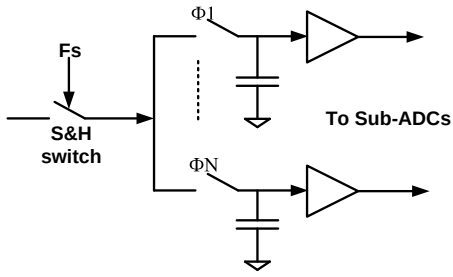
On the other hand, an important issue about the implementation of interleaving converters is the connection between the S&Hs and ADCs. There are two possible structures, which are illustrated in Fig. 14 (Gupta et al., 2006). One of them uses only one S&H connected to several ADCs (Fig. 14a). In this case, the main inconvenience is that the number of ADCs connected to the S&H is limited and, therefore, since this number of ADCs is directly proportional to the total sampling rate, the scalability will be limited as well. When each interleaved ADC is preceded by its own S&H (Fig. 14b) the scalability is theoretically increased because this architecture is not limited by a maximum number of ADCs connected to the S&H. However, the clock skew effect between the different S&Hs will degrade the final SNDR and, therefore, the final number of interleaved ADCs will also be limited in this case, as it is shown in Eq. 7.

Fig. 14. Architectures based on: (a) one S&H and (b) several sub-S&H.



With the objective of reducing the number of S&Hs, Gupta et al. (2006) propose a structure based on double sampling (Fig. 15). Since using this solution the loading of the S&H is not directly depending on the number of interleaved ADCs, the scalability will be increased with respect to the structure shown in Fig. 14a. Moreover, the mismatch problems and the power consumption will be reduced with respect to the structure shown in Fig. 14b.

Fig. 15. Architecture based on double sampling.



CONCLUSIONS

In this chapter, two different alternatives to the typical analog-to-digital conversion structures have been explored in order to avoid the current limitations of the ADCs used for high frequency applications. Techniques based on subsampling and interleaving ADCs have been described, detailing their advantages and drawbacks, considering the implementation of the Software Radio paradigm (with the digitalization just after the antenna).

On the one hand, subsampling techniques are extremely suitable for wideband applications, although they have some cons, such as the jitter and the folded noise, which limit the final resolution. On the other hand, the use of interleaving techniques makes possible to maximize the sampling rate, while the main disadvantage of this method is that calibration is needed to compensate the mismatch between parameters as gain, offset and clock skew.

In the last section, a complete study of the implemented systems with both of these conversion techniques has been made, detailing the features (i.e., the achieved resolution and operation frequency) and the applications (SDR, UWB, multi-standard or instrumentation) of each published work. Moreover, a data acquisition system based on subsampling has been presented and experimentally characterized, obtaining around 8.5 bits of resolution up to 3.3 GHz input frequency using a signal bandwidth equal to 20 MHz.

Finally, since this chapter mainly focuses on the maximization of the data acquisition rate for ADC systems, which is a crucial factor for applications like UWB, special attention was devoted to the different calibration methods, which are essential for the performance of interleaving converters. Thus, with the objective of minimizing the harmonics produced by the mismatches; a comparison of the different techniques (i.e., digital or analog, background or foreground, based on DACs, extra ADCs or randomization) has been made to determine the most appropriate technique for each application in terms of power consumption or digital processing capabilities.

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9.5.3 Conference communications

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High frequency Analog-to-Digital Conversion based on subsampling

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***Abstract*— The focus of this work is the implementation of a Analog-to-Digital Converter System using techniques based on subsampling. Its main objective is to improve the features of a receiver used for wideband communications reducing the number of elements of the system with a higher flexibility and resolution. This proposed system is based on commercial devices, mainly a Low Jitter and Wideband Sample&Hold and a High Resolution Intermediate-frequency Analog-to-Digital Converter.**

***Keywords*— Analog-to-Digital Converter, ENOB, Jitter, Sample&Hold, Software Defined Radio, SNDR, Thermal Noise**

I. INTRODUCTION

In general, the analog building blocks determine the sensitivity and selectivity of a receiver. The Analog-to-Digital Converter (ADC) is becoming an extremely important block of the receiver architecture, because the place of the ADC into the receiver architecture marks which functions are implemented with analog circuitry and what functionality is done in the digital signal processor.

Nowadays there is a trend of increasing the resolution and speed of the ADC of a receiver so that it is possible to place it closer the antenna. Thus the analog front end is greatly simplified and the flexibility of the receiver is improved.

The current state of the art of high-frequency ADCs does not allow the use of the ADC directly in the RF domain to get the paradigm of the Software Defined Radio (SDR). However, many research projects focus on finding new solutions towards the SDR, where all the analog functionalities (e.g. mixers, filters, amplifiers, modulators/demodulators) are performed in the digital domain. Nowadays, with a conventional Analog-to-Digital conversion on the header-receiver, only 7-8 bits are obtained with 3 GS/s Analog-to-Digital Converters.

The basic specifications of the implemented system in this paper are illustrated with the Table I:

TABLE I
SPECIFICATIONS OF THE IMPLEMENTED SYSTEM

Analog Input Frequency	DC-3 GHz
Signal Bandwidth	20 MHz
Sampling Frequency	400-500 MHz
Resolution	9 bits

In this paper an architecture based on subsampling is presented in order to improve the flexibility of a communication receiver, reducing the number of analog components. Using techniques based on subsampling, like those shown in this paper, we implement an Analog-to-Digital Conversion System with a resolution higher than 8 bits and with a maximum of 3,1 GHz of center frequency of the RF signals and close to 9 bits with a maximum center frequency of 2 GHz input approximately.

This paper is organized as follows: section II introduces subsampling and theoretical concepts on how to obtain the optimal subsampling frequency and to evaluate effect of the main non-idealities that will limit the implemented system. These non-idealities help us to justify the choice of components in section III. In section IV, experimental issues present the attained results about noise and distortion. The paper finishes with conclusions in section V.

II. THEORETICAL STUDIES ON SUBSAMPLING

A. Concept of subsampling and optimal frequency choice

In this section we study the way to calculate optimal subsampling frequency, using the signal bandwidth (BW) and its carrier frequency (f_c), in order to avoid aliasing and to maintain the copy generated between $-f_s/2$ and $f_s/2$ and the replicas as far as possible to the desired signal [1-6].

Hereafter, we will use the following notations (see Fig.1):

- f_s: subsampling frequency
- BW: signal bandwidth
- f_c: carrier frequency
- B: f_c+BW/2

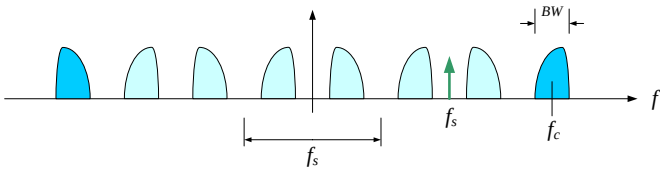

Fig. 1 Subsampling concept (m=3)

The minimal sampling frequency is established by the Nyquist Theorem, $f_s > 2B$. However, we can avoid aliasing with less f_s when expression (1) is true:

$$\frac{2f_c - BW}{m} > f_s > \frac{2f_c + BW}{m+1} \qquad (1)$$

m is an entire number whose meaning is the number of copies of the original signal that appears in the range [0, f_c-BW/2]. The maximum number of copies needed to avoid aliasing is calculated by the expression (2):

$$m_{\max} = floor\left(\frac{f_c - \frac{BW}{2}}{BW}\right) \qquad (2)$$

floor(x) is the entire number nearest to x y less than x. The last expression establishes the limits of f_s, the optimal frequency in this range. Concretely, the optimal value to avoid aliasing is one that produces a copy on $f_s/4$. This frequency equals:

$$f_s = \frac{4f_c}{m_{odd}} \qquad (3)$$

m_{odd} is an entire odd number more than 1:

- with $m_{odd} = 5,9,13, \ldots$ there is not spectral inversion
- with $m_{odd} = 3,7,11, \ldots$ there is spectral inversion

B. Main non-idealities

A general scheme of the implemented receiver is shown in the Figure 2. Its main advantage is its simplicity, eliminating a large amount of components in the traditional heterodyne structure. However, the specifications of the Sample&Hold are much more restrictive than in a traditional receiver. This device will be the most critical in our system because it processes high frequency signals.

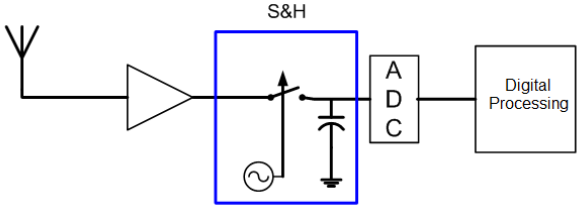

Fig. 2 Schematic of the receiver implemented

The main non-idealities produced in Sample&Hold are the following:

1) Jitter: Ideally, the input signal is sampled in equal frequency f_s intervals. Nevertheless, these intervals are different due to jitter [7-9]. This jitter produces an increment of the total noise, thus limiting the effective number of bits (ENOB).

Jitter is produced by two different sources: the phase noise associated to the oscillator and the aperture jitter of the Sample&Hold. At a first approximation we can consider these two sources of jitter as non-correlated Gaussian stochastic processes.

Aperture jitter of a Sample&Hold depends on the changes of the threshold voltage according to the input voltage so that its feature is dependent on the signal. This section shows how jitter affects Signal to Noise Distortion Ratio (SNDR) in the Sample&Hold output. The focus is the establishment of the maximum allowed jitter standard deviation depending on input frequency and the resolution specifications.

When the input is a sinusoidal signal like $y(t) = A\sin(2\pi f_{in} t)$, SNDR is determined by the expression (4):

$$SNDR = \frac{\frac{A^2}{2}}{\overline{N_\tau}} = \begin{cases} \dfrac{1}{4\pi^2 f_{in}^2 \sigma_\tau^2} : 2\pi f_{in\sigma_\tau} << 1 \\ \dfrac{1}{2(1 - e^{-2\pi^2 f_{in}^2 \sigma_\tau^2})} : other\_case \end{cases} \qquad (4)$$

Where $\overline{N_\tau}$ is the average power noise and σ_τ is the jitter standard deviation. To deduce the last expression, the spectral density was integrated between 0 and $f_s/2$.

To obtain more realistic values of the effect fot he jitter we performed simulations (by MATLAB® Software) while considering only the noise in the signal bandwidth is integrated (20 MHz) and the jitter presented by a stochastic process with an average of zero and standard deviation σ_τ. The equation (3) has been used to choose the optimal subsampling frequency f_s.

These simulations verify how the allowed jitter is lower for higher input frequencies. Figure 3 illustrates these conclusions to the following cases:

- *fc=4GHz, fs=484.84MHz*
- *fc=2GHz, fs=470.59MHz*
- *fc=1GHz, fs=444.44MHz*

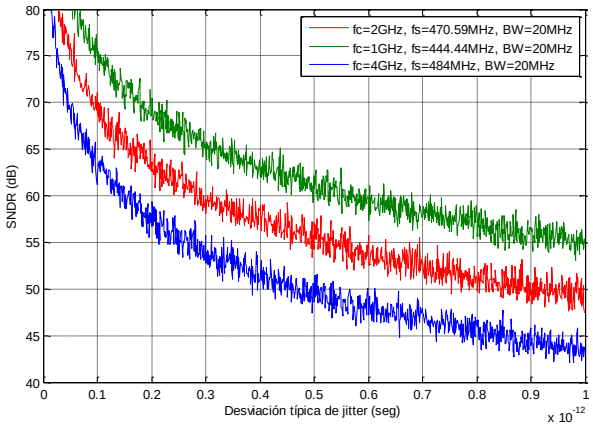

Fig. 3 Jitter effect depending on input frequency

2) *Overlapped Thermal Noise:* a typical Sample&Hold produces kT/C noise. To simplify the noise analysis we consider a sampling model as it is illustrated in Figure 4 [10]. This scheme consists of an input band pass signal (V_{in}), with an associated noise (N_{in}), which is filtered and later applied to a Sample&Hold modelled by a switch and capacitor. Due to the multiple overlapping produced by subsampling, many parts of the signal spectrum will be inside of the band of interest.

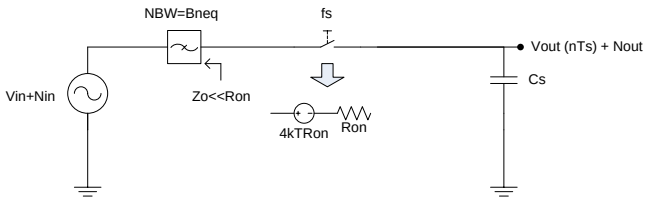

Fig. 4 Scheme of noise analysis

The equivalent switch resistance has a white noise power spectral equal to $4kTR_{ON}$ and it is filtered by the transfer function:

$$H(f) = \frac{1}{1 + 2\pi f R_{ON} C_S} \qquad (5)$$

The result is a filtered white noise with a power equal to $\frac{kT}{C_S}$, whose value is independent of the resistance and subsampling frequency.

We assume:

$$f_s << \frac{1}{2\pi R_{ON} C_S} \qquad (6)$$

Then, due to the subsampling process, we can approximate all noise power overlapped between 0 and $\frac{f_s}{2}$, as illustrated in Figure 5.

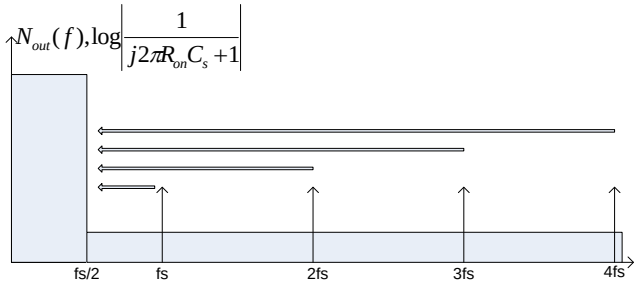

Fig. 5 Subsampling effect over the Sample&Noise

Although the total noise power is not dependent on subsampling frequency, noise floor reduces if this frequency grows. Concretely, noise floor is reduced 3 dB if subsampling frequency is doubled. Thus, it is convenient to choose a maximum subsampling frequency to distribute noise floor throughout the entire Nyquist band.

3) Other considerations in choosing Sample&Hold:

- Its bandwidth should be maximized in order to not filter GHz signals.
- Although it has a high bandwidth, the Sample&Hold should be able to sample frequencies close to MHz, due to these values are the maximum sample frequencies for high resolution commercial A/D converters.
- Its output ENOB can be limited by linearity, so we should study its THD and SFDR.

III. USED COMPONENTS

The theoretical study that was briefly explained in section II allows fixing the specifications of the main building blocks of the system, i.e., the Sample&Hold and the ADC.

After a study on commercial components, we decided to use an external Sample&Hold for the A/D Converter since an internal Sample&Hold bandwidth is limited to 3 GHz approximately with a resolution around 7-8 bits. However, when using an external Sample&Hold, it is possible to obtain a higher resolution for a wider bandwidth.

The chosen Sample&Hold is the Inphi 1821 TH [11], with the following features:

- Wider bandwidth (18 GHz).
- Wider frequency range (0-6 GHz) for 10-bit linearity.
- Thermal noise is not an obstacle (SNR>60 dB)
- Low phase noise, with SNR > 60 dB in the range 0-3,2 GHz.
- Capability to sample at the interested frequency (around 500 MS/s)

This requirement (500 MS/s) is given by the maximum sampling frequency for commercial 10-bit A/D converters, since using a maximum sampling frequency is convenient in

order to reduce the overlapping noise effects. Concretely, the A/D converter chosen is E2V AT84AS001 [12].

IV. Experimental Results

The receiver system implemented is illustrated in Figure 6. In this system the GHz input signal is generated and converted to differential to be sampled by the Sampled&Hold. By the other side, a unique clock signal is generated to the Sample&Hold and the ADC that is converted to differential signal too, with baluns at lower frequencies. We used the evaluation boards of these devices connected by cables. Also DC blocks and bias tee are used to block the DC signal and to adapt the impedances.

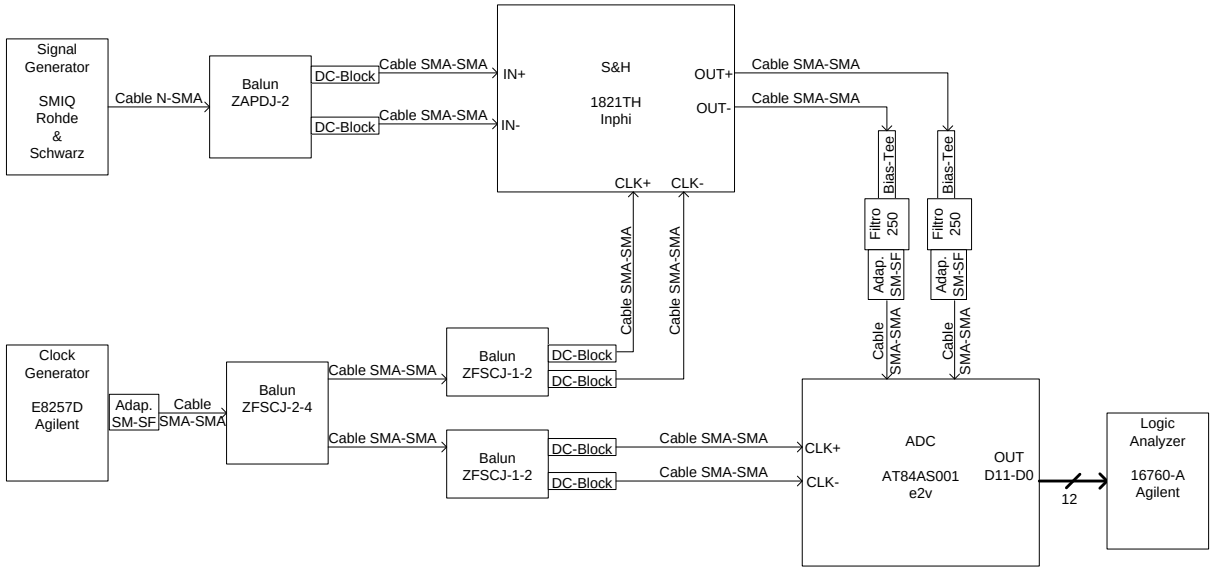

Fig. 6 A/D converter system implemented

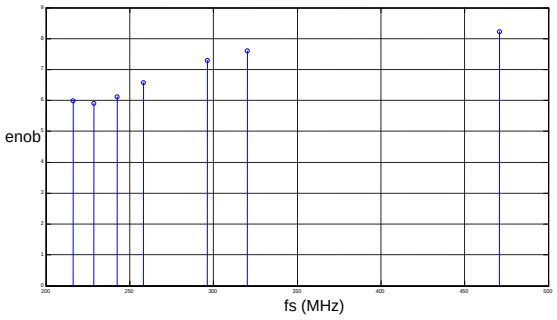

Fig. 7 Measurement of the effect of overlapping noise (ENOB vs. the different Subsampling Optimal Frequencies)

Another interesting measurement is the influence of the jitter, which is more critical at higher frequencies and hence the main limitation in the implemented system. This effect is illustratedin Figure 8, using the optimal subsampling frequency immediately less than 500 MHz.

This system can be used to illustrate some subsampling effects studied in the previous sections, like the overlapping thermal noise within band signal, which is dependent on the subsampling frequency. This effect is illustrated in Figure 7, where we use the optimal frequency so that third order harmonics are overlapped with the signal (as it is deduced from the theoretical studies), and this way we only measure the noise effect (SNR) integrated in the signal bandwidth, because the second order harmonics will be the furthest possible to the desired signal. Signal amplitude is equal to -1 dBm and noise is integrated in 20 MHz.

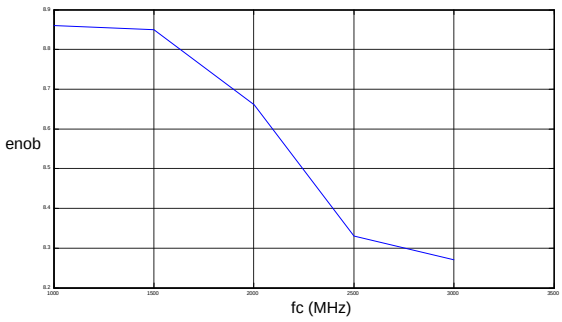

Fig. 8 Jitter effect measurement (ENOB vs. Carrier frequency)

The total resolution of this system is illustrated in Figure 9, using the optimal subsampling frequency immediately lower than 500 Mhz. The final result is an A/D converter system that converts signals up to 3,1 GHz with more than 8 effective bits.

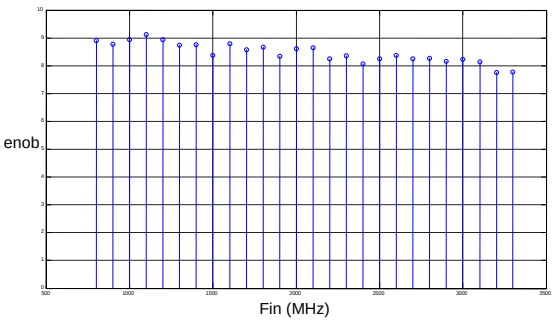

Fig. 9 ENOB of the implemented system vs. Caarrier Frequency

As an example, the output spectrum is illustrated in Figure 10, for a 3 GHz input frequency and a 480,2 MHz optimal subsampling frequency.

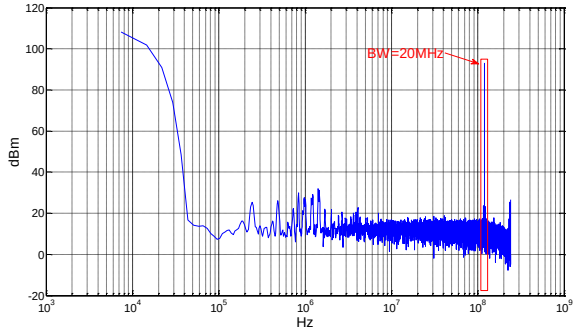

Fig. 10 Output Spectrum to a 3 GHz Analog Input Signal

V. Conclusions

In the present document we have discussed the current limitations of the resolution of A/D converters, which is an obstacle for the use of the digital signal processor directly in RF. In this paper an Analog-to-Digital Converter System using techniques based on subsampling has been presented.

We have introduced the subsampling concept and its main non-idealities, like jitter or overlapping thermal noise. The theoretical study has been used to design a system that demonstrates experimentally that the performance of subsampling based system.

Experimental features of the proposed receiver system (for signals with a 20 MHz bandwidth) are:

- ENOB is around 9 bits to 1-2 GHz input frequency.
- ENOB is more than 8 bits up to 3,1 GHz input frequency.

Therefore, the experimental results place the subsampling based receiver as an alternative to the typical receiver architectures with an enhanced reconfigurability and programmability.

Acknowledgments

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"Multiple Clocking High Analog-to-Digital Conversion Based on Subsampling", *XXVI Conference of Design of Circuits and Integrated Systems (DCIS'2011)*, 2011.

Multiple Clocking High Analog-to-Digital Conversion based on Subsampling

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***Abstract*— This paper presents a Data Acquisition System for testing wideband multi-standard receivers using techniques based on subsampling. With the Software Defined Radio paradigm in mind, the ultimate goal is the design of an Analog-to-Digital conversion system which, configured by software at the Radio Frequencies, can be a part of low-cost certification equipment. Its main objective is to improve the features of a previously presented data acquisition module that uses a common clock reference. This proposed system is based on commercial devices, mainly a Low Jitter and Wideband Sample&Hold and a High Resolution Intermediate-frequency Analog-to-Digital Converter.**

***Keywords*— Analog-to-Digital Converter, ENOB, Jitter, Sample&Hold, Software Defined Radio, SNDR, Thermal Noise**

I. Introduction

Nowadays, due to the acceptance of wireless technologies, in the consumer market (mobile phones, personal computers, TV sets, etc.) there is a large number of different communication standards. As a consequence, there is a trend to design multi-standard receivers [1-6], preferably low cost, using only a few components.

In order to get the paradigm of the Software Defined Radio (SDR) to increase the resolution and speed of the Analog-to-Digital Conversion stage, it is crucial to be able to place it closer the antenna [7-8]. Thus the analog front end is greatly simplified and the flexibility of the receiver is improved, due to the fact that more analog functionalities (e.g. filters, mixers) are performed in the digital domain.

Subsampling receivers use a Sample&Hold (S&H) to produce low frequency replicas of the RF signal based on pass-band sampling technique. Therefore, the main advantage of the system based on subsampling is its flexibility, because it is possible to process most of the signal digitally. Also, the number of analog building blocks is lower and we can use an Analog-to-Digital Converter (ADC) whose specifications are more relaxed for a very wide input frequency band. On the other hand, some of the main disadvantages of the system based on subsampling are the demanding specifications required for the S&H (wide input bandwidth and low aperture jitter) and the high noise figure due to the effect of the folded thermal noise in the band of interest.

The current state-of-art of high-frequency ADCs does not allow the use of the ADC directly in the RF domain. In a previous work [9] we presented an Analog-to-Digital Converter system based on subsampling that improved the current specifications for the conventional conversion (7-8 bits with 3 GS/s ADCs) on the header-receiver, obtaining a resolution higher than 8 bits and with a maximum of 3,1 GHz of center frequency of the RF signals.

In the last years, the specifications of the state-of-art have been improved, making it possible to obtain a resolution around 8-9 bits for 3.6 GS/s ADCs [10].

Therefore, we proposed to improve the resolution of our system using two different optimal sampling frequencies in order to reduce the effect of the folded thermal noise and thus, increasing the total resolution.

The basic specifications of the implemented system in this paper are illustrated in Table I:

TABLE I
SPECIFICATIONS OF THE IMPLEMENTED SYSTEM

Analog Input Frequency	DC-3 GHz
Signal Bandwidth	20 MHz
Sampling Frequency S&H	<2 GHz
Sampling Frequency ADC	<500 MHz
Resolution	>9 bits

With a signal bandwidth of 20 MHz, the proposed ADC system achieves between 8,8 and 9,8 bits of resolution for a programmable carrier frequency ranging from 0 up to 3.2 GHz. By proper selection of the center frequency and signal bandwidth this data acquisition system can be used in most of present wireless standards.

This paper is organized as follows: section II reviews subsampling and theoretical concepts on how to obtain the optimal subsampling frequency and to evaluate effects of the main non-idealities that will limit the implemented system. These non-idealities help us to justify the choice of the new sampling frequency plan in this section and the choice of the components in section III. In section IV, experimental issues present the attained results about noise and distortion. The paper finishes with conclusions in section V.

II. A REVIEW OF SUBSAMPLING

A. Concept of subsampling

Subsampling is the process of sampling a signal with a frequency lower than twice the signal highest frequency. Subsampling a bandpass Radio Frequency (RF) signal will fold the signal spectrum to lower frequencies, where these replicas of the RF signal at baseband or IF can be used to extract the original baseband signal (see Fig. 1).

B. Selecting the sampling frequency

For a given signal bandwidth (BW) and carrier frequency (f_c) it is convenient to select an appropriate sampling frequency. The minimal sampling frequency is determined by the Nyquist Theorem: $f_s > 2\ (f_c+BW/2)$. However, for a bandpass signal a sampling frequency lower than the Nyquist frequency can be selected if expression (1) still holds [11], in order to avoid aliasing and to maintain the copy generated between $-f_s/2$ and $f_s/2$:

$$2(f_c - BW/2)/(m-1) \geq f_s \geq 2(f_c + BW/2)/m \qquad (1)$$

where m is the number of replicas of the signal spectrum in the range $[0, f_c\text{-}BW/2]$ between 1 and $floor((f_c+BW/2)/BW)$. An appropriate value is $f_s=4f_c/m_{odd}$ which produces a replica at $f_s/4$. The number of replicas is selected from the odd number m_{odd}.

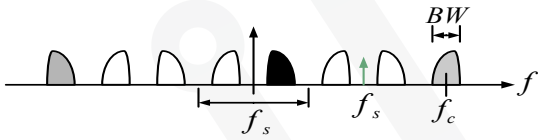

Fig. 1 Subsampling concept (m=3)

C. Main non-idealities

The main non-idealities produced in S&H are the following:

1) *Jitter Noise*: There are two main sources of jitter noise, the phase noise associated to the clock reference and the aperture jitter of the S&H. In a first order approach, they can be considered to be non-correlated Gaussian stochastic processes.

For a sinusoidal input signal the Signal-to-Noise and Distortion Ratio (SNDR) at the S&H output is approximately given by expression (2) [12]:

$$SNDR = \frac{A^2/2}{\overline{N}} \begin{cases} 1/4\pi^2 f_{in}^2 \sigma_j^2 & : 2\pi f_{in}\sigma_j \ll 1 \\ 1/2\left(1 - e^{-2\pi^2 f_{in}^2 \sigma_j^2}\right) & : otherwise \end{cases} \qquad (2)$$

where A is the signal amplitude, $\overline{N}$ the average noise power, f_{in} the input frequency, and σ_j the jitter standard deviation. With these expressions we can see how the jitter increases with the frequency.

Concerning the system clock, there are two primary mechanisms that cause jitter: the thermal noise and the coupling noise. The latter can be caused by crosstalk and/or ground loops within, or adjacent to, the area of the circuit.

2) *Folded Thermal Noise:* the S&H suffers from *kT/C* noise, as the entire wideband noise folds inside the band of interest (Fig. 2). Therefore, it is convenient to select the largest sampling frequency among the set of possible sampling frequencies set by the Digital Signal Processing blocks specifications to distribute noise floor throughout the entire Nyquist band. This one will be termed as the "optimal" sampling frequency.

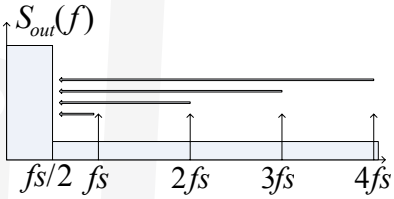

Fig. 2 Subsampling effect over the Sample&Hold

D. New frequency plan

Due to the effect of the folded thermal noise, in the previous work [1] we chose the maximum optimal sampling frequency possible for commercial 10-bit A/D converters, i.e., around 400-500 MHz to generate the same signal clock for both components (S&H and ADC). Therefore, we implemented the subsampling process with the S&H, obtaining a replica at $f_s/4$, i.e., at 100-125 MHz. Thus this signal is converted to digital by the ADC sampling with a sampling frequency higher than the Nyquist Frequency.

However, if the ADC analog bandwidth is larger than half of its maximum sampling frequency we can take advantage of this in order to implement a second subsampling process with the ADC.

Thus, using the new frequency plan, the S&H will be able to sample at higher frequencies (in the range of GHz for commercial devices) in order to reduce the effect of the folded thermal noise.

Moreover, the output of the S&H at intermediate frequencies will need to be filtered by a band pass filter so that the noise does not fold at the band of interest due to the second subsampling process done by the ADC.

Fig. 3 illustrates the difference between both works:

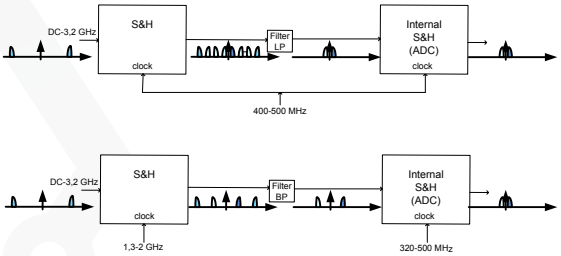

Fig. 3 Schemes of previous work (above) and current work (below)

III. USED COMPONENTS

The theoretical study that was reviewed in section II allowed fixing the specifications of the main building blocks of the system, i.e., the Sample&Hold and the ADC.

The chosen Sample&Hold in the previous work was the Inphi 1821 TH [13], with the following features:

- Low aperture jitter (50 fs).
- Wider bandwidth (18 GHz).

- Wider frequency range (0-6 GHz) for 10-bit linearity.
- Thermal noise is not an obstacle (Signal-to-Noise Ratio (SNR)>60 dB)
- Low phase noise, with SNR > 60 dB in the range 0-3,2 GHz.

Moreover, the maximum clock frequency of this device is equal to 2 GHz, thus this will be the maximum subsampling frequency for the proposed solution.

In order to use the maximum sampling frequency for commercial 10-bit A/D converters, we chose E2V AT84AS001 [14] in the previous work, with a maximum sampling frequency equal to 500 MS/s. Moreover, this component has an analog input bandwidth equal to 1 GHz, so we can implement a second subsampling process with the ADC whose maximum input frequency will be equal to 500 MHz, according to the first subsampling process.

IV. Experimental Results

The receiver system implemented is illustrated in Figure 4. In this system the GHz input signal is generated and converted to differential to be sampled by the Sampled&Hold. On the other hand, we generate two different clock signals, one of them up to 2 GHz (S&H) and the other one up to 500 MHz (ADC). At intermediate frequency the signal is subsampled by the internal S&H of the ADC. Moreover we use other components, such as baluns to convert the signals to differential or DC blocks and bias tee, which are used to block the DC signal and to adapt the impedances.

The system performances obtained from measurements are summarized in Table II. The ENOB (based on the maximum SNDR) is between 8,8 and 9,8 bits for sinusoidal input signals up to 3.2 GHz. The Spurious Free Dynamic Range (SFDR) is about 60 dBc regardless of the input frequency.

TABLE II
System Performances

Maximum Input Frequency	3.2 GHz
Signal Bandwidth	20 MHz
Sampling Frequency S&H	1.3-2 GHz
Sampling Frequency ADC	320.1-480.3 MHz
ENOB (SNDR)	>8.77 bits
SFDR	>61.2 dBc
Voltage Supply S&H	-5,2 V
Voltage Supplies ADC	5 V (Analog), 3.3 V (Digital, Output)
Power Consumption	3.7 W

These performances have been obtained by a measurement setup summarized in Table III:

TABLE III
Measurement Setup

Analog Input Amplitude Range	[-1,3] dBm
Clock Signal Amplitude	16 dBm
Digital Signal Acquisition	Synchronous Mode Full-Channel 800 Mbps
Digital Signal Processing	65536 points-FFT, Kaiser window

Figure 5 shows the ENOB as a function of the carrier frequency up to 3,2 GHz for a signal bandwidth equal to 20 MHz. The results are compared with those from the previous work. Moreover this figure shows expected results according to the increase of the S&H sampling frequency. These expected results are calculated by the ratio between the new sampling frequency and the previous sampling frequency. For instance, if we used 500 MHz as S&H sampling frequency for a concrete input frequency and the new sampling frequency is 2 GHz the ratio will be 4, i.e., 6 dB.

Figure 5 shows how the expected results and those that are measured are very similar and how the resolution is improved around 1 bit. Moreover, Figure 5 shows how the resolution falls as the input frequency increases, mostly due to the influence of jitter.

On the other hand, the ADC sampling frequencies must be slightly different from the ADC sampling frequencies used in the previous work. This fact can be the main cause of the difference between the obtained results and the expected results.

Moreover, we can use lower sampling frequencies if the Digital Signal Processing specifications are more restrictive. Figure 6 shows the resolution for different ADC clock frequencies, which will be imposed by the digital restrictions about the maximum sampling rate. In these cases there will be a compromise between the allowed maximum speed and resolution.

This figure also illustrates how the resolution grows as the sampling frequency increases due to the decreasing integrated noise in the 20 MHz signal bandwidth.

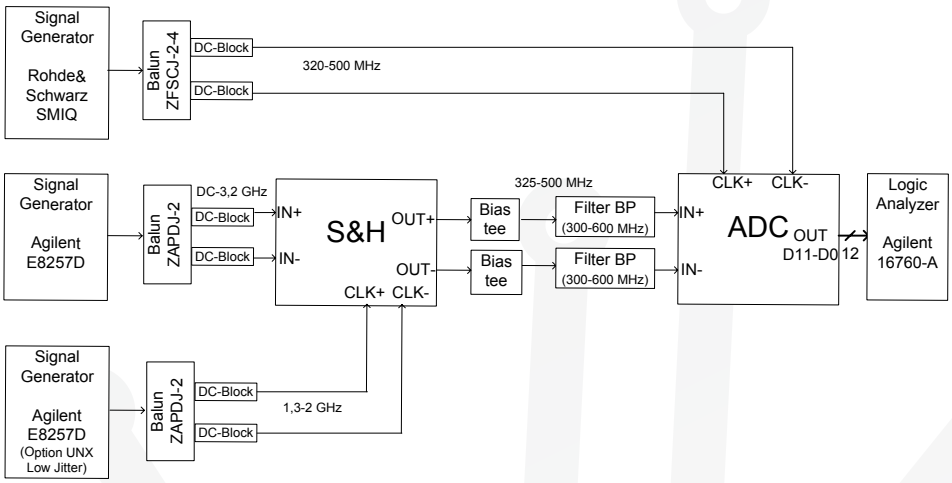

Fig. 4 Implemented A/D converter system

TABLE IV
STANDARDS SPECIFICATIONS AND RESULTS

	Carrier Frequency (MHz)	Signal BW (MHz)	Resolution Specifications (bits)	SNDR Specifications (dB)	Resolution Results (bits)	SNDR Results (dB)
GSM	1800	0.2	9	55.94	12.72	78.35
UMTS (I)	2110-2170	10	6	37.88	9.3	57.75
Blue-tooth	2400	1	11	67.98	11.26	69.55
IEEE 802.11b (Wi-Fi)	2400	20	8	49.92	9.1	56.54

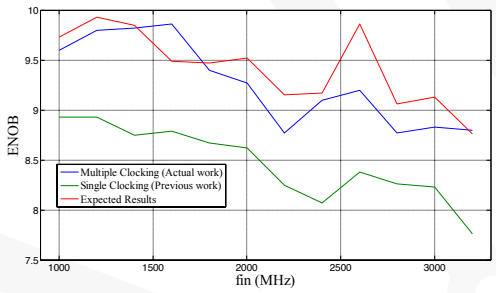

Fig. 5 ENOB of the implemented system vs. Carrier Frequency

Table IV shows the configuration parameters and specifications [15] required for some of the most common wireless communication standards. Also this table shows the experimental results obtained for the different standards. Note that the maximum signal bandwidth is 20 MHz. For lower bandwidths, the entire 20 MHz band around the central frequency is converted, and the selected bandwidth is reduced by means of digital signal processing increasing the resolution.

Therefore, we can observe how the implemented data acquisition system can be used in order to evaluate most communication standards in terms of tuning frequency, linearity and noise. Also we can observe how the specifications were not achieved by the previous work [9] for some wireless standards. For instance, the resolution obtained with [9] for Blue-tooth was 10.3 bits while it is 11.26 with the proposed system. Thus, the current work covers more wireless communication standards than the previous work.

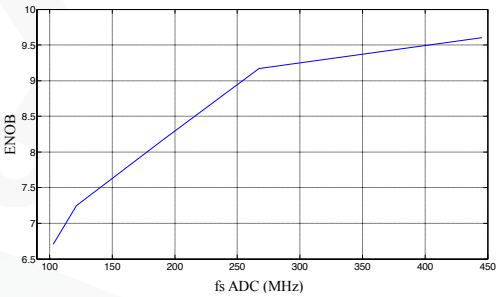

Fig. 6 Measurement of the effect of folded noise (ENOB vs. different Subsampling Optimal Frequencies)

V. Conclusions

This paper has presented the design of a data acquisition system for testing wireless receivers based on subsampling, which covers most current communication standards. The implemented system is very simple, with only a few components, when compared to conventional testing equipment.

The proposed system is an improvement of a previous work presented by using two different sources of clock in order to implement two different sampling frequencies. The focus of this new frequency plan is to increase the first S&H sampling frequency in order to reduce the effect of the folded thermal noise.

Experimental results of the proposed system show (for a 20 MHz signal bandwidth) an ENOB between 8,8 and 9,8 bits up to 3,2 GHz center frequency. The obtained resolution is around 1 bit higher than the previous work, such as we expected. These results show that, for testing purposes, the subsampling based receiver is an alternative to other typical frequency mixer receiver architectures.

Acknowledgments

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"Optimization of Subsampling Dual Band Receivers Design in a Nonlinear Systems," *IEEE MTT-S International Microwave Symposium Digest (IMS'2012)*, 2012.

Optimization of Subsampling Dual Band Receivers Design in Nonlinear Systems

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***Abstract* — This paper presents an optimization of the noise performance for a dual band receiver based on subsampling in a nonlinear scenario. The focus is on designing a multiband receiver for software defined radio. Thus, another goal of the presented architecture is its flexibility, focusing on the jitter and folded noise optimization of the subsampling receiver and covering as many wireless standards as possible. To approach these objectives, different architectures based on subsampling technique are investigated and analyzed.**

***Index Terms* — Dual Band, Jitter, Nonlinear Systems, Receivers, Signal Sampling, Software Radio, Thermal Noise**

I. Introduction

Due to the emergence of several co-existing wireless technologies, there is a trend to design multi-standard receivers and to optimize their flexibility and simplicity. Subsampling techniques [1], which fold the RF signals to IF replicas, may be used as a solution for receiver design with fewer number of components. Using subsampling architectures would relax the requirements and specifications of the analog-to-digital converters (ADC) in order to get the paradigm of the Software Defined Radio (SDR) [2].

Some of the main drawbacks of the subsampling techniques are found in the constraints in the Sample_&_Hold (S&H), which processes the high frequency signals as described in the section-II-B. There is a challenge in utilizing the subsampling techniques in nonlinear systems, because the replicas of the generated harmonics are folded in the interest band and may overlap with the desired signals. This issue had been addressed and studied in [3] where a universal formula for bandpass sampling in nonlinear systems was developed. The extension of this approach for dual band nonlinear systems had been employed in this paper.

For dual band applications the main problem of using subsampling is the possible overlapping between the two desired signals in IF frequency band. Although this drawback has been studied in [4], this paper extends this approach in designing the subsampling based receiver and optimizes the system in respect to the typical non idealities of subsampling receivers, i.e., jitter and folded noise.

This paper is organized as follows: section II reviews the subsampling concepts and the main sources of noise. Section III presents the formulas employed for dual band and nonlinear systems using subsampling techniques. In section IV, different architectures are presented in order to optimize the system based on SNR and hardware requirements.

II. Review of Subsampling

A. Concept of subsampling

Subsampling is the process of sampling a signal with a frequency lower than twice the highest signal frequency (or Nyquist rate). Using subsampling, the RF signal will fold the signal spectrum to lower frequencies, where it can be used to extract the original baseband signal.

For a given signal bandwidth (BW) and carrier frequency (f_c), and to avoid aliasing and maintain the copy of the generated signal between $-f_s/2$ and $f_s/2$, the subsampling frequency can be selected if expression (1) satisfies [1]:

$$\frac{2(f_c + BW/2)}{m} < f_s < \frac{2(f_c - BW/2)}{m-1} \tag{1}$$

where m is the number of replicas of the signal spectrum in the range $[0, f_c\text{-}BW/2]$ between 1 and $floor((f_c+BW/2)/BW)$.

B. Main sources of noise

The main non idealities produced in S&H are the jitter noise and the folded thermal noise.

Jitter noise, for a sinusoidal signal, can be defined as [5]:

$$N_j = (2\pi f_{RF}\sigma_j)^2 \tag{2}$$

where f_{RF} is the input frequency and σ_j is the variance of the jitter error.

The folded thermal noise is caused by the aliasing inside the Nyquist band. It is defined as follows:

$$N_F = (k-1)N_{out} \tag{3}$$

where N_{out} is the out-of-band noise, $k=floor(2B_{eff}/f_s)$ and B_{eff} is the effective noise bandwidth.

III. Subsampling For Dual Band and Nonlinear Systems

The effect of subsampling a dual band signal in a third order nonlinear system is illustrated in Fig. 1, showing the spectrum due to in-band intermodulation and cross modulation.

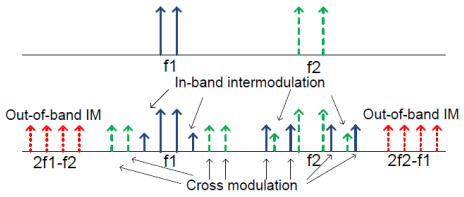

Fig. 1. Power spectrum at the input (top) and the output (bottom) of a nonlinear system

The universal formula to find valid sampling frequencies in the presence of harmonics is given by [3]:

$$if_1 + n_k f_s \le jf_1 < if_1 + (n_k + 1)f_s \qquad (4)$$

Being if_1 and jf_1 two harmonics of f_1 and $n_k = floor((jf_1 - if_1)/f_s)$.

An algorithm to find the range of valid subsampling frequencies for multiband systems is presented in [4]. From the general equations obtained in [4], and considering the particular case of dual band system, the maximum replica order of the lower band (n_1) meets the following equation:

$$n_1 = floor\left(\frac{f_{L1}}{f_s}\right) \le floor\left(\frac{f_{L1}}{2((f_{U1} - f_{L1}) + (f_{U2} - f_{L2}))}\right) \qquad (5)$$

Where f_{L1} and f_{U1} are the low and the high limits of the lower band and f_{L2} and f_{U2} are the low and the high limits of the upper band. Knowing $f_2 = R_1 f_1$, replica orders of the upper band (n_1) meet the following constraint:

$$floor(R_1 n_1) \le n_2 \le floor(R_1 n_1 + R_1) \qquad (6)$$

The eight possible ranges for dual band applications are listed in [4]. Thus, the final sampling ranges will be given the following expression:

$$F = F_{db} \cap F_{imd} \cap F_{cmd} \cap F_{hmd} \qquad (7)$$

Where F is the intersection of all the valid ranges calculated from (4) and (5), F_{db}, F_{imd}, F_{cmd} and F_{hmd} are the valid sampling frequency sets for the fundamental signals, intermodulation, cross modulation and harmonic distortion, respectively.

In order to find F an algorithm has been developed and written in MATLAB script. This algorithm calculates these ranges and the location of the replicas where the input parameters are the fundamental frequencies, the number of harmonics and the signal bandwidth. As an example, Table I shows the three first valid ranges immediately lower than 2 GHz for the fundamentals signals at 1.82 and 2.4 GHz, considering five harmonics and a signal bandwidth equal to 25 MHz. The subsampled spectrum is illustrated in Fig. 2 for a sampling frequency equal to 2 GHz, showing that there is no overlapping between signals.

TABLE I
VALID SAMPLING FREQUENCIES BELOW 2 GHZ

Lower Frequency Bound (MHz)	Upper Frequency Bound (MHz)
1995	2000
1837.5	1978.33
1801.67	1802.5

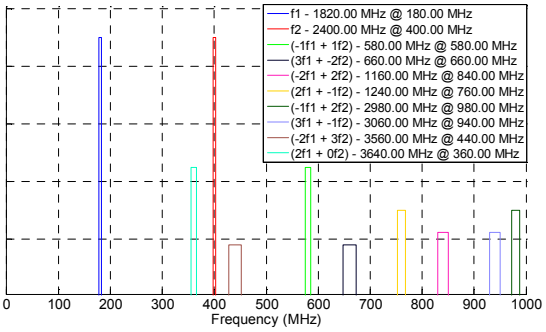

Fig. 2. Subsampled spectrum for 1.82 and 2.4 GHz input frequency

IV. OPTIMIZATION OF THE RECEIVER ARCHITECTURE

In order to optimize the proposed receiver, seven input frequencies have been selected to study the selective combinations for different dual band applications. These chosen standards are WCDMA (V) at 880 MHz, GSM-DCS at 1.82 GHz, WCDMA (I) at 2.12 GHz, Bluetooth at 2.4 GHz, WiMAX at 3.5 and 5.8 GHz, and 802.11a at 5.2 GHz.

Since the main focus is to cover the maximum number of standards, it is mandatory to use a S&H before the ADC in order to have enough analog bandwidth. The S&H from Inphi with part number 1821TH has been selected for this work, because of its high input analog bandwidth (up to 18 GHz), minimum aperture jitter (50 fs) and a maximum clock frequency equal to 2 GHz.

The first studied scenario is based on high resolution ADC with a high sampling frequency to reduce the folded noise effect. With this focus in mind the selected ADC was a 12-bit ADS5400 from Texas Instruments with maximum clock frequency of 1 GHz. Using a sampling frequency of almost 1 GHz, it is possible to cover all the dual band applications, as illustrated in Fig. 3 (Case 1), where the meaning of axis x is illustrated in Table II. Using as reference a typical SNR of the ADC equal to 58 dB, the theoretical SNR for each dual band application was calculated from (2) and (3).

Another option is to use a higher resolution ADC, like the 14-bit ADS5474 from Texas Instruments (Case 2 in Fig. 3). This device was selected because its maximum sampling frequency is 400 MHz and, therefore, the folded noise would only be around 4 dB higher than Case 1.

TABLE II
DUAL BAND APPLICATIONS AND AXIS X CORRESPONDENCE

X axis	1	2	3	4	5	6
Input Freq. (GHz)	0.88-1.82	0.88-2.12	0.88-2.4	0.88-3.5	0.88-5.2	0.88-5.8
X axis	7	8	9	10	11	12
Input Freq. (GHz)	1.82-2.12	1.82-2.4	0.88-3.5	1.82-5.2	1.82-5.8	2.12-2.4

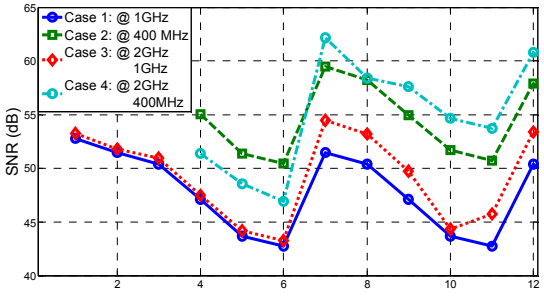

Fig. 3. Expected SNR for single and multiple clock architectures

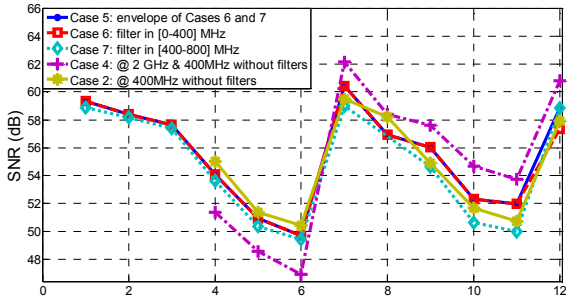

Fig. 4. Expected SNR for different architectures based on BP filters

However, as shown in Fig. 3, this option is less flexible, because it is not possible to find any sampling frequency lower than 400 MHz for the first three scenarios. In order to improve the SNR without losing flexibility, two steps subsampling approach is proposed, where the sampling frequency of S&H was set at around 2 GHz and the sampling frequency of ADC at around 1 GHz (Case 3 in Fig. 3). Although this architecture improves the SNR by approximately 3 dB from (3) in respect to Case 1, it could be necessary to implement a second subsampling process and, therefore, a new folded noise effect will be added.

The last option is to use a multiple clock architecture employing the ADS5474 (Case 4 in Fig. 3) and a first sampling frequency around 2 GHz. Theoretically the SNR is improved around 3 dB in respect to Case 3. In this case, due to the second subsampling process, folded noise effects must be added as well.

For the rest of combinations of frequencies the curves present the same tendency, being possible to cover all the scenarios. However, since cases 2 and 4 present the best results about SNR the next step will be to cover all the dual band applications for these cases. The proposed solution is to use a bank of band-pass filters between the S&H and the ADC. This solution will be applied to Case 4, because it has more flexible architecture, with a higher number of available valid ranges. Using this solution, some harmonics will be removed and the flexibility of the receiver will be increased.

The solution is based on two filters, whose band-pass ranges are [0-400] and [400-800] MHz. The maximum sampling frequency was selected in order to have both fundamental replicas in each range. The selected filter corresponds to the higher of these two frequencies (Case 5 in Fig. 4).

Another solution is to fix a unique BP filter for all the applications (Case 6 and 7 in Fig. 4). In these cases it is possible to cover almost all the standards with only one of these filters, without considerably reducing the resolution. Although in order to maximize the flexibility and the SNR, the optimal architecture is like the one illustrated in Fig. 5, for a more concrete application or more relaxed SNR specifications a single BP filter could be used in order to reduce the complexity of the system.

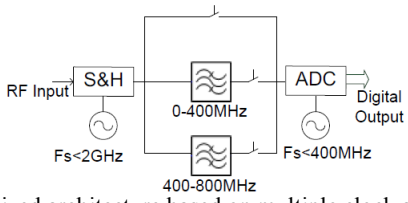

Fig. 5. Optimized architecture based on multiple clock and BP filters

V. Conclusion

In this paper an optimization for a dual band multi-standard receiver based on subsampling in a non linear environment has been presented. Subsampling techniques have been selected due to the simplicity that these systems present in comparison to traditional receivers. However, receivers based on subsampling have additional sources of noise whose minimization has been the main focus of this work from the study of different architectures. Moreover, dual band systems in nonlinear scenarios have an additional problem because of the overlapping of harmonics. An efficient algorithm has been developed in order to find the valid sampling frequencies, increasing the flexibility of the receiver and covering the maximum number of dual band applications for different communication standards.

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9.5.4 Publications partially related with this thesis

"An 8-bit 19 MS/s low-power 0.35 μm CMOS pipelined ADC for DVB-H", *Integration, the VLSI Journal*, 2012

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An 8-bit 19 MS/s low-power 0.35 μm CMOS pipelined ADC for DVB-H

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ABSTRACT

This paper proposes an 8b 19 MHz CMOS pipelined analog-to-digital converter (ADC) for DVB-H. In order to reduce the power consumption a combination of techniques has been used, such as op-amp sharing, low-power amplifiers with gain boosting and an aggressive capacitor scaling. The prototype ADC fabricated in 0.35 μm CMOS demonstrates a maximum differential nonlinearity (DNL) of 0.63 least significant bit (LSB) and a maximum integral nonlinearity (INL) of 0.58 LSB with a peak signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of 42.76 and 51.57 dB at 19 MHz. The ADC with an active area of 4.78 mm^2 consumes less than 4 mW at the mentioned sampling frequency.

1. Introduction

During the last few years much effort has been devoted towards the reduction of the supply power of mixed signal CMOS systems. This is primarily due to the increasing importance of battery-powered electronics, and the continued down-scaling of device sizes. Pipelining has been accepted as one of the best approaches to implement high-speed medium-to-high resolution analog-to-digital converters with minimum power consumption.

Digital video broadcasting (DVB) system becomes very attractive for applications in wireless mobile communication devices, such as laptop computers, mobile phone and vehicles [1]. Recently, digital video broadcasting-handheld (DVB-H) has made it possible to deliver broadcast television or other multimedia services to a mobile or handheld device [2]

The block diagram of a DVB analog front-end is shown in Fig. 1. The tuner selects the channel converting the OFDM RF signal to a first intermediate frequency around 35 MHz after which it is bandpass filtered by a SAW-filter stage. The SAW filter is followed by a controllable gain amplifier (AGC) in order to adapt the signal level. Finally the resulting signal is converted into a digital signal using an ADC.

The proposed receiver implements a subsampling technique as this is the most efficient solution from a power consumption point of view. This technique performs, at the same time, the mixing and sampling process, taking advantage of the band folding inherent to the sampling process.

For an intermediate frequency value of 34 MHz and the maximum signal bandwidth defined in the DVB standard (8 MHz), the optimum value for the sampling frequency is next to 19 MHz. Attending to the Mobile and Portable DVB-T Radio Access Interface (MBRAI) from EICTA, the SNR for the demodulation process should be 27 dB in the worst case. An 8 bit ADC achieves the specification, including a security margin in order to anticipate interfering components influence.

This paper is organized as follows: the pipelined ADC 1.5-bit per stage architecture is shown in Section 2. Section 3 enumerates and details the low power techniques applied to the ADC in order to achieve such a low consumption. Section 4 describes the circuit implementation and the measurement results. The paper is concluded in Section 5.

2. ADC Architecture

A 1.5-bit-per-stage architecture has been used in the pipelined ADC because it shows both the lower power consumption and smallest area compared with architectures based on higher resolution stages. The power efficiency of the 1.5 bit configuration [3–5] rely on that the amplifiers operate at a low closed-loop gain leading to a best settling time for minimum power consumption.

A block diagram of the pipeline 1.5-bit/stage architecture is shown in Fig. 2. It consists of a cascade of seven stages. Each stage resolves two bits with a sub-ADC, subtracts the converted value, which only can take values $-V_{ref}$,V_{ref} or 0 (where V_{ref} is differential reference voltage), from its inputs, and amplifies the

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Compact low-power implementation for continuous-time ΣΔ modulators

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ABSTRACT

This paper presents a low-area continuous time (CT) sigma–delta (ΣΔ) modulator implementation based on a local feedback. The proposed structure provides a very low impedance node without the need of classical op-amps, which leads to a reduction in power and area consumption. Two versions of a conventional first-order CT ΣΔ modulator prototype have been fabricated with the purpose of evaluating the idea. The modulator requirements have been set for a passive RFID tag with sensing capability application, so that achieving minimum active area and very low power consumption are the main objectives for the presented design. Experimental results of the first version of the modulator show 8 bits of Effective-Number-Of-Bits (ENOB) in a 25 kHz signal bandwidth with 7 μW of power consumption. The proposed implementation has also shown to be very robust against supply voltage and bias current variations. A second approach has also been designed, using the same principle of operation, in order to increase the input voltage range without any power consumption penalty at the expense of decreasing the input impedance and stingily increased area. This second approach shows 9 bits of ENOB in the same signal bandwidth with a power consumption of 4.35 μW. A Figure Of Merit (FOM) of 0.267 pJ/state has been achieved with a total area consumption (without pads) of 110 μm × 125 μm in a 0.35 μm CMOS technology.

1. Introduction

RFID (Radio Frequency Identification) systems have been traditionally used for identification and tracking applications, replacing the classic barcodes in several applications such as supply chain management, inventory control in warehousing, airport baggage control and manufacturing.

The RFID system is made up of two main blocks called transponder (tag), normally embedded in a label, and the reader. RFID tags can either be passive or active. An active tag takes the energy from a battery, so that it can transmits longer distances and uses more sophisticated signal processing. A passive tag scavenges the energy from the electromagnetic field emitted by the reader. As it does not need any battery it can be smaller and cheaper than an active tag and with unlimited lifetime. Interest for the passive applications is growing due to the high fabrication and maintenance costs of active tags.

Combining sensors with passive RFID tags opens the way for new applications of RFID in consumer electronics, automotive, medicine and healthcare. As the passive RFID sensor nodes are powered by energy scavenging, ultra-low power consumption and robustness against process variation and changes in the supply voltage are essential requirements. In addition, as typical in mass production applications, low area consumption is crucial in order to decrease the fabrication cost.

In the design of passive RFID tags with sensing capability, most of the reported works are focused on antenna and RF front-end design. However, much effort is still needed on the sensor interface, in which the ADC (Analog-to-Digital Converter) is a crucial component. The design of ADCs for passive RFID systems is a current challenge for the IC design research community as it must combine low power consumption, small area and robustness against power supply variations.

This paper presents a compact ADC implementation which converts the signal coming from a MEMS (Micro Electro–Mechanical System) accelerometer, which has a high potential for a variety of applications in mobile phones, laptops, game consoles and handheld devices. The accelerometer is a single-ended output signal structure presently available in a 0.35 μm CMOS technology, which is still a reliable and cheap technology for MEMS. The whole system is intended to be powered by an UHF RFID front-end, which provides a 3 V nominal supply voltage typical for the selected technology [1]. As the ADC will be integrated in the same die with the MEMS accelerometer, it has been designed in the same technology with a single-ended input.

The basic ADC specifications are summarized in Table 1. A resolution of 8 bits is required in a 25 kHz signal bandwidth. Although the nominal supply voltage is 3 V, the ADC must have a

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"A Novel CMOS Tunable Linear Transconductor Based on Quasi Floating Gate Transistors," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, 2008.

A Novel CMOS Tunable Linear Transconductor Based on Quasi Floating Gate Transistors

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***Abstract*— A novel CMOS low voltage tunable linear transconductor is presented. It is based on the transconductor presented in [1] and [2]. The transconductor presented in [2] employs Floating-Gate Transistors at the input stage of each inverter of the architecture presented by Nauta in [1], improving its low voltage operation capabilities. The approach proposed here employs quasi-floating gate transistors instead of floating gate transistors, obtaining further improvements such as higher transconductance and rejection DC common mode voltage. Moreover, a dynamic biasing technique has been incorporated, in order to solve one of the mayor drawbacks of previous implementations, the sensitivity of the linearity of the transconductor to process variations. The presented transconductor achieves very high speed operation and it is suitable for high frequency continuous time filters. It has been designed in a 0.5 µm CMOS technology from 1.4 V power supply.**

***Index Terms*—Analog CMOS, Quasi-Floating Gate Transistors, Transconductor.**

I. INTRODUCTION

THE market in which we are involved is looking for high-speed and low-power transconductor amplifiers for portable communications systems [1]-[4]. The reduction in power consumption and the scaling down of supply voltages can be achieved using specific low-voltage techniques as the one proposed in [5] and high frequency operation can be obtained using transconductors with a reduced number of internal nodes (poles) as in [1] and [2].

The main advantage of the transconductor presented by Nauta in [1] is that the absence of internal nodes leads to very high frequency operation. Despite of this attractive feature, there are some drawbacks which do not allow reliable programmability methods, biasing schemes to overcome process variations or low voltage operation capabilities:

- The supply voltage must be larger than the sum of the threshold voltages of a p-mos and a n-mos transistors.
- Programmability of the transconductance is achieved by modifying the supply voltage.
- It is quite sensitive to the input common mode voltage and process variations (any offset at the input appears at the output and any variation at the value of the input common mode voltage degrades the output common mode voltage decreasing the linearity of the transconductor).

Although the approach in [2] allows simple implementation of programmability schemes and low voltage operation by using Multiple-Input Floating-Gate transistors, this is at the cost of a reduction of the transconductance due to the capacitive divider in the floating gate transistor terminals, and therefore, the maximum achievable working frequency is reduced. Moreover, the sensitivity of the transconductor to process variations was still an open issue.

In this paper a new transconductor based on quasi-floating gate transistors is presented. It solves the problem of the sensitivity of the transconductor to process variations, provides a simple programmability scheme, and increases the transconductance, while maintaining the low voltage operation capabilities and the very high frequency operation due to the absence of internal nodes.

In Section II the proposed transconductor architecture will be described and its advantages will be explained. Moreover, section III will provide simulation results of the transconductor that confirms the theoretical assumptions. As it will be seen in this section, the transconductor presents improved performances in terms of programmability, sensitivity to process variations and low voltage operation capabilities while maintaining noise, linearity and power consumption figures.

The OTA has been laid-out and sent for fabrication in a standard 0.5 µm CMOS technology, so as experimental results will be provided during the conference.

II. PROPOSED TRANSCONDUCTOR

A. Quasi-Floating Gate Transistors

Quasi-Floating Gate Transistors have recently been used for many analog circuits as they present improved performances for circuits in which any possible offset at the input voltage cause degradation of the circuit operation [5].

As it is reported in [6], a quasi floating gate (QFG)

"A Very Low Power 8-Bit 16MSamples/s Pipelined Converter for DVB-H," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, 2008.

A VERY LOW POWER 8-BIT 16MSAMPLES/S CMOS PIPELINED CONVERTER FOR DVB-H

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Abstract. A 2.5V, 8-bit, 16 MS/s pipeline analog-to-digital converter (ADC) for DVB application and battery powered systems has been implemented in 0.35 μm CMOS technology. In order to reduce the power consumption a combination of techniques has been used, such as op-amp sharing, low-power amplifiers with gain boosting and an aggressive capacitor scaling. The post-layout simulation shows a peak signal-to-noise-and-distortion ratio (SNDR) of 48.51 dB, maximum differential nonlinearity (DNL) of 0.40 least significant bit (LSB), maximum integral nonlinearity (INL) of 1.06 LSB, and a power consumption of less than 4 mW.

1. INTRODUCTION

During the last few years much effort has been devoted towards the reduction of the supply power of mixed signal CMOS systems. This is primarily due to the increasing importance of battery-powered electronics, and the continued down-scaling of device sizes. Pipelining has been accepted as the best approach to implement high-speed medium-to-high resolution analog-to-digital converters with minimum power consumption.

2. 1.5-BIT/STAGE STRUCTURE

This 1.5 bit configuration is particularly suitable to minimize the converter's total power dissipation [1]-[3] because the amplifiers operate at a low closed-loop gain leading to a best settling time for minimum power consumption.

A block diagram of the pipeline 1.5-bit/stage architecture is shown in Fig 1. It consists of a cascade of seven stages. Each stage resolves two bits with a sub–ADC, subtracts the converted value from its inputs, and amplifies the resulting residue by a gain of two. The last stage of the pipeline does not need to generate a residue and, then, it does not require an op-amp. The resulting 14 bits are combined with digital correction to yield eight bits at the output of the ADC. Comparators offset up to $\pm V_{ref}/4$ can be tolerated without degradation of the overall SNDR using the mentioned technique.

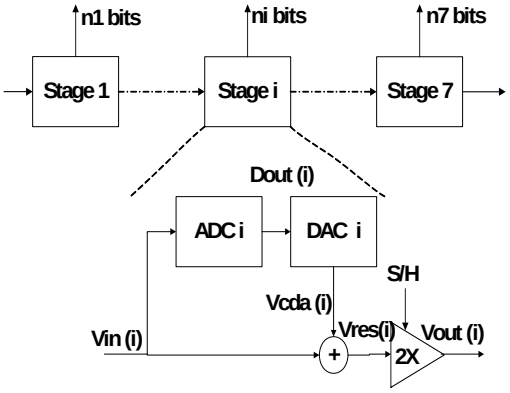

Figure1. Pipeline-ADC 1.5-bit/stage architecture.

A fully differential solution has been implemented to maximize the power supply rejection ratio (PSRR) and to minimize even harmonic distortion. A switched-capacitor implementation was also selected, which operates using a non-overlapping two-phase clock.

3. LOW POWER TECHNIQUES

The main contribution of this paper is the clever combination of different power saving techniques to achieve a very low power solution, which will be now described.

3.1. The sample and hold amplifier

The sample and hold amplifier (SHA) at the input of the pipelined converter usually takes one third of the overall converter power consumption [8]. The dedicated SHA has been removed in our design and the sampling operation is performed by the switched-capacitor residue amplifier (based on a MDAC) of the first stage. In this case, special care needs to be paid to the input switches involved in the sampling process, and a clock-boosting technique [4] has been implemented to improve its linearity. In this way a resistance independent on the input signal is achieved in the "on" state, as a constant voltage is applied across the gate-to source terminals of the NMOS transistor switch.

"A 185 mW, 6-Bit, 1GS/s, Flash A/D Converter Based on a New Autozering Technique," *XXIII Conference of Design of Circuits and Integrated Systems (DCIS'2008)*, 2008.

A 185 mW, 6-bit, 1GS/s flash A/D converter based on a new autozeroing technique

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Abstract. This paper presents a CMOS flash Analog-to-Digital converter for Ultra Wide Band applications. The flash converter is based on a new autozeroing technique which combines very high-speed operation, low-power consumption and low input switching interferences. Simulation results show 5.65-bit at 1GS/s with a power consumption of only 185 mW.

1. INTRODUCTION

Many applications, such as high-speed hard disk drives and Ultra-Wide Band communication, have created a great demand of high-speed Analog-to-Digital Converters (ADCs). Traditionally, these high-speed ADCs are built using a flash architecture.

In current CMOS technologies, the performances of flash ADCs are mainly limited by errors caused by process variations. To solve this problem a chain of gain stages is usually placed in front of the flash comparators.

A popular technique to reduce the number of such front-end amplifiers, and thus the input capacitance and power consumption, is the capacitive interpolation with autozeroing [1][2].

The main advantages of the capacitive interpolation are [1]:

- It does not require overrange comparators or any static averaging termination.
- No an external Sampled-and-Hold (S&H) is required, because a distributed S&H is implemented by the autozeroing technique.

However, there are some important drawbacks [3]

- The autozeroing technique requires two non-overlapping clock phases at very high frequencies.
- The switched capacitors at the input of the ADC lead to a large input capacitance and produce interferences at the input node.
- Only half a period is available to charge interpolation capacitors, limiting the rate of operation of the converter.

In this paper, a new architecture to implement a flash ADC is presented. The proposed scheme does not have capacitors at the ADC input, reducing the input loading and thus, the power consumption of the previous receiver blocks. Moreover, the interference of the switching at the input node is eliminated.

Another advantage of the proposed scheme is that, except for the first amplification stage, the amplifiers do not charge any capacitor, so that the whole clock period is available for their output settling. As a consequence, the bandwidth requirement of the amplifiers is relaxed, further reducing the power consumption.

Finally, we would like to emphasize that the proposed ADC only needs a single clock signal, instead of two non-overlapping ones. This also results on a reduction of complexity and power consumption.

2. THE ADC FOR UWB APPLICATIONS

Table I summarises the specifications of a flash ADC for UWB applications:

TABLE I
ADC BASIC SPECIFICATIONS

Sampling frequency	1 Ghz
Resolution	6 bits
Supply Voltage	1.2 V
Power consumption	Minimize
Input Voltage Range	400 mVpp

To design a converter with the specifications of Table I, a flash architecture based on interpolations has been used (Fig. 1). The

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Towards an unified IP verification and robustness analysis platform

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Abstract— **In this work, we propose to develop and to combine in a same tool functional verification and robustness analysis of IP cores. The overall purpose of this methodology unifying functional verification and robustness analysis is to help designers in getting more quickly "first right time" hardened IP designs. Indeed, re-using the results of the functional verification analysis, i.e. mutation score, will help us to analyze more quickly the IP robustness. In this paper, we discuss about the synthesizable Mutation Function performing the transient fault injection. We focus on its efficiency to model realistic transient faults and to fit with the already existing Aligator platform performing the functional verification analysis of digital IP.**

Keywords- fault injection, mutation based testing, digital IP verification, SEU

I. INTRODUCTION

When designing Intellectual Properties (IP) dedicated to robust applications, the validation process is becoming an endless task for designers. This validation involves several different issues. In addition to the functional verification, designers also have to validate the design robustness proving the efficiency of the on-purpose mechanisms. Indeed, while for usual IC resistance to perturbation is not the main concern, for IC dedicated to secure applications (such as smartcard) or safety applications (such as aeronautics for instance), a strong focus is required on the robustness evaluation. Even if such IC robustness is characterized after fabrication, designers are looking for means and methods to evaluate robustness at a first glance during RT level design. Such evaluation greatly helps the designers in adding robust structures within the design [LEV07]. Indeed, consider a circuit in which one wants to add redundancy on registers in order to detect fault attacks. Inserting redundancy mechanism on all registers in this circuit is a far too much expensive solution. At the contrary, designers have to pick some registers which will be made more robust. By fault injection at the RT-Level, designers will then be able to check if the registers which have been chosen are the most pertinent ones to catch as much as injected faults and also to prevent the unwanted behaviors.

Moreover, such IP designers are facing an additional difficulty: the certification. Certification processes such as *Common Criteria* [wwwCC] for security or *DO254* [wwwDO] standard for aeronautics require a complete verification flow from specification to fabrication. Thus, each function, including its robustness mechanism, must be (1) analyzed to evaluate its robustness and (2) be traced and verified during all the design process. However, while functional verification is clearly bounded by the product specification, robustness specifications are generally more difficult to formalize.

Functional verification methods and tools could highly help designers in achieving this certification. In fact, functional verification tools allow finding bugs into RTL designs. Indeed, finding bugs at the RT-Level is cheaper than finding bugs at the lowest abstraction levels. In addition, RT Level simulations are more efficient than Gate level simulations and numerous verification tools exist at this level: code coverage analyzers, guided random generators, equivalence and property checkers and high level specification languages (i.e. PSL). In this paper, we will focus on the circuit robustness analysis at the RT Level using another well known RTL functional verification technique: we used a reconfigurable FPGA-based platform to achieve a hardware acceleration of the simulations.

In fine, unifying functional verification and robustness analysis could be a plus for accelerating transient fault injection campaign. First coverage results of functional verification analysis could be used to select the test cases to be runned for a subset of transient faults. Indeed, if a test case does not cover a vhdl line or can not kill a permanent mutation on a register, we can imagine it will not be well suited to analysis the effect of a transient faults on it. Faults injection campaign can be very time consuming, and it is quite difficult to be sure of its efficiency. Indeed, when a fault is not detected, two reasons are possible: either the circuit is robust against the injected fault; either the test case or the response checker used during the injection campaign is not suitable. Unifying the functional verification environment with the fault injection environment would thus allow using functional verification results (test cases, property assertions, response checker, etc) in order to analyze the results of the transient faults injection campaign.

The remainder of this paper is organized as follows: section 2 introduces the motivations of our work introducing the main definitions. Section 3 describes our fault injection method proposed to perform transient fault injection at Register Transfer Level and complying with the motivations earlier

"A Very Low-Area Amplifier-Less Sigma-Delta Modulator for RFID Applications," *XXVI Conference of Design of Circuits and Integrated Systems (DCIS'2011)*, 2011.

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A Very Low-area Amplifier-less ΣΔ Modulator for RFID Applications

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***Abstract*— In this paper, a first-order continuous-time sigma-delta (ΣΔ) modulator for a passive RFID tag with sensing capability is presented. The main objectives in this application are minimum active area and very low power consumption. A robust and simple implementation has been achieved based on a new implementation of local feedback without operational amplifiers. Experimental results show 9 bits of resolution in a 25 kHz signal bandwidth with a power consumption of 4.35 µW. A Figure Of Merit of 0.267 pJ/state has been achieved with an active area of 110µm *x* 125µm in a 0.35µm CMOS technology.**

***Index Terms*— Delta-sigma (ΔΣ) modulator, low power, RFID, local feedback.**

I. INTRODUCTION

RFID (Radio Frequency Identification) systems have been used for identification and tracking applications. Combining sensors with passive RFID tags opens the way for new applications of RFID in consumer electronics, automotive, medicine and healthcare. In the design of passive RFID tags with sensing capability, the ADC (Analog-to-Digital Converter) is a crucial component, as it must combine low power with small area and high resolution.

This paper presents an ADC which converts the signal coming from a MEMS (Micro Electro-Mechanical System) accelerometer, which has a high potential for a variety of applications in mobile phones, laptops, game consoles and handheld devices. The accelerometer is a single-ended structure presently available in a 0.35 µm CMOS technology, which is still a reliable and cheap technology for MEMS.

The basic ADC specifications are summarized in Table I. A resolution of 8 bits is required in a 25 kHz signal bandwidth. The ADC will be integrated in the same die with the MEMS accelerometer, so that it has to be designed in the same 0.35 µm CMOS technology with single-ended input. In addition, robustness against process variation and changes in the operating condition is a key issue in this application, as the circuit is intended to be used in a battery-less application with energy harvesting coming from the RF front-end. Low cost (i.e., small area occupancy) and low power consumption are also important issues. Finally, as the sensor is being presently migrated to an advanced digital technology, the ADC has to be easily scalable to nano-metric technologies and compatible with digital CMOS.

In this paper, a new implementation of a continuous time ΣΔ modulator is proposed as an alternative to traditional opamp-based or gm-C circuits. This new implementation uses local feedback to provide a virtual ground node for reference subtraction. The resulting modulator shows very low power consumption with an extremely small area. Moreover, the simplicity of the circuit makes it robust against process variation and changes in the operating conditions.

TABLE I
BASIC SPECIFICATIONS

BASIC SPECIFICATIONS OF THE ADC	
Nyquist frequency	25kHz
Resolution	8 bits
Supply Voltage	2.5 to 5 V
Power consumption	Less than 10µW
Input Voltage Range	Single-ended 200 mV peak-peak
BASIC SPECIFICATIONS OF THE ΣΔ MODULATOR	
Sampling frequency	3.2MHz
OSR	64
Simulated DR	52dB

II. MODULATOR ARCHITECTURE

Algorithmic converters, like the well-known successive approximation register (SAR) converter, achieve high resolution with low power consumption [1]-[3]. However, they require a large active area and have a high input capacitance. Due to the area constraint, which is of capital importance in this project, a ΣΔ modulator architecture has been selected.

Traditionally, low speed ΣΔ modulators use an op-amp-RC topology. The op-amp feedback configuration provides a high linearity at the cost of a high open-loop gain. On the other hand, the operational amplifier is the main contributor for noise and power consumption.

There is a recent trend in the area of low-power ADC design to simplify the analog circuitry by replacing the op-amp with simple analog blocks [4]. Following this trend, in this work, the ΣΔ modulator has been implemented without op-amps or Operational Transconductance Amplifiers (OTAs). Local feedback is used instead to guarantee the required linearity with a low cost in terms of noise and power consumption, as it will be shown in Section III.